CDx4HC112, CDx4HCT112 Dual J-K Flip-Flop with Set and Reset with Negative-Edge Trigger

1 Features

- Hysteresis on clock inputs for improved noise immunity and increased input rise and fall times
- Asynchronous set and reset
- Complementary outputs
- Buffered inputs
- Typical f_{MAX} = 60 MHz at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1$ µA at V_{OL}, V_{OH}

2 Description

The ’HC112 and ’HCT112 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

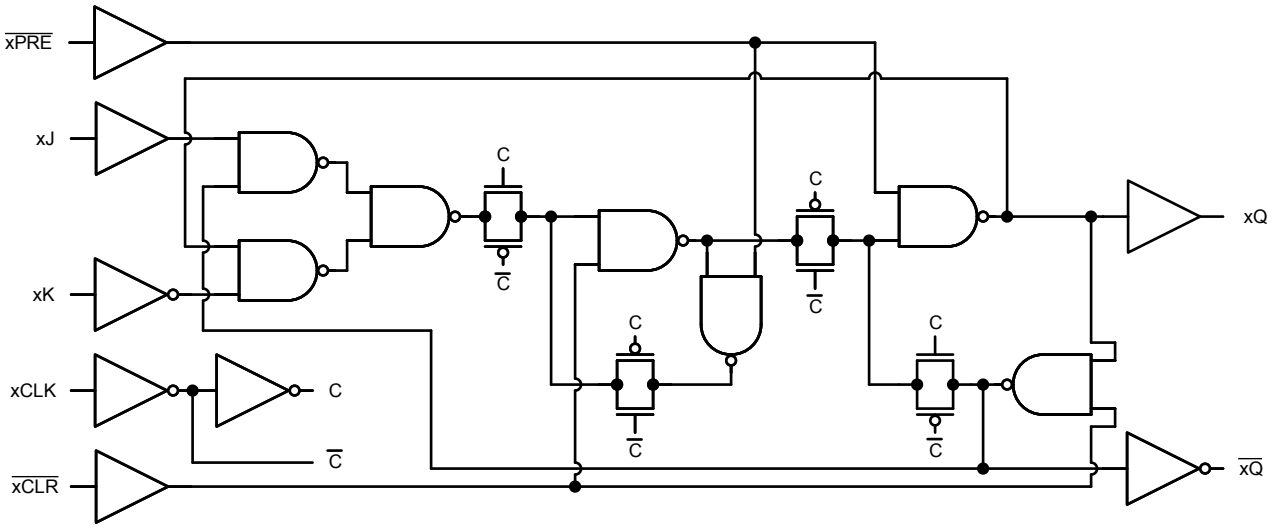
These flip-flops have independent J, K, $\overline{PRE}$, $\overline{CLR}$, and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. $\overline{PRE}$ and $\overline{CLR}$ are accomplished asynchronously by low-level inputs.

The HCT logic family is functionally as well as pin compatible with the standard LS logic family.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC112F3A	CDIP (16)	24.38 mm × 6.92 mm
CD74HC112M96	SOIC (16)	9.90 mm × 3.90 mm
CD74HC112E	PDIP (16)	19.31 mm × 6.35 mm
CD74HCT112E	PDIP (16)	19.31 mm × 6.35 mm
CD74HC112NSR	SO (16)	6.20 mm × 5.30 mm
CD74HC112PW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagram

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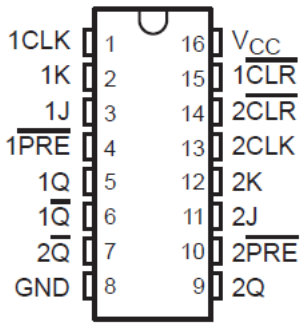
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (January 2022) to Revision J (October 2022)	Page
• Increased RθJA for packages: D (73 to 117.2); N (67 to 69.3); NS (64 to 88.4); PW (108 to 137.5)	4

Changes from Revision H (October 2003) to Revision I (January 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1
• Updated pin names to match current standards. $\overline{CP}$ is now CLK; $\overline{S}$ is now $\overline{PRE}$; $\overline{1R}$ is now $1\overline{CLR}$; $\overline{2R}$ is now $2\overline{CLR}$; $\overline{2CP}$ is now 2CLK; $\overline{2S}$ is now $2\overline{PRE}$	3

4 Pin Configuration and Functions



J, N, D, NS, or PW package
16-Pin CDIP, PDIP, SOIC, SO, TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

(1)			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For V_I < -0.5 V or V_I > V_{CC} + 0.5 V		± 20	mA
I_O	Drain current, per output	For -0.5 V < V_O < V_{CC} + 0.5 V		± 25	mA
I_{OK}	Output diode current	For V_O < -0.5 V or V_O > V_{CC} + 0.5 V		± 20	mA
I_O	Output source or sink current per output pin	For V_O > -0.5 V or V_O < V_{CC} + 0.5 V		± 25	mA
I_{CC}	Continuous current through V_{CC} or GND			± 50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
t_r, t_f	Input rise and fall time	2 V		1	ms
		4.5 V		1	
		6 V		1	
T_A	Temperature range		–55	125	℃

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 16 PINS	N (PDIP) 16 PINS	NS (SO) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	117.2	69.3	88.4	137.5	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	77.2	61.8	46	75.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.6	49.3	50.6	82.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	38.1	34.6	13	25.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.3	49	50.2	81.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[2]	V_{CC}(V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
			4.5	4.4			4.4		4.4		
			6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
			4.5			0.1		0.1		0.1	
			6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Supply current	V_{CC} or GND	6			4		40		80	µA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	I_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} and GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_{CC} and GND	5.5			4		40		80	µA
ΔI_{CC} [1]	Additional supply current per input pin	$\overline{1PRE}$, $\overline{2PRE}$ inputs held at V_{CC} -2.1	4.5 to 5.5		100	180		225		245	µA
		1K, 2K inputs held at V_{CC} -2.1	4.5 to 5.5		100	216		270		294	µA
		$\overline{1CLR}$, $\overline{2CLR}$ inputs held at V_{CC} -2.1	4.5 to 5.5		100	234		292.5		318.5	µA
		1J, 2J, 1CLK, 2CLK inputs held at V_{CC} -2.1	4.5 to 5.5		100	360		450		490	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_W	Pulse width CLK	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
t_W	Pulse width $\overline{CLR}$, $\overline{PRE}$	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
t_{SU}	Setup time J, K, to CLK	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
t_H	Hold time J, K, to CLK	2	0			0		0		ns
		4.5	0			0		0		
		6	0			0		0		
t_{REM}	Removal time $\overline{CLR}$ to CLK, $\overline{PRE}$ to CLK	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
f_{MAX}	CLK frequency	2	6			5		4		MHz
		4.5	30			25		20		
		6	35			29		23		
HCT TYPES										
t_{SU}	Pulse width CLK	4.5	16			20		24		ns
t_W	Pulse width $\overline{CLR}$, $\overline{PRE}$	4.5	18			23		27		ns
t_H	Setup time J, K, to CLK	4.5	16			20		24		ns
t_{REM}	Hold time J, K, to CLK	4.5	3			3		3		ns
t_W	Removal time $\overline{CLR}$ to CLK, $\overline{PRE}$ to CLK	4.5	20			25		30		ns
f_{MAX}	CLK frequency	4.5	30			25		20		MHz

5.6 Switching Characteristics

t_r, t_f = 6 ns

PARAMETER		V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{PLH}, t_{PHL}	Propagation delay, CLK to Q, $\overline{Q}$	2			175		220		265	ns
		4.5		14[3]	35		44		53	
		6			30		37		45	
t_{PLH}, t_{PHL}	Propagation delay, $\overline{PRE}$ to Q, $\overline{Q}$	2			155		195		235	ns
		4.5		13[3]	31		39		47	
		6			26		33		40	
t_{PLH}, t_{PHL}	Propagation delay, $\overline{CLR}$ to Q, $\overline{Q}$	2			180		225		270	ns
		4.5		15[3]	36		45		54	
		6			31		38		46	
t_{TLH}, t_{THL}	Output transition time	2			75		95		110	ns
		4.5			15		19		22	
		6			13		16		19	
C_I	Input capacitance				10		10		10	pF
f_{MAX}	CLK frequency	5		60[3]						MHz
C_{PD}	Power dissipation capacitance[1] [2]	5		12[4]						pF
HCT TYPES										
t_{PLH}, t_{PHL}	Propagation delay, CLK to Q, $\overline{Q}$	4.5		14[3]	35		44		53	ns
t_{PLH}, t_{PHL}	Propagation delay, $\overline{PRE}$ to Q, $\overline{Q}$	4.5		13[3]	32		40		48	ns
t_{PLH}, t_{PHL}	Propagation delay, $\overline{CLR}$ to Q, $\overline{Q}$	4.5		14[3]	37		46		56	ns
t_{TLH}, t_{THL}	Output transition time	4.5			15		19		22	ns
C_I	Input capacitance				10		10		10	pF
f_{MAX}	CLK frequency	5		60[3]						MHz
C_{PD}	Power dissipation capacitance[1] [2]	5		20[4]						pF

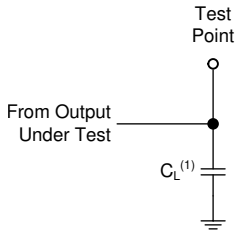
(1) C_{PD} is used to determine the dynamic power consumption, per flip-flop.
(2) $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.
(4) V_{CC} = 5 V.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

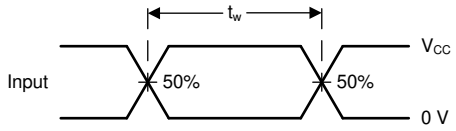


Figure 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

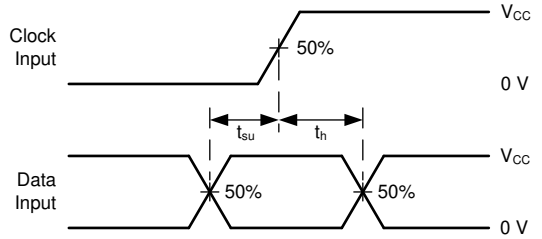
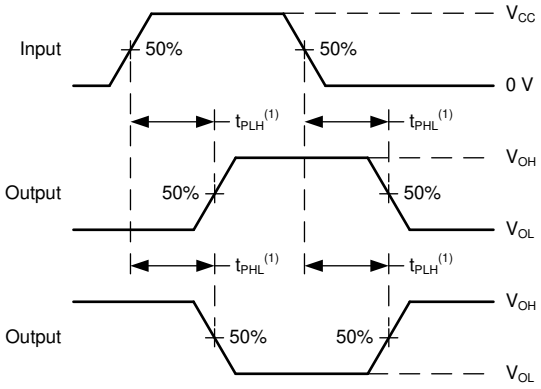
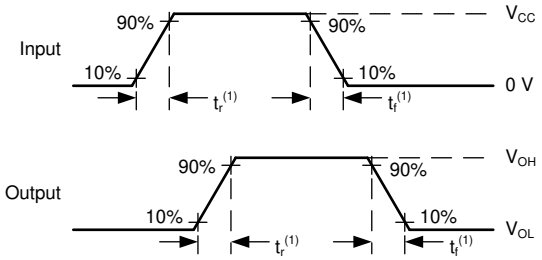


Figure 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

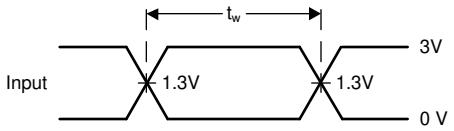


Figure 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

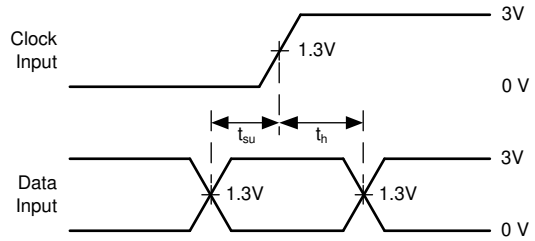
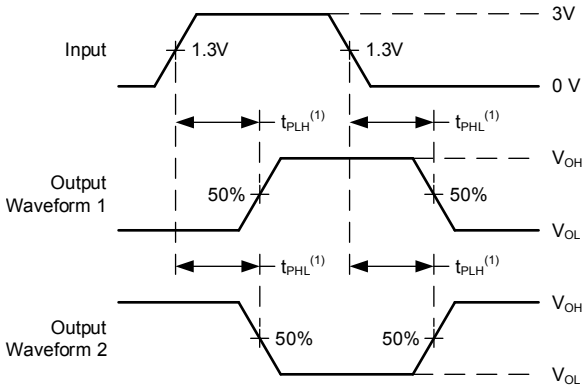


Figure 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-8. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

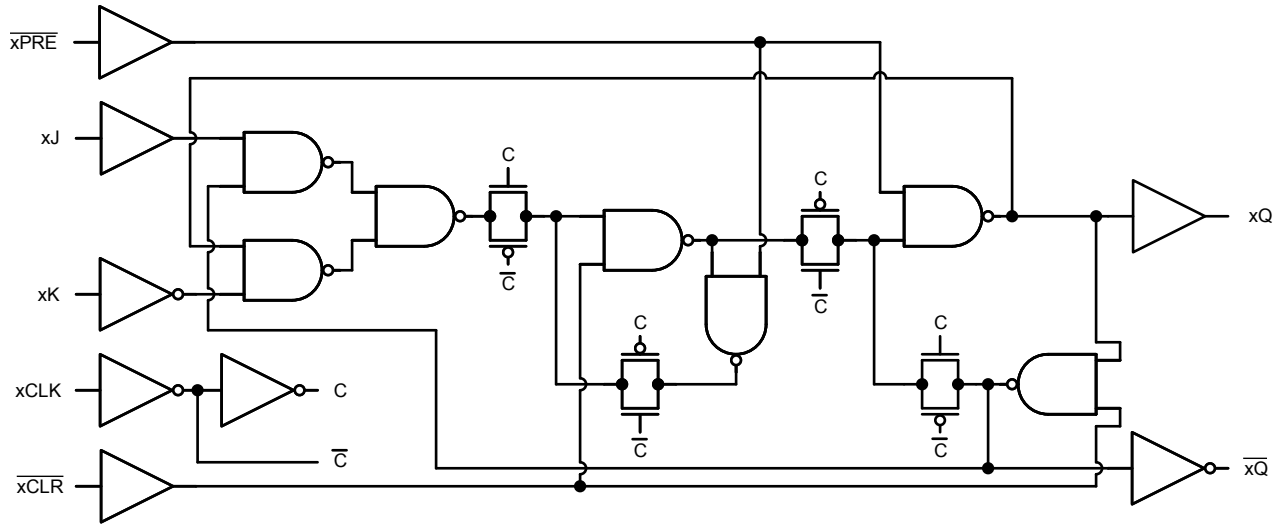
7.1 Overview

The ’HC112 and ’HCT112 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, $\overline{PRE}$, $\overline{CLR}$, and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. $\overline{PRE}$ and $\overline{CLR}$ are accomplished asynchronously by low-level inputs.

The HCT logic family is functionally and pin-compatible with the standard LS logic family.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Truth Table(1)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H(2)	H(2)
H	H	↓	L	L	No Change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	No Change	

(1) H = high level (steady state), L = low level (steady state), X = don’t care, ↓ = high-to-low transition
(2) Output states unpredictable if both $\overline{S}$ and $\overline{R}$ go high simultaneously after both being low at the same time.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8970201EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8970201EA CD54HCT112F3A
CD54HC112F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408801EA CD54HC112F3A
CD54HC112F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408801EA CD54HC112F3A
CD54HCT112F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8970201EA CD54HCT112F3A
CD54HCT112F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8970201EA CD54HCT112F3A
CD74HC112E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC112E
CD74HC112E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC112E
CD74HC112M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC112M
CD74HC112M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC112M
CD74HC112MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC112M
CD74HC112NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC112M
CD74HC112NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC112M
CD74HC112PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ112
CD74HC112PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ112
CD74HC112PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ112
CD74HCT112E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT112E
CD74HCT112E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT112E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC112, CD54HCT112, CD74HC112, CD74HCT112 :

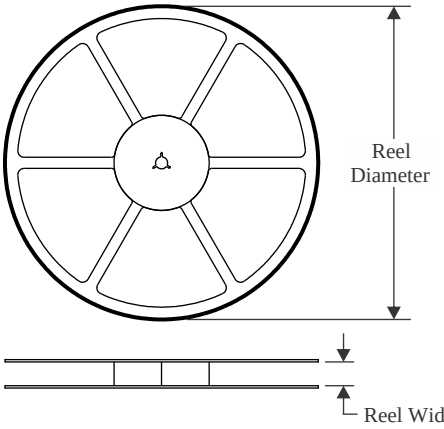
- Catalog : CD74HC112, CD74HCT112
- Military : CD54HC112, CD54HCT112

NOTE: Qualified Version Definitions:

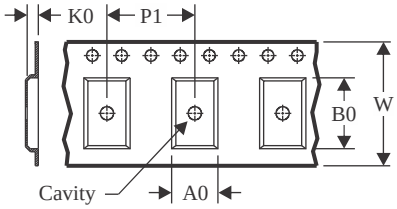
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

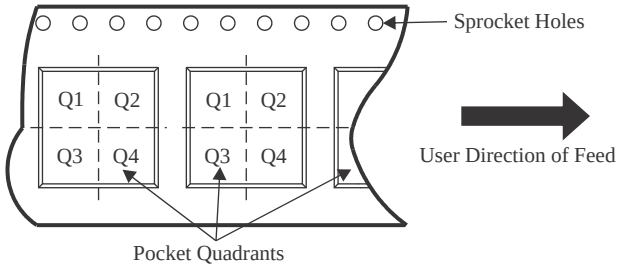


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

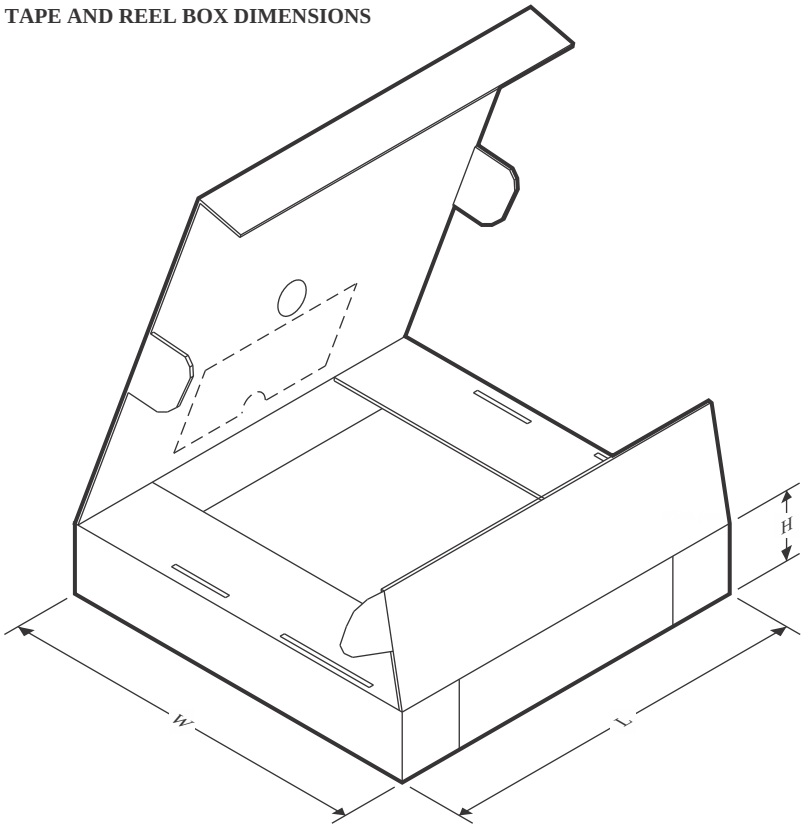
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC112M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC112NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC112PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC112PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

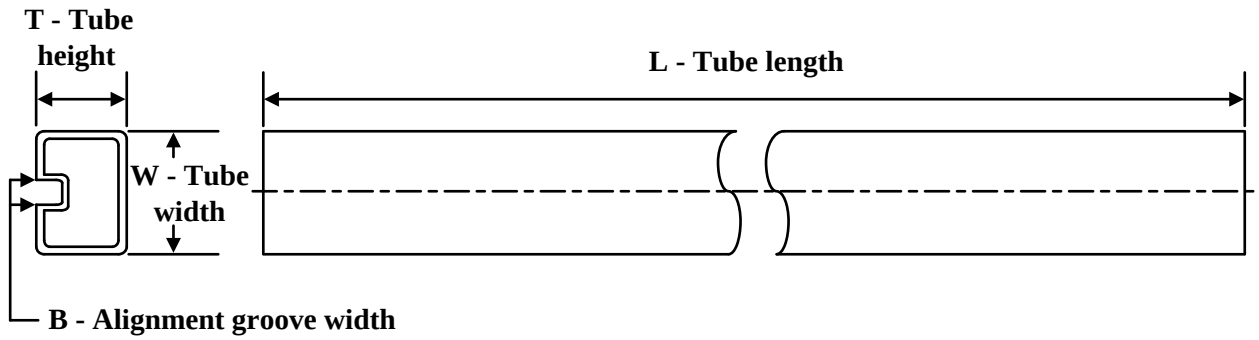
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC112M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC112NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC112PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC112PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

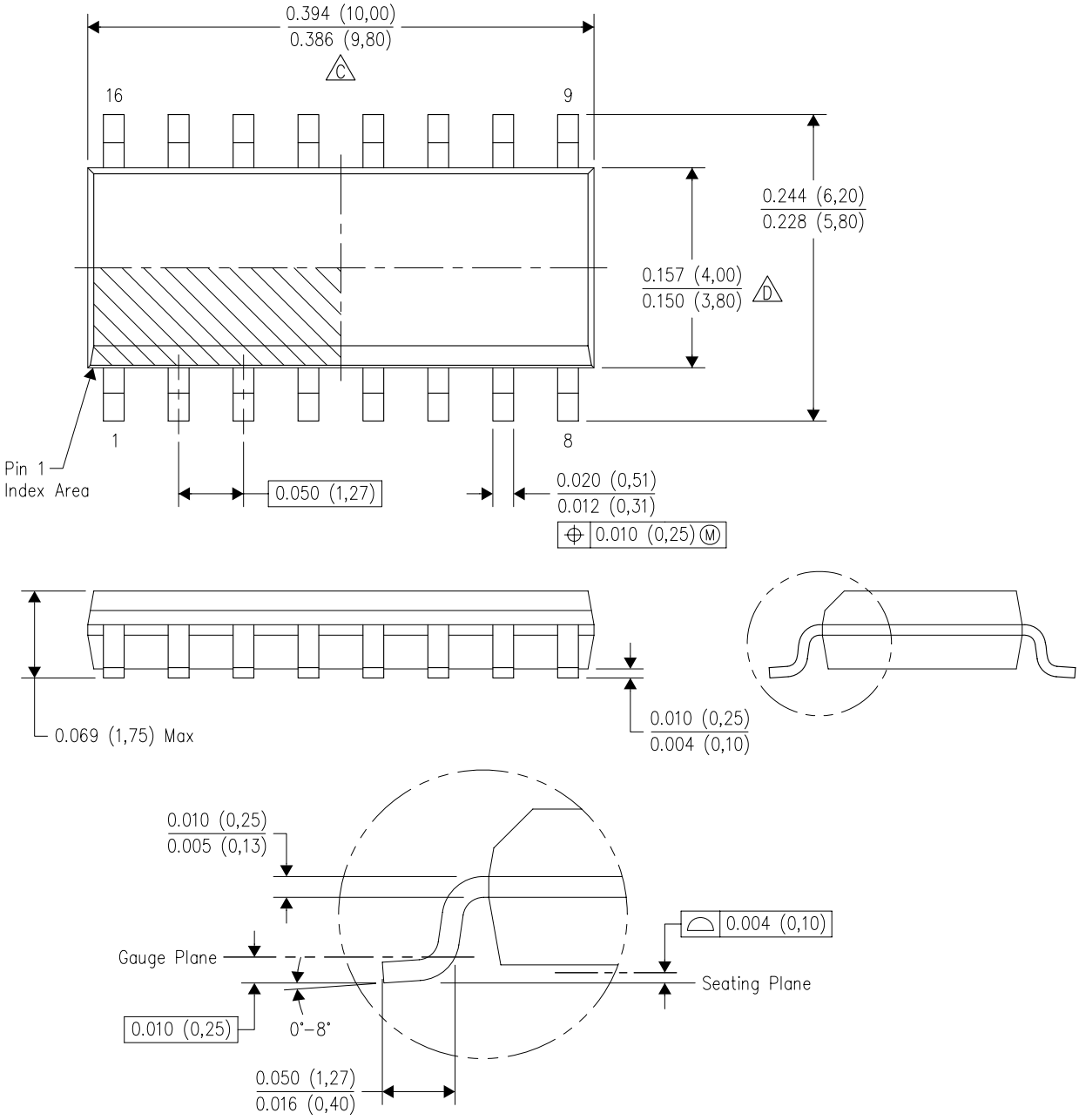
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC112E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC112E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC112E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC112E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT112E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT112E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT112E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT112E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

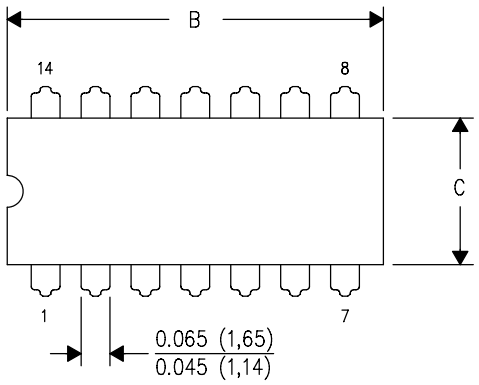


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

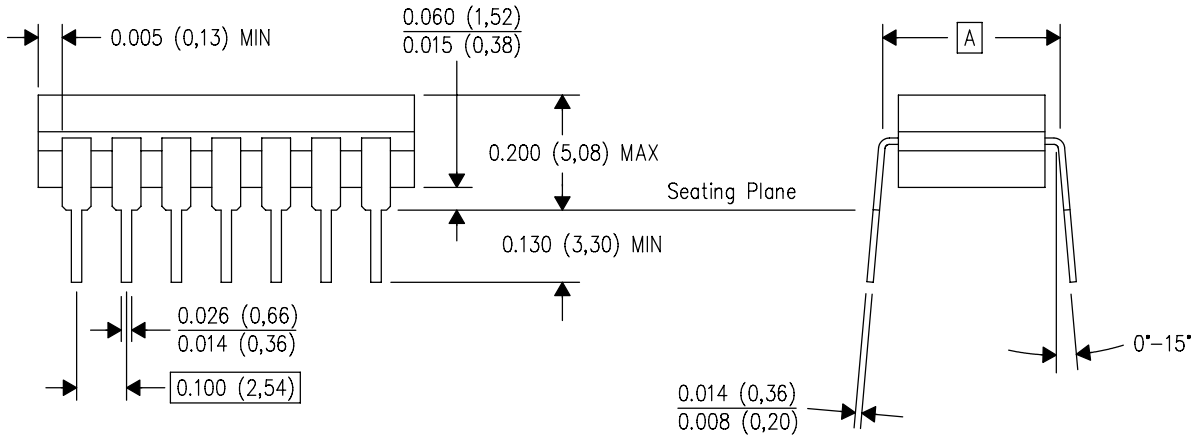
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

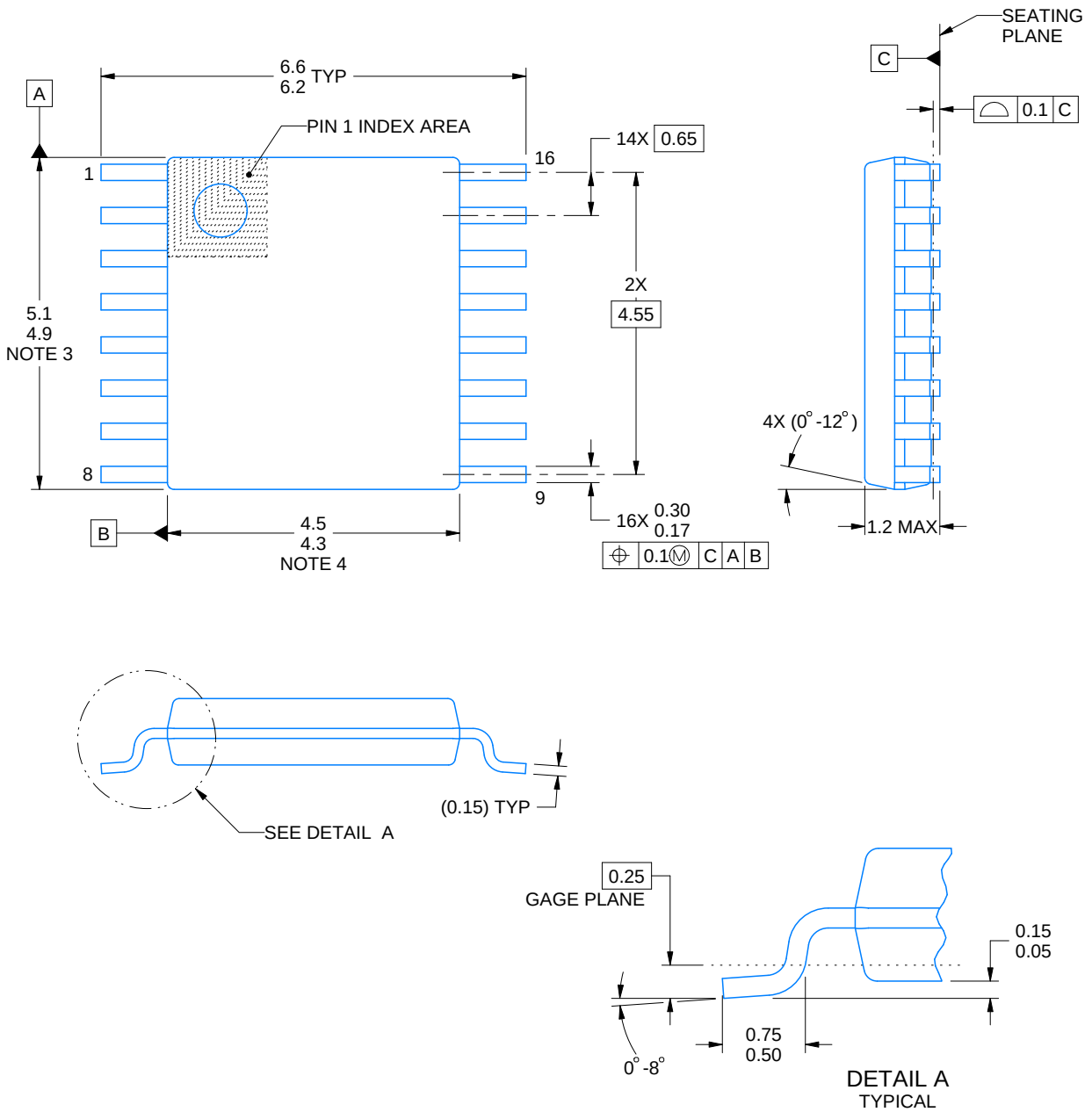
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

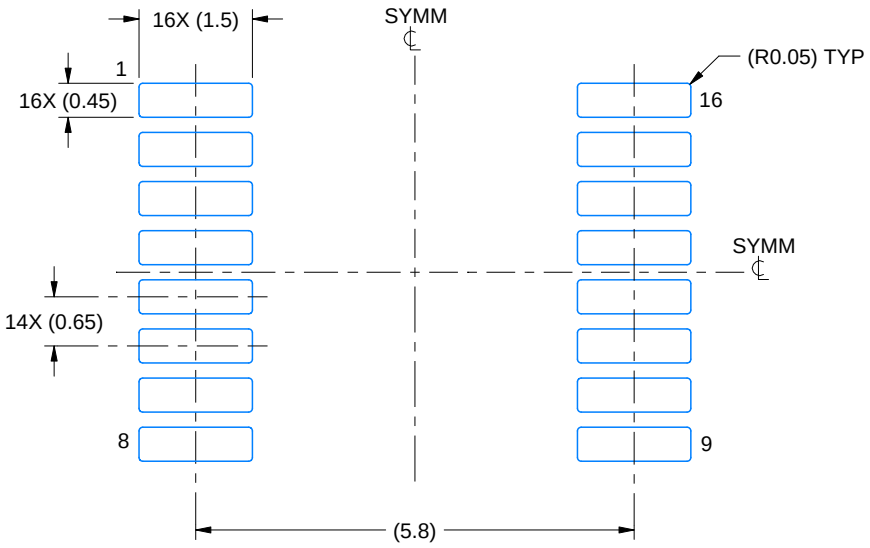
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



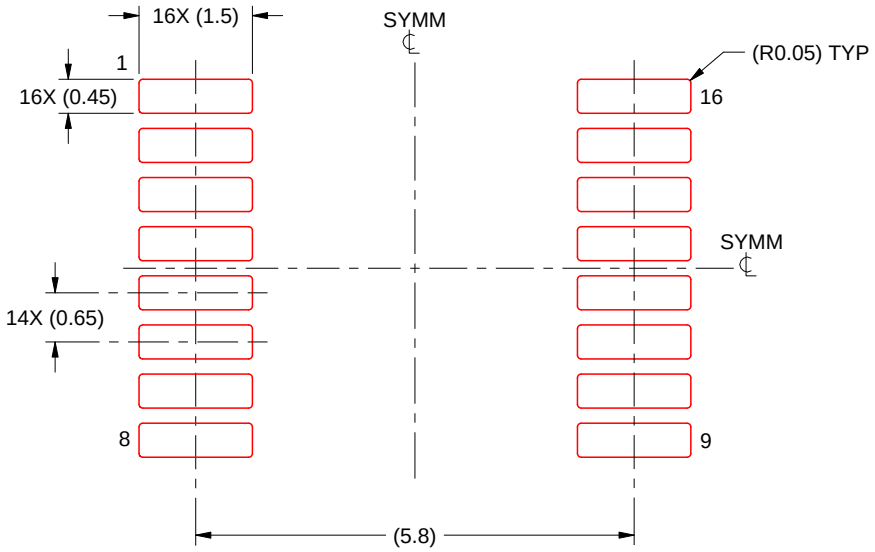
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

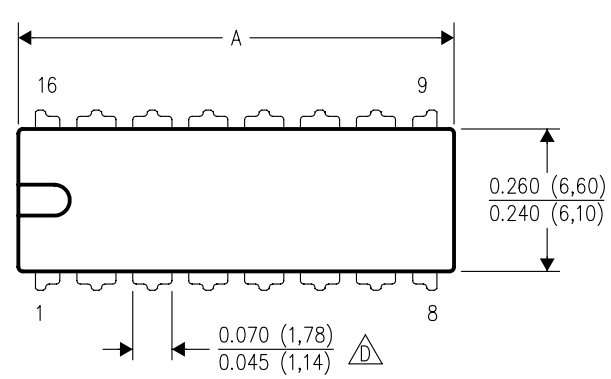
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

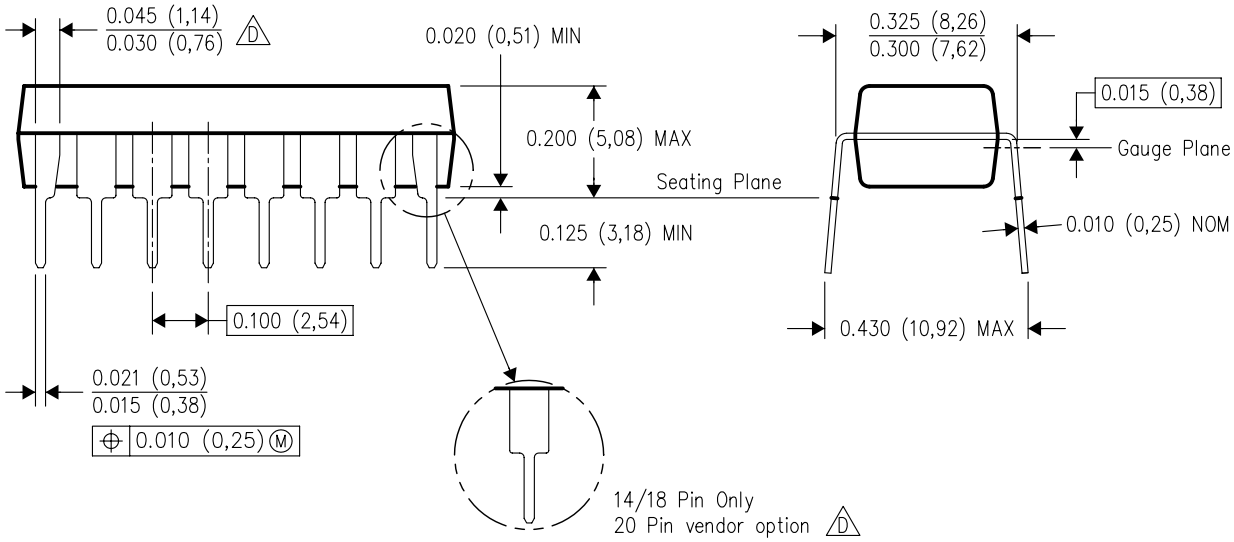
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

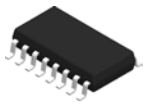


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

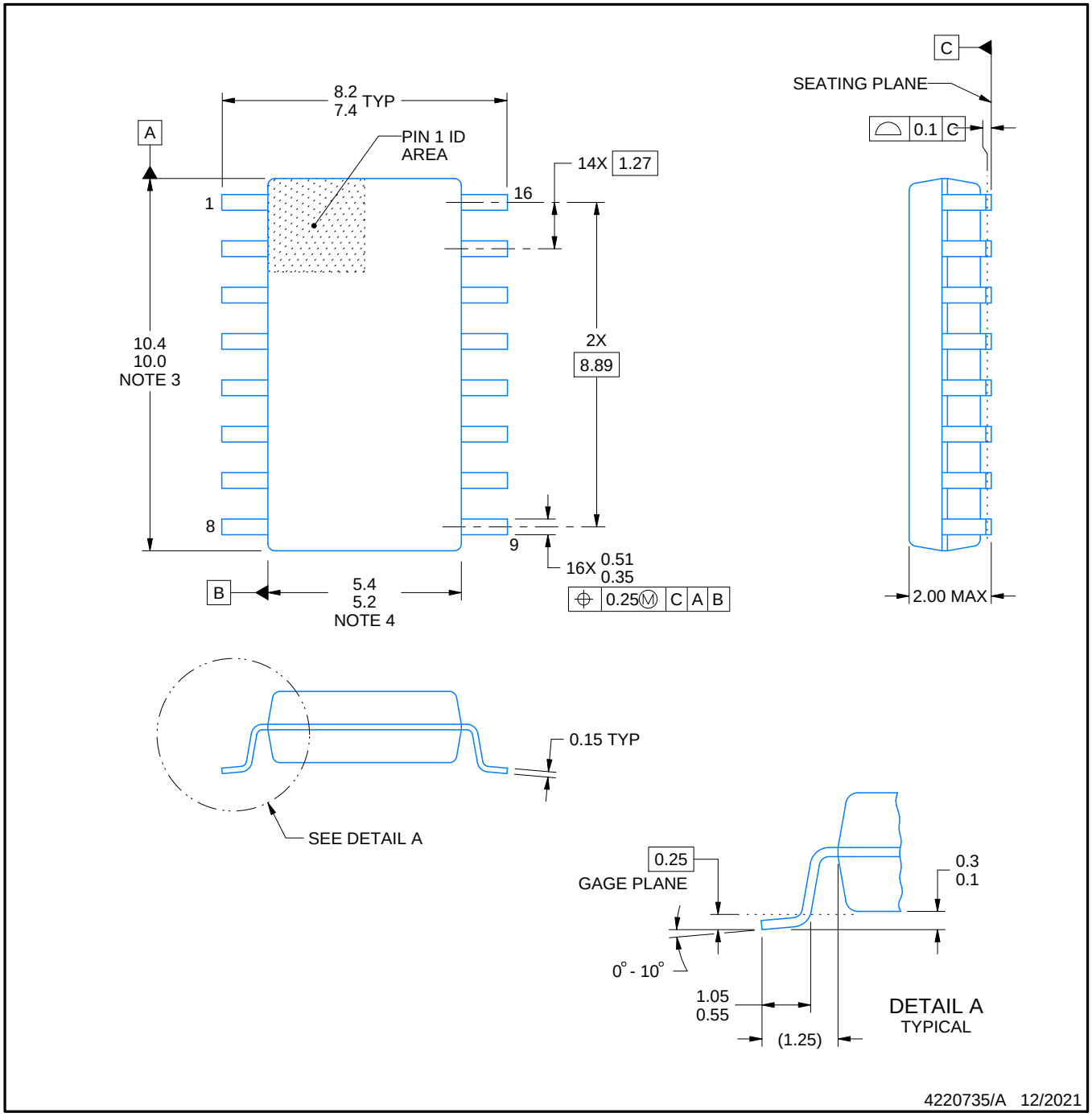


PACKAGE OUTLINE

NS0016A

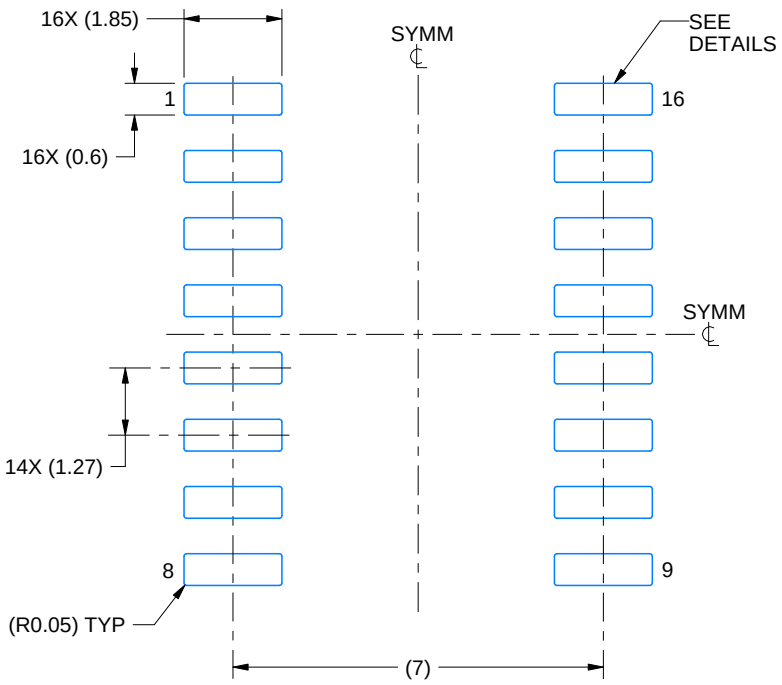
SOP - 2.00 mm max height

SOP

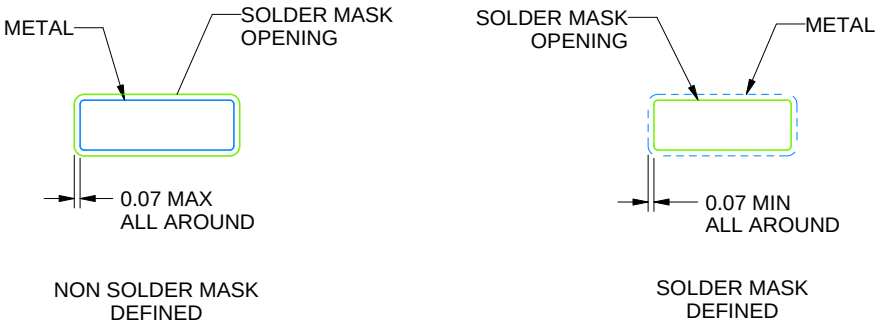


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

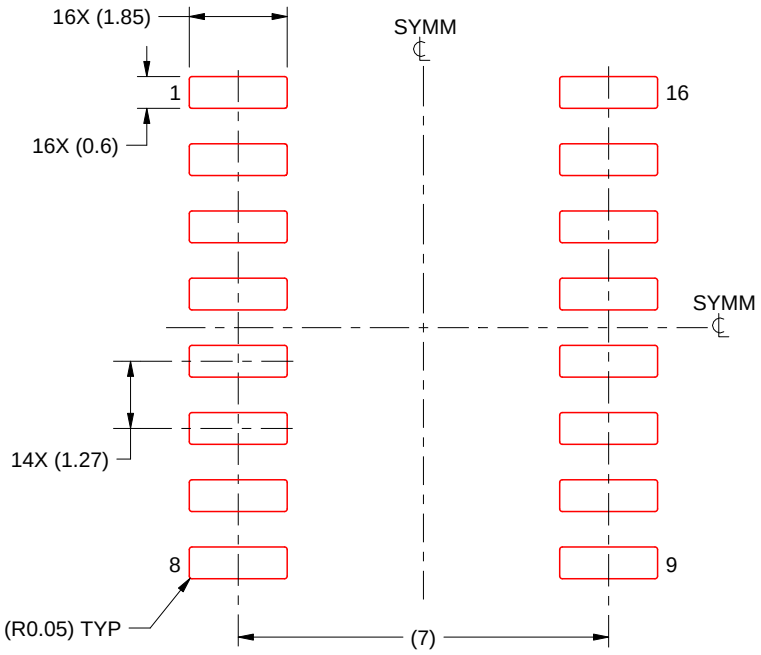
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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