

CDx4HCT125 Quadruple Buffers with 3-State Outputs

1 Features

- LSTTL input logic compatible
 - $V_{IL(max)} = 0.8V$, $V_{IH(min)} = 2V$
- CMOS input logic compatible
 - $I_I \leq 1\mu A$ at V_{OL} , V_{OH}
- Buffered inputs
- 4.5V to 5.5V operation
- Wide operating temperature range: $-55^{\circ}C$ to $+125^{\circ}C$
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

2 Applications

- [Enable digital signals](#)

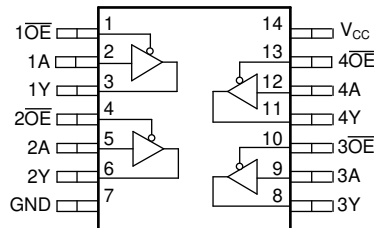
3 Description

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function $Y = A$ in positive logic.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
CDx4HCT125	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.30mm × 9.4mm	19.30mm × 6.35mm
	J (CDIP, 14)	19.56mm × 6.7mm	19.56mm × 4.57mm

- For more information, see [Mechanical, Packaging, and Orderable Information](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Functional pinout



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4 Pin Configuration and Functions

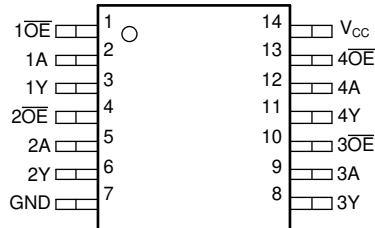


Figure 4-1. D, N, or J Package 14-Pin SOIC, PDIP, or CDIP Top View

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1 \overline{OE}	1	Input	Channel 1, Output Enable, Active Low
1A	2	Input	Channel 1, Input A
1Y	3	Output	Channel 1, Output Y
2 \overline{OE}	4	Input	Channel 2, Output Enable, Active Low
2A	5	Input	Channel 2, Input A
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3 \overline{OE}	10	Input	Channel 3, Output Enable, Active Low
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4 \overline{OE}	13	Input	Channel 4, Output Enable, Active Low
V _{CC}	14	—	Positive Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20 mA
I _{OK}	Output clamp current ⁽²⁾	V _O < -0.5 V or V _O > V _{CC} + 0.5 V		±20 mA
I _O	Continuous output current	V _O > -0.5 V or V _O < V _{CC} + 0.5 V		±35 mA
Continuous current through V _{CC} or GND				±70 mA
T _J	Junction temperature ⁽³⁾			150 °C
Lead temperature (soldering 10s)		SOIC - lead tips only		300 °C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5		5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V		2	V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V		0.8	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
t _t	Input transition time	V _{CC} = 4.5 V		500	ns
		V _{CC} = 5.5 V		400	
T _A	Operating free-air temperature	-55		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	CD74HCT125		UNIT	
	N (PDIP)	D (SOIC)		
	14 PINS	14 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	103.8	138.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	91.6	93.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	83.5	94.7	°C/W

THERMAL METRIC ⁽¹⁾		CD74HCT125		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
Ψ_{JT}	Junction-to-top characterization parameter	71.1	49.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.4	94.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
			25°C			–40°C to 85°C			–55°C to 125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage $V_I = V_{IH}$ or V_{IL}	4.5 V	4.4			4.4			4.4		V	
												$I_{OH} = -20 \mu\text{A}$
V_{OL}	Low-level output voltage $V_I = V_{IH}$ or V_{IL}	4.5 V			0.1			0.1		0.1	V	
												$I_{OL} = 20 \mu\text{A}$
I_I	Input leakage current	$V_I = V_{CC}$ and GND	$I_O = 0$	5.5 V			± 0.1		± 1		± 1	μA
I_{OZ}	Three-state leakage current	$V_I = V_{IH}$ or V_{IL}		5.5 V			± 0.5		± 5		± 10	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	$I_O = 0$	5.5 V			8		80		160	μA
$\Delta I_{CC}^{(1)}$	Additional Quiescent Device Current Per Input Pin.	$V_I = V_{CC} - 2.1$		4.5 V to 5.5 V			100	360		450	490	μA
C_i	Input capacitance						10		10		10	pF
C_o	Three-state output capacitance						20		20		20	pF

(1) For dual-supply systems theoretical worst case ($V_I = 2.4 \text{ V}$, $V_{CC} = 5.5 \text{ V}$) specification is 1.8 mA.

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	Y	$C_L = 50 \text{ pF}$	4.5 V			25			31		38	ns
				$C_L = 15 \text{ pF}$	5 V			10						
t_{en}	Enable delay	\overline{OE}	Y	$C_L = 50 \text{ pF}$	4.5 V			25			31		38	ns
				$C_L = 15 \text{ pF}$	5 V			10						
t_{dis}	Disable delay	\overline{OE}	Y	$C_L = 50 \text{ pF}$	4.5 V			28			35		42	ns
				$C_L = 15 \text{ pF}$	5 V			11						
t_t	Transition-time		Y	$C_L = 50 \text{ pF}$	4.5 V			12			15		18	ns

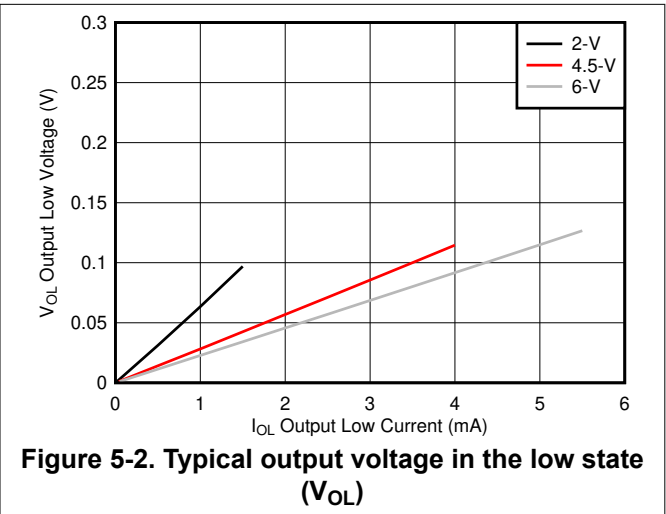
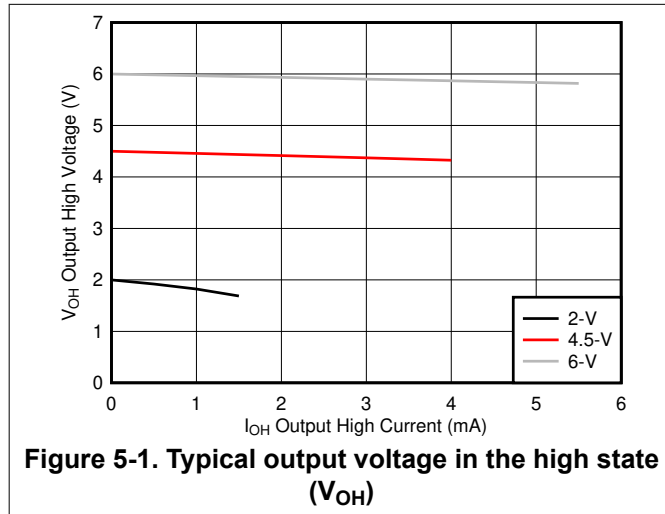
5.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd} Power dissipation capacitance per gate	No load	5 V		34		pF

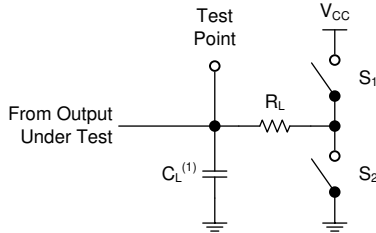
5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$



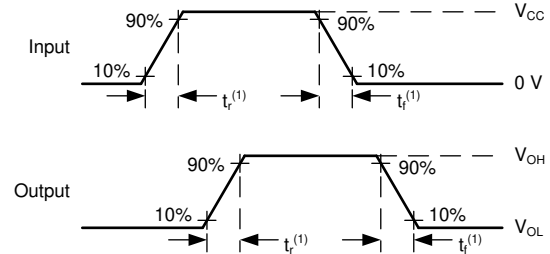
6 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.



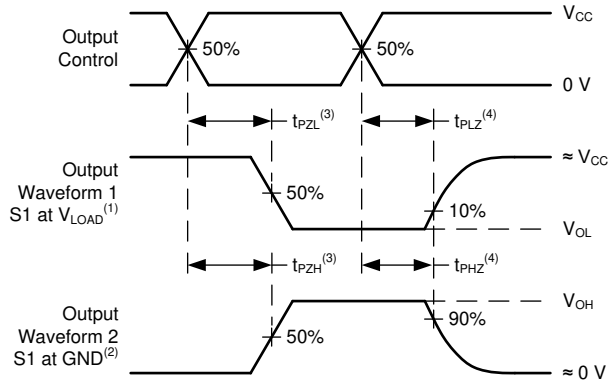
A. $C_L = 50 \text{ pF}$ and includes probe and jig capacitance.

Figure 6-1. Load Circuit



A. t_t is the greater of t_r and t_f .

Figure 6-2. Voltage Waveforms Transition Times



A. The maximum between t_{pLH} and t_{pHL} is used for t_{pd} .

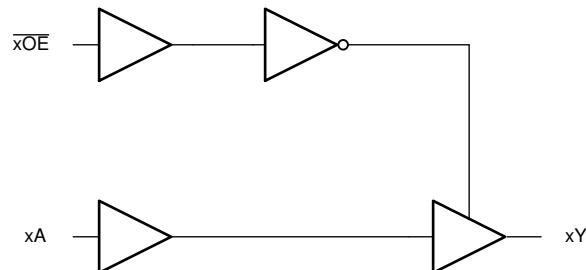
Figure 6-3. Voltage Waveforms Propagation Delays

7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function $Y = A$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Section 5.1](#) must be followed at all times.

The CD74HCT125 can drive a load with a total capacitance less than or equal to the maximum load listed in the [Section 5.6](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Section 5.1](#).

3-State outputs can be placed into a high-impedance state. In this state, the output will neither source nor sink current, and leakage current is defined by the I_{OZ} specification in the [Section 5.5](#). A pull-up or pull-down resistor can be used to ensure that the output remains HIGH or LOW, respectively, during the high-impedance state.

7.3.2 TTL-Compatible CMOS Inputs

TTL-Compatible CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Section 5.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [Section 5.1](#), and the maximum input leakage current, given in the [Section 5.5](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the [Section 5.3](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the TTL-compatible CMOS input.

TTL-Compatible CMOS inputs have a lower threshold voltage than standard CMOS inputs to allow for compatibility with older bipolar logic devices. See the [Section 5.3](#) for the valid input voltages for the CD74HCT125.

7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 7-1.

CAUTION

Voltages beyond the values specified in the Section 5.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

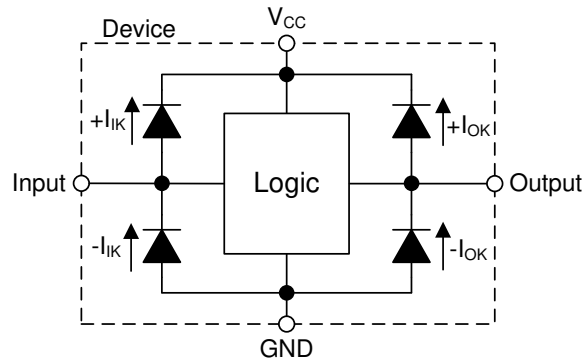


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
OE	A	Y
L	H	H
L	L	L
H	X	Z

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
 (2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, a 3-state buffer is used to enable or disable a data connection as shown in [Figure 8-1](#). It is common to see all four channels of a device used together for controlling a 4-bit data bus, however each channel of the device can be used independently. Unused channels should have the inputs terminated at ground or V_{CC} and the output left unconnected.

When the output of the device is active, the data signal will be replicated at the output. When the output of the device is disabled, the output will be in a high-impedance state, and the output voltage will be determined by the circuit connected to the output pin. This circuit is most commonly used when a bus must be completely disabled. One example of this situation is when the circuitry connected to the output is to be powered off for an extended period of time to save system power, and the inputs to that circuitry cannot have a voltage present due to protective clamp diodes.

8.2 Typical Application

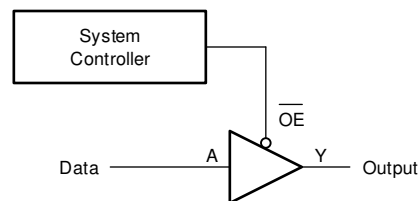


Figure 8-1. Typical application schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Section 5.3](#). The supply voltage sets the device's electrical characteristics as described in the [Section 5.5](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HCT125 plus the maximum supply current, I_{CC} , listed in the [Section 5.5](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [Section 5.1](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\text{max})$ listed in the [Section 5.1](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Section 5.1](#). These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HCT125, as specified in the [Section 5.5](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

Refer to the [Section 7.3](#) for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [Section 5.5](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [Section 5.5](#).

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to [Section 7.3](#) for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the [Section 8.4](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HCT125 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the [Section 5.1](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

8.2.3 Application Curves

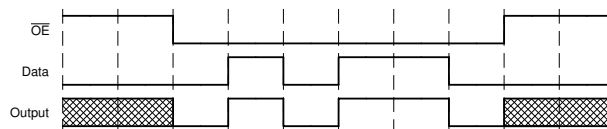


Figure 8-2. Typical application timing diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 5.3](#). Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Figure 8-3](#).

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic

devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

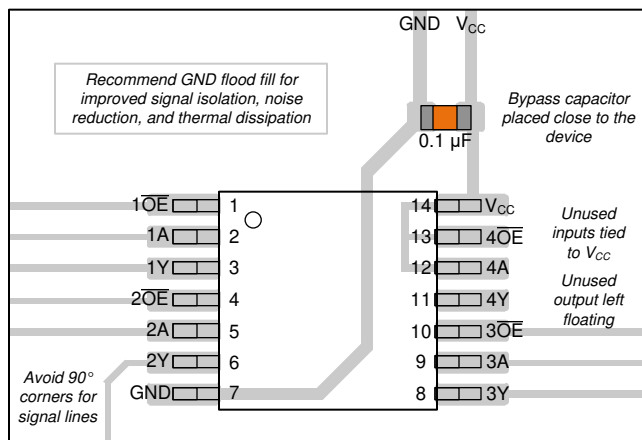


Figure 8-3. Example layout for the CD74HCT125

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision * (June 2020) to Revision A (August 2024)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1
• Added package size to <i>Device Information</i> table.....	1
• Updated RθJA values: D = 96.7 to 138.7, N = 61.5 to 103.8; Updated D and N packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.....	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HCT125F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT125F3A	Samples
CD74HCT125E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT125E	Samples
CD74HCT125M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HCT125M	
CD74HCT125M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125M96E4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125MT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HCT125M	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HCT125, CD74HCT125 :

- Catalog : [CD74HCT125](#)
- Military : [CD54HCT125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT125M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT125M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT125M96E4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT125M96E4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

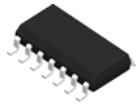
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT125M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT125M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT125M96E4	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT125M96E4	SOIC	D	14	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HCT125E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT125E	N	PDIP	14	25	506	13.97	11230	4.32

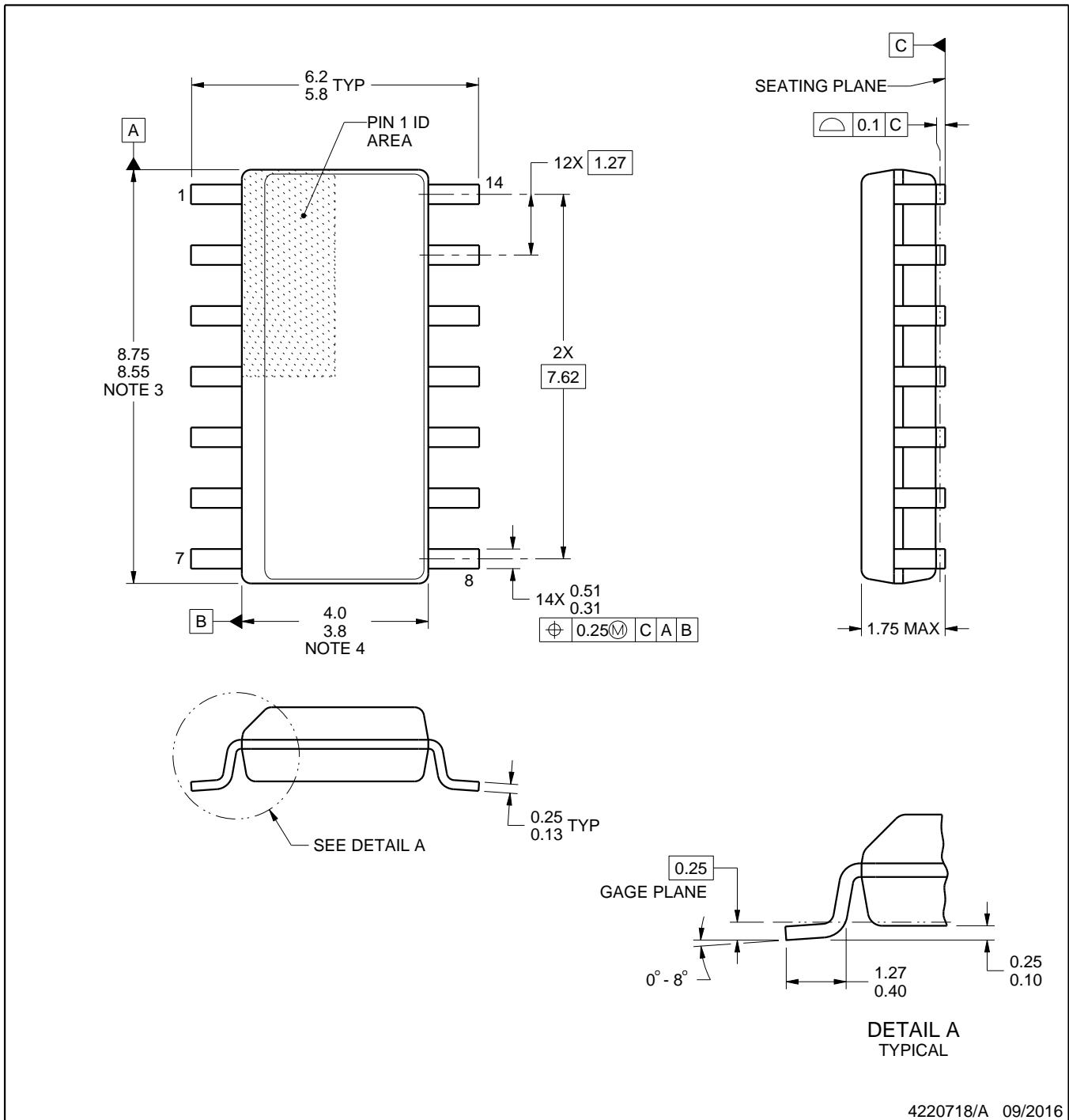
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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