CD74AC14 Hex Schmitt-Trigger Inverter

1 Features

- 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply voltage
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Greater noise immunity than standard inverters
- Operates with much slower than standard input rise and fall slew rates
- Balanced propagation delays
- ±24mA output drive current − fanout to 15F devices
- SCR latchup-resistant CMOS process and circuit design

2 Description

The CD74AC14 contains six independent inverters.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CD74AC14	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.35mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.

Simplified Schematic

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3 Pin Configuration and Functions

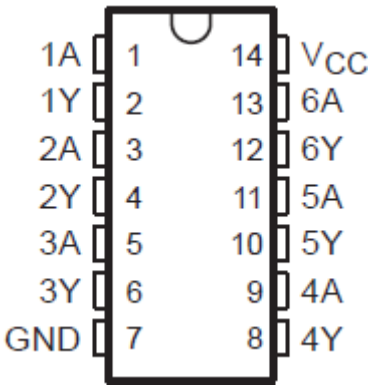


Figure 3-1. N or D Package, 14-Pin PDIP or SOIC Top View

Table 3-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	—	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V_{CC}	14	—	Positive Supply

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(3)		-0.5	6	V
V_{CC}	Supply voltage range(4)		-0.5	7	V
V_I	Input voltage range(2)		-0.5	V_{CC} + 0.5V	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5V	V
I_{IK}	Input clamp current	V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous output current through V_{CC} or GND(3)			±100	mA
	Continuous output current through V_{CC} or GND(4)			±200	mA
T_{stg}	Storage temperature		-65	150	°C
T_J	Junction temperature			150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) PDIP package only
(4) SOIC package only

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage(1)		1.5	5.5	V
	Supply voltage(2)		1.5	6	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8V(2)		-1	mA
		V_{CC} = 2.5V(2)		-2	mA
		V_{CC} = 3V(2)		-12	mA
		V_{CC} = 4.5 to 5.5V		-24	mA
I_{OL}	Low-level output current	V_{CC} = 1.8V(2)		1	mA
		V_{CC} = 2.5V(2)		2	mA
		V_{CC} = 3V(2)		12	mA
		V_{CC} = 4.5 to 5.5V		24	mA
T_A	Operating free-air temperature		-55	125	°C

(1) PDIP package only.
(2) SOIC package only.

4.3 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
N (PDIP)	14	80	—	—	—	—	N/A	°C/W
D (SOIC)	14	132.2	64.8	88.4	11.9	87.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

4.4 Electrical Characteristics (PDIP Package)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	TA = 25°C		− 55°C to 125°C		− 40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going threshold			5V	2.6	3.4	2.6	3.4	2.6	3.4	V
V_{T-} Negative-going threshold			5V	1.6	2.4	1.6	2.4	1.6	2.4	V
ΔVT Hysteresis ($V_{T+} - V_{T-}$)			5V	0.5		0.5		0.5		V
V_{OH}	$V_I = V_{T+}$	I_{OH} = −50µA	1.5V	1.4		1.4		1.4		V
			3V	2.9		2.9		2.9		
			4.5V	4.4		4.4		4.4		
		I_{OH} = −4mA	3V	2.58		2.4		2.48		
		I_{OH} = −24mA	4.5V	3.94		3.7		3.8		
		I_{OH} = −50mA(1)	5.5V			3.85				
		I_{OH} = −75mA(1)	5.5V					3.85		
V_{OL}	$V_I = V_{T-}$	I_{OL}= 50µA	1.5V		0.1		0.1		0.1	V
			3V		0.1		0.1		0.1	
			4.5V		0.1		0.1		0.1	
		I_{OL} = 12mA	3V		0.36		0.5		0.44	
		I_{OL} = 24mA	4.5V		0.36		0.5		0.44	
		I_{OL} = 50mA(1)	5.5V				1.65			
		I_{OL} = 75mA(1)	5.5V							
I_I	$V_I = V_{CC}$ or GND		5.5V		± 0.1		± 0.1		± 0.1	µA
I_{CC}	$V_I = V_{CC}$ or GND	I_O = 0	5.5V		4		80		40	µA
C_i					10		10		10	pF

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50Ω transmission-line drive capability at 85°C and 75Ω transmission-line drive capability at 125°C.

4.5 Electrical Characteristics (SOIC package)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 85°C			-55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going input threshold voltage	1.5V	0.76	0.9	1.05	0.73	0.87	1.01	0.71	0.92	1.15	V
		1.8V	0.87	1.02	1.19	0.84	0.99	1.16	0.82	1.03	1.25	
		2.5V	1.08	1.29	1.51	1.06	1.26	1.48	1.05	1.29	1.55	
		3V	1.23	1.46	1.71	1.21	1.44	1.69	1.21	1.46	1.73	
		4.5V	1.69	1.98	2.3	1.68	1.98	2.31	1.68	1.98	2.31	
		5V	1.84	2.16	2.5	1.83	2.16	2.51	1.83	2.16	2.52	
		5.5V	1.99	2.33	2.7	1.98	2.34	2.72	1.98	2.34	2.73	
V_{T-}	Negative-going input threshold voltage	1.5V	0.4	0.46	0.52	0.4	0.46	0.53	0.33	0.43	0.54	V
		1.8V	0.46	0.53	0.61	0.46	0.54	0.62	0.42	0.51	0.62	
		2.5V	0.61	0.7	0.8	0.61	0.7	0.8	0.61	0.7	0.8	
		3V	0.72	0.82	0.92	0.72	0.82	0.93	0.71	0.82	0.94	
		4.5V	1.01	1.16	1.32	1.01	1.17	1.33	1	1.17	1.34	
		5V	1.1	1.27	1.45	1.1	1.28	1.46	1.09	1.28	1.47	
		5.5V	1.19	1.38	1.57	1.2	1.39	1.59	1.18	1.39	1.6	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.5V	0.35	0.45	0.55	0.33	0.4	0.48	0.31	0.51	0.74	V
		1.8V	0.4	0.49	0.6	0.37	0.46	0.55	0.35	0.53	0.73	
		2.5V	0.46	0.58	0.72	0.44	0.56	0.69	0.43	0.59	0.78	
		3V	0.5	0.64	0.79	0.49	0.62	0.76	0.48	0.64	0.83	
		4.5V	0.67	0.82	0.99	0.66	0.81	0.98	0.66	0.82	1.01	
		5V	0.74	0.89	1.06	0.72	0.88	1.06	0.72	0.89	1.07	
		5.5V	0.8	0.96	1.14	0.78	0.95	1.13	0.77	0.95	1.15	
V_{OH}	I_{OH} = -50µA	1.5V	1.4			1.4			1.4	1.499		V
		1.8V	1.7	1.79		1.7			1.7	1.799		
		2.5V	2.4	2.49		2.4			2.4	2.499		
		3V	2.9	2.99		2.9			2.9	2.999		
		4.5V	4.4	4.49		4.4			4.4	4.499		
		5.5V	5.4	5.49		5.4			5.4	5.499		
	I_{OH} = -1mA	1.8V	1.53			1.5			1.44			
	I_{OH} = -2mA	2.5V	2.13			2.1			2			
	I_{OH} = -4mA	3V	2.58			2.48			2.4			
	I_{OH} = -12mA	3V	2.58			2.48			2.4			
	I_{OH} = -24mA	4.5V	3.94			3.8			3.7			
	I_{OH} = -24mA	5.5V	4.94			4.8			4.7			
	I_{OH} = -75mA(1)	5.5V				3.85			3.85			
	I_{OH} = -50mA(1)	5.5V							3.85			

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 85°C			-55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	I_{OL} = 50µA	1.5V			0.1			0.1		0.001	0.1	V
		1.8V			0.1			0.1		0.001	0.1	
		2.5V			0.1			0.1		0.001	0.1	
		3V		0.002	0.1			0.1		0.001	0.1	
		4.5V		0.001	0.1			0.1		0.001	0.1	
		5.5V		0.001	0.1			0.1		0.001	0.1	
	I_{OL} = 1mA	1.8V			0.2			0.3			0.36	
	I_{OL} = 2mA	2.5V			0.36			0.44			0.5	
	I_{OL} = 4mA	3V			0.36			0.44			0.5	
	I_{OL} = 12mA	3V			0.36			0.44			0.5	
	I_{OL} = 24mA	4.5V			0.36			0.44			0.5	
	I_{OL} = 24mA	5.5V			0.36			0.44			0.5	
	I_{OL} = 75mA(1)	5.5V						1.65			1.65	
	I_{OL} = 50mA(1)	5.5V									1.65	
I_I	V_I = 5.5V or GND	0V to 5.5V			±0.1			±1			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5V			2			20			20	µA
C_I	V_I = V_{CC} or GND	5V		2								pF
C_{PD}	C_L = 50pF, F = 1MHz	5V		12								pF

(1) Duration not to exceed 2ms

4.6 Switching Characteristics (PDIP Package)

over operating free-air temperature range V_{CC} = 5V ± 0.5V, C_L = 50pF (unless otherwise noted)

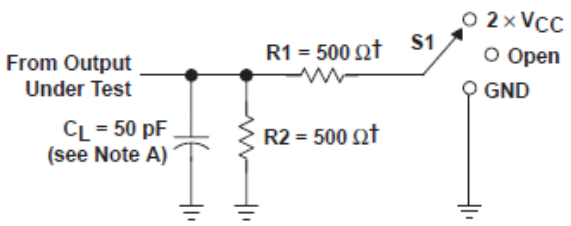
PARAMETER	FROM (INPUT)	TO (OUTPUT)	− 55°C TO 125°C		− 40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.6	10.5	2.7	9.5	ns
t_{PHL}			2.6	10.5	2.7	9.5	

4.7 Switching Characteristics (SOIC package)

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

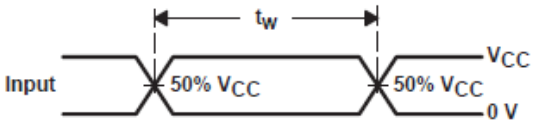
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			-40°C to 85°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1.5V	8.7	14.9	22.2	8.2	15.1	23	8.1	15.2	23.4	ns
			1.8V	7	10.8	15.2	6.6	11.1	16.4	6.4	11.3	17	ns
			2.5V	5.5	7.7	10.3	5.1	7.9	11.2	5	8.1	11.7	ns
			3.3V	4.9	6.8	8.9	4.6	6.9	9.6	4.5	7	9.9	ns
			5V	4	5.4	6.9	3.8	5.5	7.4	3.8	5.6	7.8	ns
t_{PHL}	A	Y	1.5V	9	15	22	8.7	15	22.3	8.7	15	22.3	ns
			1.8V	7.3	11.3	16	6.9	11.4	16.5	6.8	11.5	16.9	ns
			2.5V	5.1	7.5	10.1	4.8	7.5	10.6	4.7	7.6	10.9	ns
			3.3V	4.5	6.4	8.5	4.2	6.5	9.1	4.1	6.6	9.4	ns
			5V	3.4	4.8	6.3	3.2	4.9	6.7	3.1	4.9	6.9	ns

5 Parameter Measurement Information

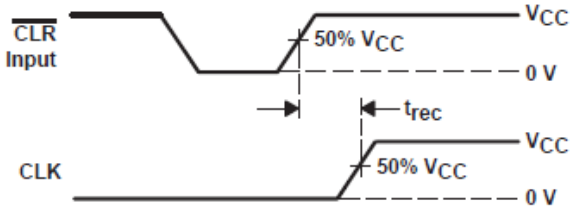


LOAD CIRCUIT

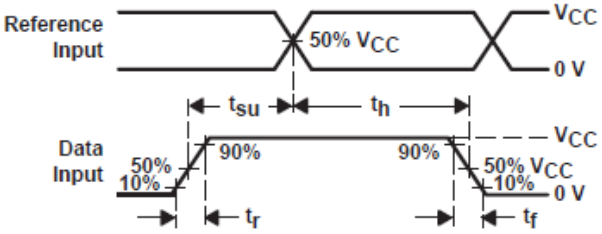
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × VCC GND



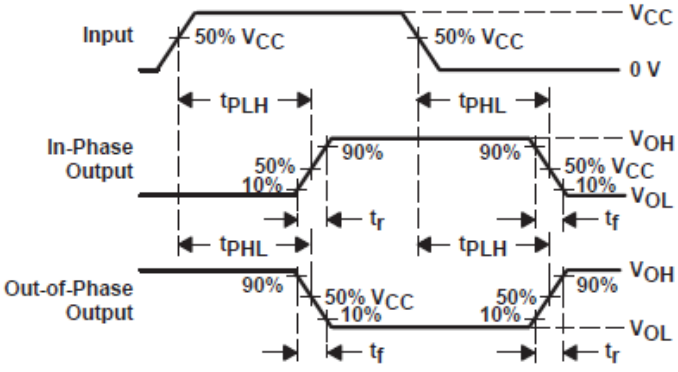
VOLTAGE WAVEFORMS
PULSE DURATION



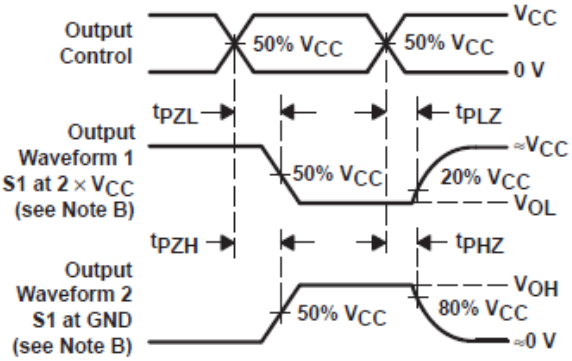
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Figure 5-1. Parameter Measurement Information

6 Detailed Description

6.1 Overview

The CD74AC14 device performs the Boolean function $Y = \overline{A}$. Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_T+) and negative-going (V_T-) signals.

6.2 Functional Block Diagram

Figure 6-1. Logic Diagram, Each Inverter (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table (Each Inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in Section 4.2.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with one supply, 0.1µF is recommended. If there are multiple V_{CC} pins, 0.01µF or 0.022µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. 0.1µF and 1µF are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Section 7.2.2 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

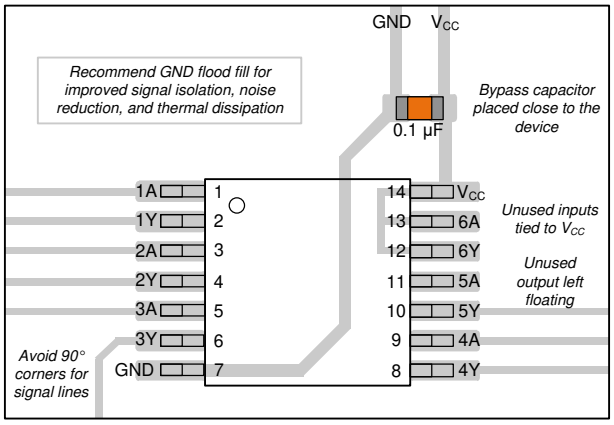


Figure 7-1. Layout Diagram

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2024) to Revision E (June 2026)	Page
• Changed the document status from *Production Mix* to *Production Data*	1
• Added input voltage, output voltage, and junction temperature limits to absolute maximum ratings	4
• Changed supply voltage maximum from 6V to 7V, and continuous current through VCC or GND from 100mA to 200mA in absolute maximum ratings for SOIC package only	4
• Added output current values for 1.8V, 2.5V, and 3V in recommended operating conditions for SOIC package only	4
• Changed supply voltage maximum from 5.5V to 6V in recommended operating conditions for SOIC package only	4
• Changed $R_{\Theta JA}$ for D package from 89.9°C/W to 132.2°C/W	5
• Added Electrical Characteristics table for SOIC package only	6
• Added specifications for 1.5V, 1.8V, 2.5V, 3V, 4.5V, 5V, and 5.5V supply voltages to Electrical Characteristics table for SOIC package only	6
• Changed VT- at 5V (min, max) at 25°C from (1.6V, 2.4V) to (1.1V, 1.45V), at -40°C to 85°C from (1.6V, 2.4V) to (1.1V, 1.46V), at -55°C to 125°C from (1.6V, 2.4V) to (1.09V, 1.47V) for SOIC package only	6
• Changed ΔVT at 5V (min, max) at 25°C from (0.5V, —) to (0.74V, 1.06V), at -40°C to 85°C from (0.5V, —) to (0.72V, 1.06V), at -55°C to 125°C from (0.5V, —) to (0.77V, 1.15V) for SOIC package only	6
• Changed duration of 50mA and 75mA test maximum from 1s to 2ms for SOIC package only	6
• Changed maximum static supply current at 25℃ from 4µA to 0.1µA, at -40℃ to 85℃ from 40µA to 20µA, and at -55℃ to 125℃ from 80µA to 20µA for SOIC package only	6
• Changed typical input capacitance from 4.5pF to 2pF, and typical power dissipation capacitance from 25pF to 12pF for SOIC package only	6
• Added Switching Characteristics table for SOIC package only	7

- Removed Operating Characteristics table; C_{pd} moved to Electrical Characteristics table..... 7
- Updated *Layout Example* image..... 10

Changes from Revision C (May 2023) to Revision D (August 2024) **Page**

- Added *Application and Implementation*section, Device and Documentation Support section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Added package size to *Package Information* table..... 1
- Changed packages from E and M to N and D throughout data sheet.....1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74AC14E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC14E
CD74AC14E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC14E
CD74AC14EE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC14E
CD74AC14M	Obsolete	Production	SOIC (D) | 14	-	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC14M
CD74AC14M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC14M
CD74AC14M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC14M
CD74AC14M961G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC14M
CD74AC14M961G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC14M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

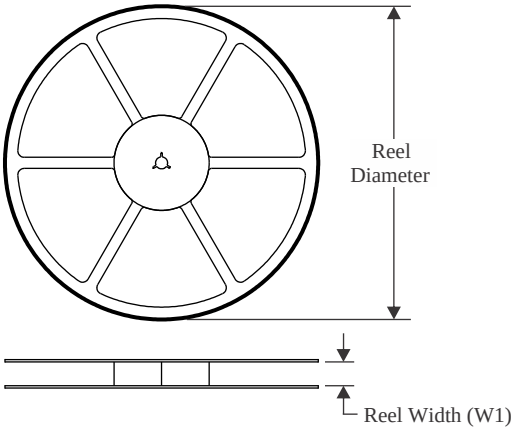
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

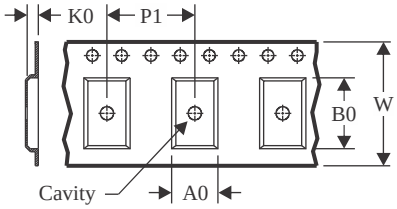
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

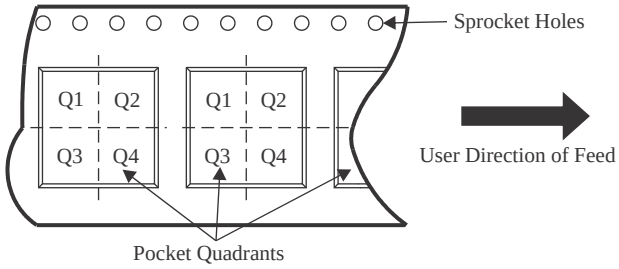


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

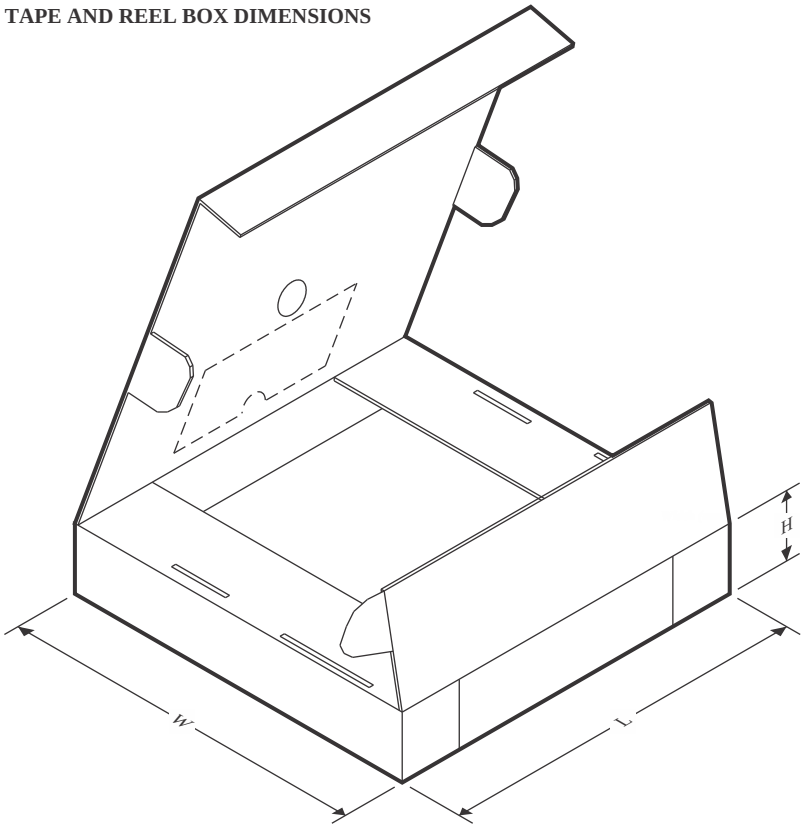
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC14M96	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
CD74AC14M961G4	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

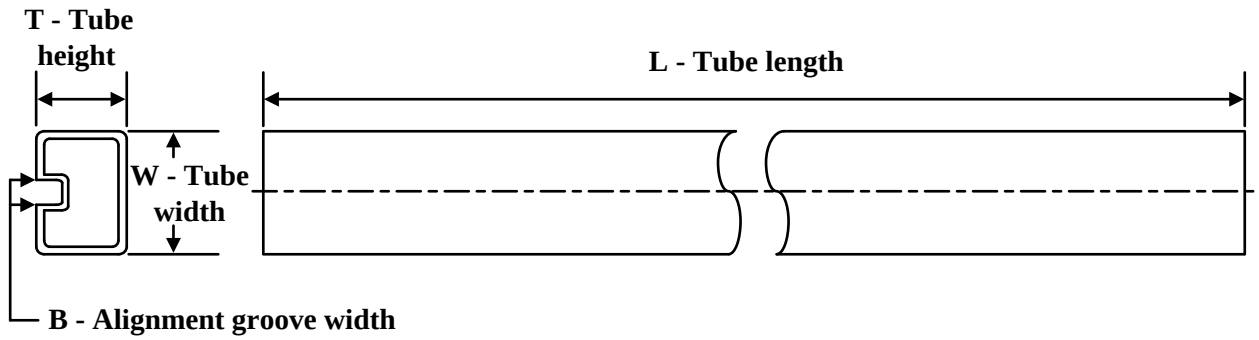
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

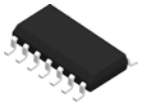
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC14M96	SOIC	D	14	2500	340.5	336.1	32.0
CD74AC14M961G4	SOIC	D	14	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC14E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14M	D	SOIC	14	50	506.6	8	3940	4.32

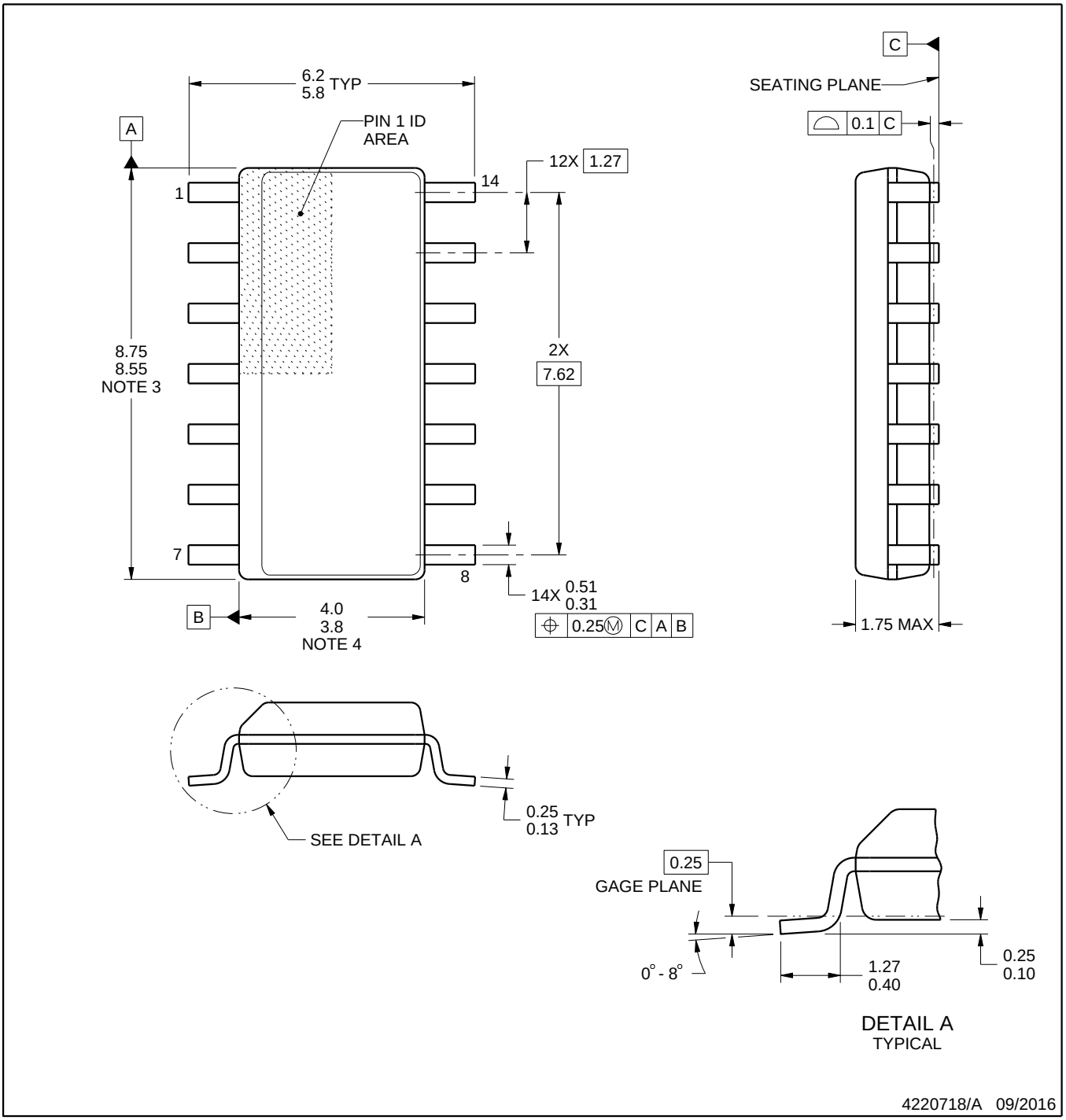


PACKAGE OUTLINE

D0014A

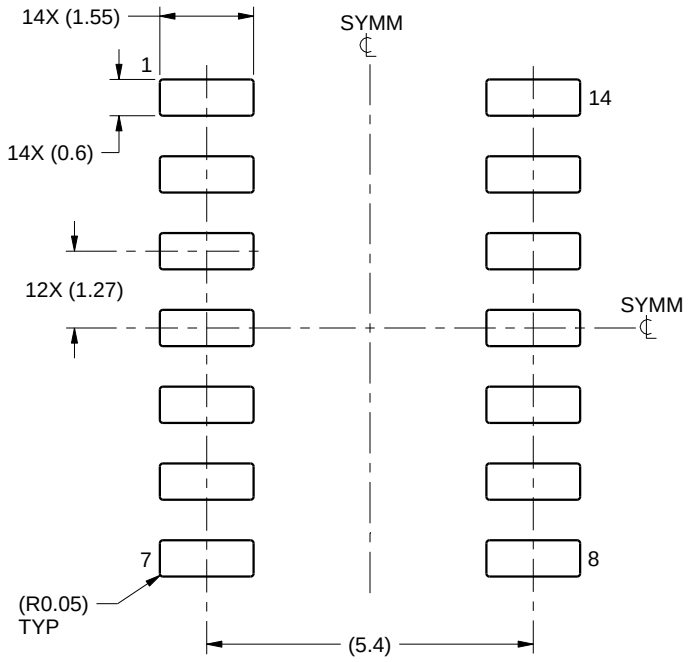
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

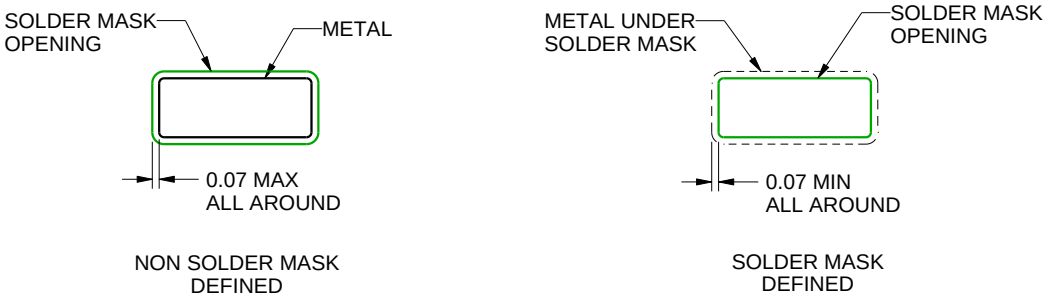


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

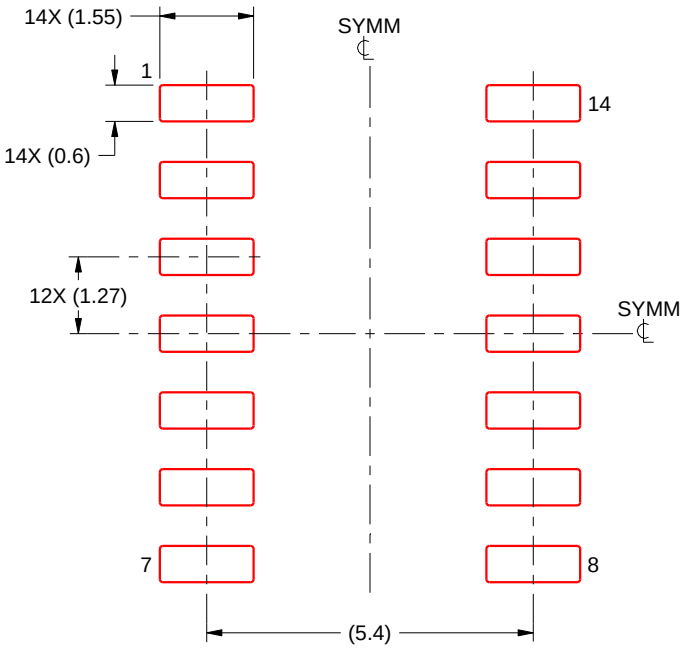
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

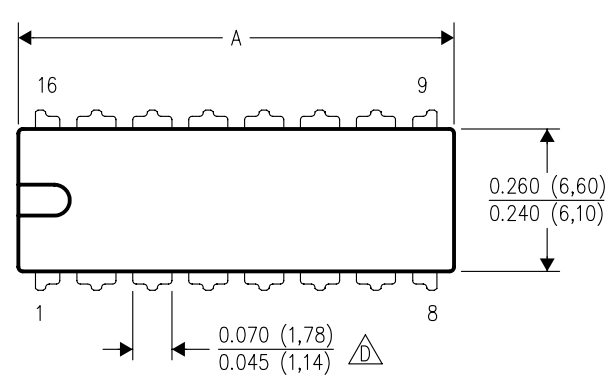
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

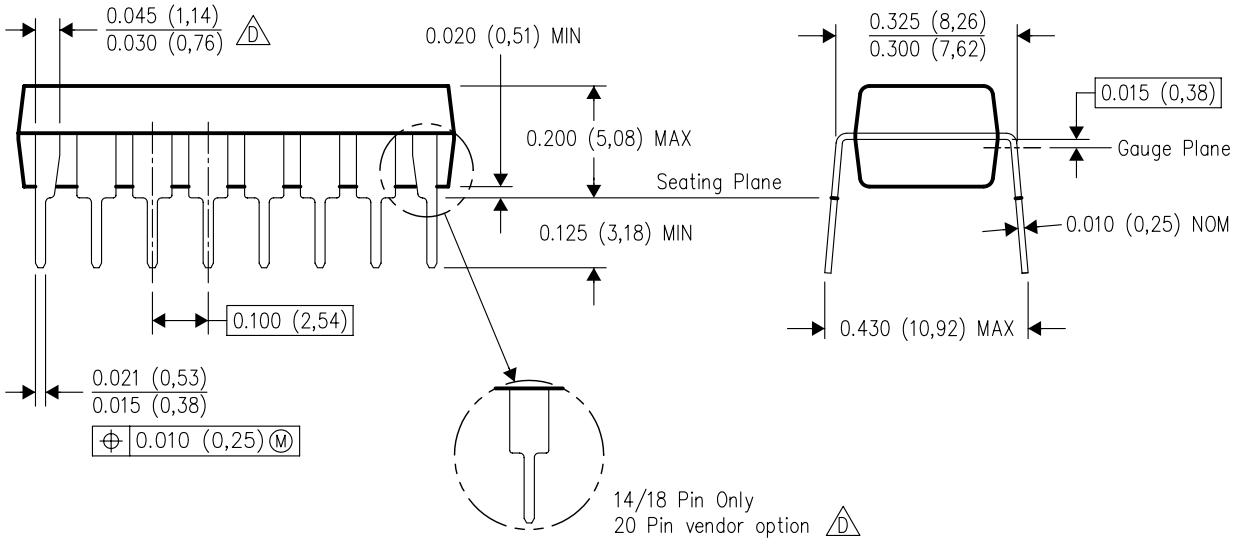
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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