

High-Speed CMOS Logic 4-Bit Parallel Access Register

Features

- Asynchronous Master Reset
- J, \bar{K} , (D) Inputs to First Stage
- Fully Synchronous Serial or Parallel Data Transfer
- Shift Right and Parallel Load Capability
- Complementary Output From Last Stage
- Buffered Inputs
- Typical $f_{MAX} = 50\text{MHz}$ at $V_{CC} = 5\text{V}$,
 $C_L = 15\text{pF}$, $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{V}$

Description

The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The two modes of operation, shift right (Q_0 - Q_1) and parallel load, are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \bar{K} inputs when the \overline{PE} input is high, and is shifted one bit in the direction Q_0 - Q_1 - Q_2 - Q_3 following each Low to High clock transition. The J and K inputs provide the flexibility of the JK-type input for special applications and by tying the two pins together, the simple D-type input for general applications. The device appears as four common-clocked D flip-flops when the \overline{PE} input is Low. After the Low to High clock transition, data on the parallel inputs (D0-D3) is transferred to the respective Q_0 - Q_3 outputs. Shift left operation (Q_3 - Q_2) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the \overline{PE} input low.

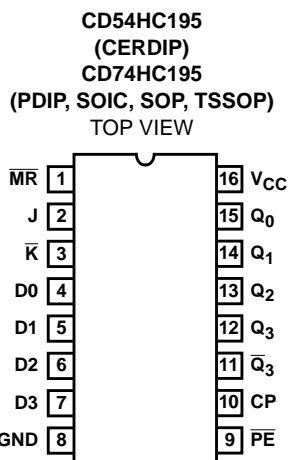
All parallel and serial data transfers are synchronous, occurring after each Low to High clock transition. The 'HC195 series utilizes edge triggering; therefore, there is no restriction on the activity of the J, K, Pn and \overline{PE} inputs for logic operations, other than set-up and hold time requirements. A Low on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs Low, independent of any other input condition.

Ordering Information

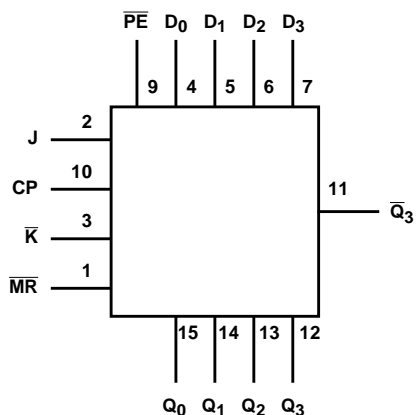
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|--------------|------------------|--------------|
| CD54HC195F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC195E | -55 to 125 | 16 Ld PDIP |
| CD74HC195M | -55 to 125 | 16 Ld SOIC |
| CD74HC195NSR | -55 to 125 | 16 Ld SOP |
| CD74HC195PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC195PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC195PWT | -55 to 125 | 16 Ld TSSOP |

NOTE: When ordering, use the entire part number. The suffix R denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



Functional Diagram



TRUTH TABLE

| OPERATING MODES | INPUTS | | | | | | OUTPUT | | | | |
|---------------------------|-----------------|----|-----------------|---|----------------|----|------------------|----------------|----------------|----------------|------------------|
| | \overline{MR} | CP | \overline{PE} | J | \overline{K} | Dn | Q ₀ | Q ₁ | Q ₂ | Q ₃ | $\overline{Q_3}$ |
| Asynchronous Reset | L | X | X | X | X | X | L | L | L | L | H |
| Shift, Set First Stage | H | ↑ | h | h | h | X | H | q ₀ | q ₁ | q ₂ | $\overline{q_2}$ |
| Shift, Reset First Stage | H | ↑ | h | l | l | X | L | q ₀ | q ₁ | q ₂ | $\overline{q_2}$ |
| Shift, Toggle First Stage | H | ↑ | h | h | l | X | $\overline{q_0}$ | q ₀ | q ₁ | q ₂ | $\overline{q_2}$ |
| Shift, Retain First Stage | H | ↑ | h | l | h | X | q ₀ | q ₀ | q ₁ | q ₂ | $\overline{q_2}$ |
| Parallel Load | H | ↑ | l | X | X | dn | d ₀ | d ₁ | d ₂ | d ₃ | $\overline{d_2}$ |

H = High Voltage Level

L = Low Voltage Level,

X = Don't Care

↑ = Transition from Low to High Level

l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

h = Low Voltage Level One Set-up Time prior to the High to Low Clock Transition,

dn (q_n) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low to High Clock Transition.

CD54HC195, CD74HC195

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | ±20mA |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | ±20mA |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | ±25mA |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | ±50mA |

Operating Conditions

| | |
|--|----------------|
| Temperature Range (T_A) | -55°C to 125°C |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | .4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

Thermal Information

| | |
|--|----------------|
| Package Thermal Impedance, θ_{JA} (see Note 1): | |
| E (PDIP) Package | 67°C/W |
| M (SOIC) Package | 73°C/W |
| NS (SOP) Package | 64°C/W |
| PW (TSSOP) Package | 108°C/W |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |
| (SOIC - Lead Tips Only) | |

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|----------|----------------------|------------|--------------|------|-----|------|---------------|------|----------------|------|-------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

CD54HC195, CD74HC195

Prerequisite For Switching Function

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|------------------|-----------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Clock Frequency | f _{MAX} | - | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | | 4.5 | 30 | - | 25 | - | 20 | - | MHz |
| | | | 6 | 35 | - | 29 | - | 23 | - | MHz |
| MR Pulse Width | t _w | - | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Clock Pulse Width | t _w | - | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Set-up Time J, \bar{K} , \bar{PE} to Clock | t _{SU} | - | 2 | 100 | - | 125 | - | 150 | - | ns |
| | | | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| | | | 6 | 17 | - | 21 | - | 26 | - | ns |
| Hold Time J, K, \bar{PE} to Clock | t _H | - | 2 | 3 | - | 3 | - | 3 | - | ns |
| | | | 4.5 | 3 | - | 3 | - | 3 | - | ns |
| | | | 6 | 5 | - | 3 | - | 3 | - | ns |
| Removal Time, MR to Clock | t _{REM} | - | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | 17 | - | 20 | - | ns |

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|--|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
| | | | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | | | |
| Propagation Delay, CP to Output | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | | 6 | - | 30 | 37 | 45 | ns |
| Propagation Delay, MR to Output | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| Output Transition Times (Figure 1) | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | 75 | 95 | 110 | ns |
| | | | 4.5 | - | 15 | 19 | 22 | ns |
| | | | 6 | - | 13 | 16 | 19 | ns |
| Input Capacitance | C _{IN} | - | - | - | 10 | 10 | 10 | pF |
| CP to Q _n Propagation Delay | t _{PLH} , t _{PHL} | C _L = 15pF | 5 | 14 | - | - | - | ns |
| MR to Q _n | t _{PHL} | C _L = 15pF | 5 | 13 | - | - | - | ns |
| Maximum Clock Frequency | f _{MAX} | C _L = 15pF | 5 | 50 | - | - | - | MHz |
| Power Dissipation Capacitance (Notes 2, 3) | C _{PD} | C _L = 15pF | | 45 | - | - | - | pF |

NOTES:

2. C_{PD} is used to determine the dynamic power consumption, per flip-flop.
3. P_D = V_{CC}² f_i + ∑ (C_L V_{CC}² + f_O) where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveforms

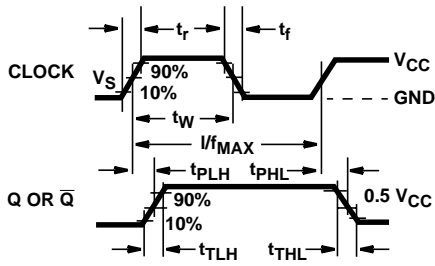


FIGURE 1. CLOCK PREREQUISITE AND PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES

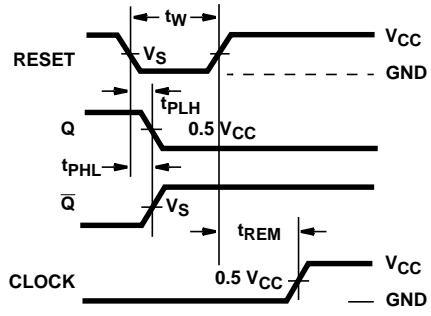


FIGURE 2. MASTER RESET PREREQUISITE AND PROPAGATION DELAYS

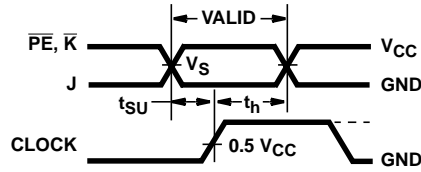


FIGURE 3. J, \bar{K} , OR PARALLEL ENABLE PREREQUISITE TIMES

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD74HC195E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC195E | Samples |
| CD74HC195M | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -55 to 125 | HC195M | |
| CD74HC195M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC195M | Samples |
| CD74HC195NSR | ACTIVE | SOP | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC195M | Samples |
| CD74HC195PW | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -55 to 125 | HJ195 | |
| CD74HC195PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ195 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

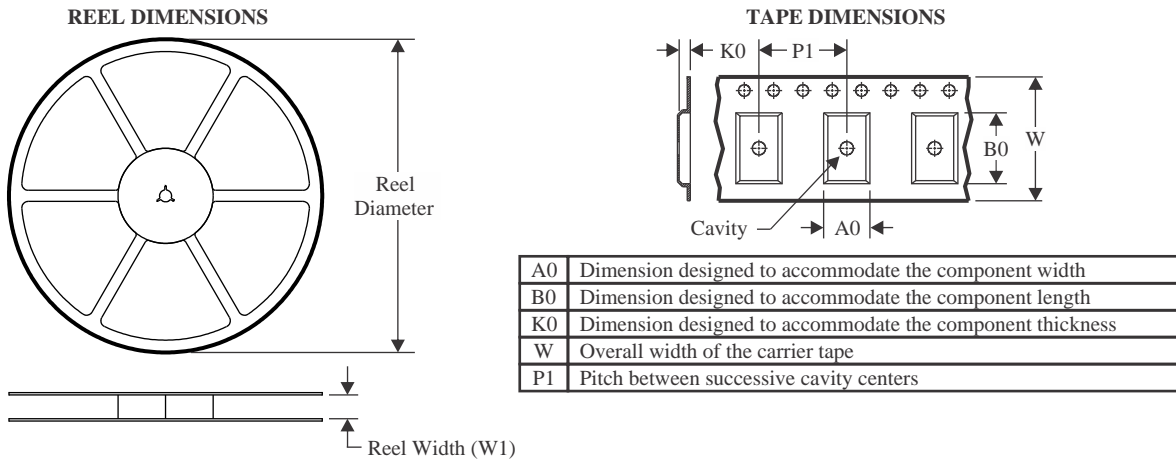
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC195M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC195NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC195PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC195M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HC195NSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD74HC195PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC195E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC195E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

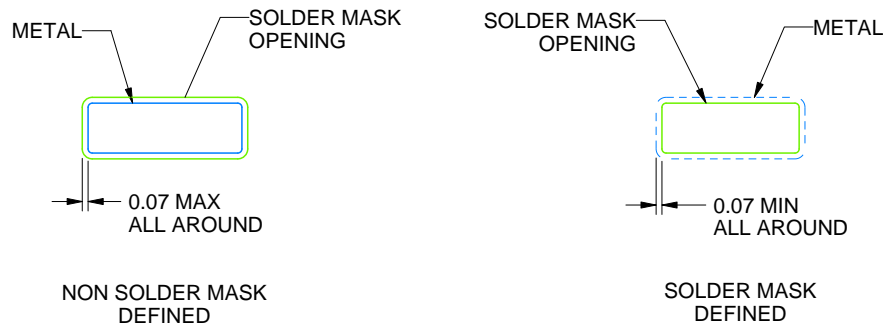
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

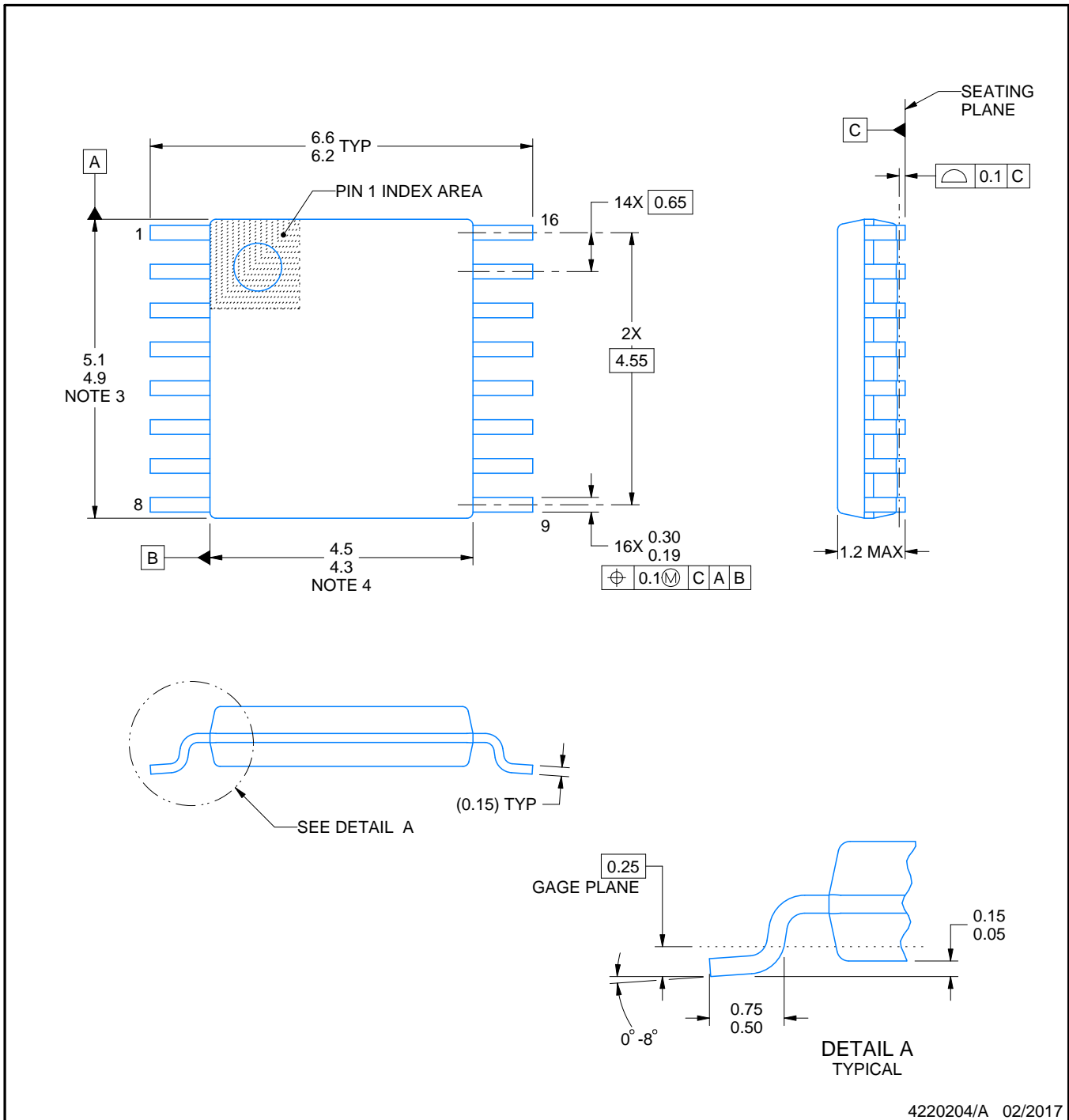
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

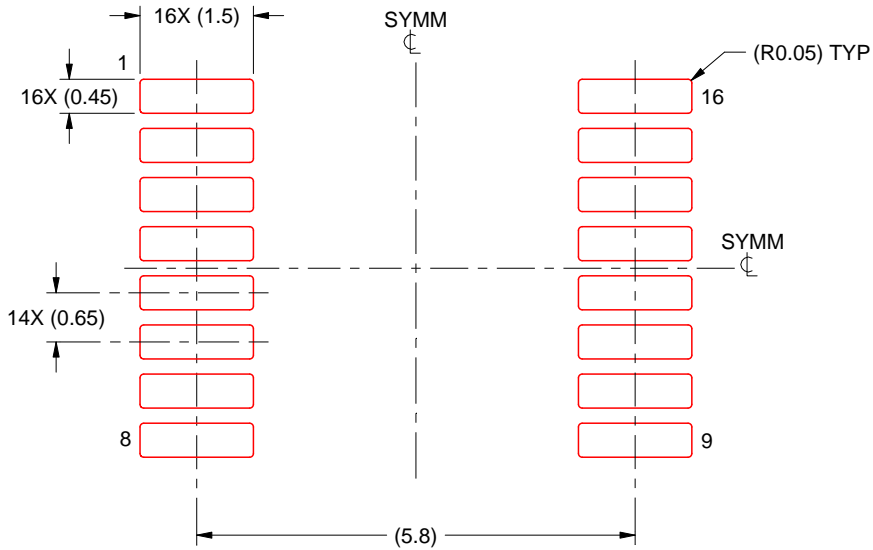
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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