TEXAS INSTRUMENTS
SCHS167G – NOVEMBER 1998 – REVISED OCTOBER 2022

CDx4HC240, CDx4HCT240, CD74HC241, CDx4HCT241, CDx4HC244, CDx4HCT244 High-Speed CMOS Logic Octal Buffer/Line Drivers, Three-State

1 Features

- HC/HCT240 Inverting
- HC/HCT241 Non-inverting
- HC/HCT244 Non-inverting
- Typical propagation delay = 8ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C for HC240
- Three-state outputs
- Buffered inputs
- High-current bus driver outputs
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: –55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types:
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types:
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

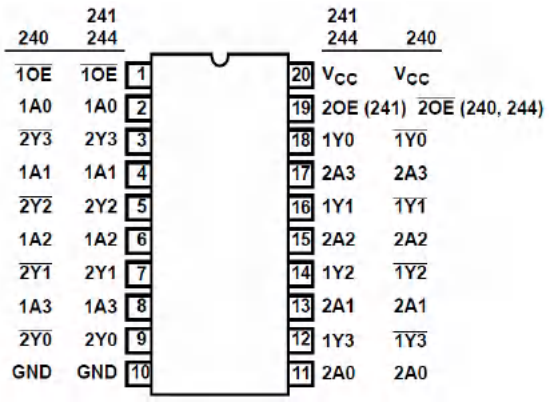
2 Description

The ’HC240 and ’HCT240 are inverting three-state buffers having two active-low output enables. The CD74HC241, ’HCT241, ’HC244 and ’HCT244 are non-inverting three-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD74HC240	M (SOIC, 20)	12.80 mm × 7.50 mm
	E (PDIP, 20)	25.40 mm × 6.35 mm
CD54HC240	F (CDIP, 20)	26.92 mm × 6.92 mm
CD74HCT240	M (SOIC, 20)	12.80 mm × 7.50 mm
	E (PDIP, 20)	25.40 mm × 6.35 mm
	PW (TSSOP, 20)	6.50 mm × 4.40 mm
CD54HCT240	F (CDIP, 20)	26.92 mm × 6.92 mm
CD74HC241	M (SOIC, 20)	12.80 mm × 7.50 mm
	E (PDIP, 20)	25.40 mm × 6.35 mm
CD74HCT241	M (SOIC, 20)	12.80 mm × 7.50 mm
	E (PDIP, 20)	25.40 mm × 6.35 mm
CD54HCT241	F (CDIP, 20)	26.92 mm × 6.92 mm
CD74HC244	M (SOIC, 20)	12.80 mm × 7.50 mm
	E (PDIP, 20)	25.40 mm × 6.35 mm
CD54HC244	F (CDIP, 20)	26.92 mm × 6.92 mm
CD74HCT244	M (SOIC, 20)	12.80 mm × 7.50 mm
	E (PDIP, 20)	25.40 mm × 6.35 mm
CD54HCT244	F (CDIP, 20)	26.92 mm × 6.92 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pinout Diagram

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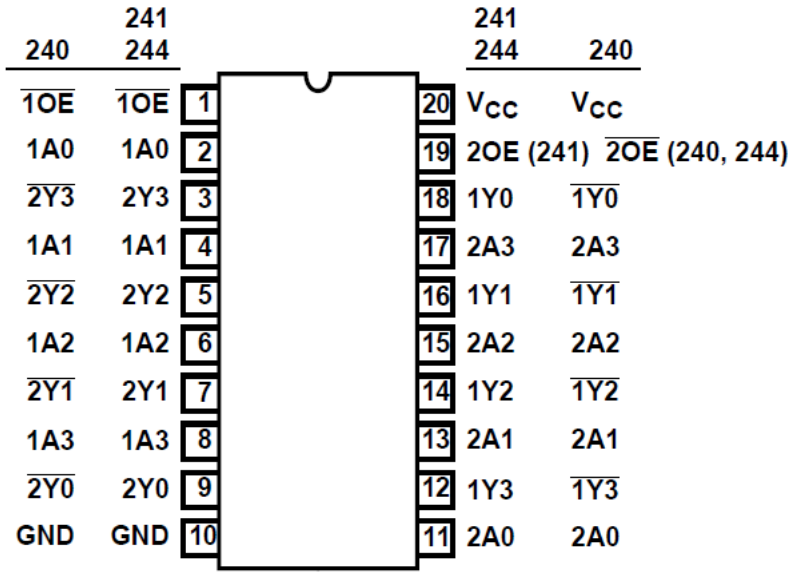
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2004) to Revision F (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1

Changes from Revision F (February 2022) to Revision G (October 2022)	Page
• Increased RθJA for packages: DW (73 to 109.1); DB (82 to 122.7); N (67 to 84.6); NS (64 to 113.4); PW (108 to 131.8)	4

4 Pin Configuration and Functions



J, N, DW, or PW package
20-Pin CDIP, PDIP, SOIC, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp diode current	For $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp diode current	For $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Drain current, per output	For $–0.5 V < V_O < V_{CC} + 0.5$ V		±35	mA
I_O	Output source or sink current per output pin	For $V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		±25	mA
I_{CC}	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	℃
T_{stg}	Storage temperature range		–65	150	℃
	Lead temperature (Soldering 10s) (SOIC - lead tips only)			300	℃

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
t_t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	℃

5.3 Thermal Information

THERMAL METRIC		DW (SOIC) 20 PINS	DB (SSOP) 20 PINS	N (PDIP) 20 PINS	NS (SO) 20 PINS	PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	109.1	122.7	84.6	113.4	131.8	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	76	81.6	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	78.4	82.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	51.5	46.1	55.3	47.1	21.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	°C/W
$R_{\theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics '240

PARAMETER		TEST CONDITIONS[2]	V_{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 7.8 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 µA	6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 6 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 7.8 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			8		80		160	µA
I_{OZ}	Three-state leakage current		6			±0.5		±0.5		±10	µA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	V_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	V_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	V_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage	V_{OL} = 6 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5			8		80		160	µA
I_{OZ}	Three-state leakage current		5.5			±0.5		±5		±10	µA
ΔI_{CC} [1]	Additional supply current per input pin	nA0 - A3 inputs held at V_{CC} – 2.1	4.5 to 5.5		100	540		675		735	µA
		$1\overline{OE}$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	252		315		343	µA
		$2\overline{OE}$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	252		315		343	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Electrical Characteristics '241

PARAMETER		TEST CONDITIONS(2)	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 7.8 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 µA	6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 6 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 7.8 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			8		80		160	µA
I_{OZ}	Three-state leakage current		6			±0.5		±0.5		±10	µA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	V_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	V_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	V_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage	V_{OL} = 6 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5			8		80		160	µA
I_{OZ}	Three-state leakage current		5.5			±0.5		±5		±10	µA
ΔI_{CC} (1)	Additional supply current per input pin	nA0 - A3 inputs held at V_{CC} – 2.1	4.5 to 5.5		100	252		315		343	µA
		$1\overline{OE}$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	252		315		343	µA
		2OE inputs held at V_{CC} – 2.1	4.5 to 5.5		100	540		675		735	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.6 Electrical Characteristics '244

PARAMETER		TEST CONDITIONS(2)	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 7.8 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 µA	6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 6 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 7.8 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			8		80		160	µA
I_{OZ}	Three-state leakage current		6			±0.5		±0.5		±10	µA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	V_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	V_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	V_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage	V_{OL} = 6 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5			8		80		160	µA
I_{OZ}	Three-state leakage current		5.5			±0.5		±5		±10	µA
ΔI_{CC} (1)	Additional supply current per input pin	nA0 - A3 inputs held at V_{CC} – 2.1	4.5 to 5.5		100	252		315		343	µA
		$1\overline{OE}$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	252		315		343	µA
		$2\overline{OE}$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	252		315		343	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.7 Switching Characteristics '240

C_L = 50 pF, Input t_r, t_f = 6 ns

PARAMETER		V_{CC} (V)	25°C			–40°C to 85°C			–55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
t_{PLH}, t_{PHL}	Propagation delay Data to outputs	2			100			125			150	ns
		4.5		8[3]	20			25			30	
		6			17			21			26	
t_{THL}, t_{TLH}	Output enable and disable time	2			150			190			225	ns
		4.5			30			38			45	
		5		12								
		6			26			33			38	
t_{TLH}, t_{THL}	Output transition time	2			60			75			90	ns
		4.5			12			15			18	
		6			10			13			15	
C_I	Input capacitance		10		10		10			10		pF
C_O	Three-state output capacitance				20			20			20	pF
C_{PD}	Power dissipation capacitance[1] [2]	5		38[3]								pF
HCT TYPES												
t_{PHL}, t_{PLH}	Data to outputs	4.5		9[3]	22			28			33	ns
t_{TLH}, t_{THL}	Output enable and disable times	4.5			30			38			45	ns
t_{THL}, t_{TLH}	Output transition time	4.5			12			15			18	ns
C_I	Input capacitance		10		10		10			10		pF
C_{PD}	Power dissipation capacitance[1] [2]	5		40								pF

(1) C_{PD} is used to determine the dynamic power consumption, per channel.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.

5.8 Switching Characteristics '241

C_L = 50 pF, Input t_r, t_f = 6 ns

PARAMETER		V_{CC} (V)	25°C			–40°C to 85°C			–55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
t_{PLH}, t_{PHL}	Propagation delay Data to outputs	2			110			140			165	ns
		4.5		9[3]	22			28			33	
		6			19			24			28	
t_{THL}, t_{TLH}	Output enable and disable time	2			150			190			225	ns
		4.5			30			38			45	
		5		12								
		6			26			33			38	
t_{TLH}, t_{THL}	Output transition time	2			60			75			90	ns
		4.5			12			15			18	
		6			10			13			15	
C_I	Input capacitance		10		10			10			10	pF
C_O	Three-state output capacitance				20			20			20	pF
C_{PD}	Power dissipation capacitance[1] [2]	5		34[3]								pF
HCT TYPES												
t_{PHL}, t_{PLH}	Data to outputs	4.5		10[3]	25			31			38	ns
t_{TLH}, t_{THL}	Output enable and disable times	4.5			30			38			45	ns
t_{THL}, t_{TLH}	Output transition time	4.5			12			15			18	ns
C_I	Input capacitance		10		10			10			10	pF
C_{PD}	Power dissipation capacitance[1] [2]	5		38								pF

(1) C_{PD} is used to determine the dynamic power consumption, per channel.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.

5.9 Switching Characteristics '244

C_L = 50 pF, Input t_r, t_f = 6 ns

PARAMETER		V_{CC} (V)	25°C			–40°C to 85°C			–55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
t_{PLH}, t_{PHL}	Propagation delay Data to outputs	2			110			140			165	ns
		4.5		9[3]	22			28			33	
		6			19			24			28	
t_{THL}, t_{TLH}	Output enable and disable time	2			150			190			225	ns
		4.5			30			38			45	
		5		12								
		6			26			33			38	
t_{TLH}, t_{THL}	Output transition time	2			60			75			90	ns
		4.5			12			15			18	
		6			10			13			15	
C_I	Input capacitance		10		10			10			10	pF
C_O	Three-state output capacitance				20			20			20	pF
C_{PD}	Power dissipation capacitance[1] [2]	5		46[3]								pF
HCT TYPES												
t_{PHL}, t_{PLH}	Data to outputs	4.5		10[3]	25			31			38	ns
t_{TLH}, t_{THL}	Output enable and disable times	4.5			30			38			45	ns
t_{THL}, t_{TLH}	Output transition time	4.5			12			15			18	ns
C_I	Input capacitance		10		10			10			10	pF
C_{PD}	Power dissipation capacitance[1] [2]	5		40								pF

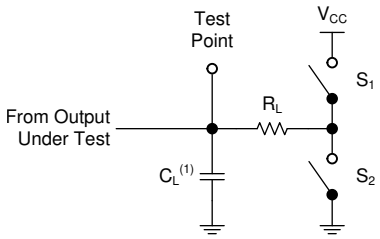
(1) C_{PD} is used to determine the dynamic power consumption, per channel.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

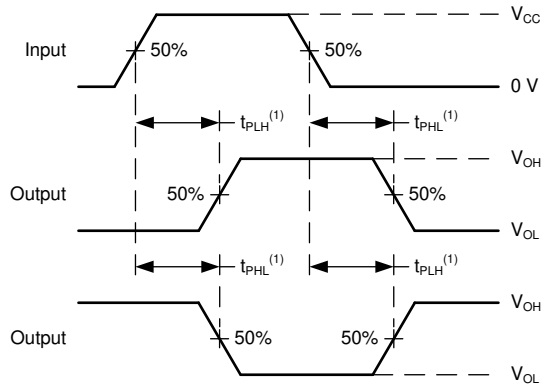
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



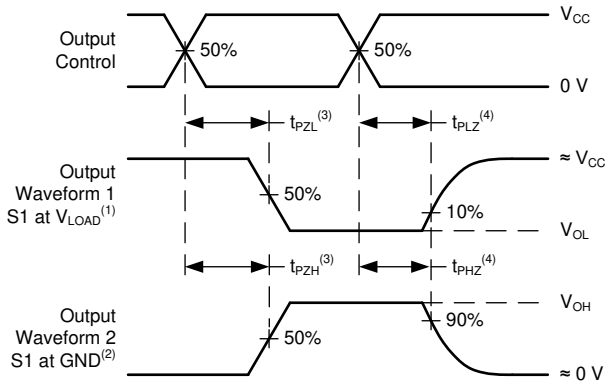
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



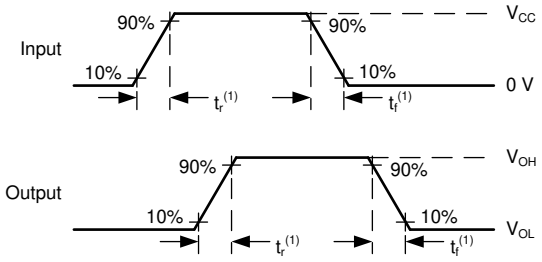
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



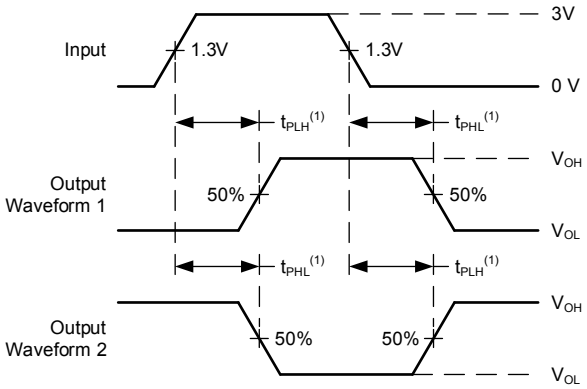
(1) S1 = CLOSED; S2 = OPEN.
(2) S1 = OPEN; s2 = CLOSED.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.
(4) t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-3. Voltage Waveforms, Standard CMOS Inputs Propagation Delays



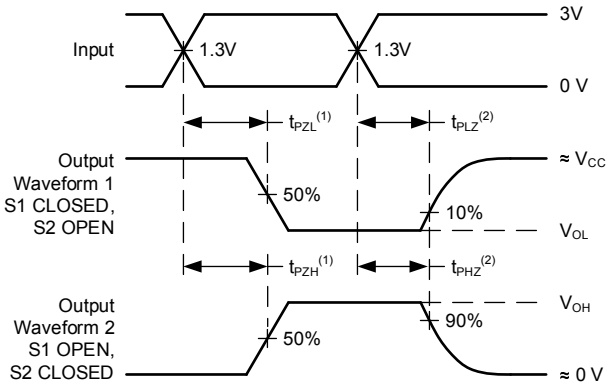
(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-5. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs



(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

7 Detailed Description

7.1 Overview

The ’HC240 and ’HCT240 are inverting three-state buffers having two active-low output enables. The CD74HC241, ’HCT241, ’HC244 and ’HCT244 are non-inverting threestate buffers that differ only in that the 241 has one activehigh and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

7.2 Functional Block Diagram

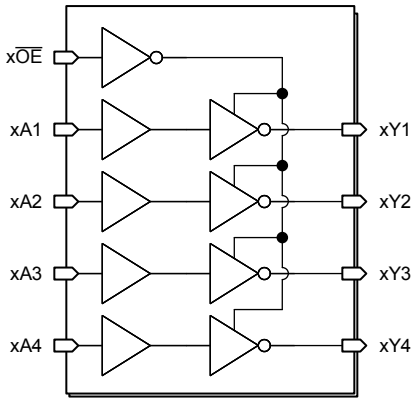


Figure 7-1. Functional Block Diagram '240

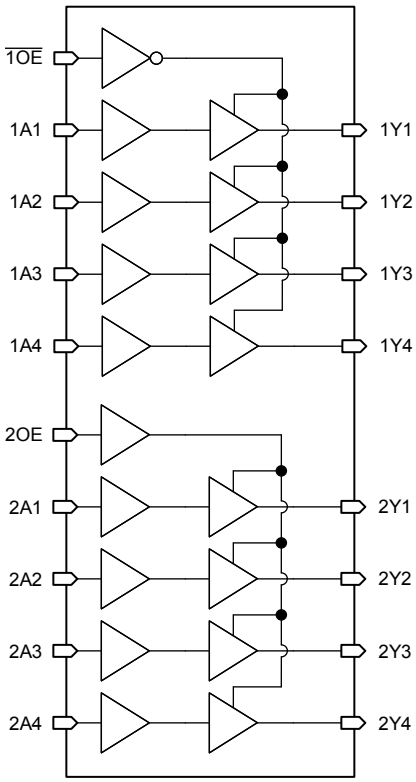


Figure 7-2. Functional Block Diagram '241

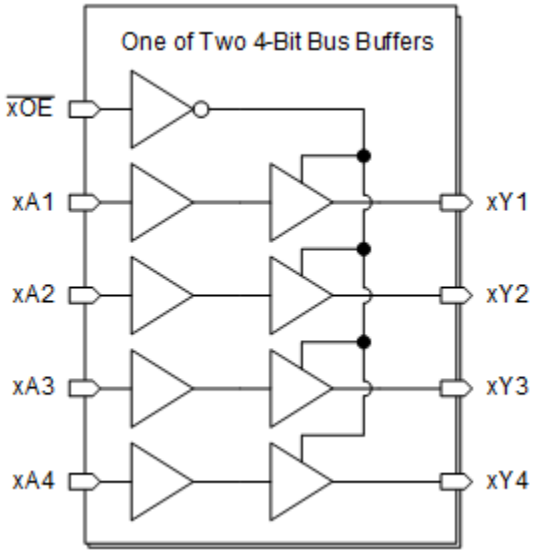


Figure 7-3. Functional Block Diagram '244

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC240F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407401RA CD54HC240F3A	Samples
CD54HC244F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC244F	Samples
CD54HC244F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409601RA CD54HC244F3A	Samples
CD54HCT240F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8550501RA CD54HCT240F3A	Samples
CD54HCT241F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT241F3A	Samples
CD54HCT244F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT244F	Samples
CD54HCT244F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8513001RA CD54HCT244F3A	Samples
CD74HC240E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC240E	Samples
CD74HC240M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HC240M	
CD74HC240M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC240M	Samples
CD74HC241E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC241E	Samples
CD74HC241M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HC241M	
CD74HC241M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC241M	Samples
CD74HC244E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC244E	Samples
CD74HC244EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC244E	Samples
CD74HC244M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HC244M	
CD74HC244M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples
CD74HC244M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples
CD74HC244M96G4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT240E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT240E	Samples
CD74HCT240EE4	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT240E	Samples
CD74HCT240M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HCT240M	
CD74HCT240M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT240M	Samples
CD74HCT240PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-55 to 125	HK240	
CD74HCT240PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK240	Samples
CD74HCT240PWT	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-55 to 125	HK240	
CD74HCT241E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT241E	Samples
CD74HCT241M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT241M	Samples
CD74HCT244E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT244E	Samples
CD74HCT244M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HCT244M	
CD74HCT244M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT244M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC240, CD54HC244, CD54HCT240, CD54HCT241, CD54HCT244, CD74HC240, CD74HC244, CD74HCT240, CD74HCT241, CD74HCT244 :

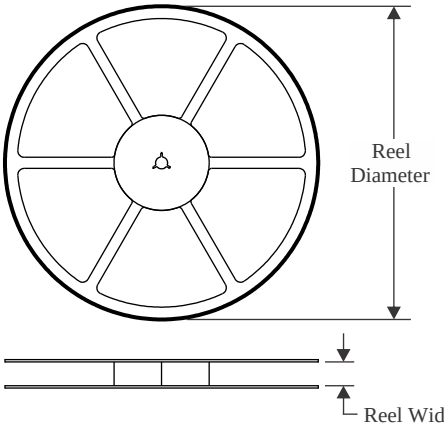
- Catalog : CD74HC240, CD74HC244, CD74HCT240, CD74HCT241, CD74HCT244
- Military : CD54HC240, CD54HC244, CD54HCT240, CD54HCT241, CD54HCT244

NOTE: Qualified Version Definitions:

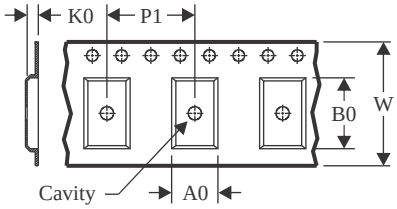
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

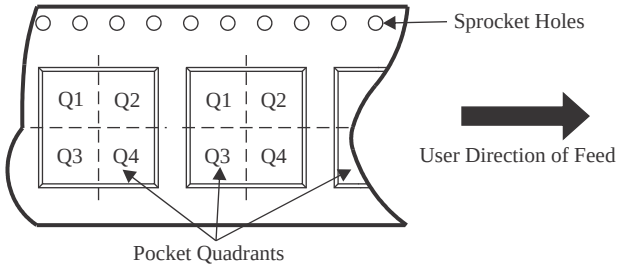


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

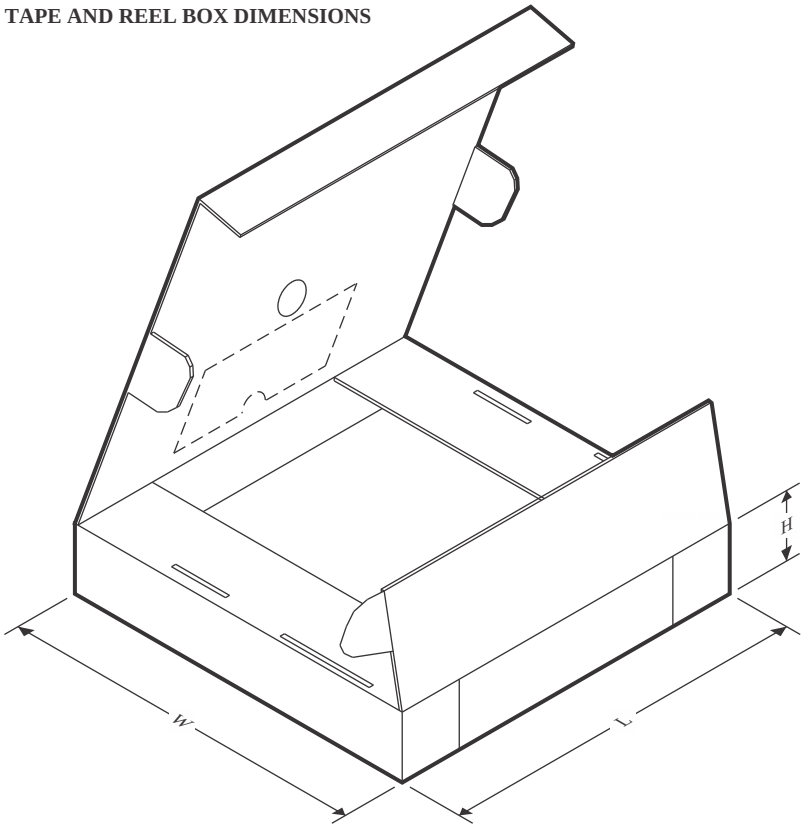
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC240M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC241M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT240M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CD74HCT241M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT241M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT244M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1

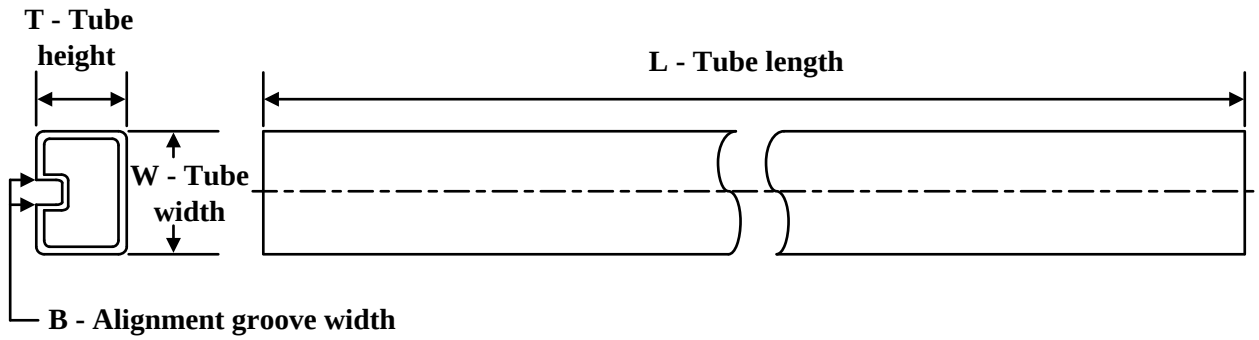
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC240M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC241M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC244M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT240M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT240PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
CD74HCT241M96	SOIC	DW	20	2000	356.0	356.0	41.0
CD74HCT241M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT244M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT244M96	SOIC	DW	20	2000	356.0	356.0	41.0

TUBE



*All dimensions are nominal

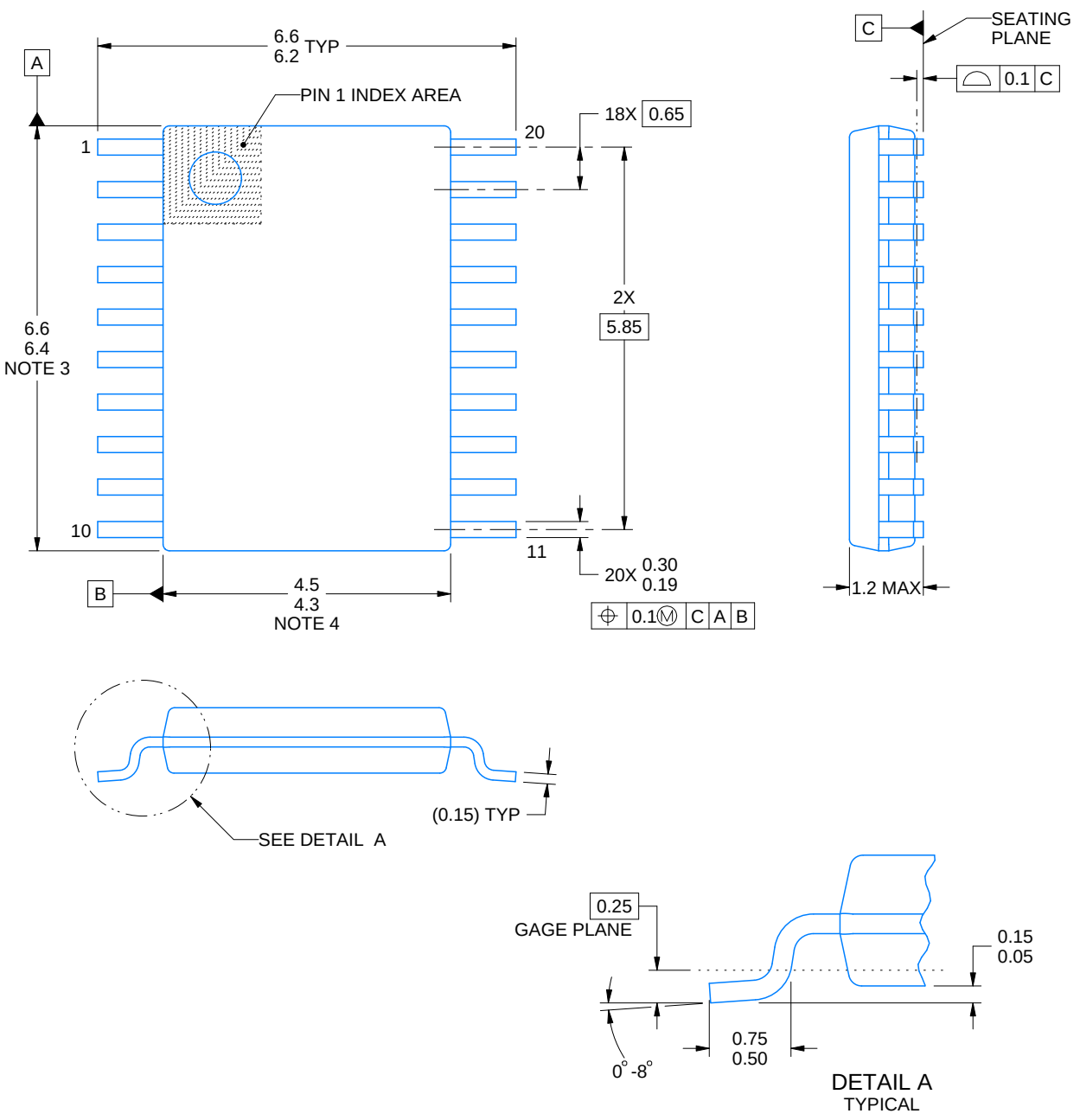
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC240E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC241E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC244E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC244EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT240E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT240EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT241E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT244E	N	PDIP	20	20	506	13.97	11230	4.32

PACKAGE OUTLINE

PW0020A

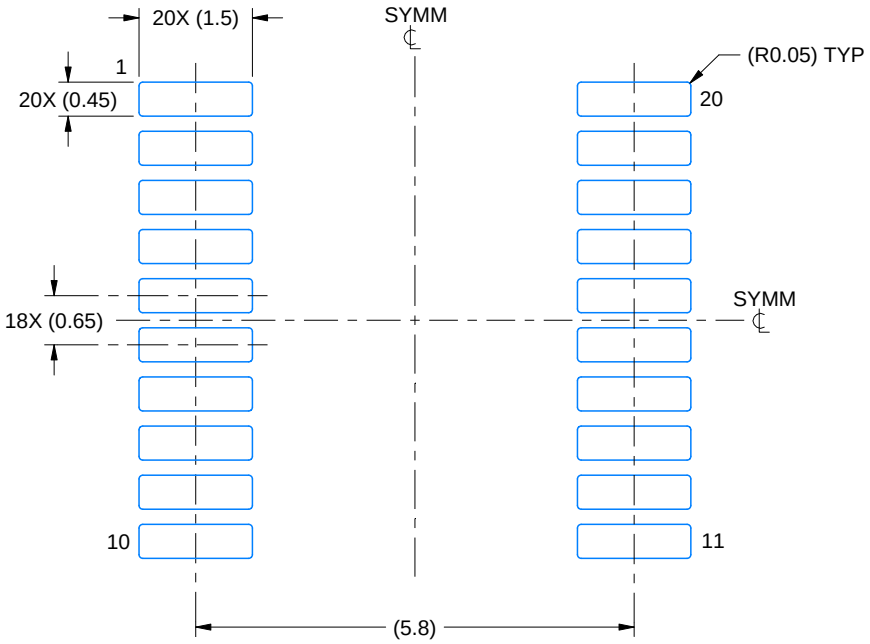
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



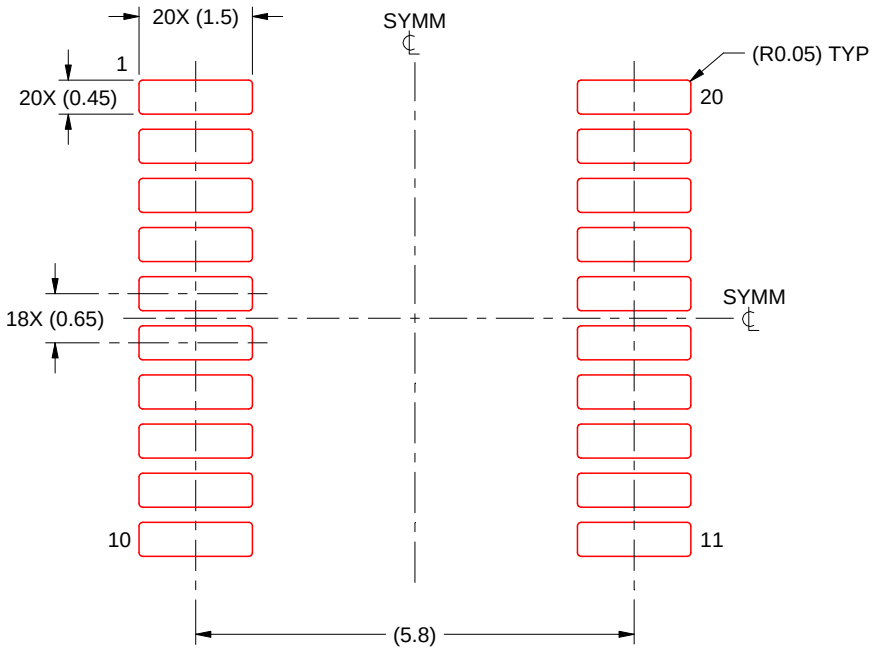
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

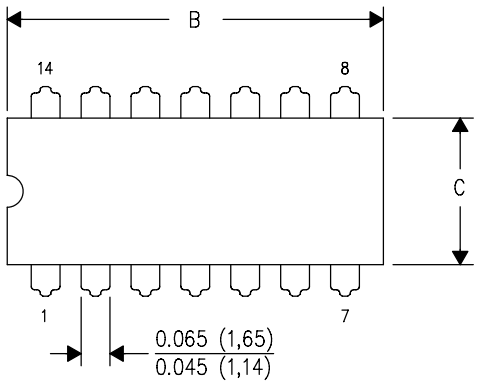
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

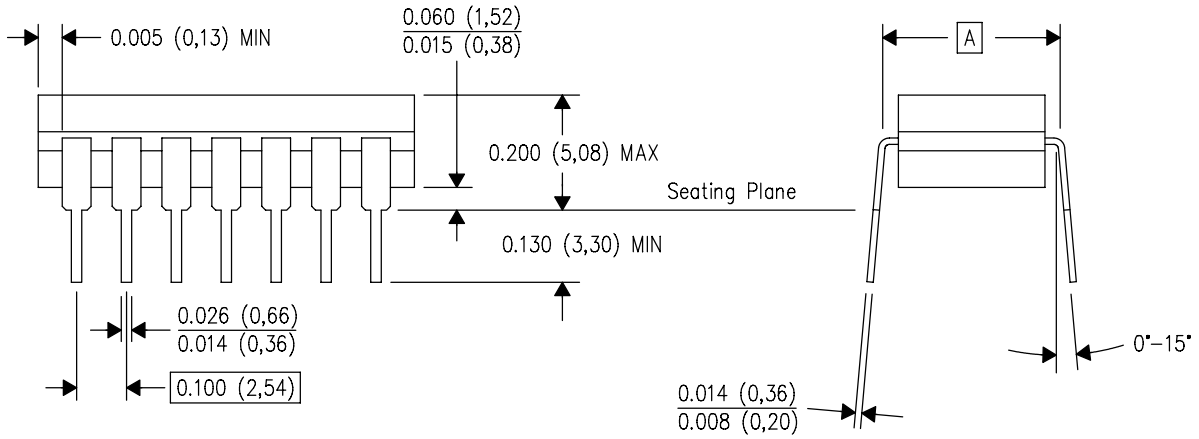
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



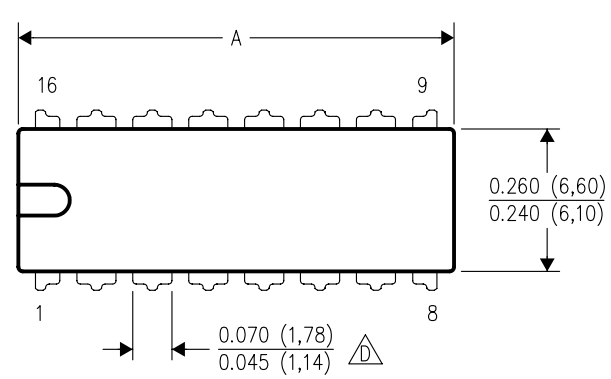
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

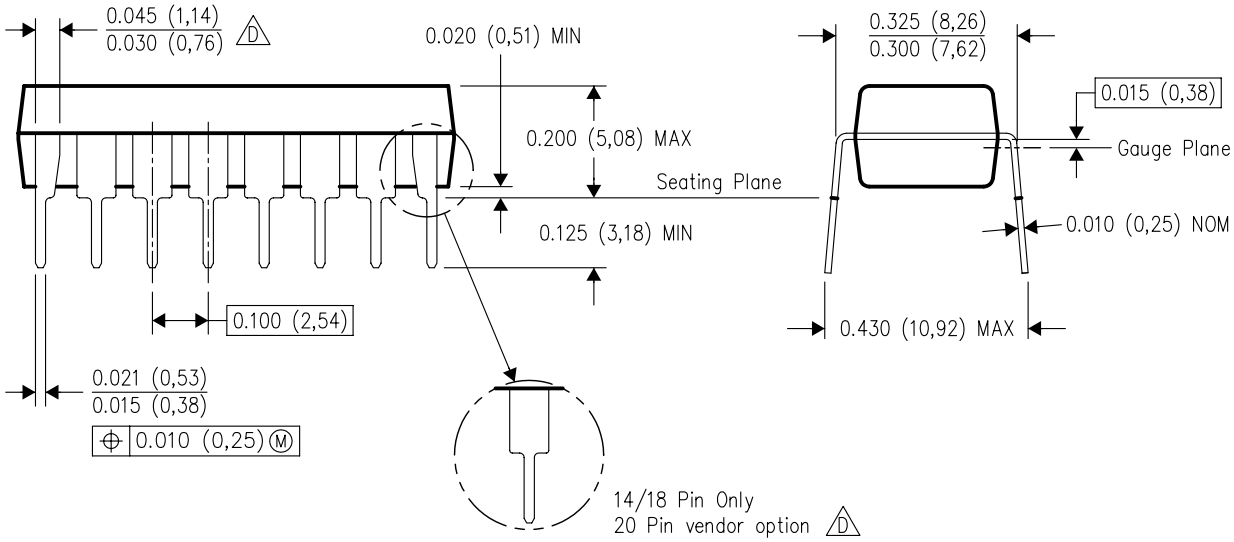
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

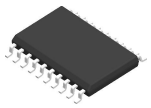


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

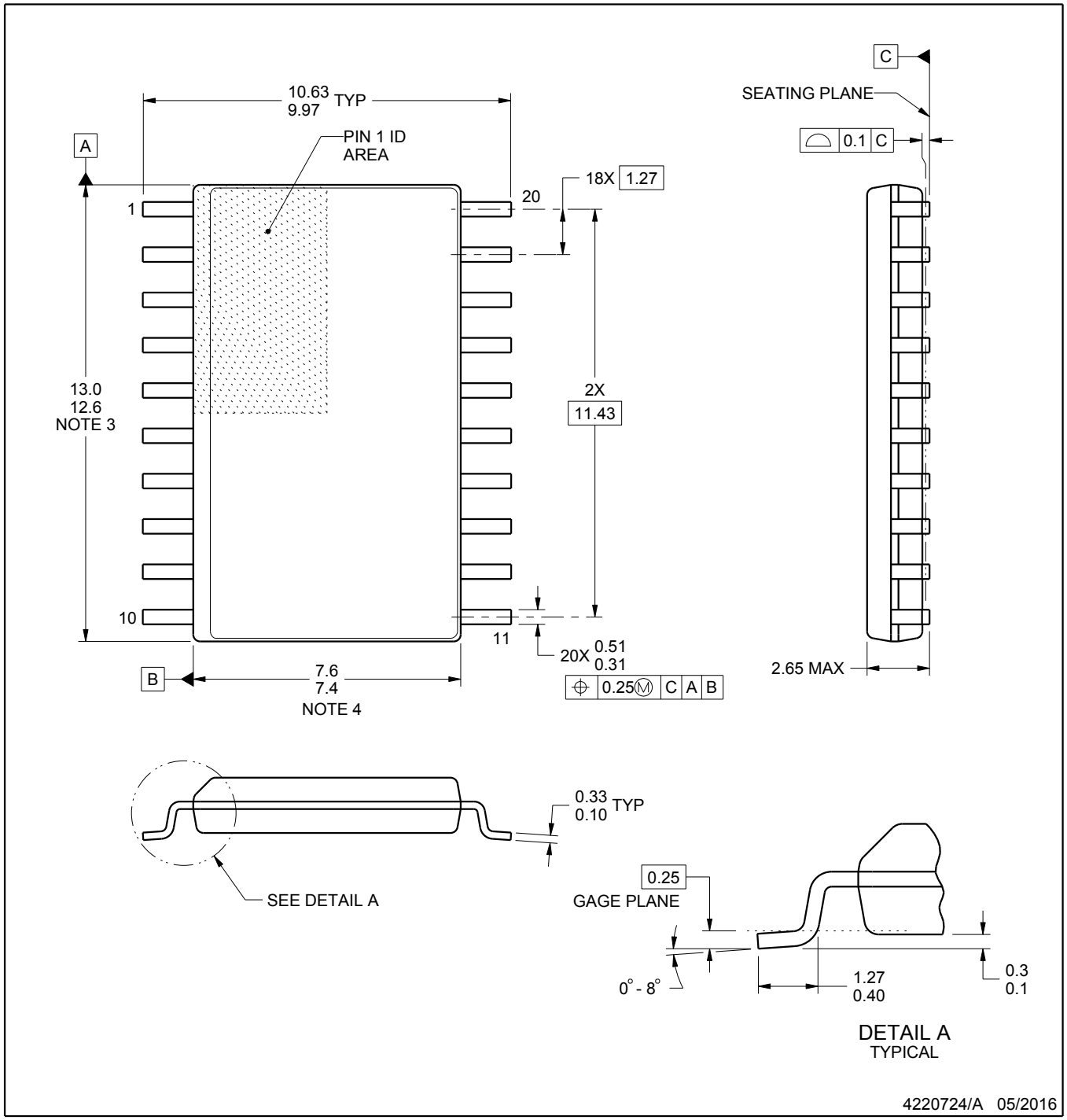


PACKAGE OUTLINE

DW0020A

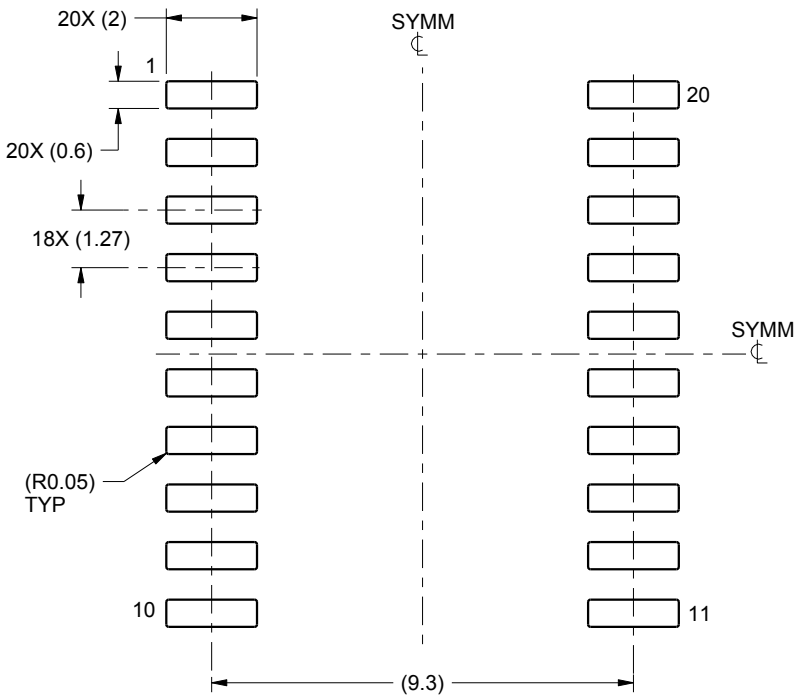
SOIC - 2.65 mm max height

SOIC

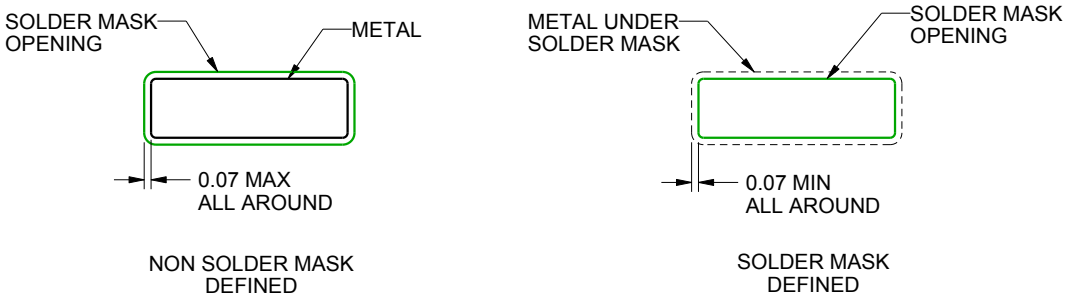


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

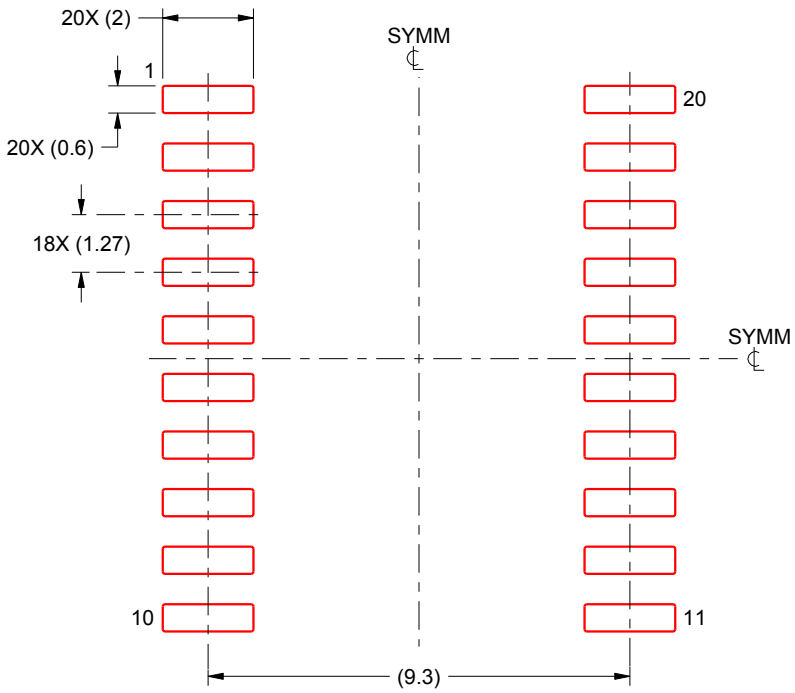


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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