CSD13302W 12 V N Channel NexFET™ Power MOSFET

1 Features

- Ultra Low On Resistance
- Low Q_g and Q_{gd}
- Small Footprint 1 mm × 1 mm
- Low Profile 0.62 mm Height
- Pb Free
- RoHS Compliant
- Halogen Free

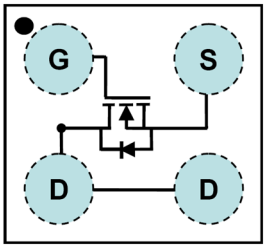
2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This 14.6 mΩ, 12 V, N-Channel device is designed to deliver the lowest on resistance and gate charge in a small 1 x 1 mm outline with excellent thermal characteristics and an ultra low profile.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	6.0		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.1		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	21.2	mΩ
		V_{GS} = 4.5 V	14.6	mΩ
$V_{GS(th)}$	Threshold Voltage	1.0		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD13302W	3000	7-Inch Reel	1.0 mm × 1.0 mm Wafer Level Package	Tape and Reel
CSD13302WT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

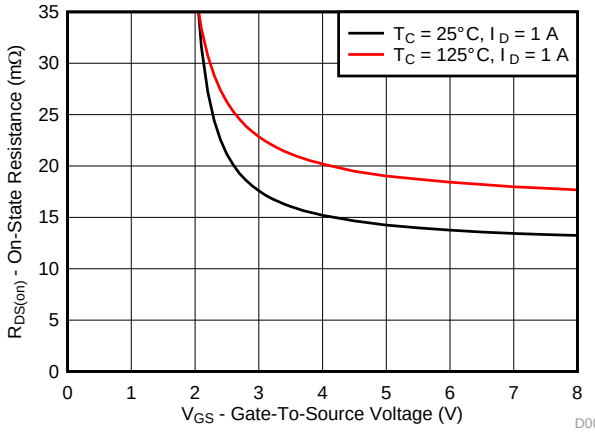
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current (1)	1.6	A
I_{DM}	Pulsed Drain Current (2)	29	A
P_D	Power Dissipation (3)	1.8	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Device Operating at a temperature of 105ºC

(2) Min Cu Typ $R_{\theta JA}$ = 275ºC/W, Pulse width ≤100 µs, duty cycle ≤1%

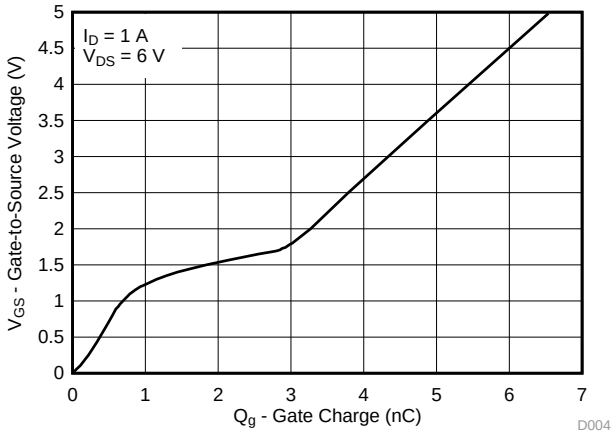
(3) Max Cu Typ $R_{\theta JA}$ = 70ºC/W

$R_{DS(on)}$ vs V_{GS}



D007

Gate Charge



D004

Table of Contents

4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C)

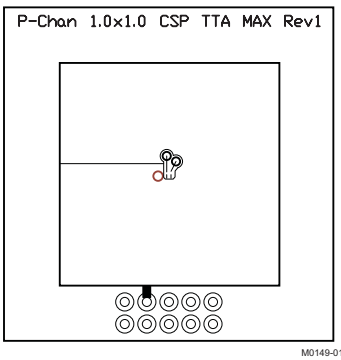
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 , I_D = 250 µA	12			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 10 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.7	1.0	1.3	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V, I_D = 1 A		21.2	25.8	mΩ
		V_{GS} = 4.5 V, I_D = 1 A		14.6	17.1	
g_{fs}	Transconductance	V_{DS} = 1.2 V, I_D = 1 A		10		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		663	862	pF
C_{OSS}	Output Capacitance			211	274	pF
C_{RSS}	Reverse Transfer Capacitance			151	196	pF
R_g	Series Gate Resistance			3.6	7.2	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 6 V, I_D = 1 A		6.0	7.8	nC
Q_{gd}	Gate Charge Gate-to-Drain			2.1		nC
Q_{gs}	Gate Charge Gate-to-Source			0.7		nC
$Q_{g(th)}$	Gate Charge at Vth			0.7		nC
Q_{OSS}	Output Charge	V_{DS} = 6 V, V_{GS} = 0 V		1.3		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 1 A R_G = 0 Ω		6		ns
t_r	Rise Time			7		ns
$t_{d(off)}$	Turn Off Delay Time			17		ns
t_f	Fall Time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = 1 A, V_{GS} = 0 V		0.7	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 6 V, I_S = 1 A, di/dt = 200 A/µs		11.6		nC
t_{rr}	Reverse Recovery Time			19.6		ns

5.2 Thermal Information

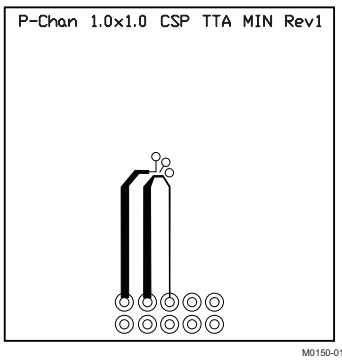
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		275		°C/W
	Junction-to-Ambient Thermal Resistance(2)		70		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Typical $R_{\theta JA}$ = 70°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Typical $R_{\theta JA}$ = 275°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

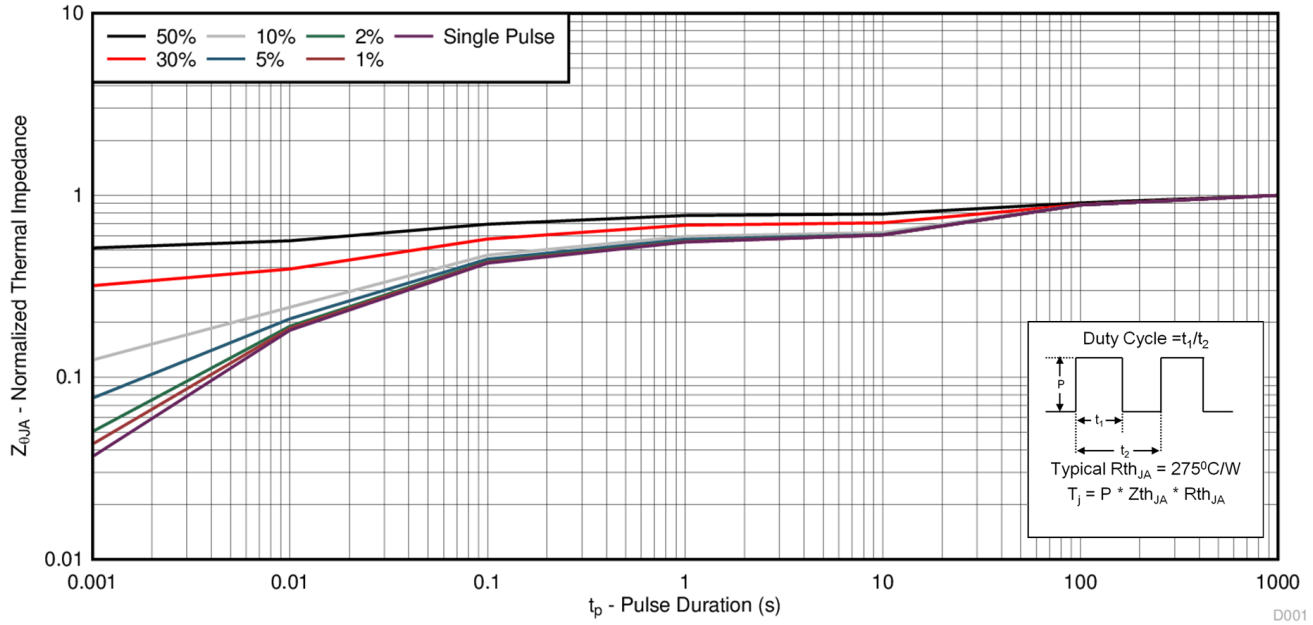


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

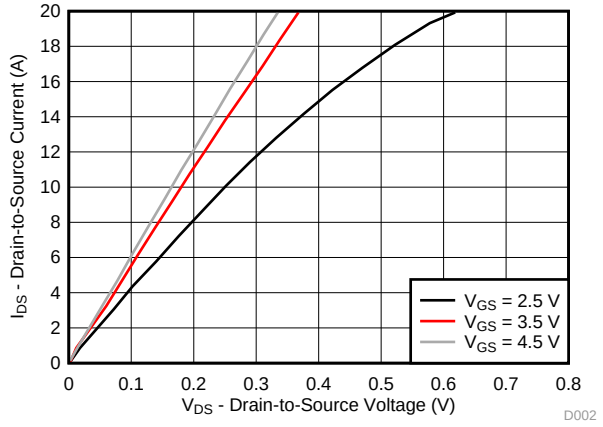


Figure 2. Saturation Characteristics

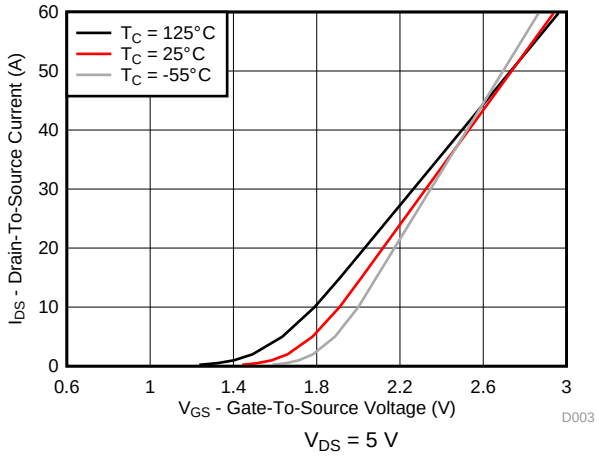


Figure 3. Transfer Characteristics

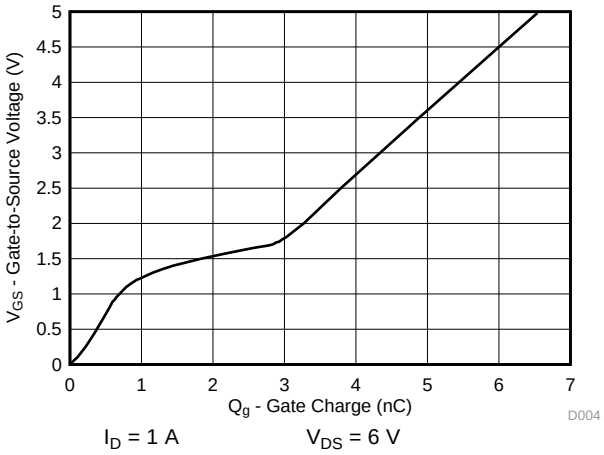


Figure 4. Gate Charge

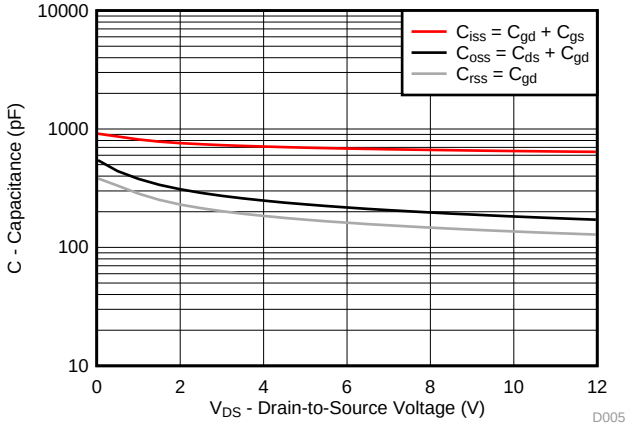


Figure 5. Capacitance

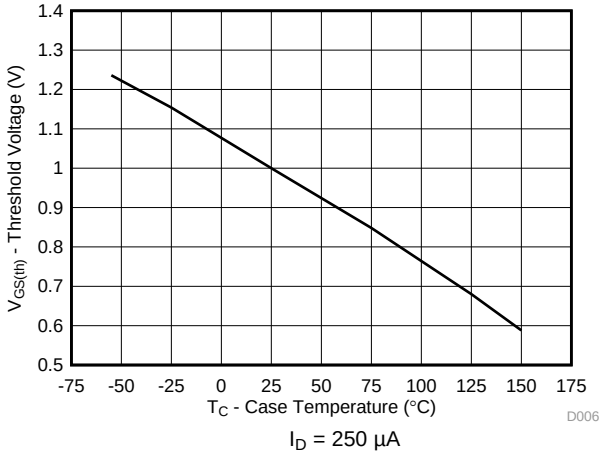


Figure 6. Threshold Voltage vs Temperature

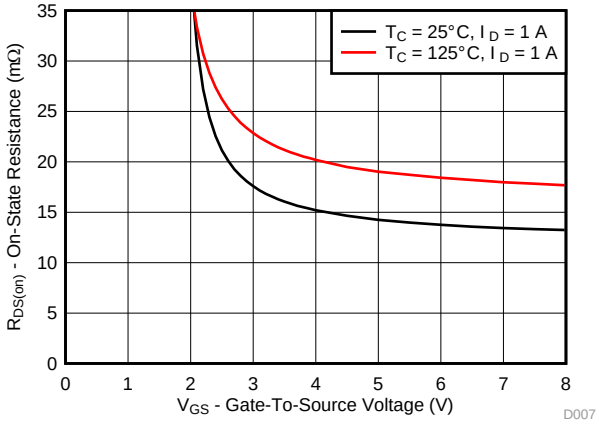


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

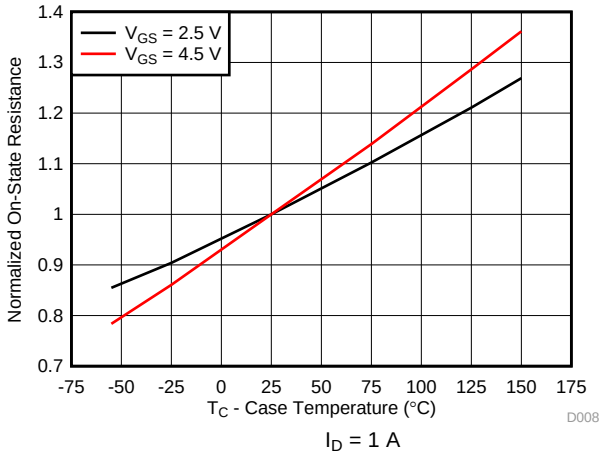


Figure 8. Normalized On-State Resistance vs Temperature

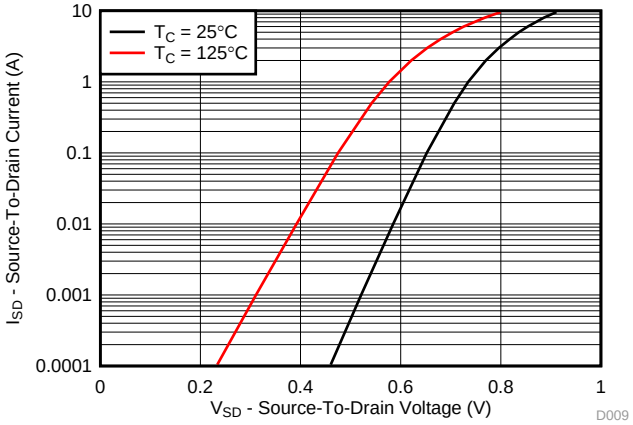


Figure 9. Typical Diode Forward Voltage

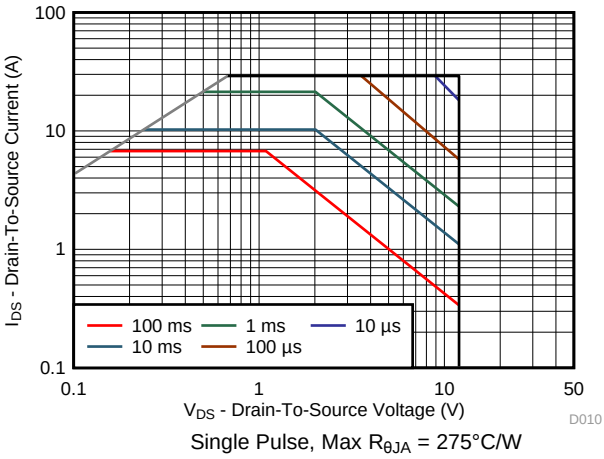


Figure 10. Maximum Safe Operating Area

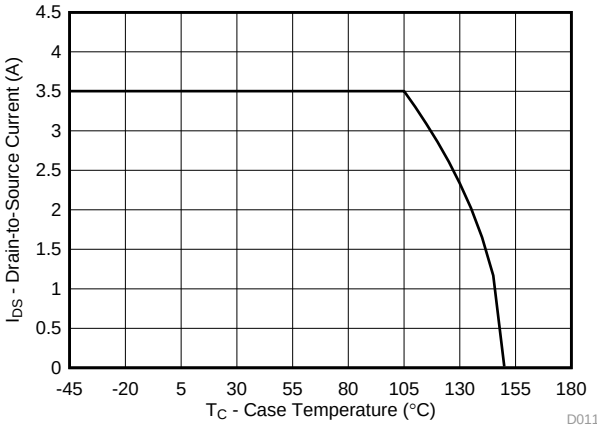


Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

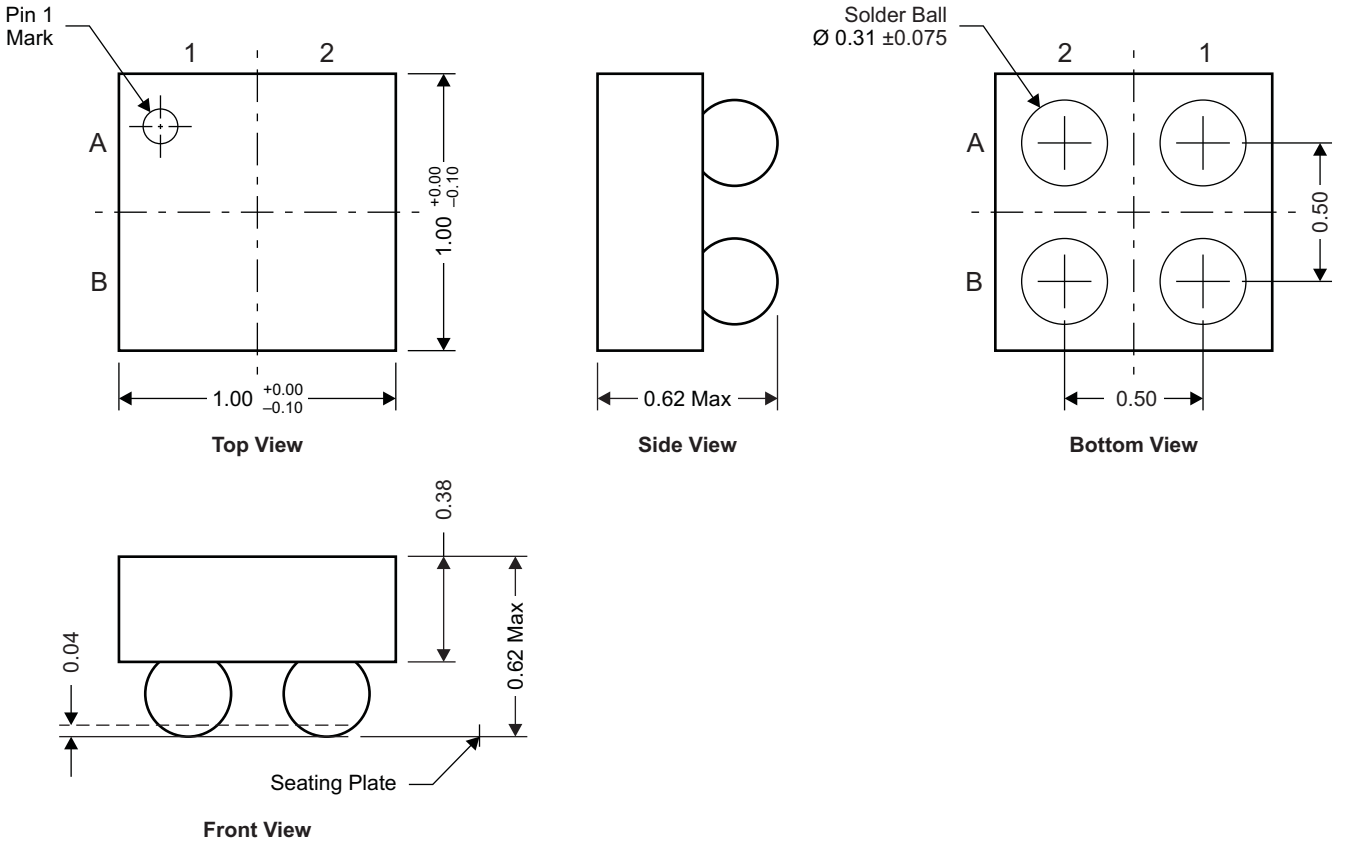
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD13302W Package Dimensions

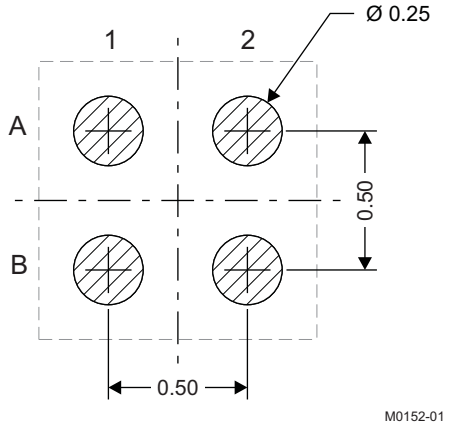


NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

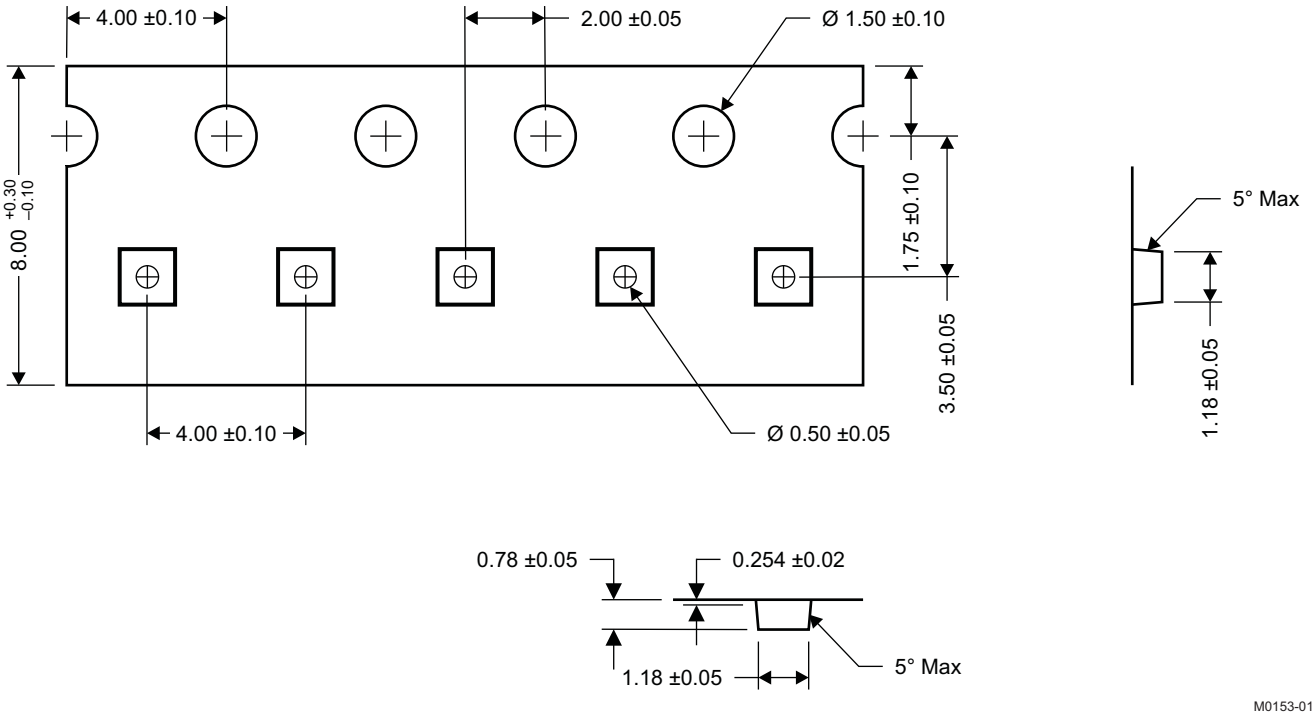
POSITION	DESIGNATION
A2	Source
A1	Gate
B1, B2	Drain

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

7.2 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13302W	ACTIVE	DSBGA	YZB	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		302	Samples
CSD13302WT	ACTIVE	DSBGA	YZB	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	302	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265