

# CSD17579Q3A 30 V N-Channel NexFET™ Power MOSFETs

## 1 Features

- Low  $Q_g$  and  $Q_{gd}$
- Low  $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

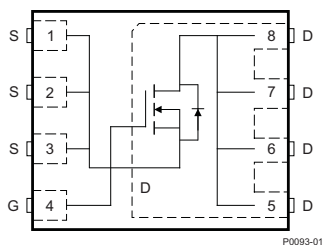
## 2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

## 3 Description

This 30 V, 8.7 mΩ, SON 3.3 mm × 3.3 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	30		V
$Q_g$	Gate Charge Total (4.5 V)	5.3		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	1.2		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	11.8	mΩ
		$V_{GS} = 10\text{ V}$	8.7	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

### Ordering Information<sup>(1)</sup>

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD17579Q3A	13-Inch Reel	2500	SON 3.3 × 3.3 mm Plastic Package	Tape and Reel
CSD17579Q3AT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

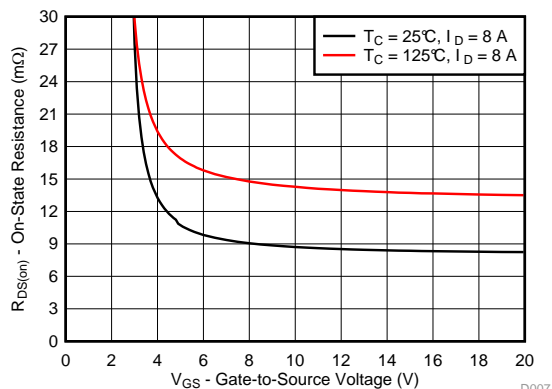
### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Continuous Drain Current (Package limited)	20	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	39	
	Continuous Drain Current <sup>(1)</sup>	11	
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	106	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.5	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	29	
$T_J, T_{stg}$	Operating Junction Temperature, Storage Temperature	-55 to 150	°C
$E_{AS}$	Avalanche Energy, single pulse $I_D = 17\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	14	mJ

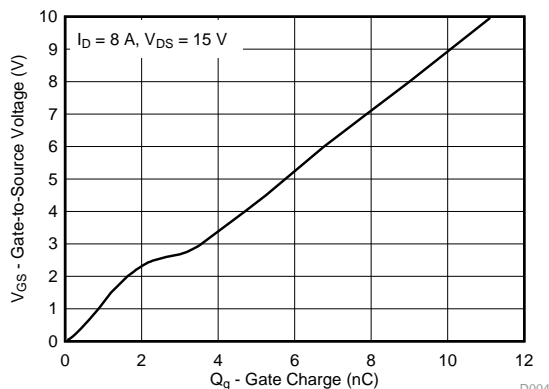
(1) Typical  $R_{\theta JA} = 50^\circ\text{C/W}$  on a 1 inch<sup>2</sup>, 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max  $R_{\theta JC} = 5.4^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$

$R_{DS(on)}$  vs  $V_{GS}$



Gate Charge



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Specifications</b> ..... 3 5.1 Electrical Characteristics..... 3 5.2 Thermal Information ..... 3 5.3 Typical MOSFET Characteristics..... 4 <b>6 Device and Documentation Support</b> ..... 7	6.1 Community Resources..... 7 6.2 Trademarks ..... 7 6.3 Electrostatic Discharge Caution ..... 7 6.4 Glossary ..... 7 <b>7 Mechanical, Packaging, and Orderable Information</b> ..... 8 7.1 Q3A Package Dimensions ..... 8 7.2 Q3A Recommended PCB Pattern ..... 9 7.3 Q3A Recommended Stencil Pattern ..... 9 7.4 Q3A Tape and Reel Information ..... 10
--	--

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (September 2014) to Revision A</b>	<b>Page</b>
• Updated Power Dissipation value in <i>Absolute Maximum Ratings</i> table. ....	1
• Added <a href="#">Community Resources</a> section .....	7
• Updated Package Dimensions drawing.....	8
• Updated PCB drawing. ....	9
• Updated Stencil Pattern drawing. ....	9

## 5 Specifications

### 5.1 Electrical Characteristics

 $(T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$V_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.1	1.5	1.9	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		11.8	14.2	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		8.7	10.2	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 3\text{ V}, I_D = 8\text{ A}$		37		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		768	998	pF
$C_{oss}$	Output capacitance			93	121	pF
$C_{rss}$	Reverse transfer capacitance			38	49	pF
$R_G$	Series gate resistance			1.9	3.8	$\Omega$
$Q_g$	Gate charge total (4.5 V)	$V_{DS} = 15\text{ V}, I_D = 8\text{ A}$		5.3	6.9	nC
$Q_g$	Gate charge total (10 V)			11.5	15.0	nC
$Q_{gd}$	Gate charge gate-to-drain			1.2		nC
$Q_{gs}$	Gate charge gate-to-source			2.2		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			1.1		nC
$Q_{oss}$	Output charge		$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		3.0	
$t_{d(on)}$	Turn on delay time	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 8\text{ A}, R_G = 0\ \Omega$		2		ns
$t_r$	Rise time			5		ns
$t_{d(off)}$	Turn off delay time			11		ns
$t_f$	Fall time			1		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 8\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.0	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 15\text{ V}, I_F = 8\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		3.4		nC
$t_{rr}$	Reverse recovery time			5		ns

### 5.2 Thermal Information

 $(T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance <sup>(1)</sup>			5.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			60	$^\circ\text{C}/\text{W}$

- $R_{\theta JC}$  is determined with the device mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.

CSD17579Q3A

SLPS527A – SEPTEMBER 2014 – REVISED JANUARY 2016

www.ti.com



Max  $R_{\theta JA} = 60^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2 oz. (0.071 mm thick)  
Cu.

M0161-01

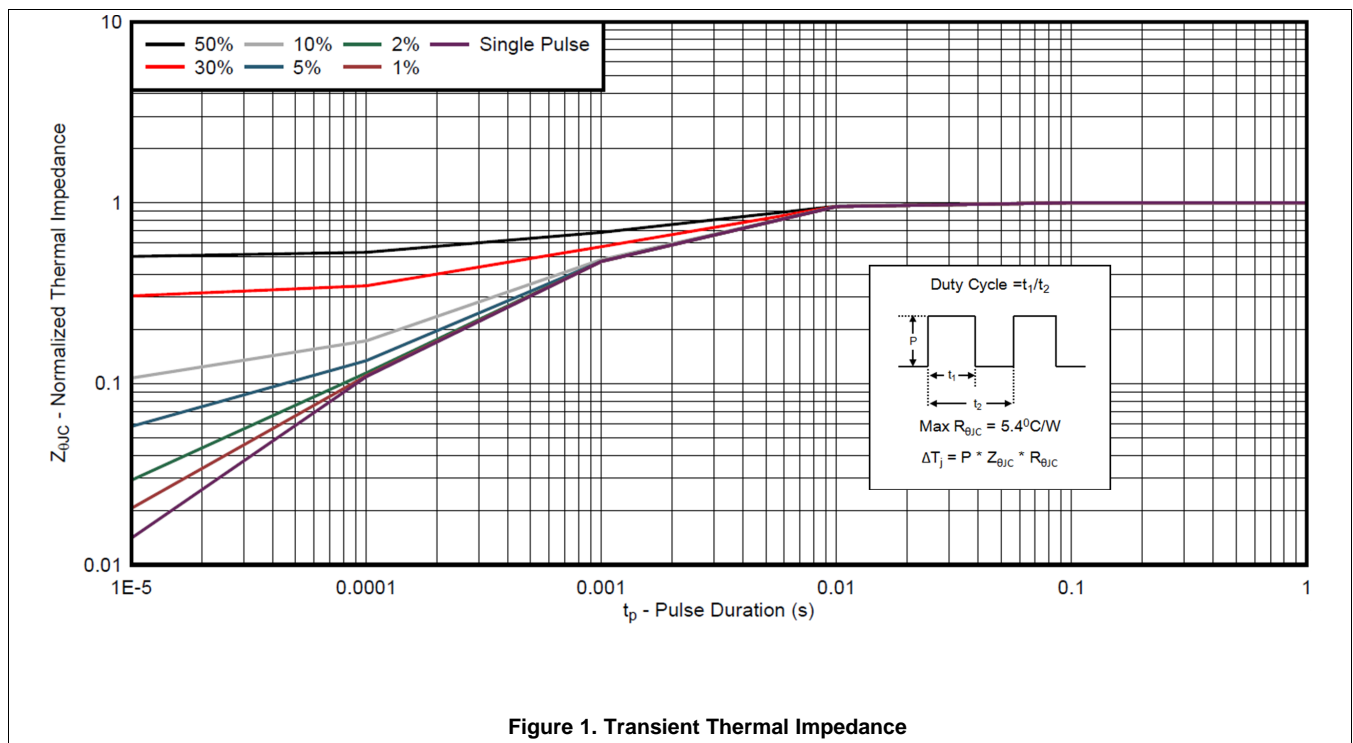


Max  $R_{\theta JA} = 145^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of 2  
oz. (0.071 mm thick)  
Cu.

M0161-02

5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

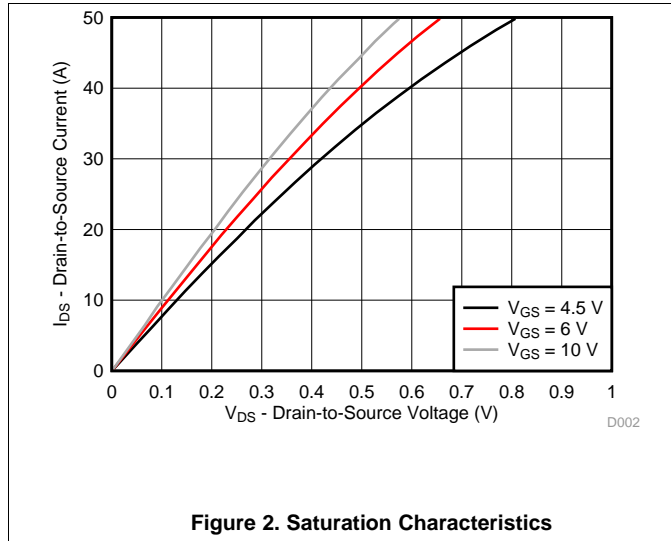


Figure 2. Saturation Characteristics

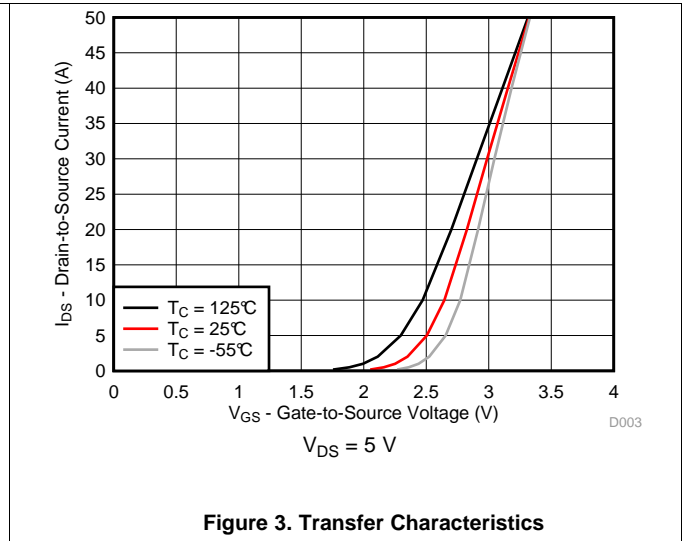


Figure 3. Transfer Characteristics

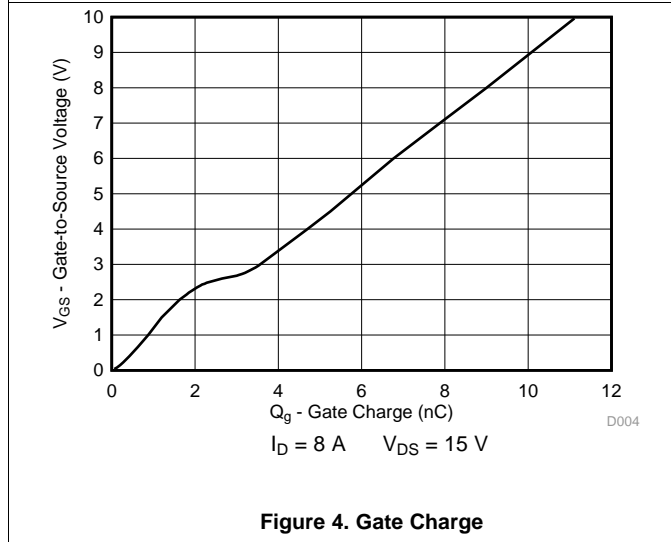


Figure 4. Gate Charge

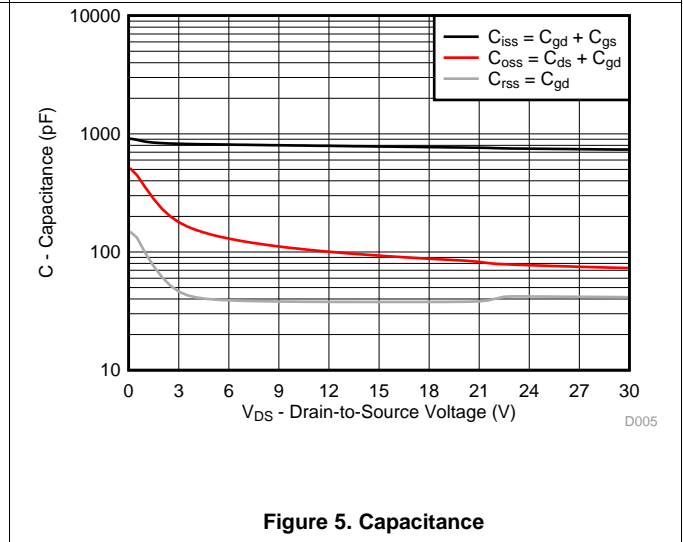


Figure 5. Capacitance

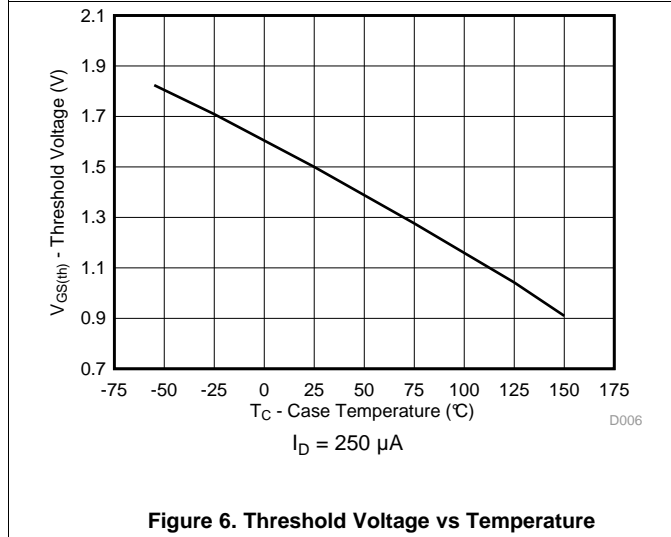


Figure 6. Threshold Voltage vs Temperature

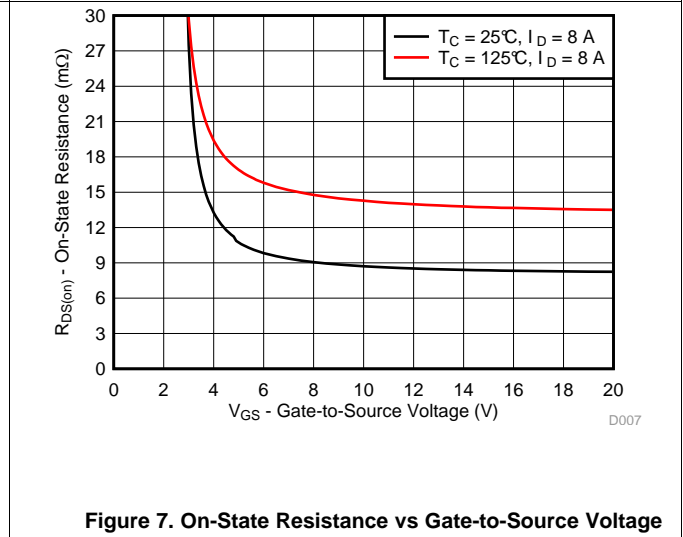


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

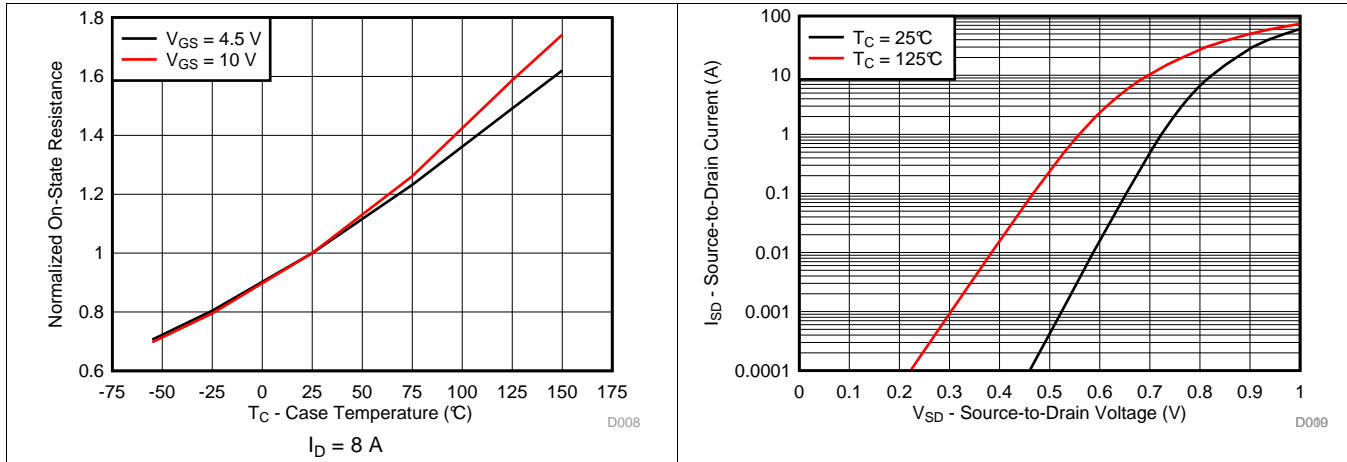


Figure 8. Normalized On-State Resistance vs Temperature

Figure 9. Typical Diode Forward Voltage

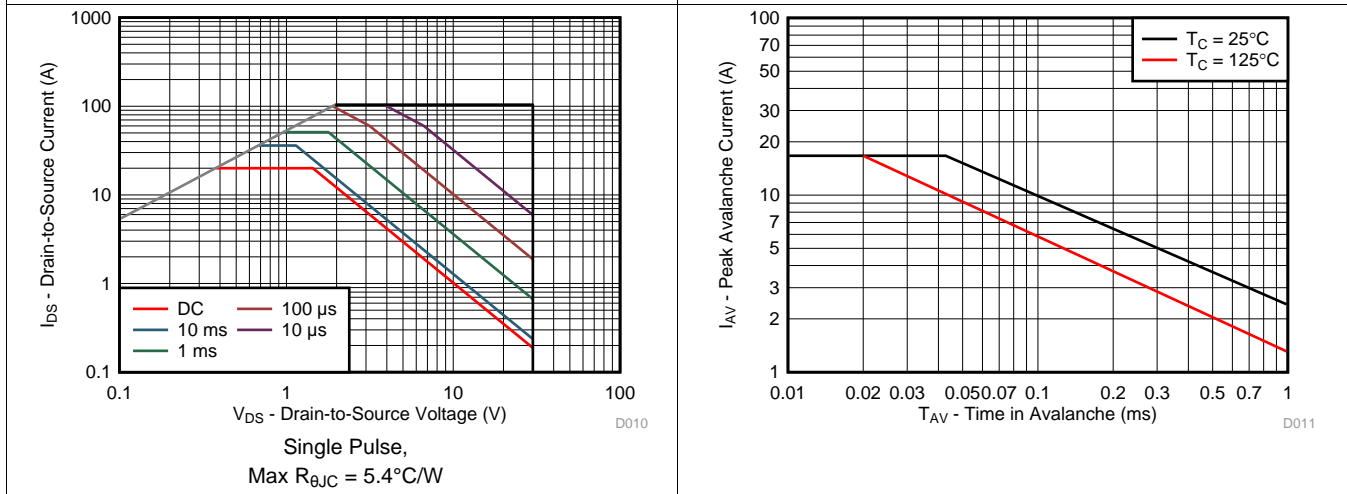


Figure 10. Maximum Safe Operating Area

Figure 11. Single Pulse Unclamped Inductive Switching

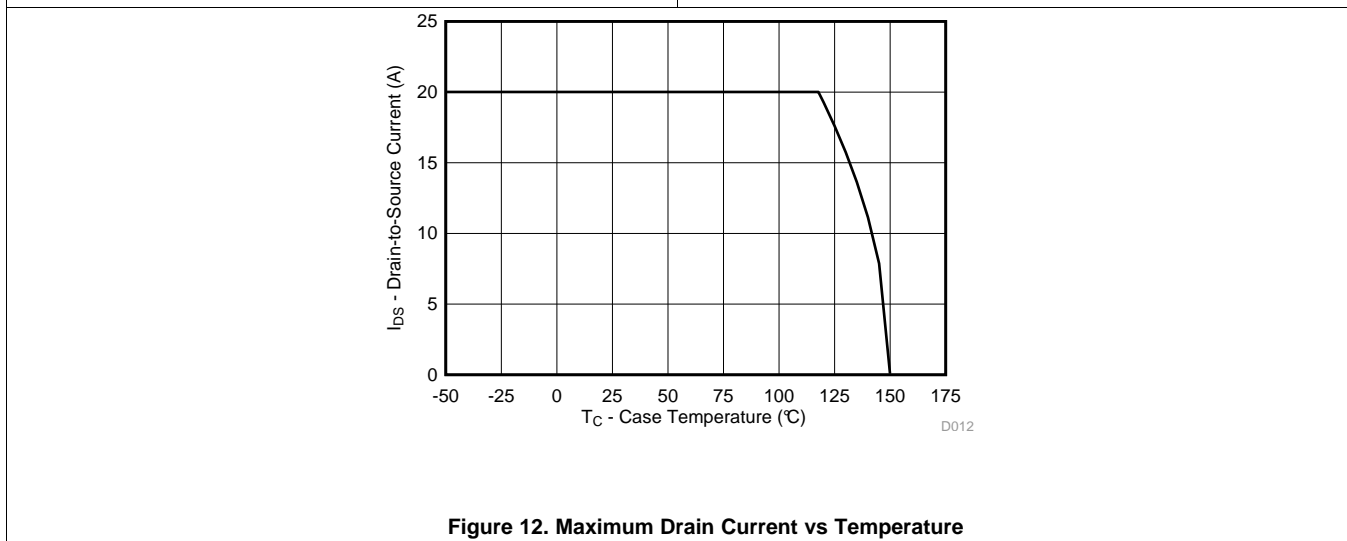


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

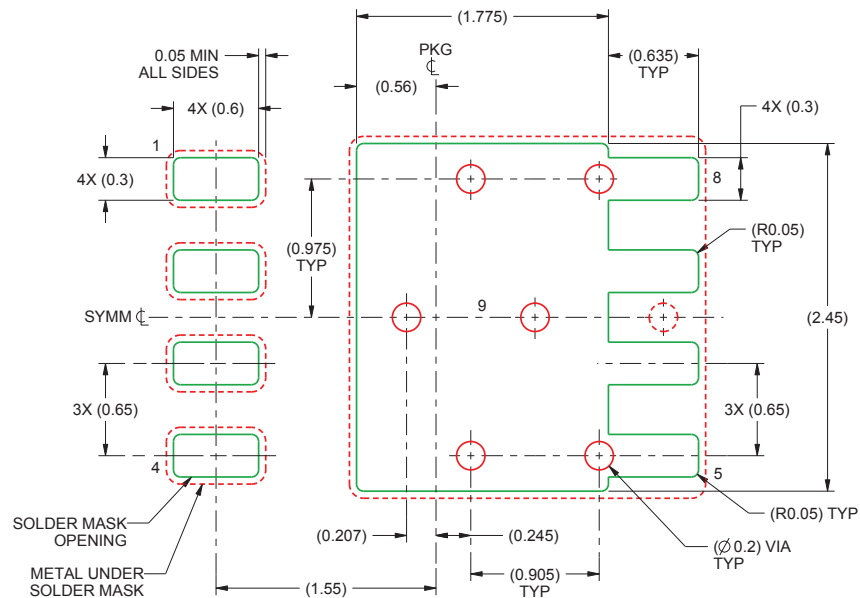
### 7.1 Q3A Package Dimensions



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.



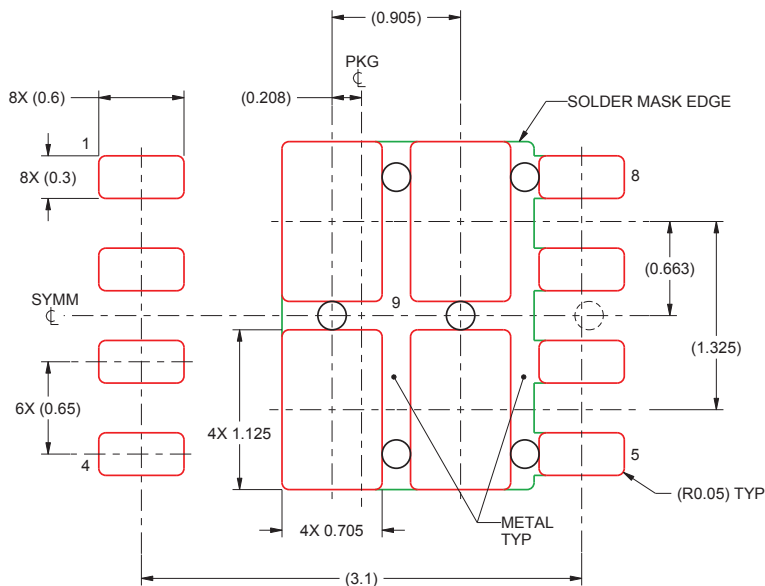
## 7.2 Q3A Recommended PCB Pattern



1. This package is designed to be soldered to a thermal pad on the board. For more information, see *QFN/SON PCB Attachment* application report, [SLUA271](#).
2. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

## 7.3 Q3A Recommended Stencil Pattern



1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 7.4 Q3A Tape and Reel Information



M0144-01

- Notes:
1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
  2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
  3. Material: black static-dissipative polystyrene
  4. All dimensions are in mm, unless otherwise specified.
  5. Thickness:  $0.30 \pm 0.05$  mm
  6. MSL1 260°C (IR and convection) PbF-reflow compatible

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17579Q3A	ACTIVE	VSONP	DNH	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM		17579	<a href="#">Samples</a>
CSD17579Q3AT	ACTIVE	VSONP	DNH	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	17579	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated