CSD22205L –8-V P-Channel NexFET™ Power MOSFET

1 Features

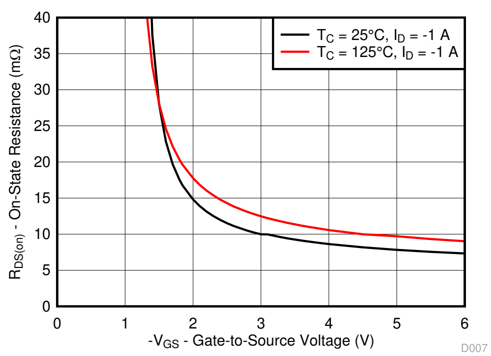
- Low resistance
- Small footprint 1.2 mm × 1.2 mm
- Low profile 0.36-mm height
- Lead free
- Gate-source voltage clamp
- Gate ESD protection
- RoHS compliant
- Halogen free

2 Applications

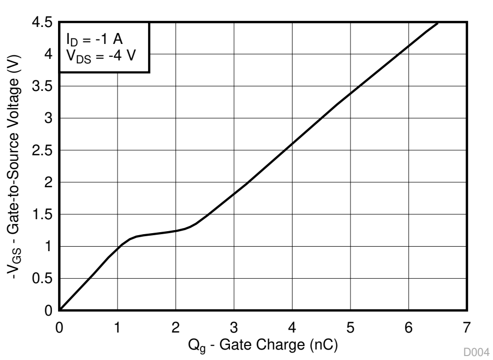
- Battery management
- Load switch
- Battery protection

3 Description

This –8-V, 8.2-mΩ, 1.2-mm × 1.2-mm Land Grid Array (LGA) NexFET™ device has been designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. The Land Grid Array (LGA) package is a silicon chip scale package with metal pads instead of solder balls.



$R_{DS(on)}$ vs V_{GS}



$R_{DS(on)}$ vs V_{GS}

Product Summary

T_A = 25°C		VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–8		V
Q_g	Gate Charge Total (–4.5 V)	6.5		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.0		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.5 V	30	mΩ
		V_{GS} = –1.8 V	20	
		V_{GS} = –2.5 V	11.5	
		V_{GS} = –4.5 V	8.2	
$V_{GS(th)}$	Threshold Voltage	–0.7		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD22205L	3000	7-Inch Reel	1.20-mm × 1.20-mm Land Grid Array Package	Tape and Reel
CSD22205LT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–8	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_D	Continuous Drain Current(1)	–7.4	A
I_{DM}	Pulsed Drain Current(2)	–71	A
P_D	Power Dissipation(1)	0.6	W
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C

(1) Min Cu $R_{\theta JA}$ = 225°C/W.
(2) Pulse width ≤ 100 μs, duty cycle ≤ 1%.

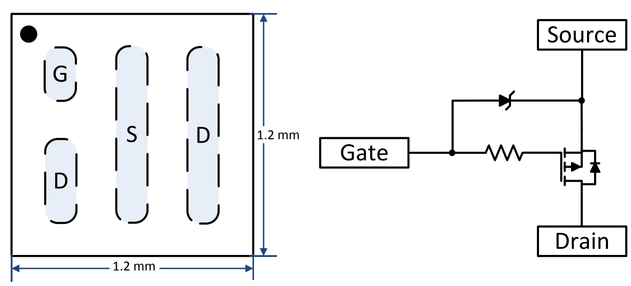


Figure 3-1. Top View and Circuit Configuration

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4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022) **Page**

- Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height....... 1
- Changed CSD22205L Package Dimensions image height from 0.35 mm to 0.36 mm....... 8

Changes from Revision * (May 2017) to Revision A (August 2017) **Page**

- Changed the units for timing parameters from µs : to ns (nanoseconds) in the *Section 5.1* table....... 3

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

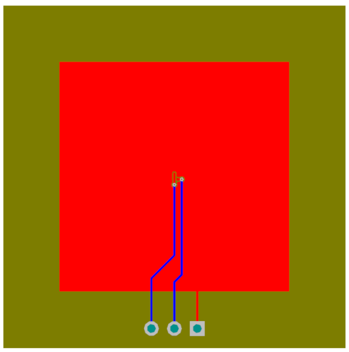
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = –250 μA	–8			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –6.4 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.4	–0.7	–1.05	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.5 V, I_D = –0.2 A		30		mΩ
		V_{GS} = –1.8 V, I_D = –1 A		20	40	
		V_{GS} = –2.5 V, I_D = –1 A		11.5	15.0	
		V_{GS} = –4.5 V, I_D = –1 A		8.2	9.9	
g_{fs}	Transconductance	V_{DS} = –0.8 V, I_D = –1 A		10.4		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = –4 V, f = 1 MHz		1070	1390	pF
C_{OSS}	Output capacitance			560	730	pF
C_{RSS}	Reverse transfer capacitance			190	250	pF
R_G	Series gate resistance			30		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –4 V, I_D = –1 A		6.5	8.5	nC
Q_{gd}	Gate charge gate-to-drain			1.0		nC
Q_{gs}	Gate charge gate-to-source			1.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.7		nC
Q_{OSS}	Output charge	V_{DS} = –4 V, V_{GS} = 0 V		4.1		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –4 V, V_{GS} = –4.5 V, I_D = –1 A , R_G = 0 Ω		30		ns
t_r	Rise time			14		ns
$t_{d(off)}$	Turnoff delay time			70		ns
t_f	Fall time			32		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = –1 A, V_{GS} = 0 V		–0.68	–1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= –4 V, I_F = –1 A, di/dt = 200 A/μs		16		nC
t_{rr}	Reverse recovery time			38		ns

5.2 Thermal Information

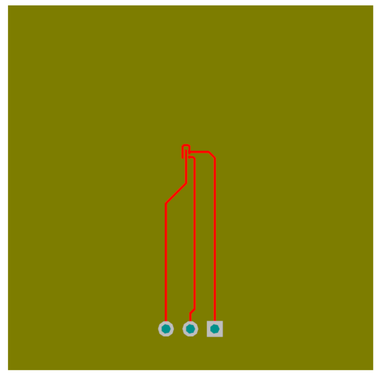
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)		75		°C/W
	Junction-to-ambient thermal resistance(1)		225		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.



Typ $R_{\theta JA}$ =75°C/W when mounted on 1 in² of 2-oz Cu.



Typ $R_{\theta JA}$ = 225°C/W when mounted on minimum pad area of 2-oz Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

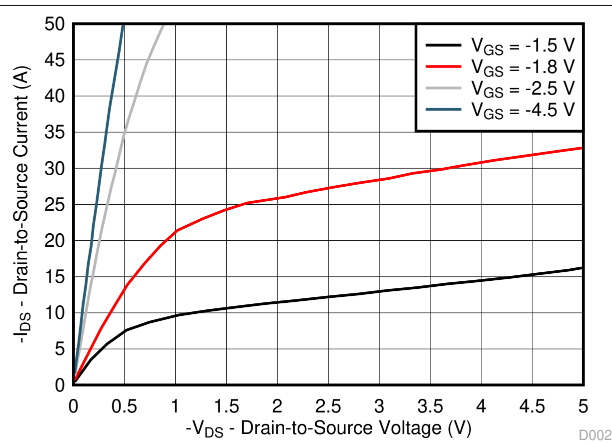
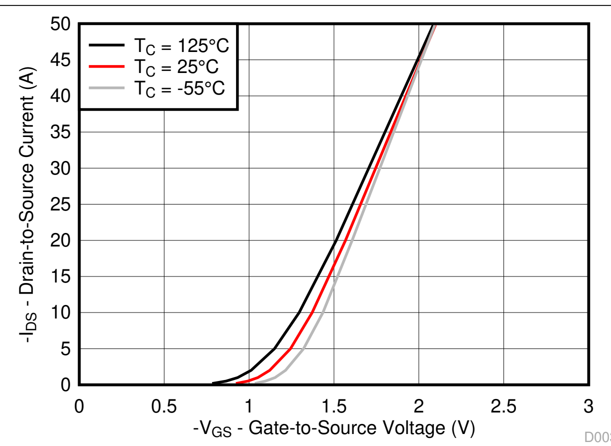


Figure 5-1. Saturation Characteristics



V_{DS} = –5 V

Figure 5-2. Transfer Characteristics

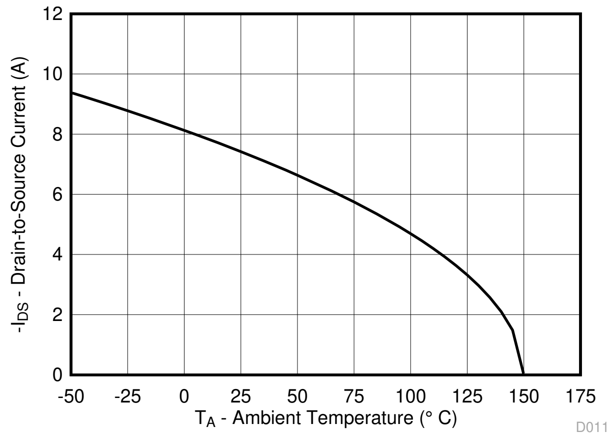
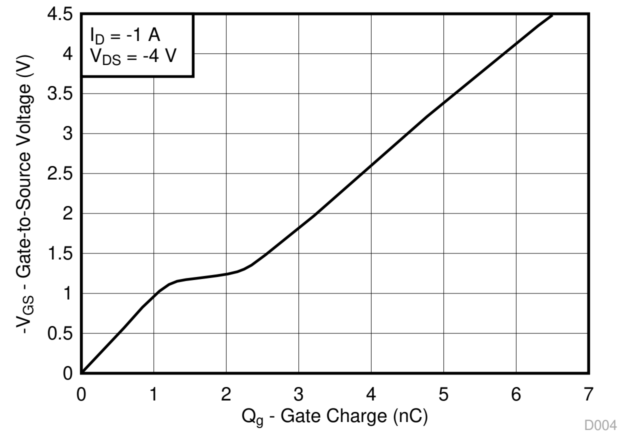


Figure 5-3. Maximum Drain Current vs Temperature



I_D = –1 A V_{DS} = –4 V

Figure 5-4. Gate Charge

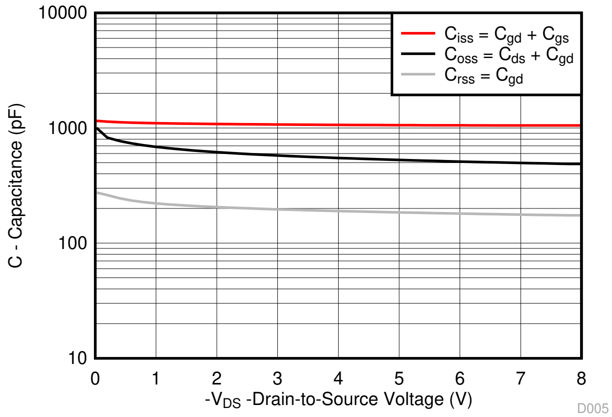
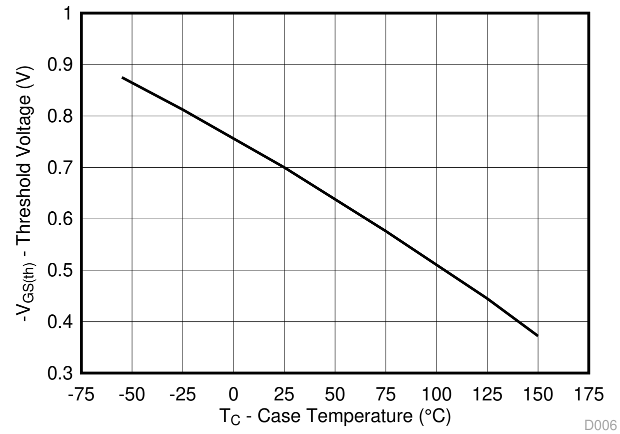


Figure 5-5. Capacitance



I_D = –250 µA

Figure 5-6. Threshold Voltage vs Temperature

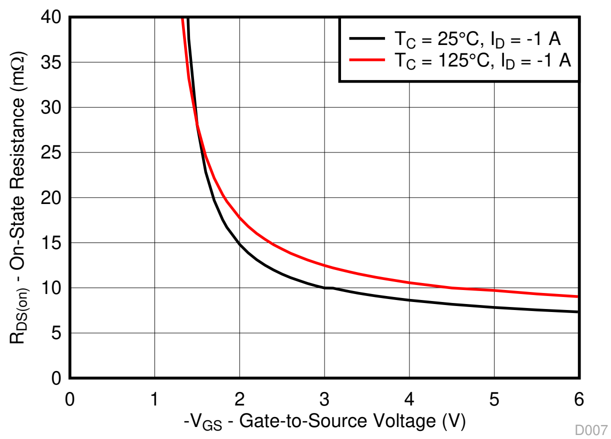
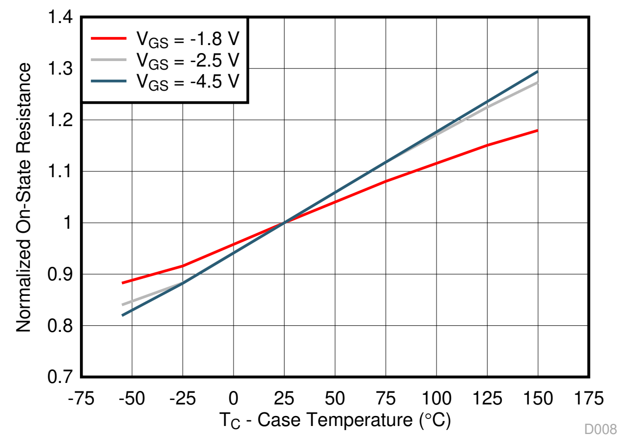


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –1 A

Figure 5-8. Normalized On-State Resistance vs Temperature

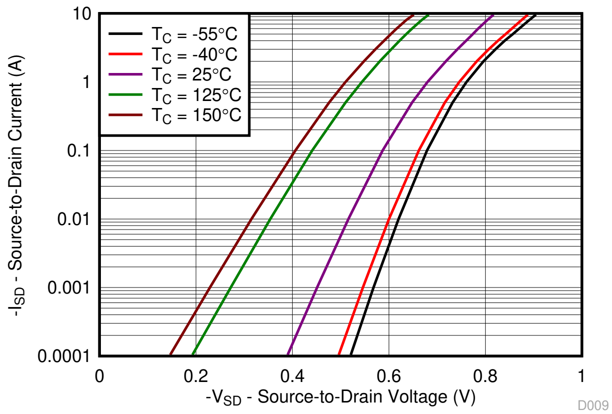
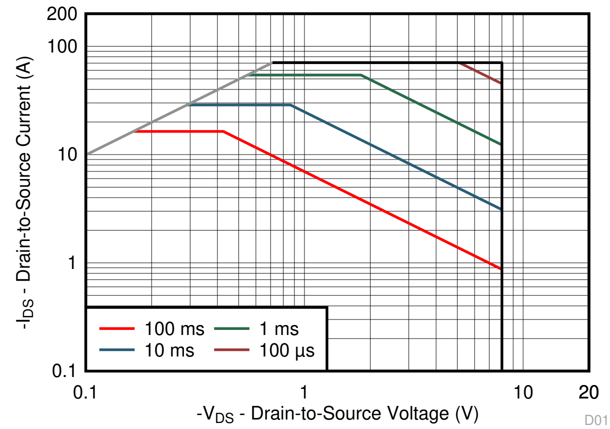


Figure 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 225°C/W

Figure 5-10. Maximum Safe Operating Area

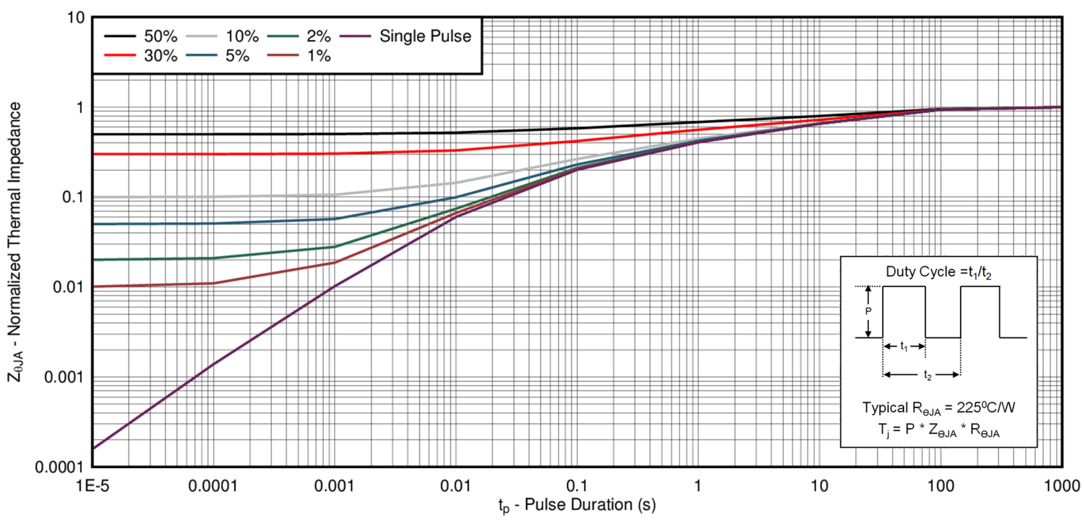


Figure 5-11. Transient Thermal Impedance

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

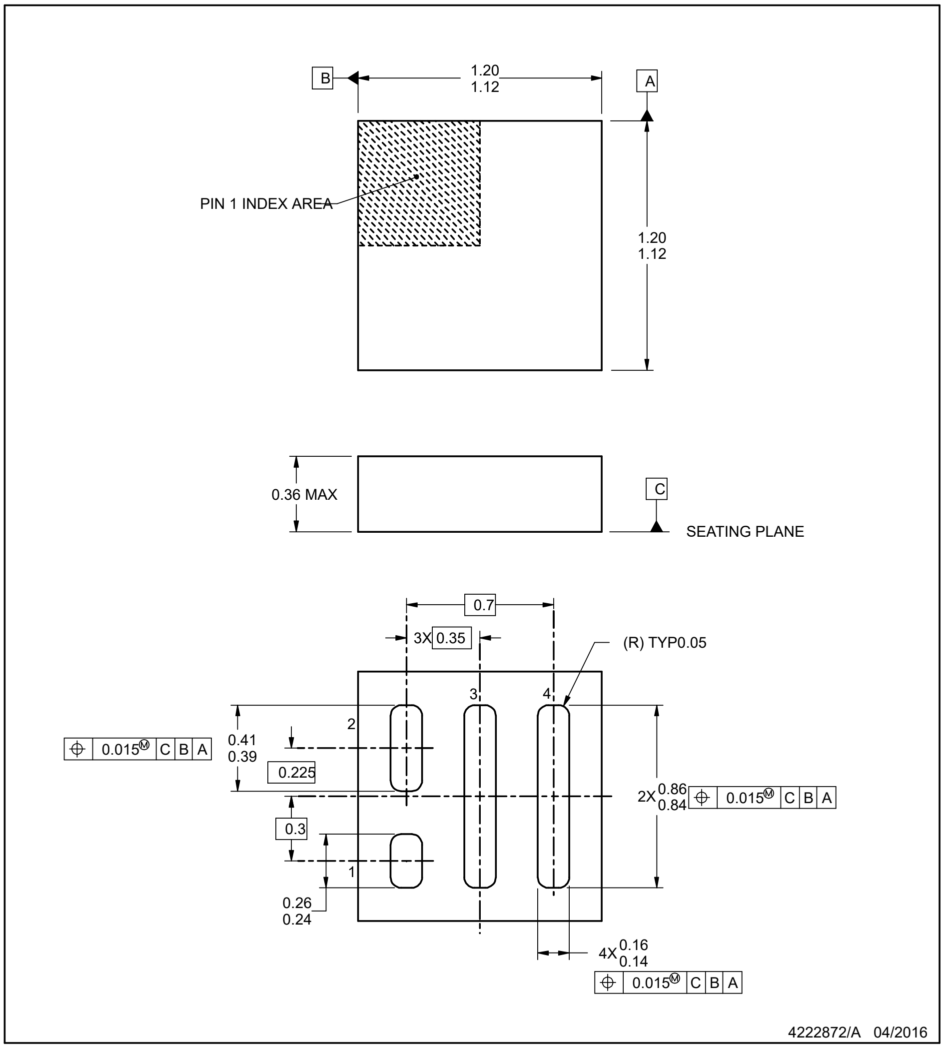
6.2 Trademarks

NexFET™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD22205L Package Dimensions

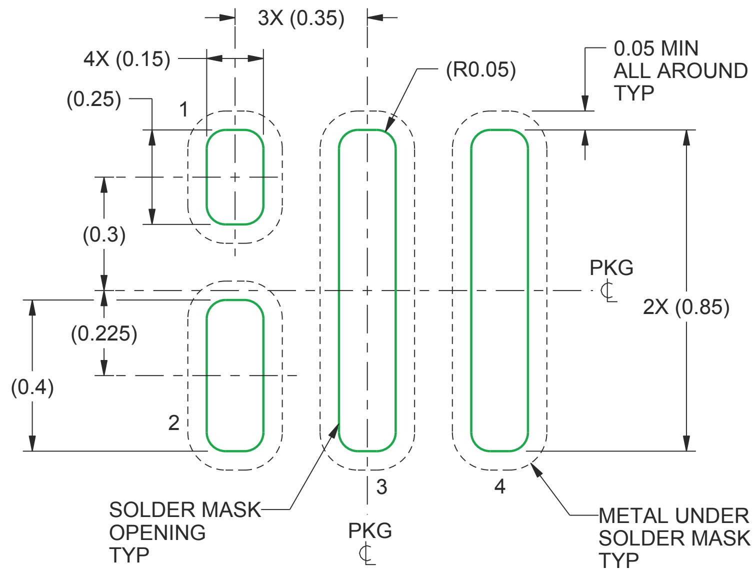


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is a lead-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

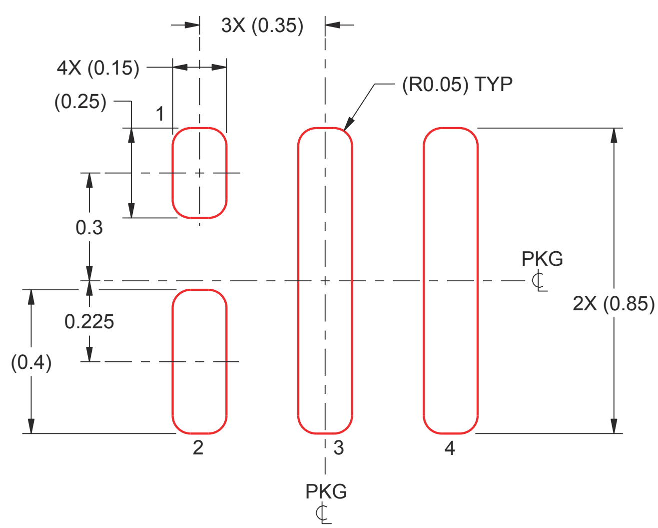
Table 7-1. Pin Configuration Table

POSITION	DESIGNATION
1	Gate
2	Drain
3	Source
4	Drain

7.2 Land Pattern Recommendation



7.3 Stencil Recommendation



A. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD22205L	Active	Production	PICOSTAR (YMG) | 4	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	205
CSD22205L.B	Active	Production	PICOSTAR (YMG) | 4	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	205
CSD22205LT	Active	Production	PICOSTAR (YMG) | 4	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	205
CSD22205LT.B	Active	Production	PICOSTAR (YMG) | 4	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	205

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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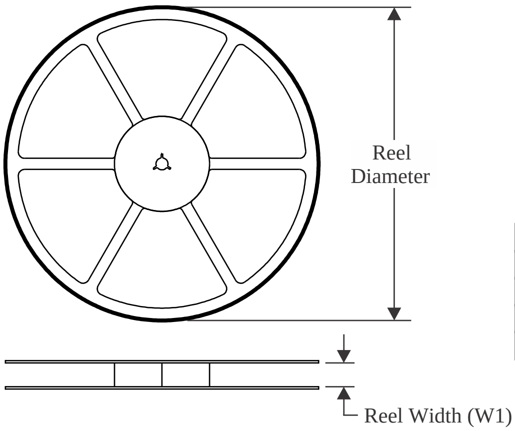
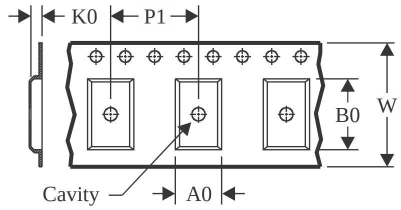
TAPE AND REEL INFORMATION

REEL DIMENSIONS

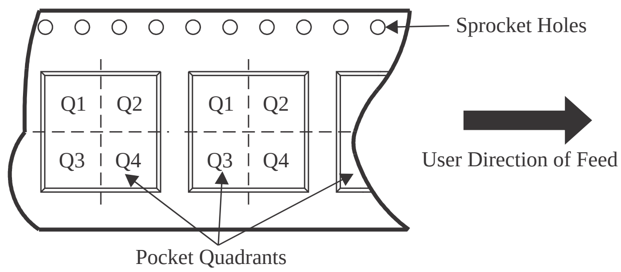


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

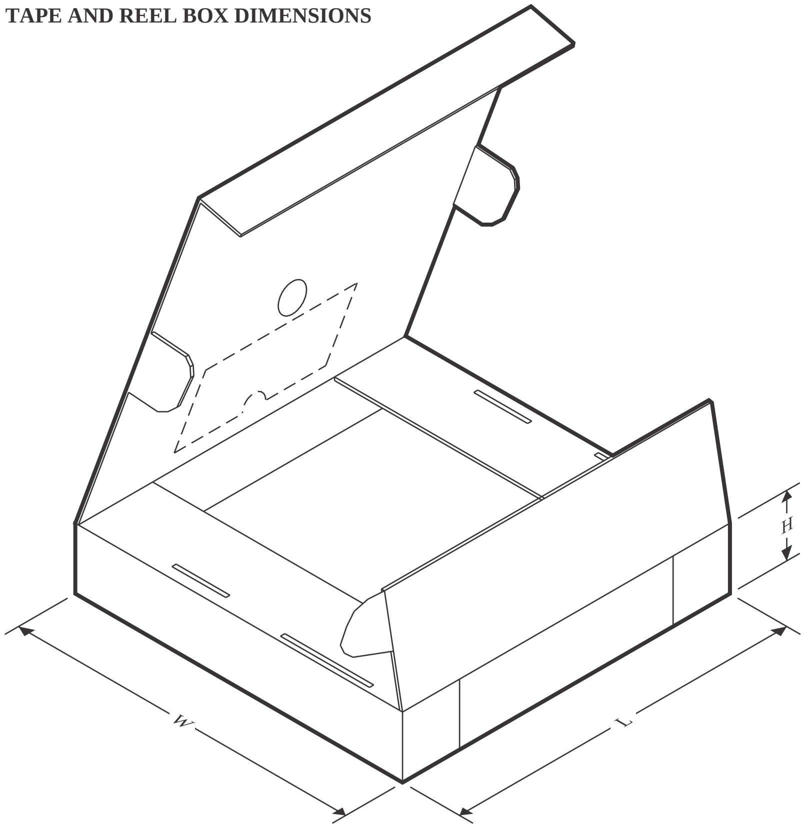
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD22205L	PICOSTAR	YMG	4	3000	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1
CSD22205LT	PICOSTAR	YMG	4	250	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD22205L	PICOSTAR	YMG	4	3000	182.0	182.0	20.0
CSD22205LT	PICOSTAR	YMG	4	250	182.0	182.0	20.0