NexFET™ Smart Synchronous Rectifier

FEATURES

- **Typical R_{on} of 0.55 mΩ at 4.5 V_{DD}**
- **Integrated FET Driver**
- **Max Rated Current 80A**
- **High Density – SON 5-mm × 6-mm Footprint**
- **Ultra Low Inductance Package**
- **System Optimized PCB Footprint**
- **TTL IN signal Compatible**
- **Halogen Free**
- **RoHS Compliant – Lead Free Terminal Plating Halogen Free**

APPLICATIONS

- **Secondary Synchronous Rectification for DC/DC Converters**

DESCRIPTION

The CSD43301Q5M NexFET™ Smart Synchronous Rectifier is a highly optimized design for secondary synchronous rectification in a high power high density DC/DC converter. This product integrates the driver IC and an ultra low R_{on} Power MOSFET to complete the synchronous rectification function. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD43301Q5M	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

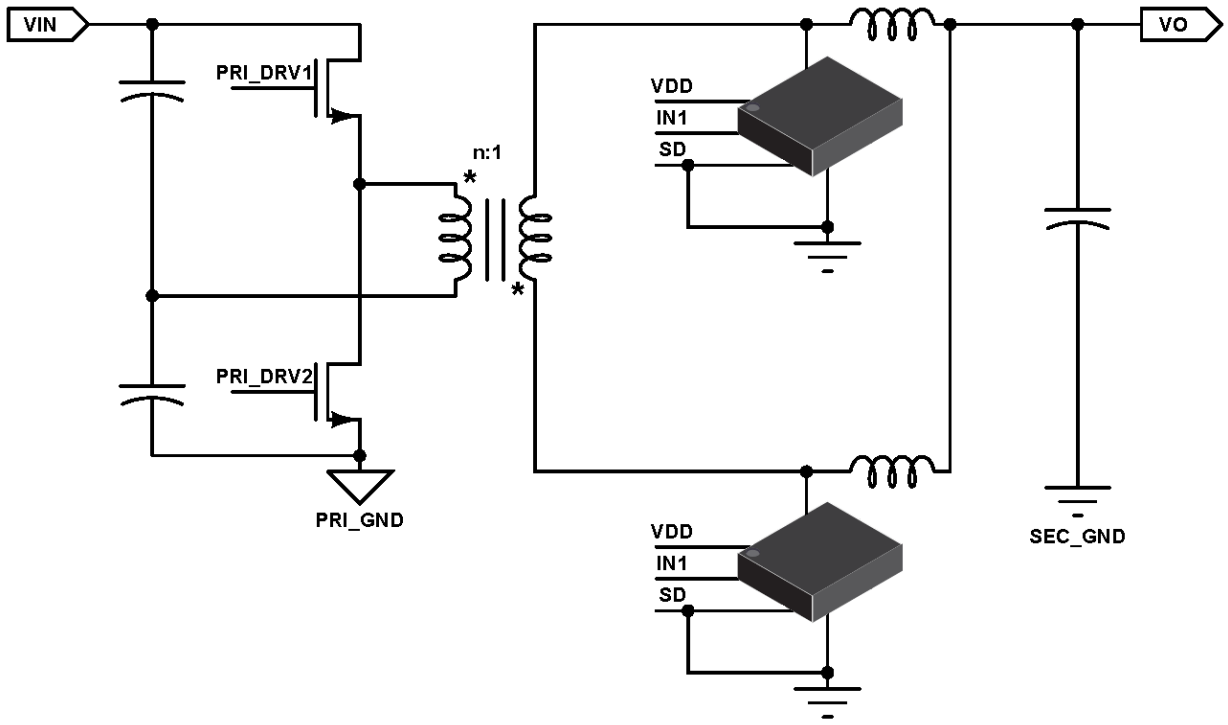


Figure 1. Application Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

T_A = 25°C (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
DRAIN to P_{GND}		-0.3	12	V
DRAIN to P_{GND} (10ns)		-7	14	V
V_{DD} to P_{GND}		–0.3	8	V
IN, SD to P_{GND}(2)		–0.3	V_{DD} + 0.3	V
ESD Rating	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V
Power Dissipation (P_D)			12	W
Operating Temperature Range, (T_J)		-40	150	°C
Storage Temperature Range, (T_{STG})		–65	150	°C

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.
(2) Must not exceed 8V

RECOMMENDED OPERATING CONDITIONS

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Bias Voltage (V_{DD})		4.5	6	V
Input Supply Voltage (V_{IN})			9.6	V
Continuous Output Current (I_{OUT})			80	A
Peak Output Current, (I_{OUT-PK})(1)			120	A
Switching Frequency, (f_{SW})			1500	kHz
Minimum IN Pulse Width		48		ns
Operating Temperature		–40	125	°C

(1) Peak Output Current is applied for t_p = 50µs.

THERMAL INFORMATION

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top of package)			20	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board(1)			2	°C/W

(1) $R_{\theta JB}$ value based on hottest board temperature within 1mm of the package.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Device On Resistance					
R_{on}	I_D = 50A, , T_J = 25°C		0.55	0.70	mΩ
	I_D = 50A, T_J = 125°C		0.70	0.88	mΩ
V_{DD}					
Standby Supply Current (I_{DD})	SD = V_{DD} = 5V		153	300	µA
Operating Supply Current (I_{DD})	SD = 0V, IN = 50% Duty Cycle, f_{SW} = 300kHz		29.5		mA
POWER-ON RESET AND UNDER VOLTAGE LOCKOUT					
Power on Reset (V_{DD} Rising)	T_A = 25°C	3.9	4.2	4.5	V
	T_A = -40°C to 140°C	3.7	4.2	4.65	V
UVLO (V_{DD} Falling)		3.45	3.9	4.35	V
Hysteresis		200	300	500	mV
IN					
IN Logic Level High (V_{INH})		2.0			V
IN Logic Level Low (V_{INL})				0.8	V
IN Input Hysteresis			0.8		V
IN to DRAIN Propagation Delay (t_{PDLH})	V_{DD} = 5V, SD = 0, I_D = 25A (See Figure 4)		32		ns
IN to DRAIN Propagation Delay (t_{PDHL})			80		ns
Minimum Pulse Width Changes Output			36	48	ns
SD					
SD Logic Level High Threshold (V_{IH})		2.0			V
SD Logic Level Low Threshold (V_{IL})				0.8	V
Hysteresis			0.8		V
SD to DRAIN Propagation Delay (t_{PDLH})	V_{DD} = 5V, IN = V_{DD}, I_D = 25A (See Figure 5)		80		ns
SD to DRAIN Propagation Delay (t_{PDHL})			32		ns
Dynamic Characteristics					
Output Capacitance (C_O)	V_{DRAIN} = 6V		10	13	nF
Output Charge (Q_O)			54		nC
Body Diode					
Forward Voltage (V_F)	I_D = 40A		0.75	0.85	V
Reverse Recovery Charge (Q_{RR})	I_D = 40A, V_{DRAIN} = 6V, di/dt = 150A/µs		161		nC
Reverse Recovery Time Delay (t_{RR})			72		ns

PIN CONFIGURATION

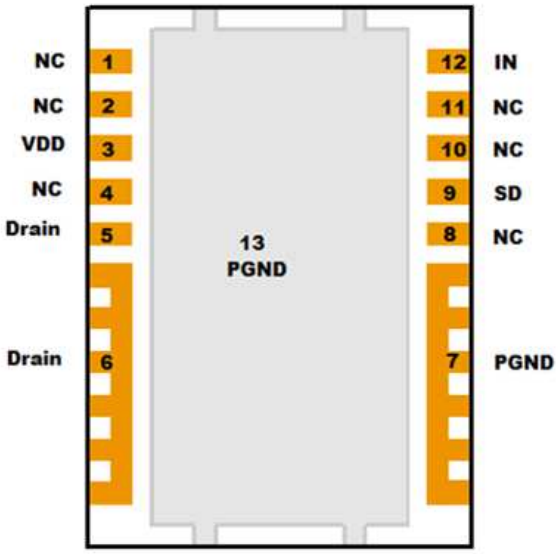


Figure 2. Pin Configuration

PIN DESCRIPTION

PIN		DESCRIPTION
NO.	NAME	
1,2,4, 8, 10,11	NC	No connect. These should not be used for any electrical connection. These pins should not be connected to each other. Connect to dead copper only.
3	V_{DD}	Supply Voltage for IC
5,6	DRAIN	Drain terminal of internal MOSFET
7	P_{GND}	Power Ground and source terminal of the internal MOSFET. Needs to be connected to Pin 13 on PCB
9	SD	Shut Down Pin: Logic High disables the Device
12	IN	Input for Gate Driver
13	P_{GND}	Power Ground and source terminal of the internal MOSFET. Needs to be connected to Pin 7 on PCB

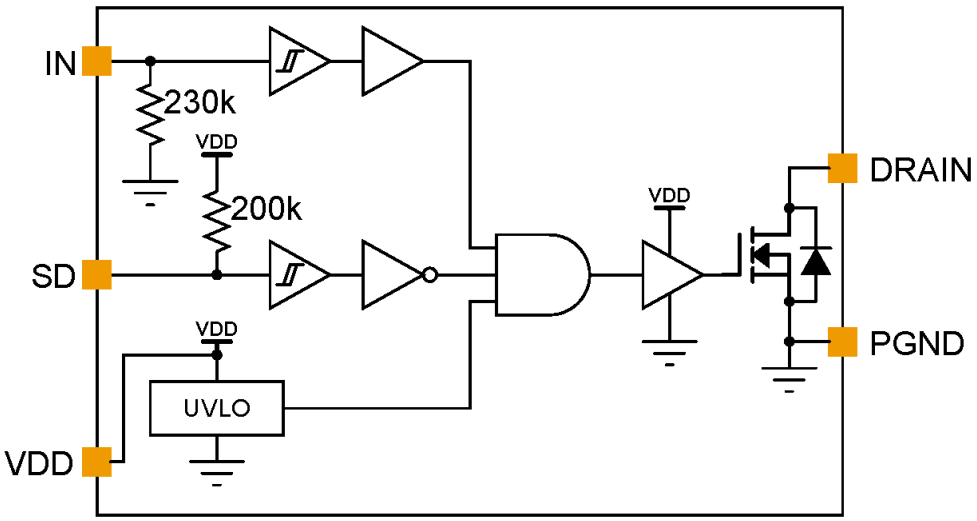


Figure 3. Functional Block Diagram

TYPICAL DEVICE CHARACTERISTICS

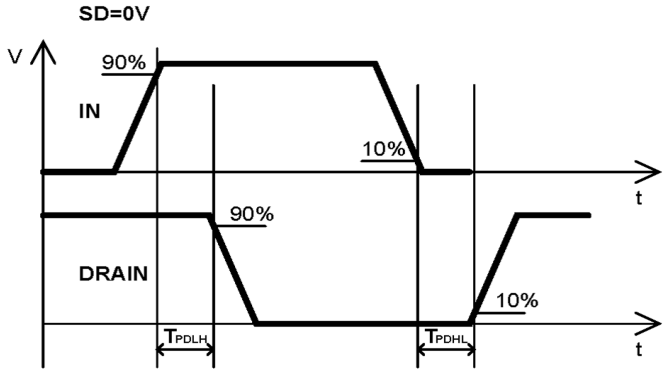


Figure 4. IN Switching Waveforms

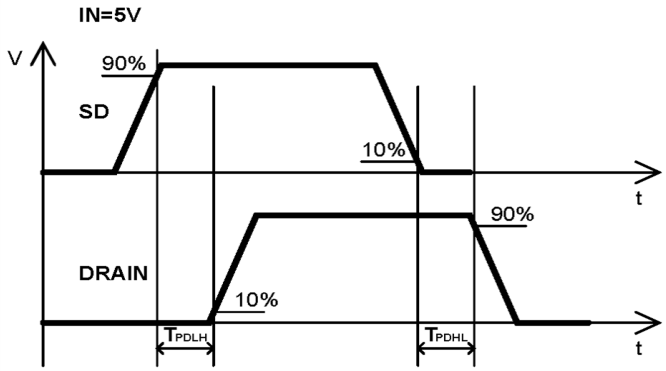


Figure 5. SD Switching Waveform

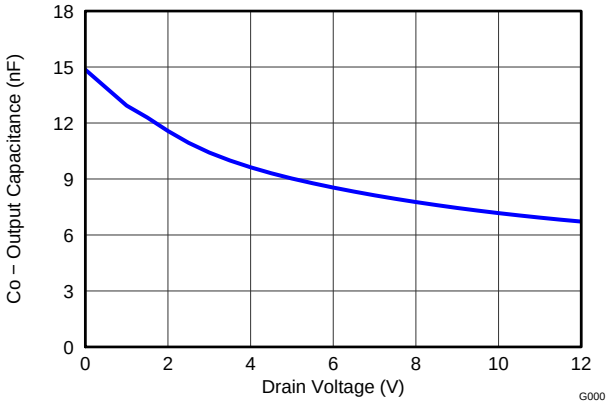


Figure 6. Output Capacitance

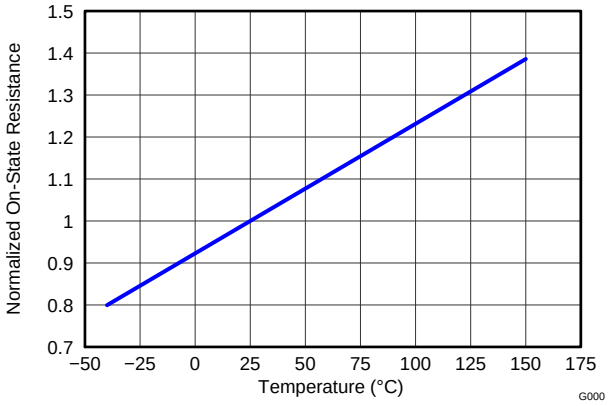


Figure 7. Normalized On Resistance R_{on}

TYPICAL DEVICE CHARACTERISTICS CONTINUED

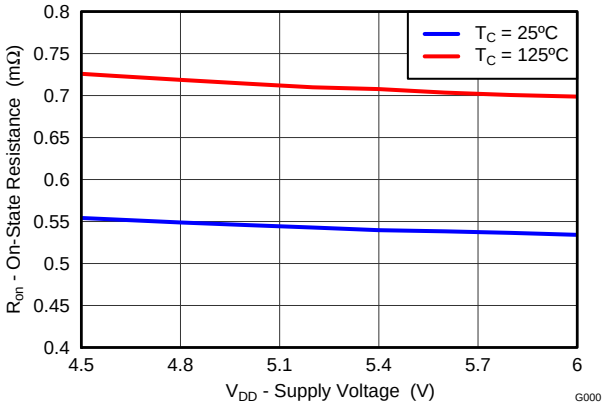


Figure 8. On Resistance vs. Supply Voltage

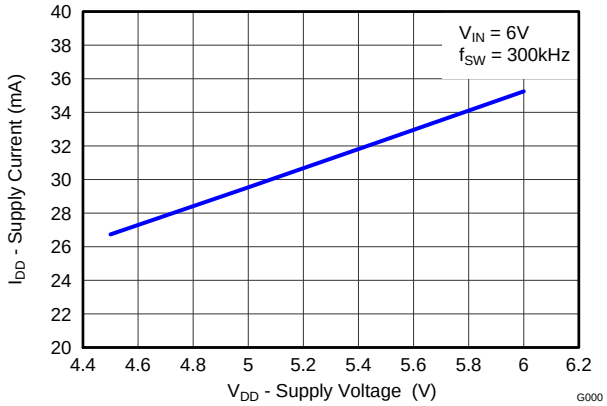


Figure 9. Supply Current vs. Supply Voltage

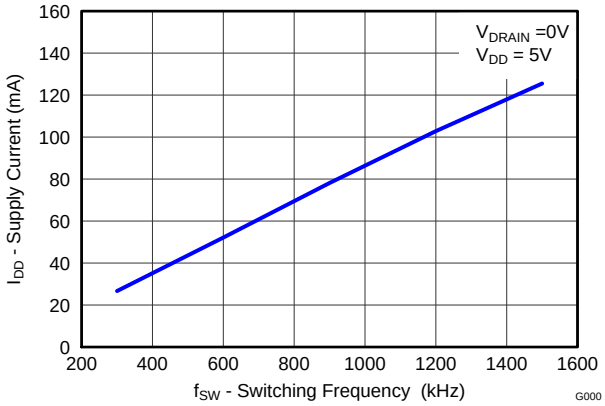


Figure 10. Supply Current vs. Switching Frequency

Application Information

V_{DD} and Under-Voltage Lockout (UVLO)

The driver IC in the CSD43301Q5M has an internal UVLO protection feature on the V_{DD} pin. Whenever the driver is in the UVLO condition (i.e. when V_{DD} voltage is less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds the gate of the integrated MOSFET LOW, regardless of the status of IN and SD. The UVLO is typically 4.2V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the V_{DD} bias voltage when the system commences switching and there is a sudden increase in I_{DD}. This provides the capability to operate at low voltage levels (below 5V), along with best-in-class switching characteristics. For example, at power up, the MOSFET remains OFF until the V_{DD} voltages reaches the UVLO threshold. This prevents operating the MOSFET in the linear region and conducting a large load current at the same time, which often results in device overheating and can potentially damage the device.

Since the driver draws current from the V_{DD} pin to bias all internal circuits, for the best high-speed circuit performance, Multi-Layer Ceramic Capacitor (MLCC) bypass capacitors are recommended to prevent noise problems. A 1 µF MLCC type capacitor should be located as close as possible to the V_{DD} to GND pins of the gate driver.

Operating Supply Current

The driver IC in the CSD43301Q5M has a low quiescent current in normal operation. I_{DDQ} is less than 0.2 mA when the device is disabled (SD = 0). The operating current vs. supply voltage is shown in Figure 9, and the operating current vs. frequency is shown in Figure 10.

Input Stage

The input pins (IN and SD) of the CSD43301Q5M are based on a TTL/CMOS compatible input threshold logic that is independent of the V_{DD} supply voltage. With a typical high threshold of 2.2 V and a typical low threshold of 1.2 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V digital power controllers. Wider hysteresis (typical of 0.8 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed. The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using a V_{DD} pull-up resistor on the SD input or a GND pull-down resistor on the IN input. This can be seen in the block diagram in Figure 3.

Power Dissipation

Power Dissipation of the CSD43301Q5M used in secondary rectification is given by the following:

$$P_{LOSS} = P_{DRV} + P_{COND} + P_{SW} \quad (1)$$

where driver loss is given by

$$P_{DRV} = V_{DD} \times I_{DD} \quad (2)$$

and conduction loss is given by

$$P_{COND} = I^2_{D\_RMS} \times R_{ON} \quad (3)$$

Switching losses consist of body diode conduction losses during dead time, body diode reverse recovery losses, and output charge losses, given by the following:

$$P_{SW} = I_D \times V_F \times (DT_R + DT_F) \times F_{SW} + Q_{RR} \times V_{DRAIN} \times F_{SW} + \tfrac{1}{2} Q_{OSS} \times V_{DRAIN} \times F_{SW} \quad (4)$$

Recommended PCB Design Overview

The CSD43301Q5M features extremely low nominal R_{ON}. In order to maximize the performance of this device, some simple layout guidelines should be followed.

- The DRAIN pins of the CSD43301Q5M should be placed as close as possible to the inductor and connected with a short wide trace. This reduces PCB conduction losses and reduce switching noise level. (1)
- The GND pin (pin 7) must be connected into the thermal pad (pin 13) on the bottom of the device via a copper pour (without thermal spokes) for maximum performance.
- The CSD43301Q5M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down via the barrel:
  - Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
  - Use the smallest drill size allowed in your design. The example in Figure 11 uses vias with a 10 mil drill hole and a 16 mil capture pad.
  - Tent the opposite side of the via with a solder mask.

  In the end, the number and size of the thermal vias should align with the end user's PCB design rules and manufacturing types.

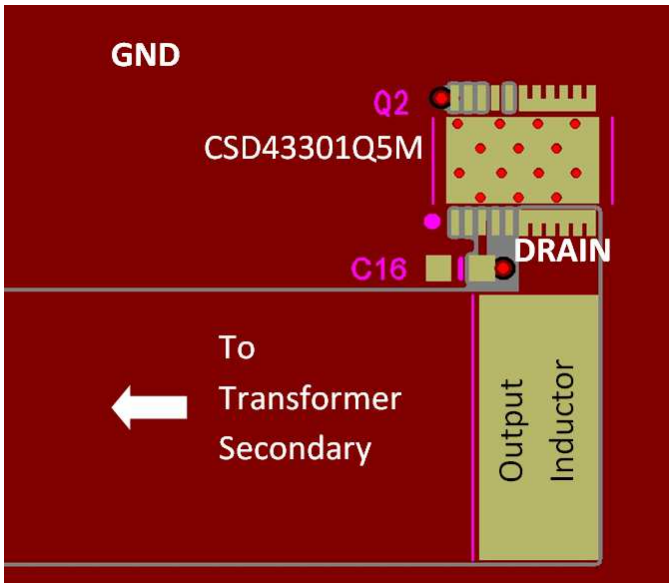
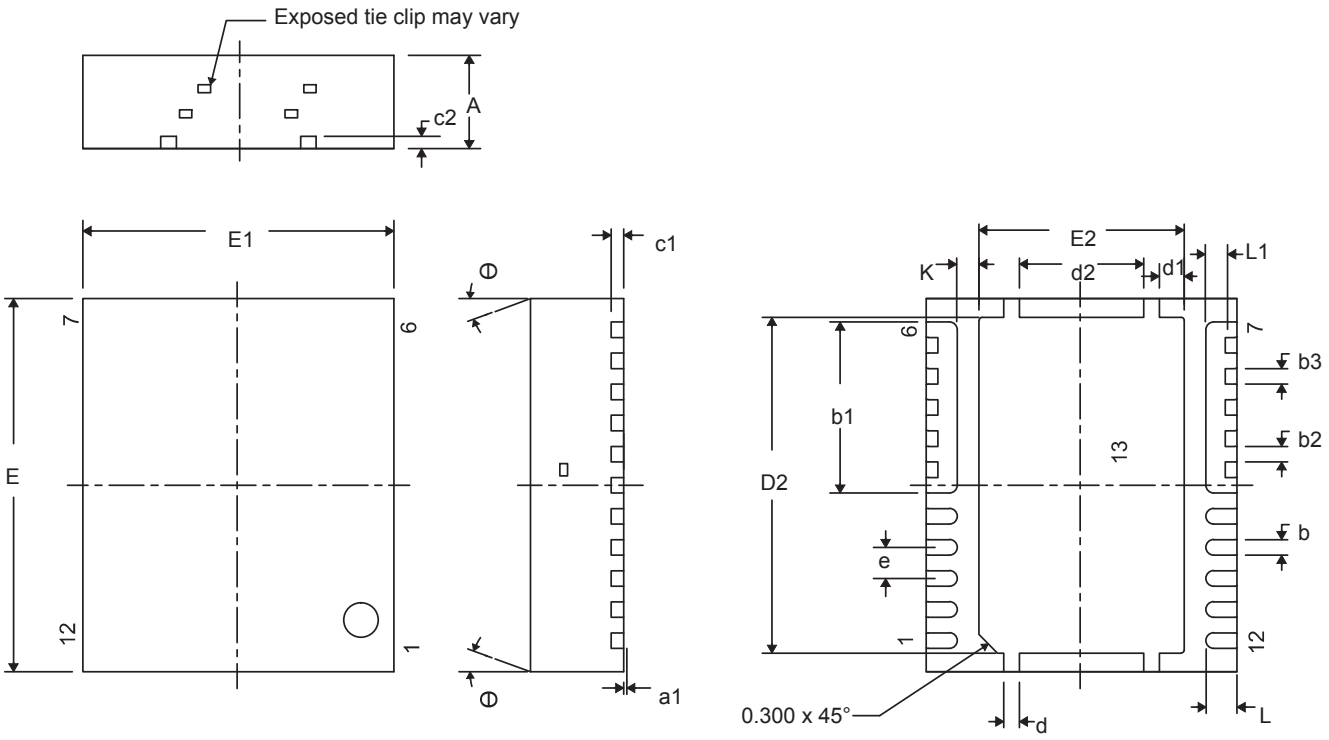


Figure 11. Recommended PCB Layout (Top Down View)

(1) Keong W. Kam, David Pommerenke, “EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis”, University of Missouri – Rolla

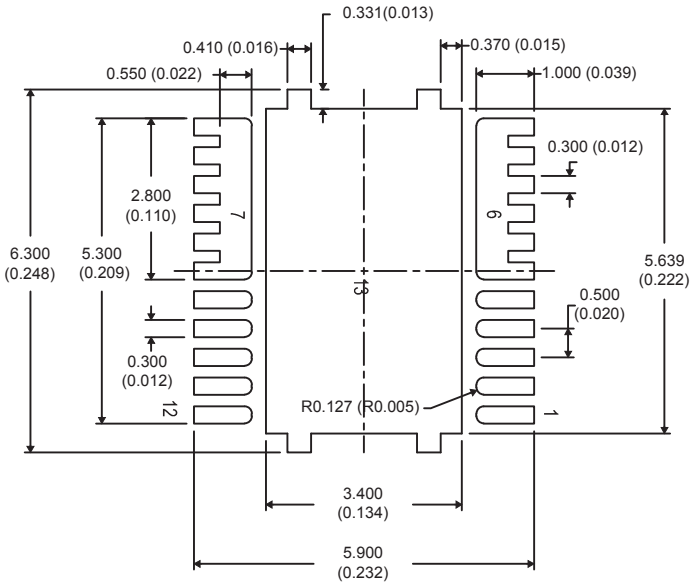
MECHANICAL DATA



TOP VIEW SIDE VIEW BOTTOM VIEW

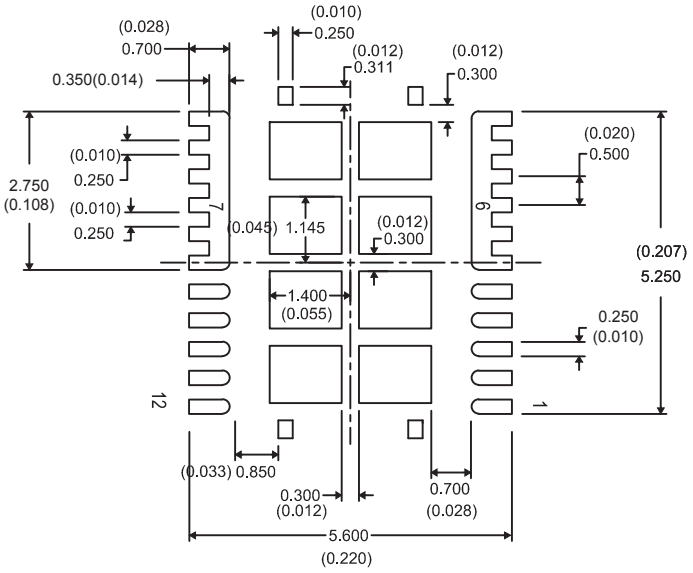
DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.400	1.450	1.500	0.055	0.057	0.059
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.350	0.008	0.010	0.013
b1		2.750 TYP			0.108 TYP	
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3		0.250 TYP			0.010 TYP	
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.150	0.200	0.250	0.006	0.008	0.010
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e		0.500 TYP			0.020 TYP	
K		0.350 TYP			0.014 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

Recommended PCB Pattern



NOTE: Dimensions are in mm (inches).

Recommended Stencil



NOTE: Dimensions are in mm (inches).

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Changed Figure 3	4

Changes from Revision A (December 2012) to Revision B	Page
• Changed the MECHANICAL DATA image and corresponding table	9
• Changed the Recommended PCB Pattern - lead width From: 0.300(0.012) To: 0.350(0.014)	10
• Changed the Recommended Stencil image	10

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD43301Q5M	Active	Production	LSON-CLIP (DQP) | 12	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	43301M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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