CSD83325L 12-V Dual N-Channel NexFET™ Power MOSFET

1 Features

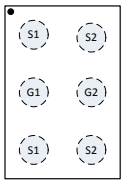
- Common drain configuration
- Low-on resistance
- Small footprint of 2.2 mm × 1.15 mm
- Lead free
- RoHS compliant
- Halogen free
- Gate ESD protection

2 Applications

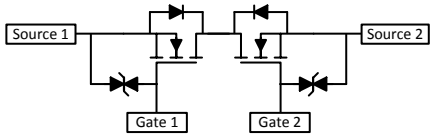
- Battery management
- Battery protection

3 Description

This 12-V, 9.9-mΩ, 2.2-mm × 1.15-mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance and gate charge in a small footprint. Its small footprint and common drain configuration make the device ideal for battery pack applications in small handheld devices.



Top View



Configuration

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{S1S2}	Source-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	8.4		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.9		nC
$R_{S1S2(on)}$	Source-to-Source On Resistance	V_{GS} = 2.5 V	17.5	mΩ
		V_{GS} = 3.8 V	10.9	mΩ
		V_{GS} = 4.5 V	9.9	mΩ
$V_{GS(th)}$	Threshold Voltage	1.0		V

Device Information(1)

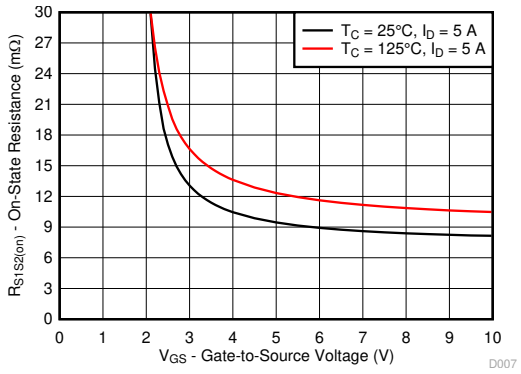
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD83325L	3000	7-Inch Reel	2.20-mm × 1.15-mm Land Grid Array (LGA) Package	Tape and Reel
CSD83325LT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

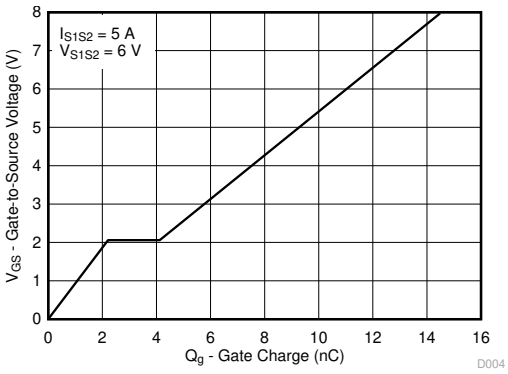
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_S	Continuous Source Current(1)	8	A
I_{SM}	Pulsed Source Current(2)	52	A
P_D	Power Dissipation	2.3	W
$V_{(ESD)}$	Human-Body Model (HBM)	2000	V
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C

(1) Device operating at a temperature of 105°C.
(2) Typical min Cu $R_{\theta JA}$ = 150°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{S1S2}	Source-to-source voltage	V_{GS} = 0 V, I_S = 250 µA	12			V
I_{S1S2}	Source-to-source leakage current	V_{GS} = 0 V, V_{S1S2} = 9.6 V			1.0	µA
I_{GSS}	Gate-to-source leakage current	V_{S1S2} = 0 V, V_{GS} = 10 V			10	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{S1S2} = V_{GS}, I_S = 250 µA	0.7	1.0	1.4	V
$R_{S1S2(on)}$	Source-to-source on resistance	V_{GS} = 2.5 V, I_S = 5 A	12.0	17.5	23.0	mΩ
		V_{GS} = 3.8 V, I_S = 5 A	8.8	10.9	13.0	mΩ
		V_{GS} = 4.5 V, I_S = 5 A	7.9	9.9	11.9	mΩ
g_{fs}	Transconductance	V_{S1S2} = 1.2 V, I_S = 5 A		36		S
DYNAMIC CHARACTERISTICS(1)						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{S1S2} = 6 V, f = 1 MHz		902	1170	pF
C_{oss}	Output capacitance			187	243	pF
C_{rss}	Reverse transfer capacitance			111	144	pF
Q_g	Gate charge total (4.5 V)	V_{S1S2} = 6 V, I_S = 5 A		8.4	10.9	nC
Q_{gd}	Gate charge gate-to-drain			1.9		nC
Q_{gs}	Gate charge gate-to-source			2.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.6		nC
Q_{oss}	Output charge	V_{S1S2} = 6 V, V_{GS} = 0 V		2.9		nC
$t_{d(on)}$	Turnon delay time	V_{S1S2} = 6 V, V_{GS} = 4.5 V, I_{S1S2} = 5 A, R_G = 0 Ω		205		ns
t_r	Rise time			353		ns
$t_{d(off)}$	Turnoff delay time			711		ns
t_f	Fall time			589		ns
DIODE CHARACTERISTICS						
$V_{F(S-S)}$	Source-to-source diode forward voltage	I_{SS} = 5 A, V_{G1S1} = 0 V, V_{G2S2} = 4.5 V		0.79	1.0	V

(1) Dynamic characteristics values specified are per single FET.

4.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		150		°C/W
	Junction-to-ambient thermal resistance(2)		55		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

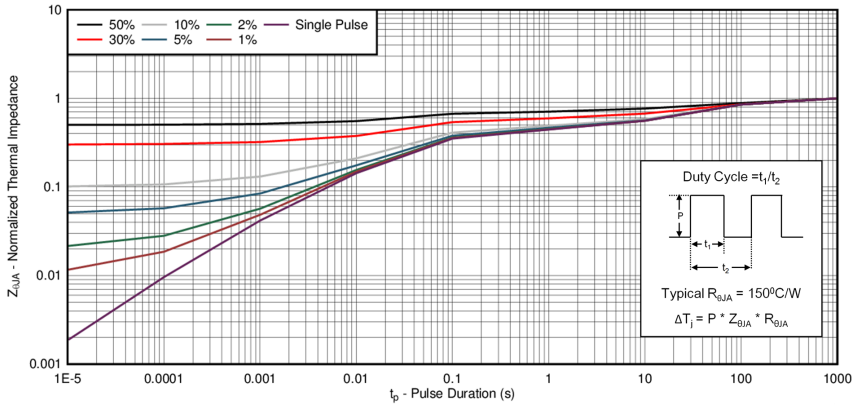


Figure 4-1. Transient Thermal Impedance

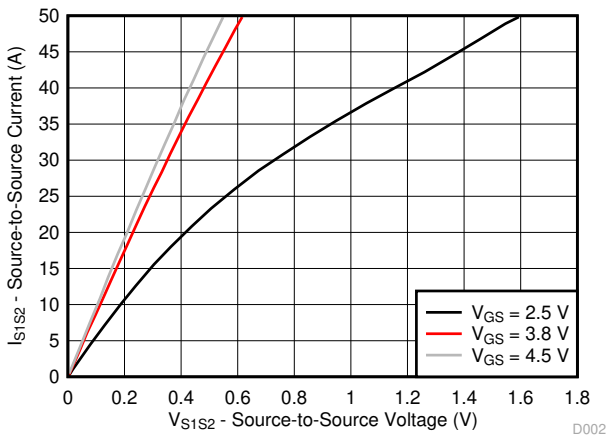
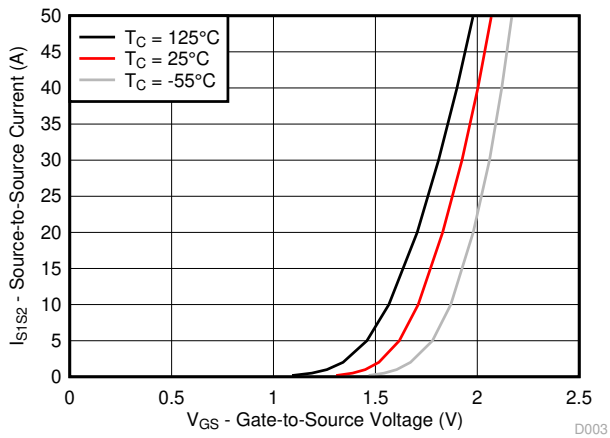
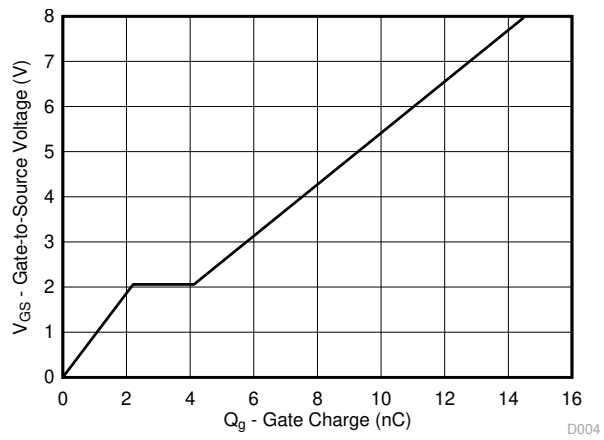


Figure 4-2. Saturation Characteristics



V_{S1S2} = 5 V

Figure 4-3. Transfer Characteristics



I_S = 5 A V_{S1S2} = 6 V

Figure 4-4. Gate Charge

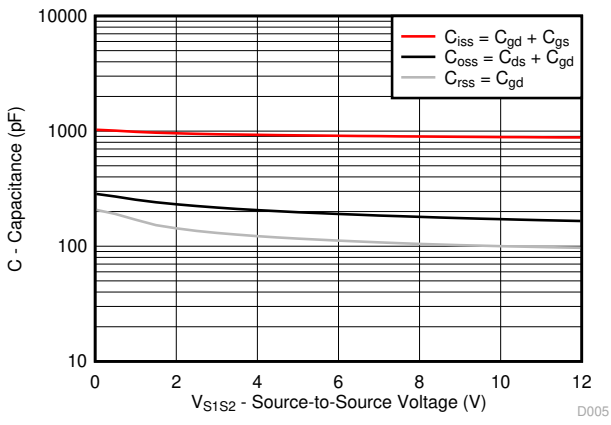
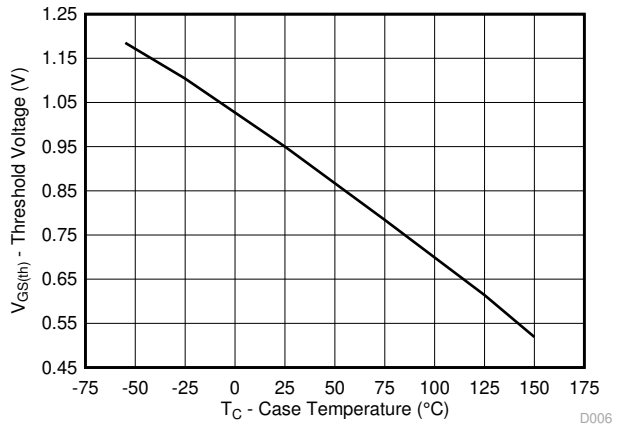


Figure 4-5. Capacitance



I_S = 250 µA

Figure 4-6. Threshold Voltage vs Temperature

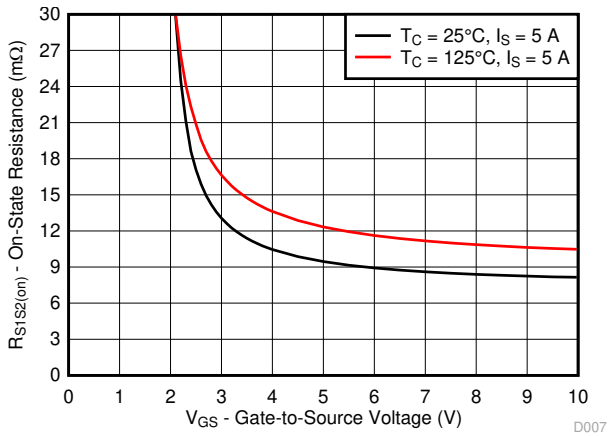
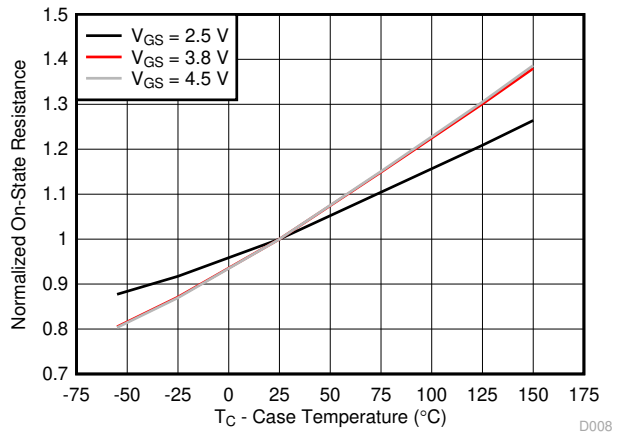


Figure 4-7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage



I_S = 5 A

Figure 4-8. Normalized On-State Resistance vs Temperature

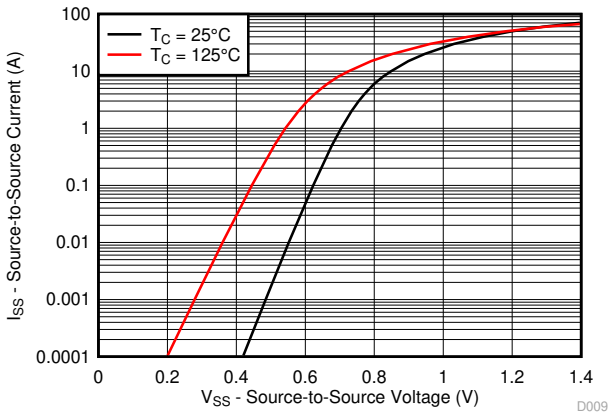
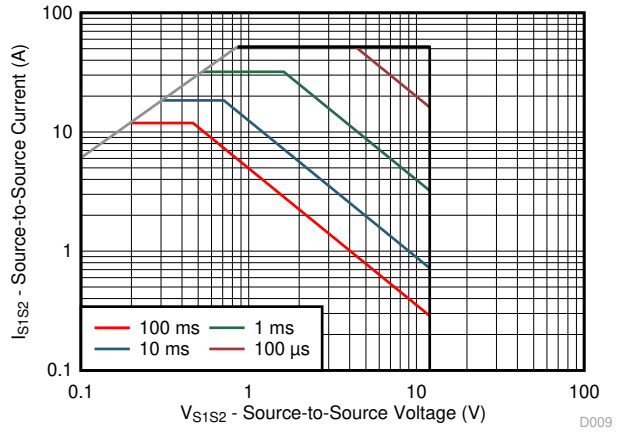


Figure 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JA}$ = 150°C/W

Figure 4-10. Maximum Safe Operating Area

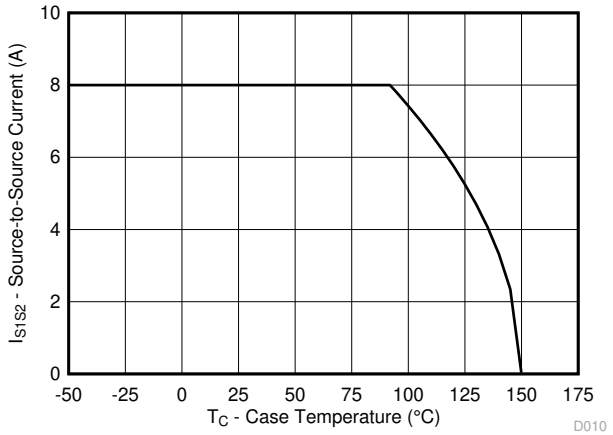


Figure 4-11. Maximum Source Current vs Temperature

5 Device and Documentation Support

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2017) to Revision C (November 2023) — **Page**

- Updated Threshold Voltage GS(th) from 0.95 V to 1.0 V 1
- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Updated Source-to-source on resistance VGS = 2.5 V from 14 mΩ to 12 mΩ 3
- Updated Gate-to-source threshold voltage from 0.75 V min, 0.95 V typ, 1.25 V max to 0.7 V min, 1.0 V typ, 1.4 V max 3

Changes from Revision A (January 2016) to Revision B (February 2017) — **Page**

- Added Diode Characteristics ($V_{F(S-S)}$) in the *Electrical Characteristics* table 3
- Added Figure 4-9 to *Typical MOSFET Characteristics* section 4

Changes from Revision * (November 2014) to Revision A (January 2016) — **Page**

- Improved graph setup for readability 4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD83325L	Active	Production	PICOSTAR (YJE) | 6	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	83325L
CSD83325L.B	Active	Production	PICOSTAR (YJE) | 6	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	83325L
CSD83325LT	Active	Production	PICOSTAR (YJE) | 6	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	83325L
CSD83325LT.B	Active	Production	PICOSTAR (YJE) | 6	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	83325L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

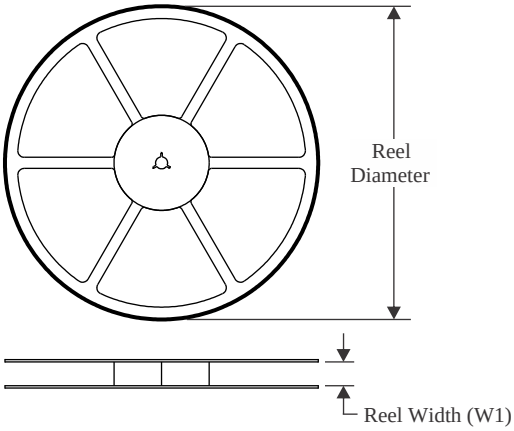
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

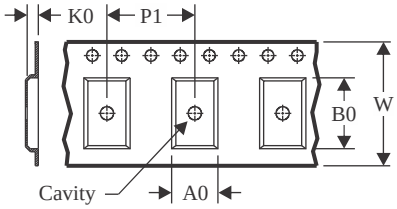
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

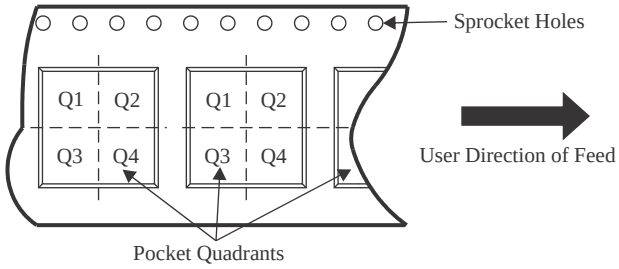


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

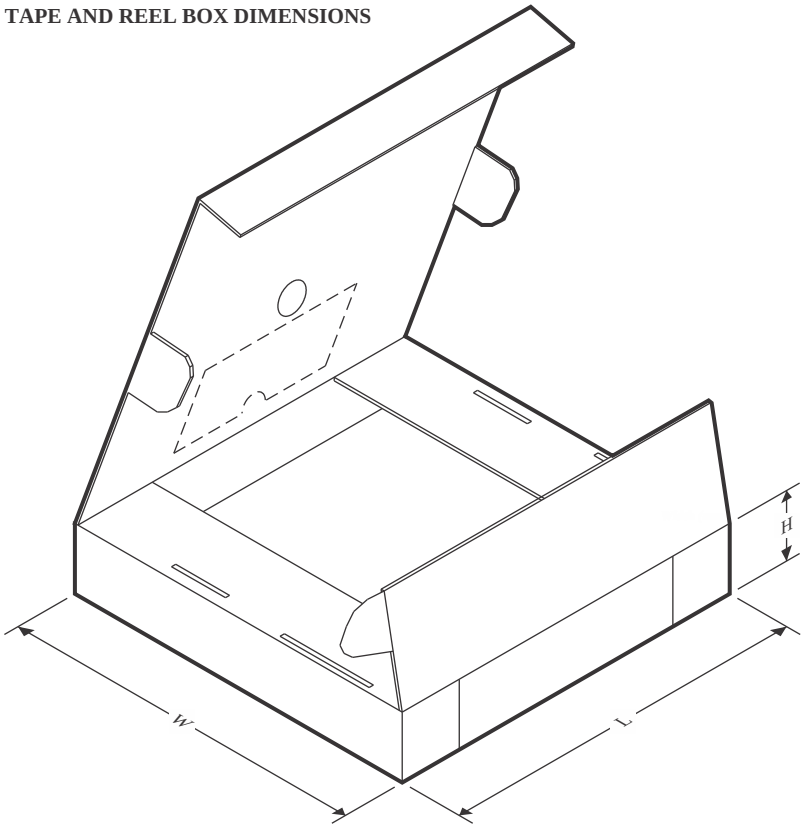
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

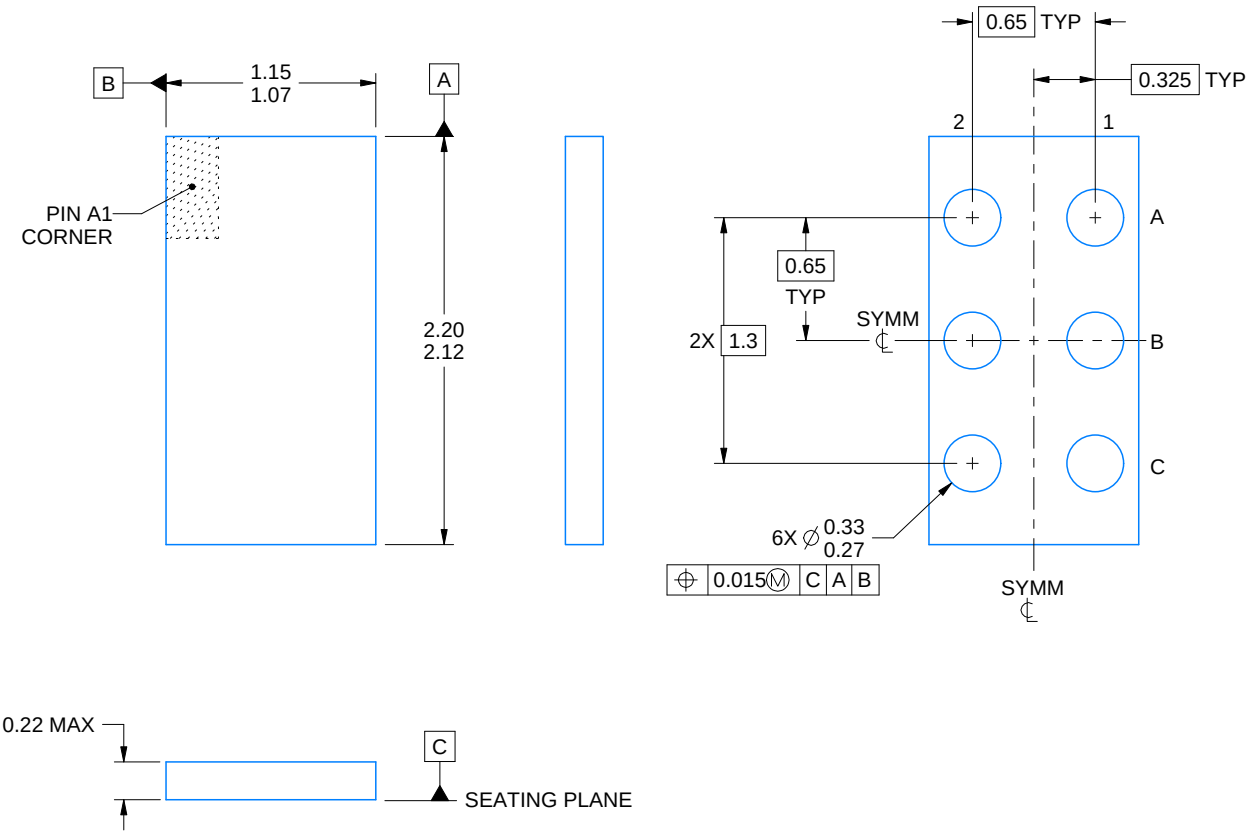
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD83325L	PICOSTAR	YJE	6	3000	180.0	8.4	1.25	2.34	0.32	4.0	8.0	Q1
CSD83325LT	PICOSTAR	YJE	6	250	180.0	8.4	1.25	2.34	0.32	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD83325L	PICOSTAR	YJE	6	3000	182.0	182.0	20.0
CSD83325LT	PICOSTAR	YJE	6	250	182.0	182.0	20.0



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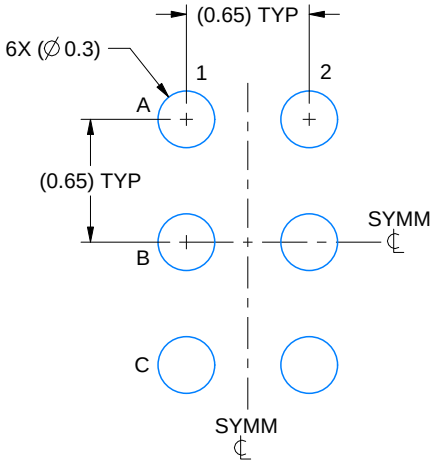
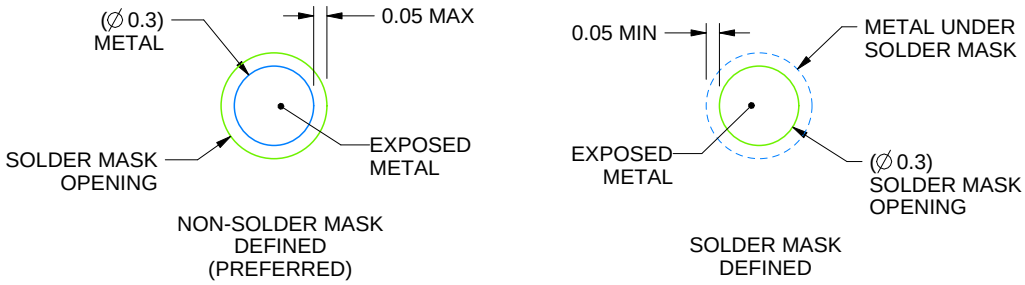
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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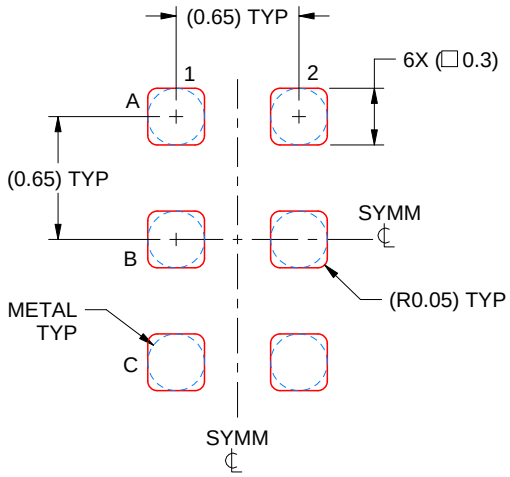
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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