TEXAS INSTRUMENTS

CSD86360Q5D

SLPS327B – SEPTEMBER 2012 – REVISED APRIL 2018

CSD86360Q5D Synchronous Buck NexFET™ Power Block

1 Features

- Half-Bridge Power Block
- 91% System Efficiency at 25 A
- Up to 50-A Operation
- High-Frequency Operation (Up to 1.5 MHz)
- High-Density SON 5-mm × 6-mm Footprint
- Optimized for 5-V Gate Drive
- Low-Switching Losses
- Ultra-Low-Inductance Package
- RoHS Compliant
- Halogen Free
- Lead-Free Terminal Plating

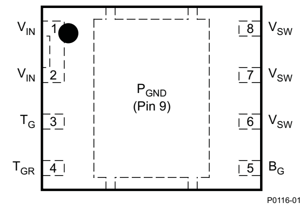
2 Applications

- Synchronous Buck Converters
  - High-Frequency Applications
  - High-Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters
- IMVP, VRM, and VRD Applications

3 Description

The CSD86360Q5D NexFET™ power block is an optimized design for synchronous buck applications offering high-current, high-efficiency, and high-frequency capability in a small 5-mm × 6-mm outline. Optimized for 5-V gate drive applications, this product offers a flexible solution capable of offering a high-density power supply when paired with any 5-V gate drive from an external controller/driver.

Figure 1. Top View

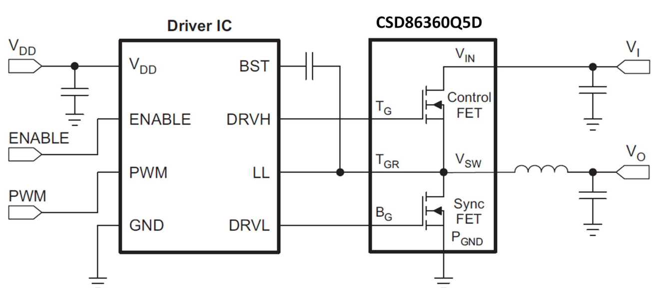


Device Information(1)

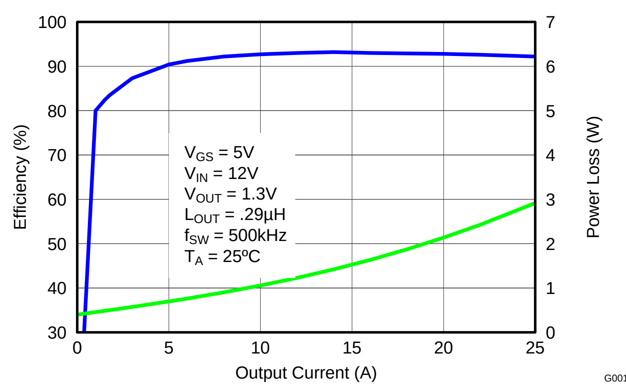
DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD86360Q5D	13-Inch Reel	2500	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit



Typical Power Block Efficiency and Power Loss



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2013) to Revision B	Page
• Changed Recommended PCB Design Overview section to *Layout* section	16
• Added *Device and Documentation Support* section	18
• Changed Mechanical Data section to *Mechanical, Packaging, and Orderable Information* section	19
• Updated *Q5D Package Dimensions* section	19
• Updated *Land Pattern Recommendation* drawing	20
• Updated *Stencil Recommendation* drawing	21

Changes from Original (September 2012) to Revision A	Page
• Changed the footnote notations in the THERMAL INFORMATION table	3
• Updated Figure 7	6
• Updated Figure 8	6
• Updated Figure 9	6
• Updated Figure 10	6

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) [(1)]

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}		25	V
	V_{SW} to P_{GND}		25	
	V_{SW} to P_{GND} (10 ns)		27	
	T_G to T_{GR}	–8	10	
	B_G to P_{GND}	–8	10	
Pulsed current rating, I_{DM} [(2)]			120	A
Power dissipation, P_D [(3)]			13	W
Avalanche energy, E_{AS}	Sync FET, I_D = 110 A, L = 0.1 mH		605	mJ
	Control FET, I_D = 61 A, L = 0.1 mH		186	
Operating junction, T_J		–55	150	°C
Storage temperature, T_{STG}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse duration ≤ 50 µs. Duty cycle ≤ 0.01%.
(3) T_{PCB} ≤ 95°C.

5.2 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{GS}	Gate drive voltage		4.5	8	V
V_{IN}	Input supply voltage			22	V
f_{SW}	Switching frequency	C_{BST} = 0.1 μF (min)	200	1500	kHz
	Operating current			50	A
T_J	Operating temperature			125	°C

5.3 Power Block Performance

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss [(1)]	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 µH, T_J = 25°C		2.6		W
I_{QVIN}	V_{IN} quiescent current	T_G to T_{GR} = 0 V B_G to P_{GND} = 0 V		10		µA

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5-V driver IC.

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) [(1)]			102	°C/W
	Junction-to-ambient thermal resistance (max Cu) [(1)(2)]			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2) Cu.

Thermal Information (continued)

T_A = 25°C (unless otherwise stated)

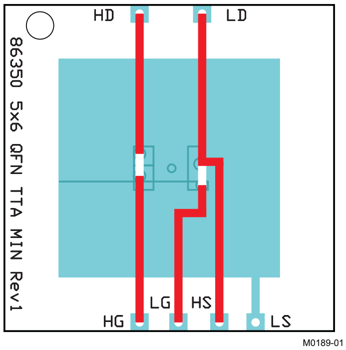
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(1)			20	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)(1)			2	

5.5 Electrical Characteristics

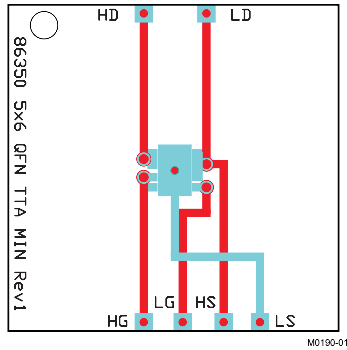
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			
			MIN	TYP	MAX	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	25			25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1		2.1	0.75		1.15	V
$Z_{DS(on)}$	Drain-to-source on-impedance	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.3 V I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 μH		3.7			0.7		mΩ
g_{fs}	Transconductance	V_{DS} = 10 V, I_{DS} = 20 A		113			169		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance(1)	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		1590	2060		3910	5080	pF
C_{OSS}	Output capacitance(1)			840	1090		1970	2560	pF
C_{RSS}	Reverse transfer capacitance(1)			42	54		53	69	pF
R_G	Series gate resistance(1)			1.2	2.5		1.1	2.2	Ω
Q_g	Gate charge total (4.5 V)(1)	V_{DS} = 12.5 V, I_{DS} = 20 A		9.7	12.6		23	30	nC
Q_{gd}	Gate charge gate-to-drain			2.3			3.6		nC
Q_{gs}	Gate charge gate-to-source			3.5			6.0		nC
$Q_{g(th)}$	Gate charge at Vth			1.9			3.5		nC
Q_{OSS}	Output charge	V_{DS} = 12.5 V, V_{GS} = 0 V		15.1			33		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_{DS} = 20 A, R_G = 2 Ω		8.4			9.5		ns
t_r	Rise time			20.4			14.8		ns
$t_{d(off)}$	Turnoff delay time			14.5			29.3		ns
t_f	Fall time			4.3			6.6		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	I_{DS} = 20 A, V_{GS} = 0 V		0.85	1		0.75	0.82	V
Q_{rr}	Reverse recovery charge	V_{dd} = 12 V, I_F = 20 A, di/dt = 300 A/μs		27			50		nC
t_{rr}	Reverse recovery time			22			34		ns

(1) Specified by design.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 102°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.6 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise.

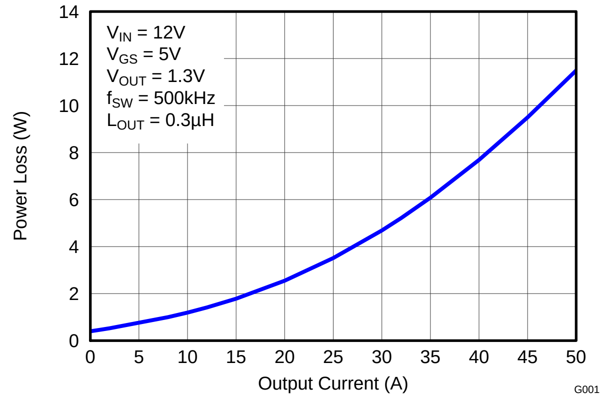


Figure 2. Power Loss vs Output Current

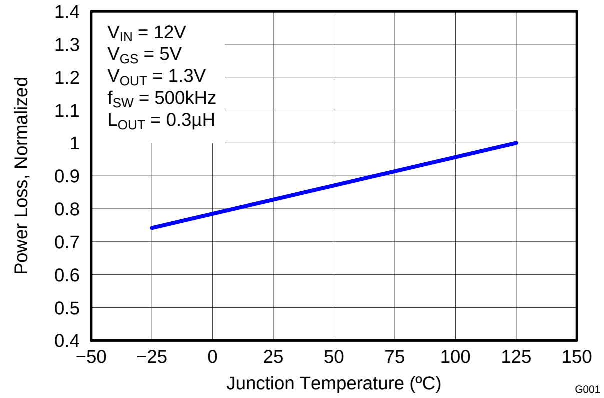


Figure 3. Normalized Power Loss vs Temperature

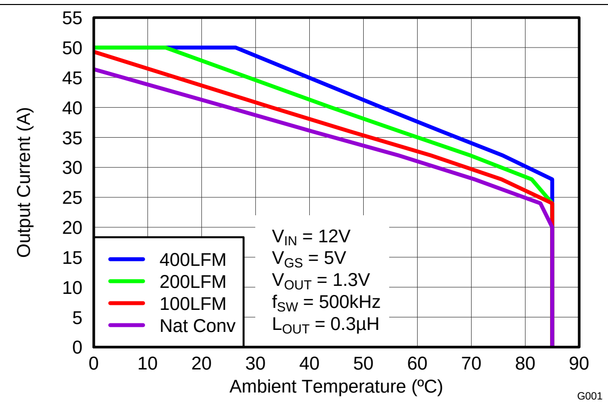


Figure 4. Safe Operating Area – PCB Vertical Mount (1)

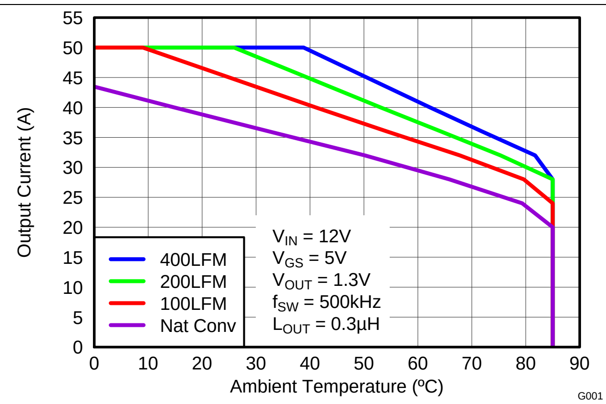


Figure 5. Safe Operating Area – PCB Horizontal Mount (1)

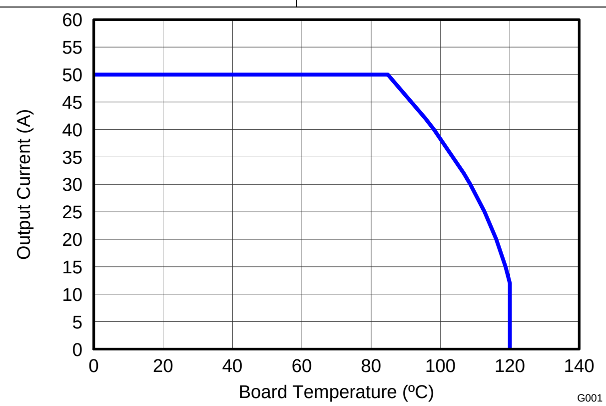


Figure 6. Typical Safe Operating Area(1)

(1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* section for detailed explanation.

Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise.

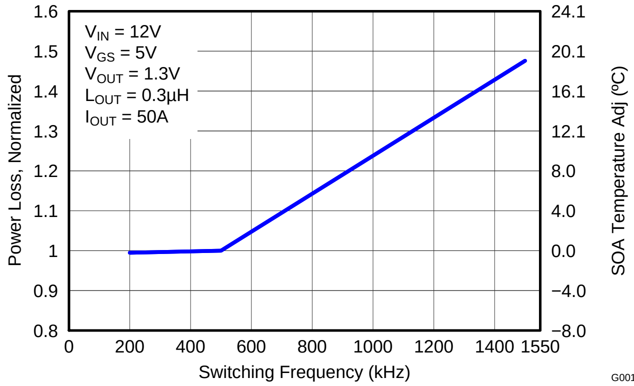


Figure 7. Normalized Power Loss vs Switching Frequency

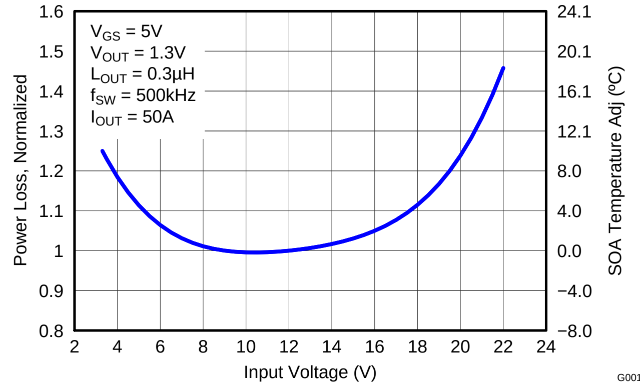


Figure 8. Normalized Power Loss vs Input Voltage

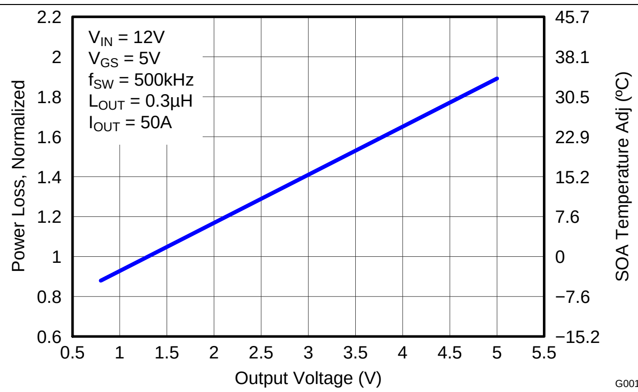


Figure 9. Normalized Power Loss vs Output Voltage

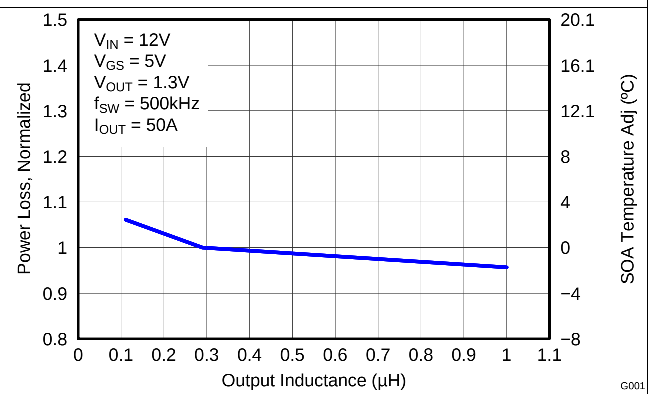


Figure 10. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

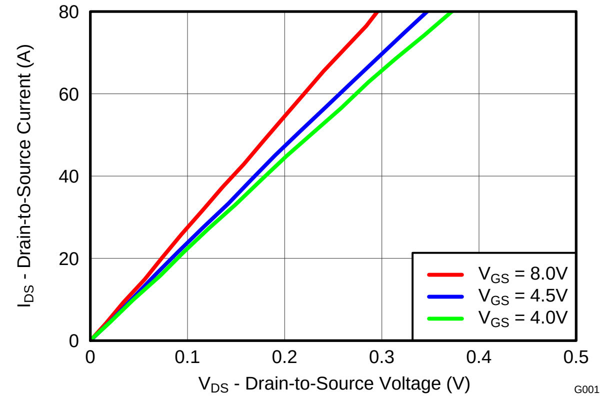


Figure 11. Control MOSFET Saturation

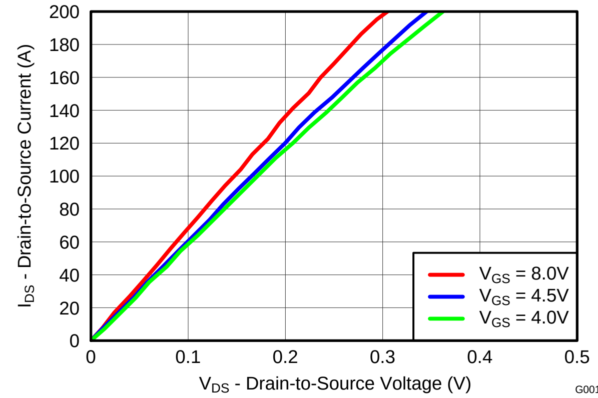


Figure 12. Sync MOSFET Saturation

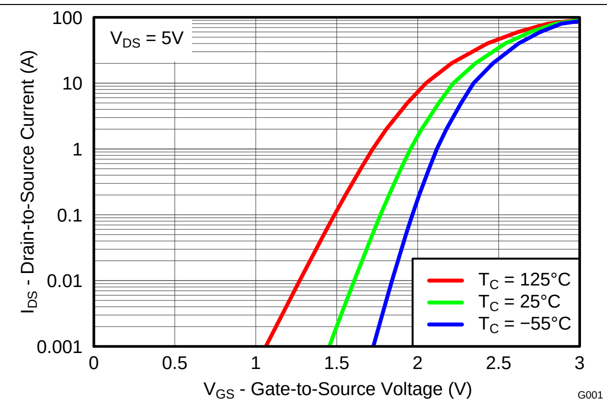


Figure 13. Control MOSFET Transfer

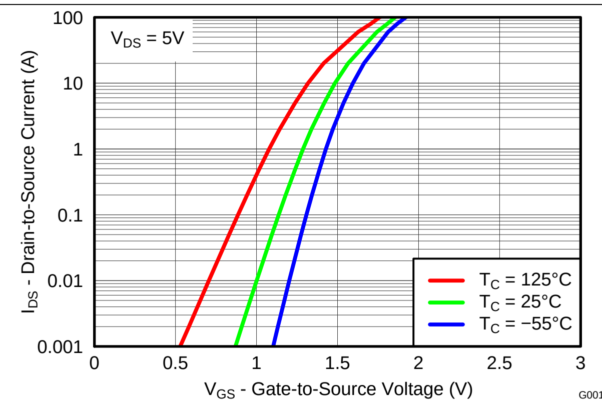


Figure 14. Sync MOSFET Transfer

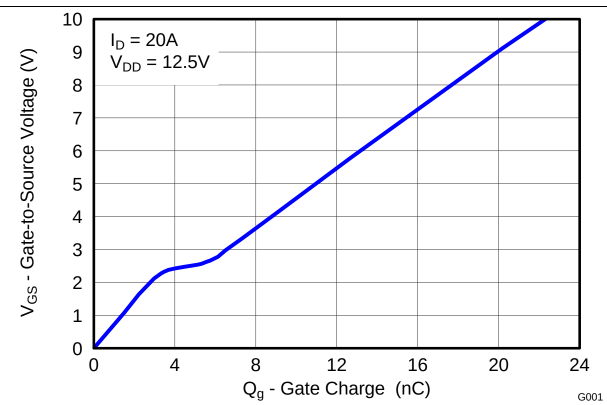


Figure 15. Control MOSFET Gate Charge

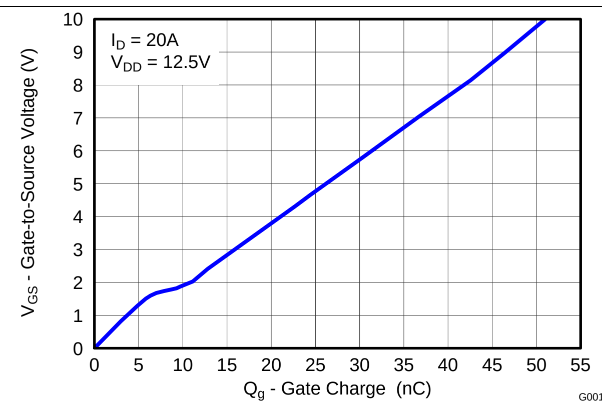


Figure 16. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

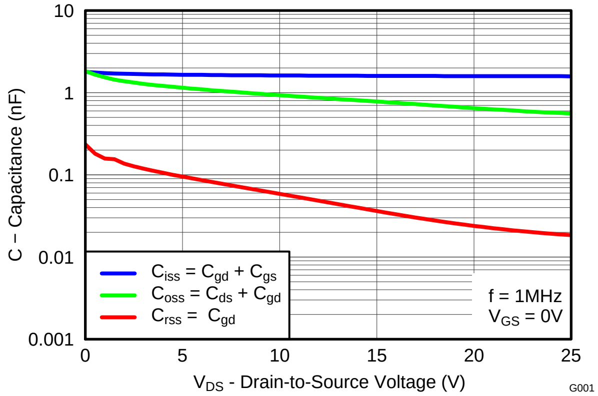


Figure 17. Control MOSFET Capacitance

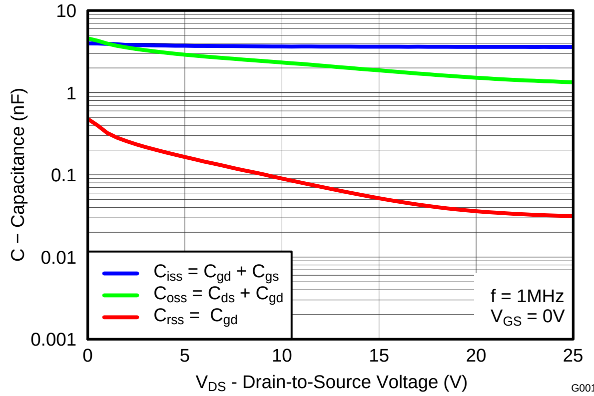


Figure 18. Sync MOSFET Capacitance

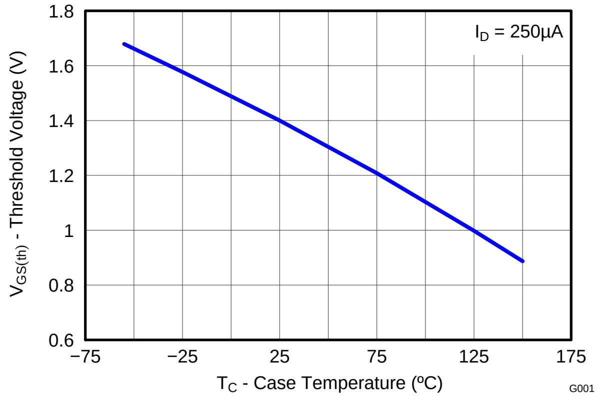


Figure 19. Control MOSFET $V_{GS(th)}$

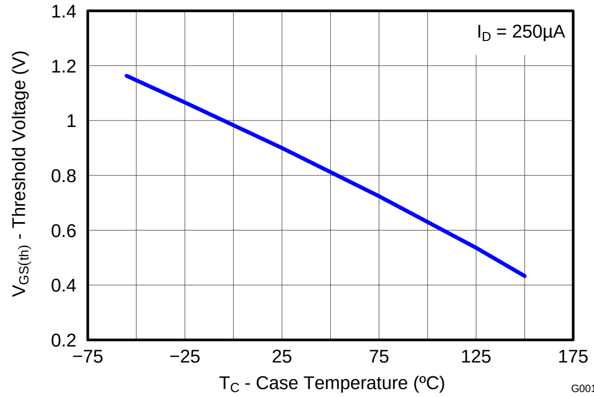


Figure 20. Sync MOSFET $V_{GS(th)}$

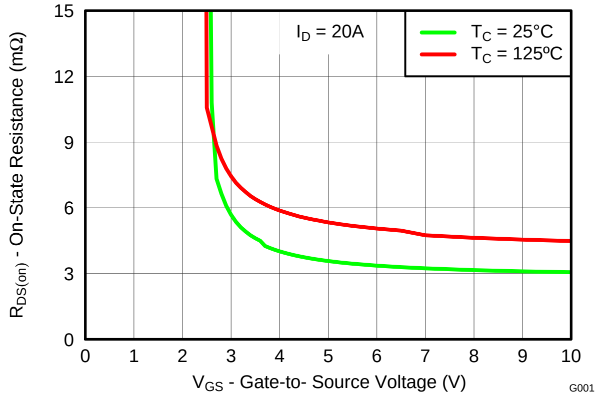


Figure 21. Control MOSFET $R_{DS(on)}$ vs V_{GS}

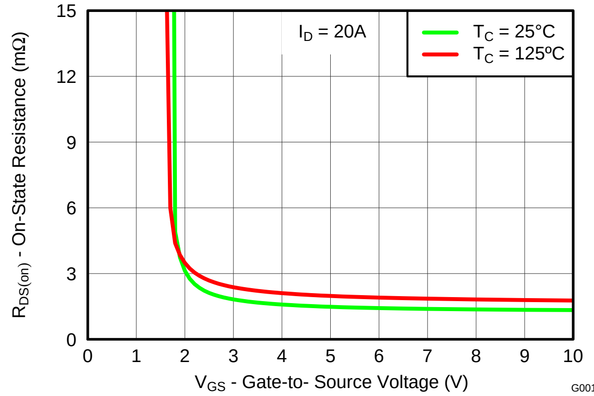


Figure 22. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

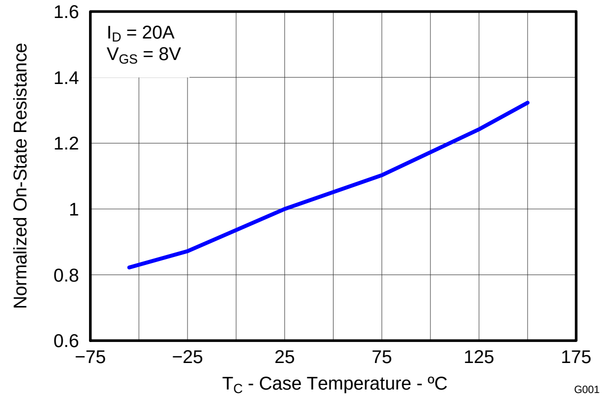


Figure 23. Control MOSFET Normalized $R_{DS(on)}$

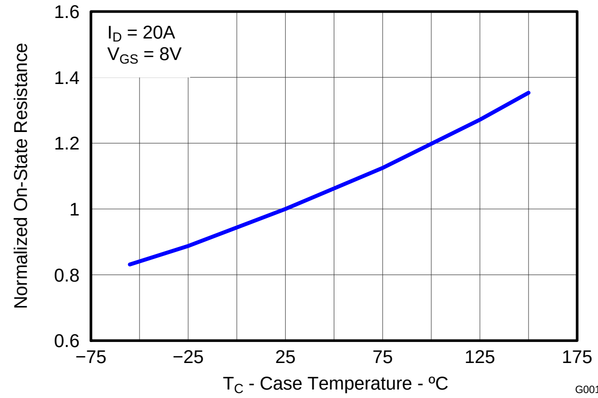


Figure 24. Sync MOSFET Normalized $R_{DS(on)}$

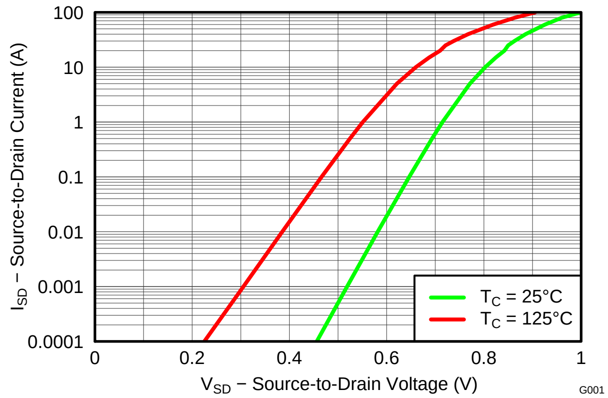


Figure 25. Control MOSFET Body Diode

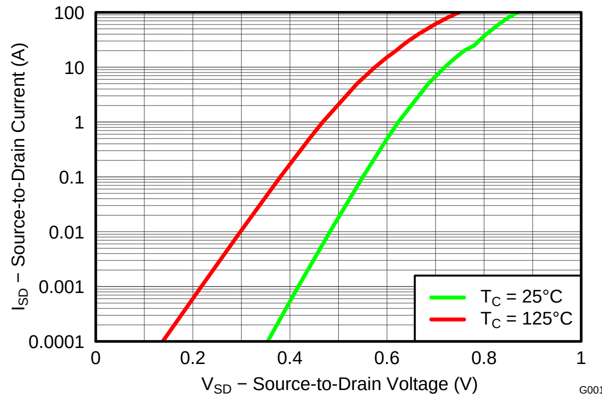


Figure 26. Sync MOSFET Body Diode

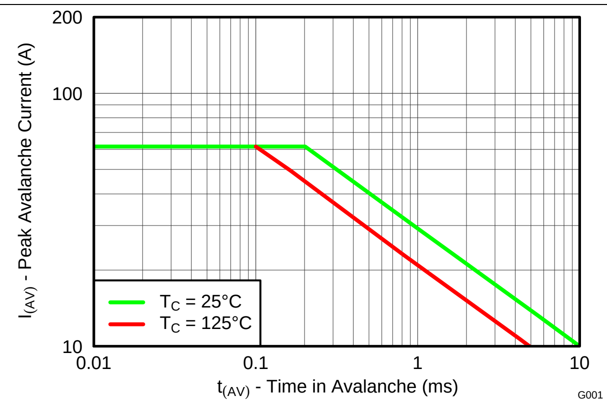


Figure 27. Control MOSFET Unclamped Inductive Switching

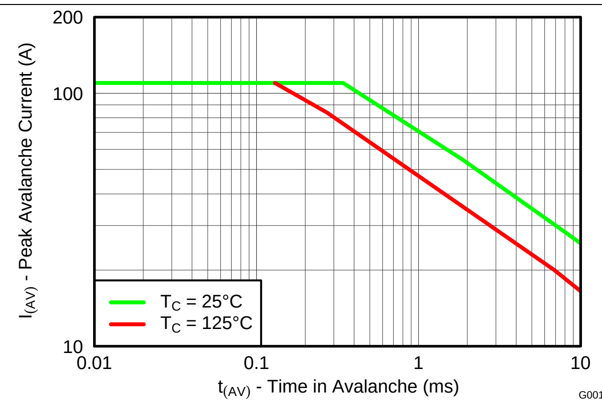


Figure 28. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following Application section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI customers are responsible for determining suitability of components selection for their designs. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Equivalent System Performance

Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see Figure 29). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

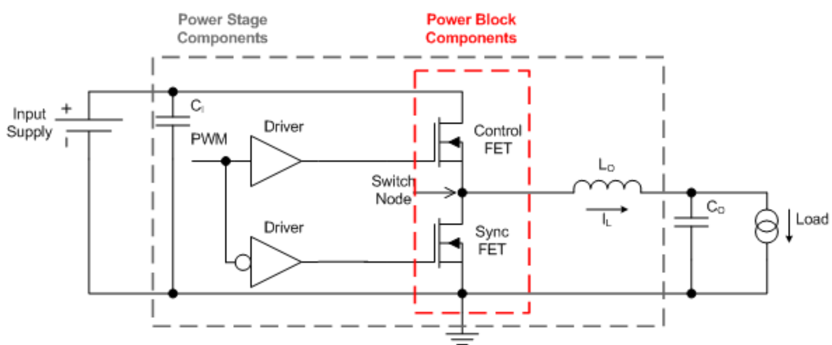


Figure 29. Equivalent System Schematic

The CSD86360Q5D is part of TI's power block product family, which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon, which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD}, Q_{GS}, and Q_{RR}. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see Figure 30). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET, which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in *Power Loss Calculation With CSI Consideration for Synchronous Buck Converters* (SLPA009).

Application Information (continued)

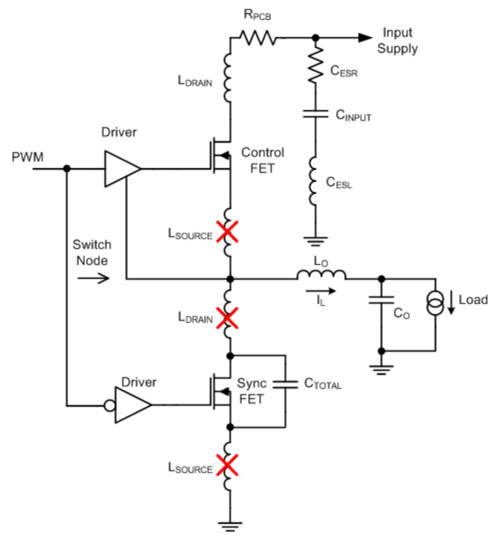


Figure 30. Elimination of Parasitic Inductances

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figure 31 and Figure 32 compare the efficiency and power loss performance of the CSD86360Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD86360Q5D clearly highlights the importance of considering the effective AC on-impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.

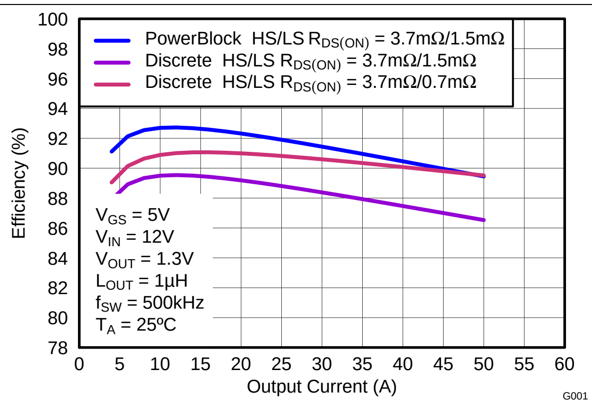


Figure 31. Efficiency Comparison for Discrete Parts vs Power Block

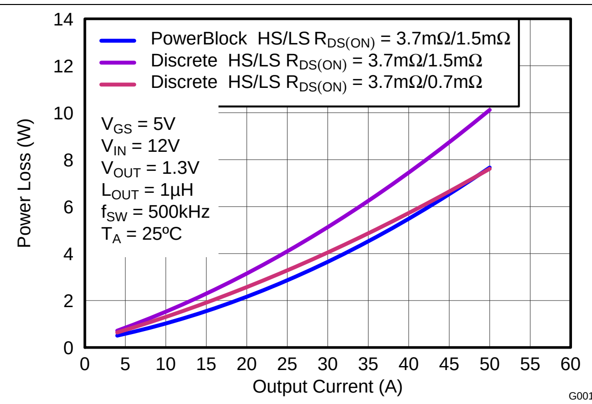


Figure 32. Power Loss Comparison for Discrete Parts vs Power Block

Application Information (continued)

Table 1 below compares the traditional DC measured $R_{DS(ON)}$ of CSD86360Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD86360Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Table 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

PARAMETER	HS		LS	
	TYP	MAX	TYP	MAX
Effective AC on-impedance $Z_{DS(ON)}$ (V_{GS} = 5 V)	3.7	—	0.7	—
DC measured $R_{DS(ON)}$ (V_{GS} = 4.5 V)	3.7	4.5	1.5	1.9

The CSD86360Q5D NexFET™ power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed, which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 2 plots the power loss of the CSD86360Q5D as a function of load current. This curve is measured by configuring and running the CSD86360Q5D as it would be in the final application (see Figure 33).The measured power loss is the CSD86360Q5D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power loss} \quad (1)$$

The power loss curve in Figure 2 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Area (SOA) Curves

The SOA curves in the CSD86360Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 4 to Figure 6 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

6.1.4 Normalized Curves

The normalized curves in the CSD86360Q5D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

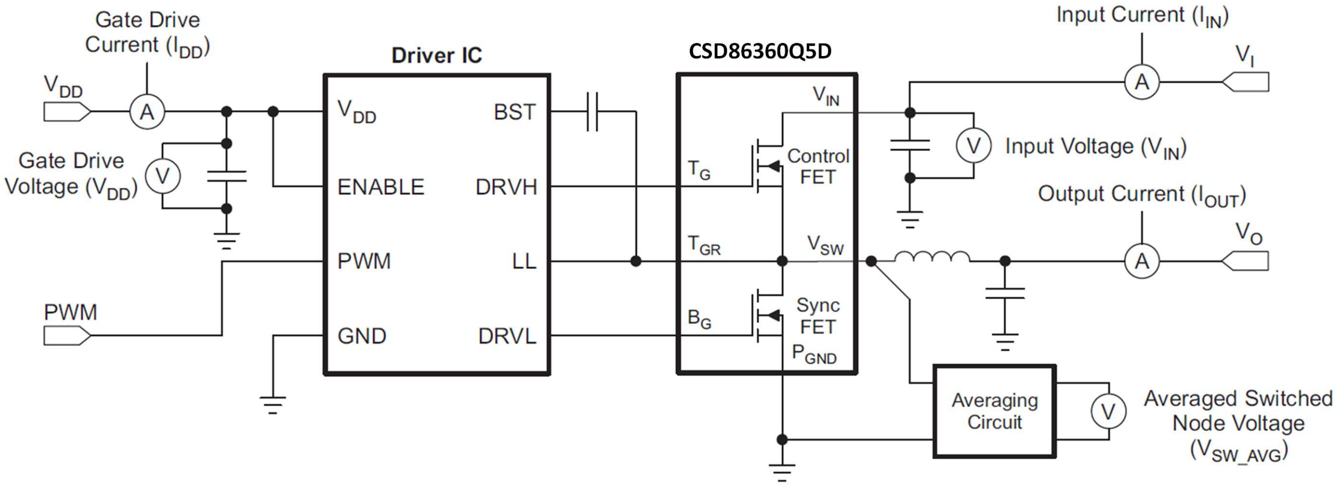


Figure 33. Typical Application

Typical Application (continued)

6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Operating Conditions* section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.1.1 Operating Conditions

- Output current = 25 A
- Input voltage = 7 V
- Output voltage = 1 V
- Switching frequency = 800 kHz
- Inductor = 0.2 µH

6.2.1.2 Calculating Power Loss

- Power loss at 25 A = 3.5 W (Figure 2)
- Normalized power loss for input voltage ≈ 1.03 (Figure 8)
- Normalized power loss for output voltage ≈ 0.90 (Figure 9)
- Normalized power loss for switching frequency ≈ 1.15 (Figure 7)
- Normalized power loss for output inductor ≈ 1.03 (Figure 10)
- **Final calculated power loss = 3.5 W × 1.03 × 0.90 × 1.15 × 1.03 ≈ 3.84 W**

6.2.1.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 1.3°C (Figure 8)
- SOA adjustment for output voltage ≈ –2.5°C (Figure 9)
- SOA adjustment for switching frequency ≈ 6.0°C (Figure 7)
- SOA adjustment for output inductor ≈ 1.3°C (Figure 10)
- **Final calculated SOA adjustment = 1.3 + (–2.5) + 6.0 + 1.3 ≈ 6.1°C**

In the design example above, the estimated power loss of the CSD86360Q5D would increase to 3.84 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 6.1°C. Figure 34 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 6.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

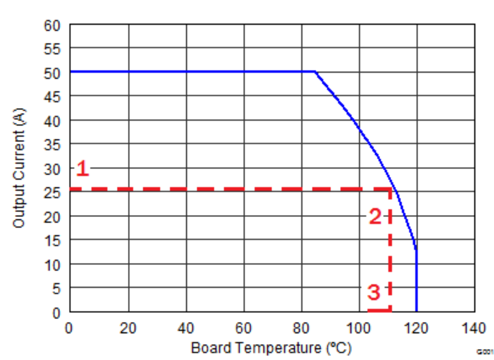


Figure 34. Power Block SOA

7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1.1 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 35). The example in Figure 35 uses 6 × 10-µF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins. T_G and B_G should connect to the outputs of the driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Please refer to TI App Note *Snubber Circuits: Theory, Design and Application* (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the VSW node and PGND see Figure 35 [(1)]

7.1.2 Thermal Performance

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 35 uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Layout Example

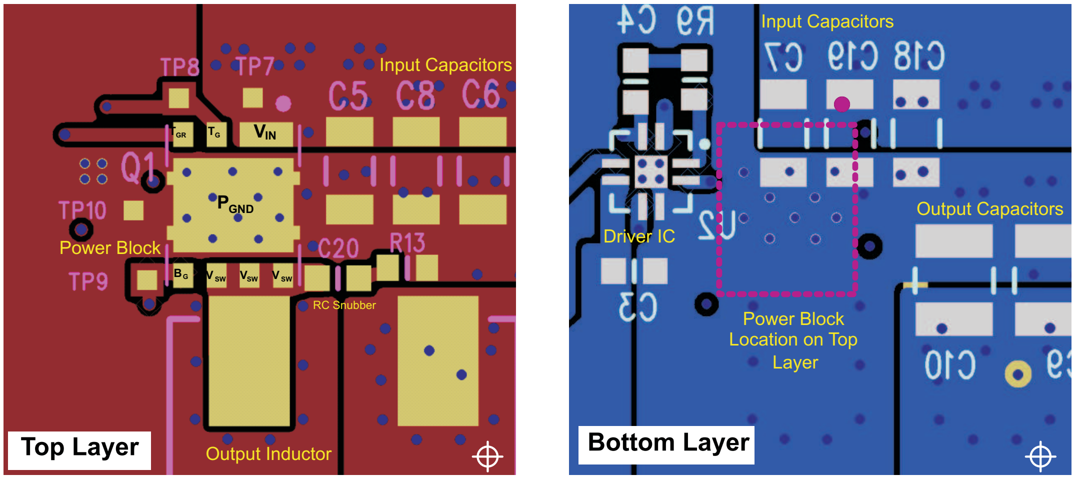


Figure 35. Recommended PCB Layout (Top Down View)

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- *Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters* (SLPA009)
- *Snubber Circuits: Theory, Design and Application* (SLUP100)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.4 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
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8.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.6 Glossary

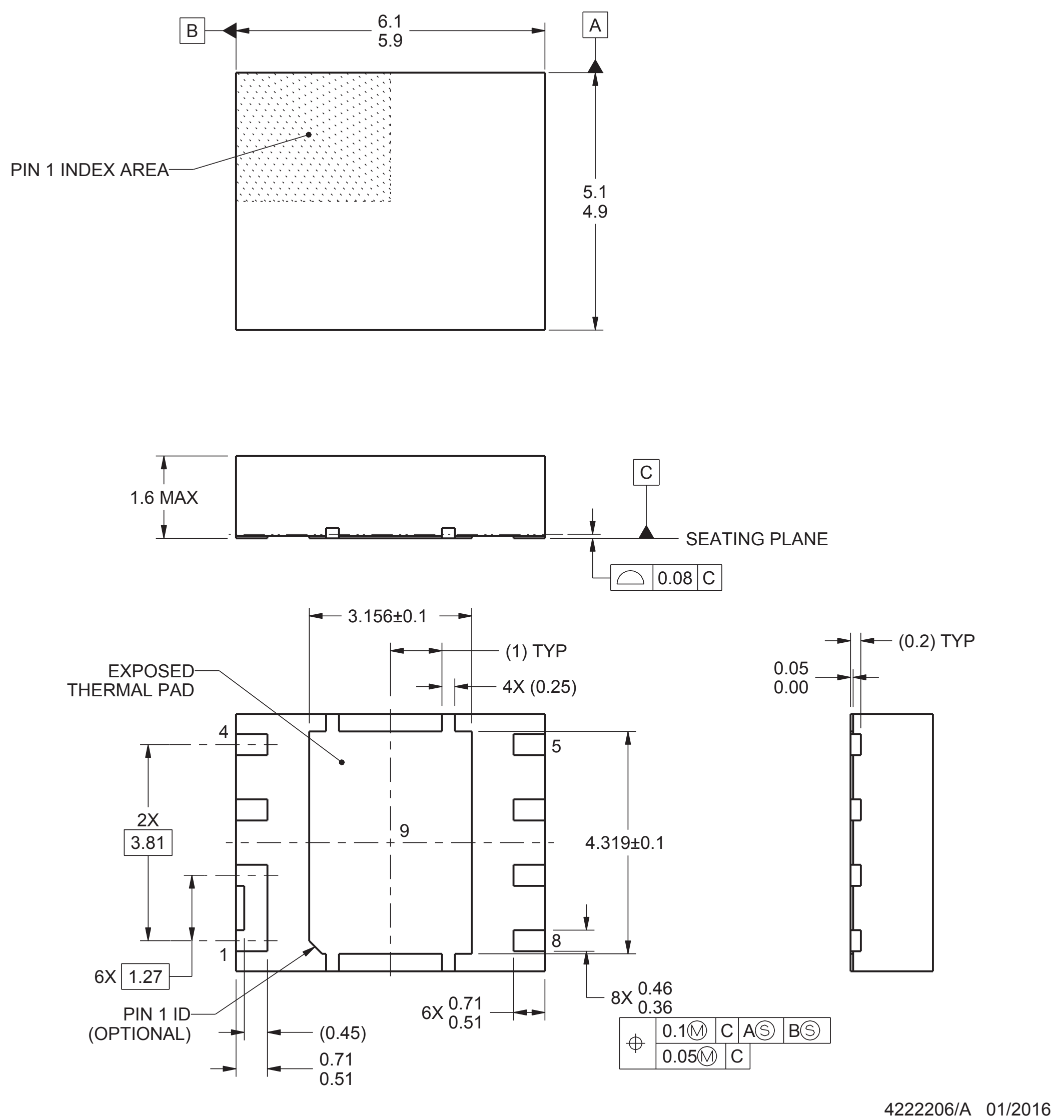
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Q5D Package Dimensions

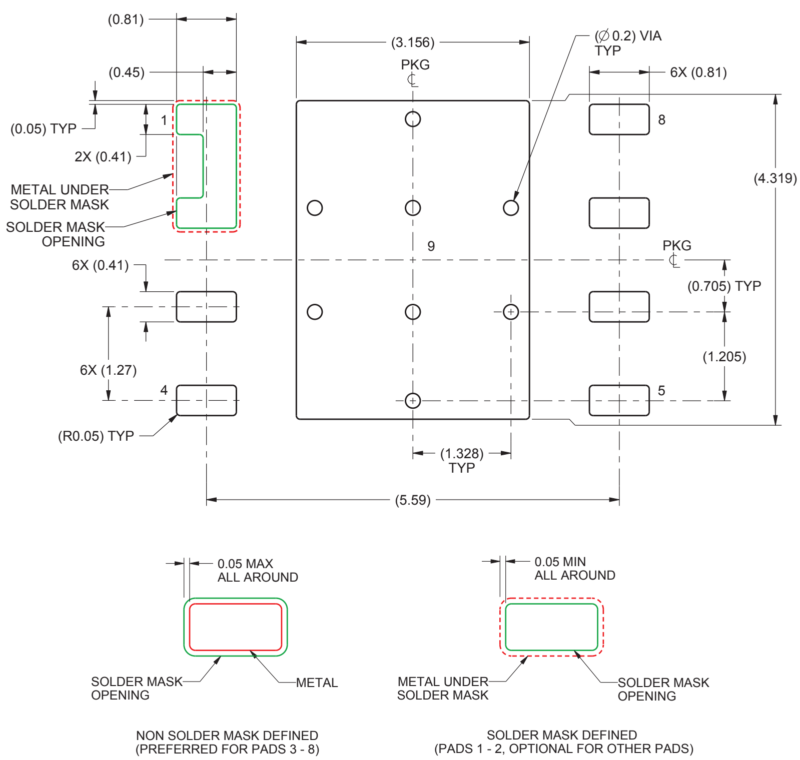


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

Q5D Package Dimensions (continued)

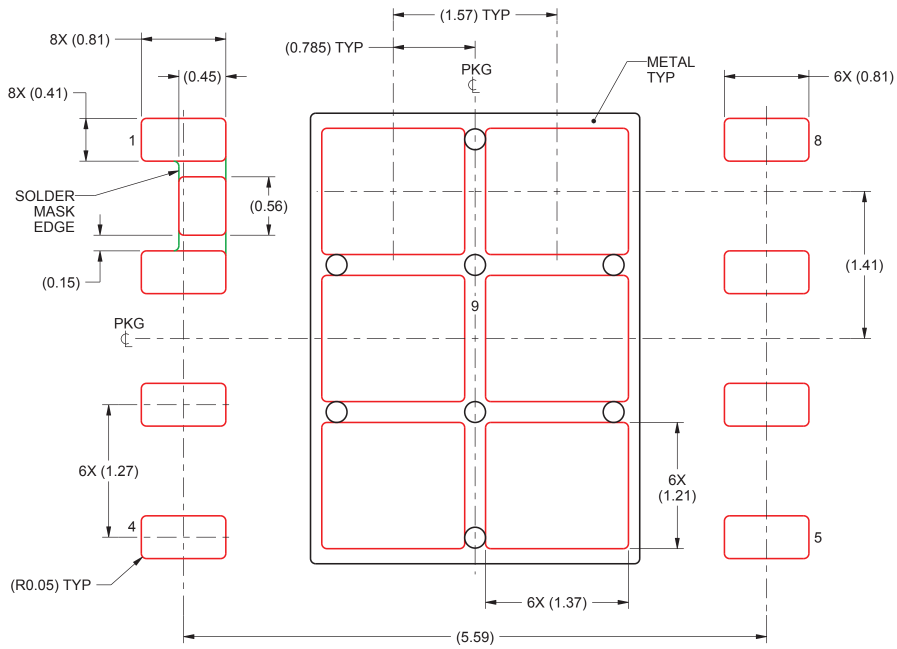
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
a	1.40	1.5	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 TYP		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—
K	0.812		0.032	

9.2 Land Pattern Recommendation



1. This package is designed to be soldered to a thermal pad on the board. For more information, see *QFN/SON PCB Attachment* (SLUA271).
2. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

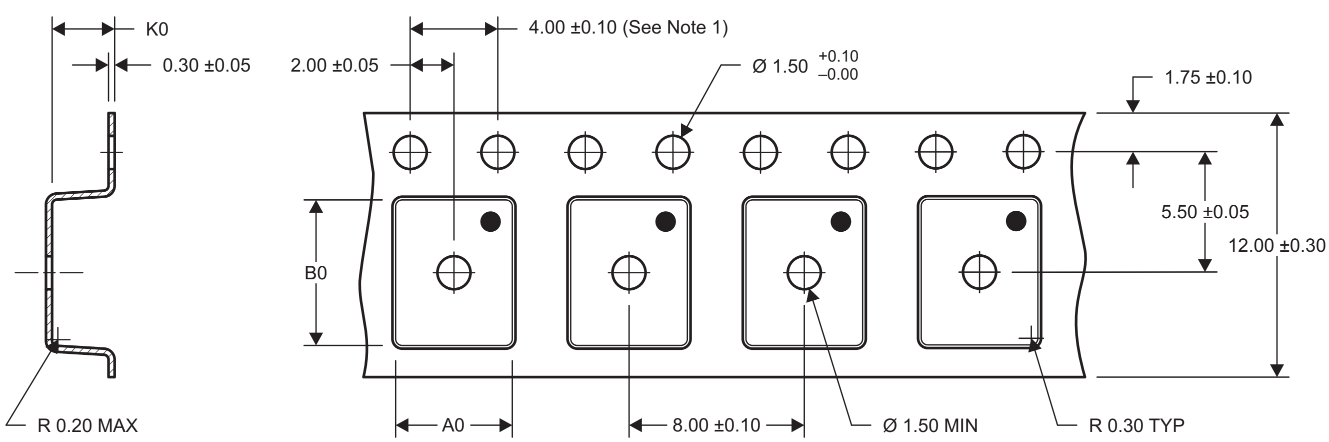
9.3 Stencil Recommendation



1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

9.4 Q5D Tape and Reel Information



A0 = 5.30 ±0.10
B0 = 6.50 ±0.10
K0 = 1.90 ±0.10

M0191-01

NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene.
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.3 ±0.05 mm.
6. MSL1 260°C (IR and convection) PbF reflow compatible.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD86360Q5D	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	86360D
CSD86360Q5D.B	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	86360D
CSD86360Q5DG4	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	86360D
CSD86360Q5DG4.B	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	86360D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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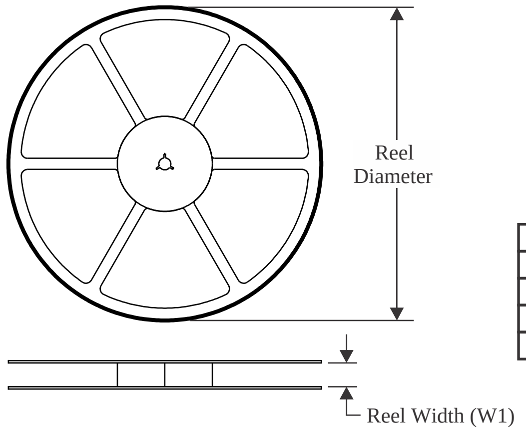
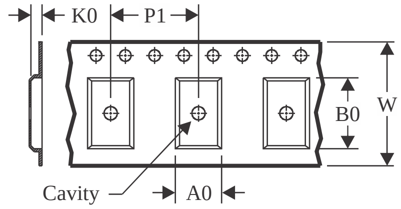
TAPE AND REEL INFORMATION

REEL DIMENSIONS

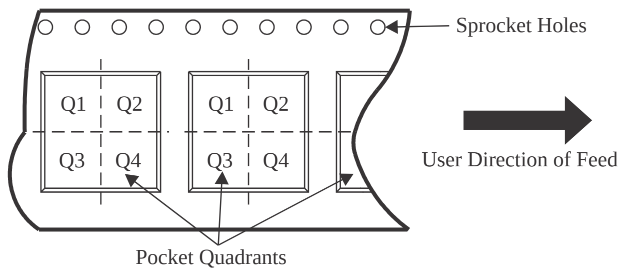


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

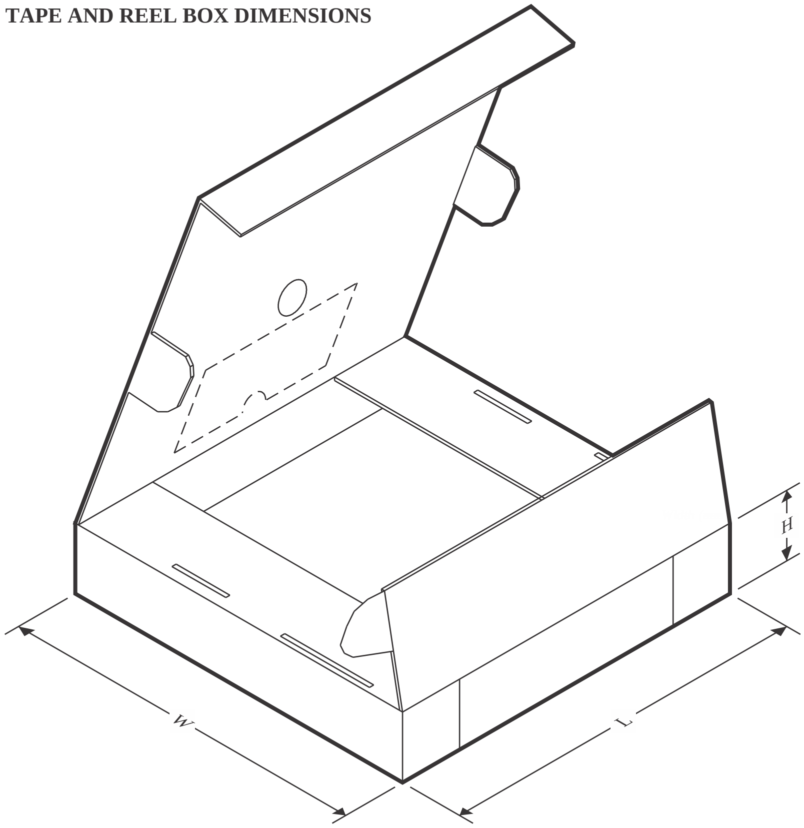
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

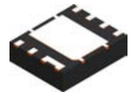
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD86360Q5D	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2
CSD86360Q5DG4	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD86360Q5D	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0
CSD86360Q5DG4	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0

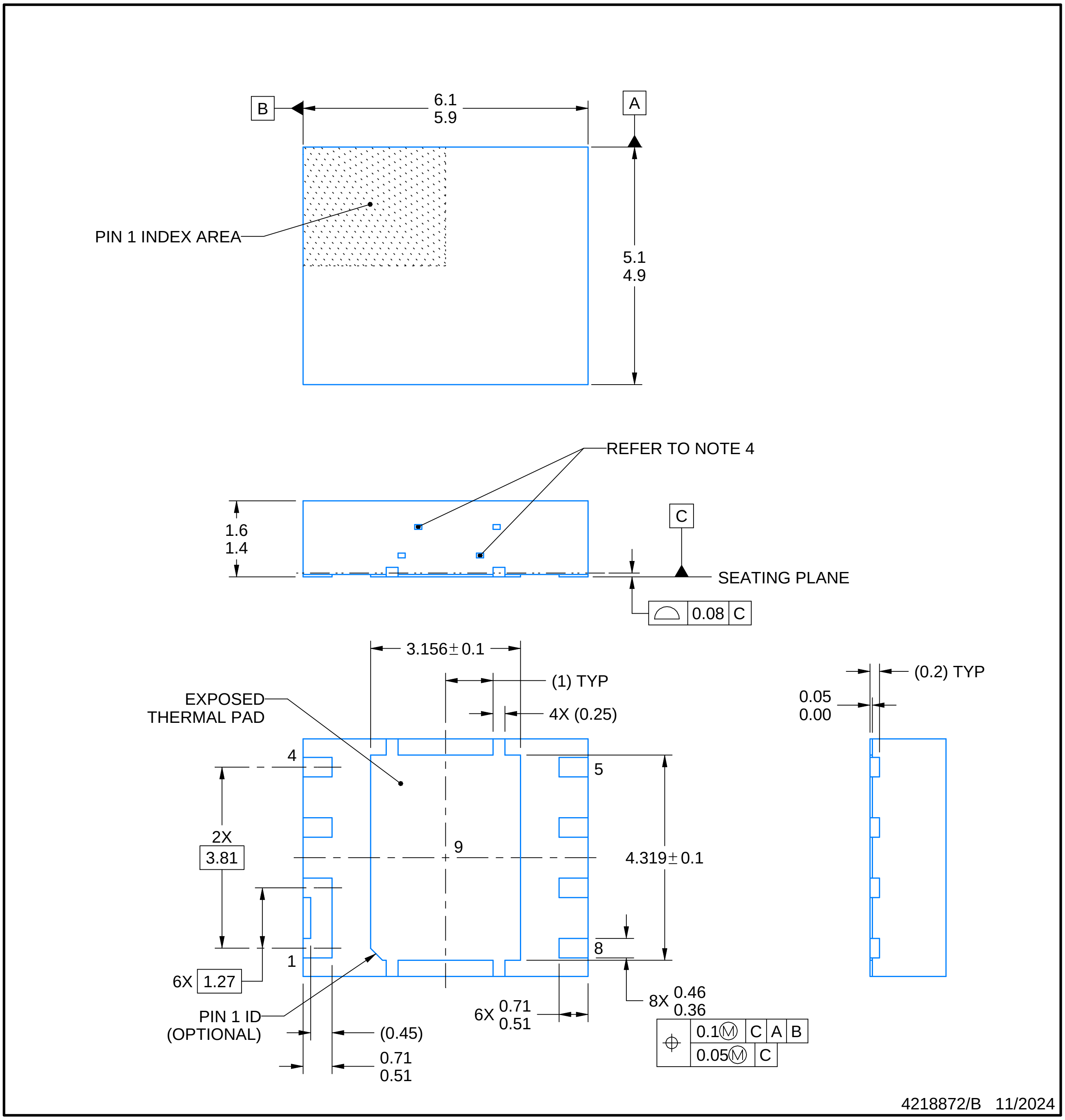


PACKAGE OUTLINE

DQY0008A

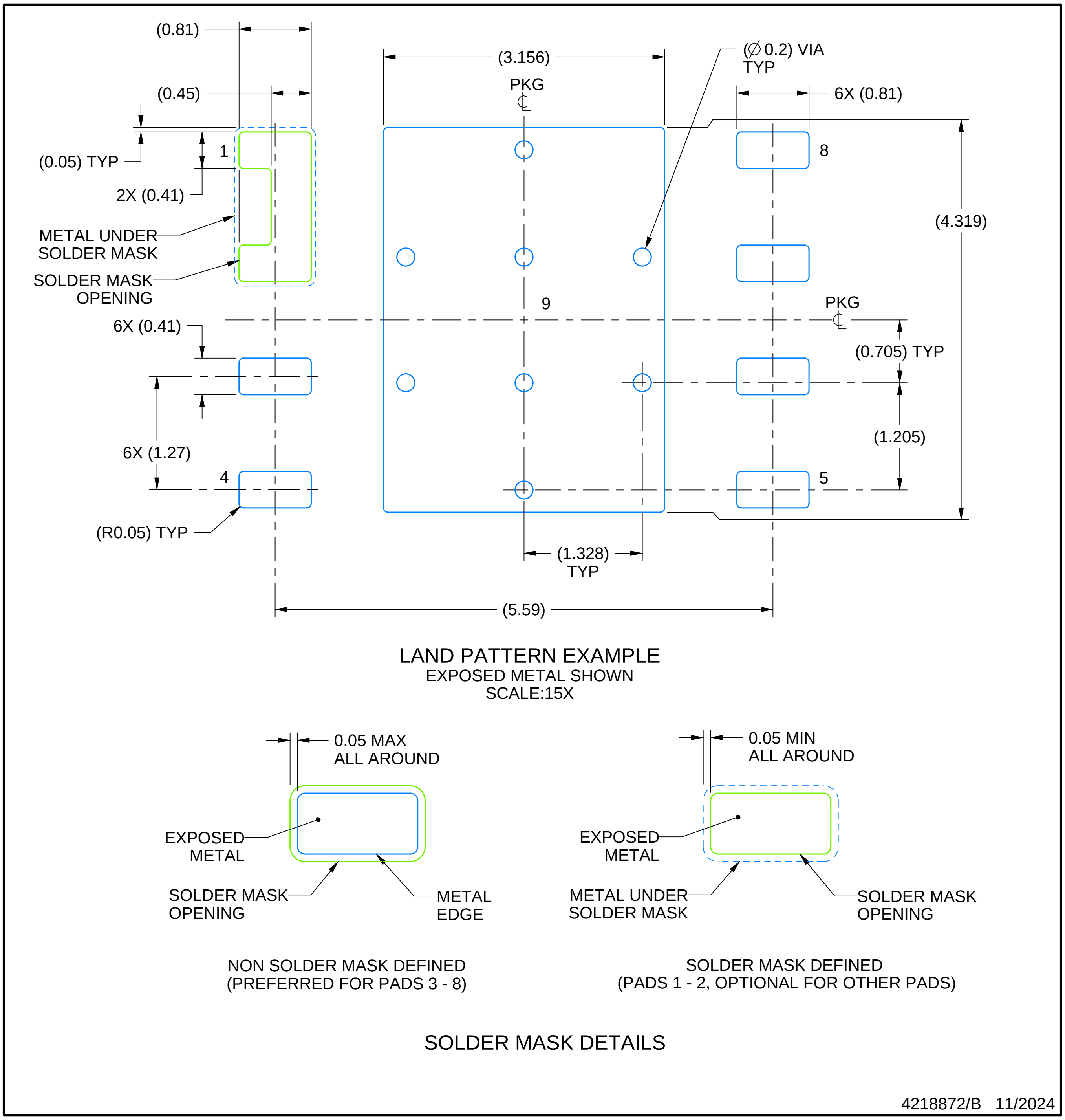
LSON-CLIP - 1.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed metals on side wall may vary or not visible



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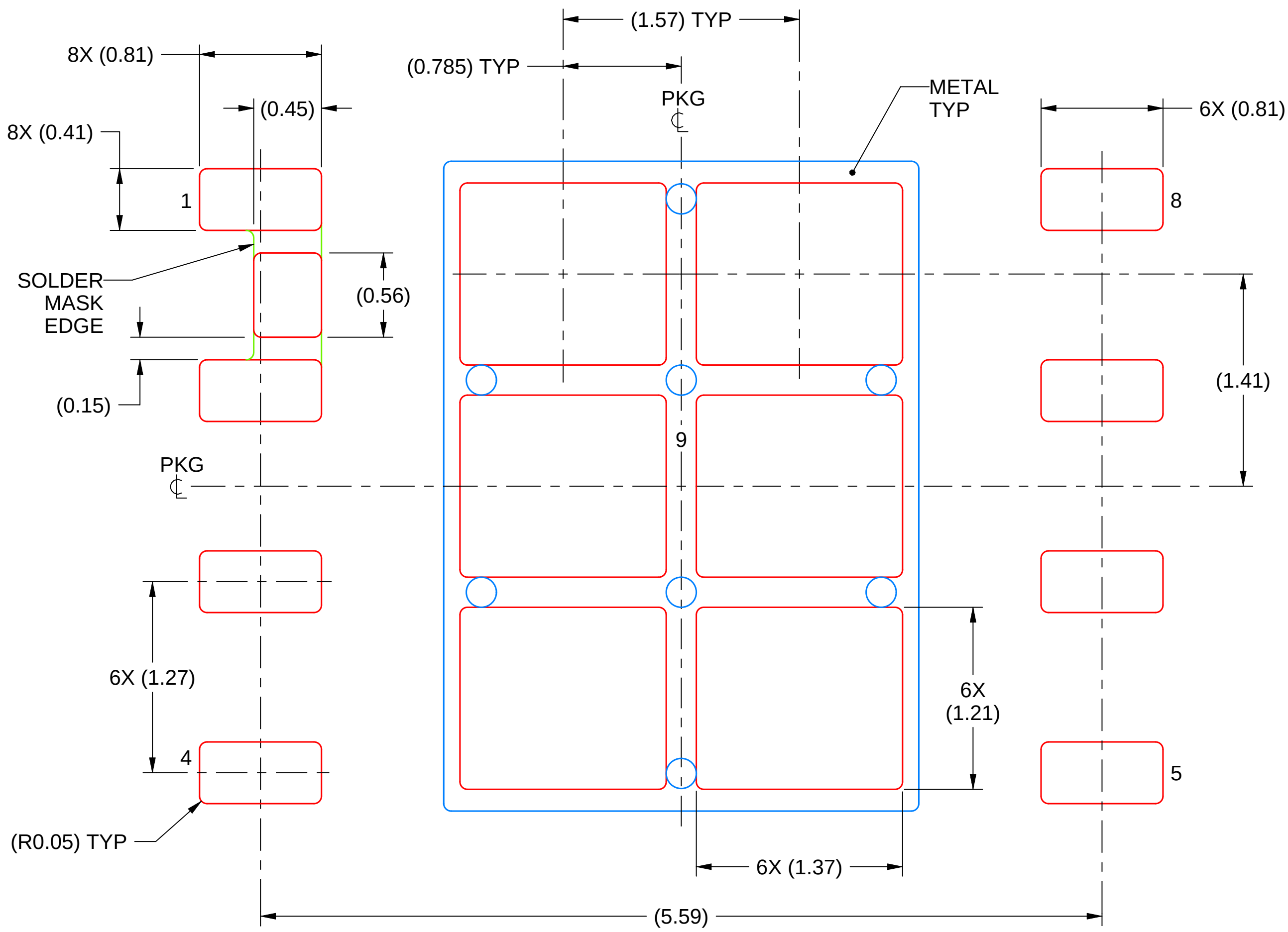
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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