CSD967201-Q1 Automotive Synchronous Buck Smart Power Stage

1 Features

- 3V to 20V input voltage range
- 60A nominal, 90A peak current capability
- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 87.7% power stage peak efficiency at 650kHz, 12V V_{IN}, 0.6V V_{OUT}
- 89.4% power stage peak efficiency at 650kHz, 12V V_{IN}, 0.8V V_{OUT}
- Reduced switch-node ringing
- High-frequency operation (up to 2MHz)
- Temperature compensated bi-directional current sense reporting (5µA/A)
- Body braking mode (BB)
- Fault detection
  - High-side short (HSS)
- Fault protection
  - Overtemperature (OT)
  - Cycle-by-cycle valley overcurrent limiting (IOC_{VALLEY})
  - Secondary peak over current protection (IOC_{PEAK})
  - Cycle-by-cycle negative overcurrent detection
- 5mm × 6mm × 0.75mm QFN industry common footprint package
- Green, RoHS compliant without exemption

2 Applications

- Automotive ADAS
- Automotive infotainment and cluster
- Software-defined vehicle: high-performance compute

3 Description

The CSD967201-Q1 power stage is a highly optimized design for use in an automotive qualified high-power, high-density synchronous buck converter. This device integrates the driver IC and power MOSFETs into one Pb-free monolithic design to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small industry standard 5mm × 6mm × 0.75mm footprint.

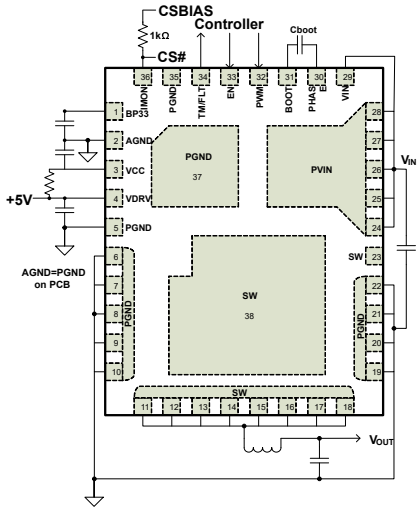
CSD967201-Q1 integrates accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. Protections include cycle-by-cycle overcurrent and negative overcurrent limiting, overtemperature shutdown, HS FET short, and UVLO on VCC, VIN, and BOOT.

The CSD967201-Q1 is compatible with the TPS64300-Q1 VRS-11 controller, as well as other standard VRS-11 controllers.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
CSD967201-Q1	VDK (WQFN-FCRLF, 38)	6mm × 5mm

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

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4 Pin Configuration and Functions

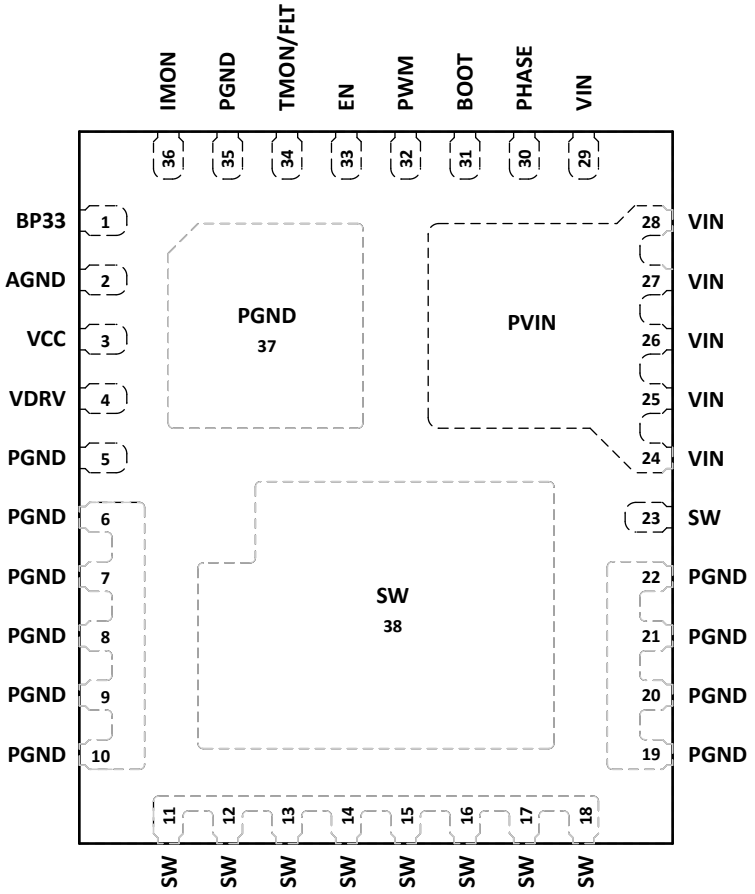

Figure 4-1. VDK Package 38-Pin WQFN-FCRLF (5mm × 6mm × 0.75mm) - Top View

Table 4-1. CSD967201-Q1 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	2	GND	Analog ground
BOOT	31	I/O	Bootstrap capacitor connection. Connect a minimum 0.1µF, 16V, X5R ceramic capacitor from BOOT to PHASE pin. The bootstrap capacitor provides the charge to switch HS FET. The bootstrap diode is integrated.
EN	33	I	This pin is used to enable the device. When EN is logic high, the gate driver responds to PWM inputs. When EN is logic low, both MOSFET gates are actively driven off.
IMON	36	O	Output of current sensing amplifier. The output of this pin is proportional to the inductor current with a gain of 5µA/A.
BP33	1	I/O	Connect a bypass capacitor from this pin to AGND. The recommendation is to use one 100nF, 16V, X7R capacitor on BP33.
PGND	5	GND	Power ground for the internal power stage.
	6 – 10		
	19-22		
	35, 37		
PHASE	30	O	Phase pin. Bootstrap capacitor connection return path for the HS FET floating driver. This pin is connected to VSW internally. Connect a minimum 0.1µF, 16V, X5R ceramic capacitor from BOOT to PHASE pin. The bootstrap capacitor provides the charge to switch HS FET. The bootstrap diode is integrated.

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Table 4-1. CSD967201-Q1 Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
PWM	32	I	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Either Body Brake or DCM is enabled if PWM stays in Hi-Z for greater than the tri-state shutdown holdoff time (t_{3HT}).
SW	11 – 18, 23, 38	O	Switch node connecting the HS MOSFET source and LS MOSFET drain - pin connection to the output inductor.
TMON/FLT	34	O	Temperature amplifier output. Reports a voltage proportional to the IC temperature. An ORing function is integrated in the IC. When used in multiphase applications, a single wire can be used to connect the TMON/FLT pins of all the ICs. Only the highest temperature is reported. TMON/FLT is pulled up to 3V if thermal shutdown detection circuit is tripped.
VCC	3	PWR	Supply voltage for internal analog circuitry. This pin is bypassed to AGND. The recommendation is to use one 2.2µF, 10V, X5R capacitor on VCC.
VDRV	4	PWR	Supply voltage for gate drivers. This pin is bypassed to PGND. The recommendation is to use one 1µF, 16V, X7R capacitor on VDRV.
VIN	24 – 29	I	Power input voltage pin. Connect input capacitors close to this pin. The recommendation is to use at least five 10µF, 25V, X7R capacitors on VIN, plus two 0.1uF, 50V, X7R caps close to the VIN pins.

(1) I = input, O = output, GND = ground

ADVANCE INFORMATION

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.2 Documentation Support

5.3 Receiving Notification of Documentation Updates

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5.4 Support Resources

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5.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

DATE	REVISION	NOTES
November 2025	*	Initial release

ADVANCE INFORMATION

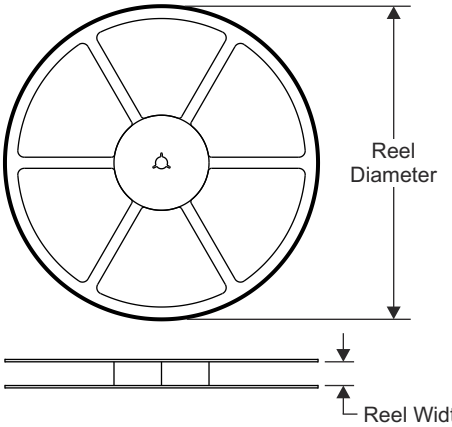
ADVANCE INFORMATION

7 Mechanical, Packaging, and Orderable Information

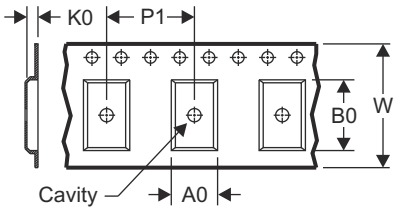
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information

REEL DIMENSIONS

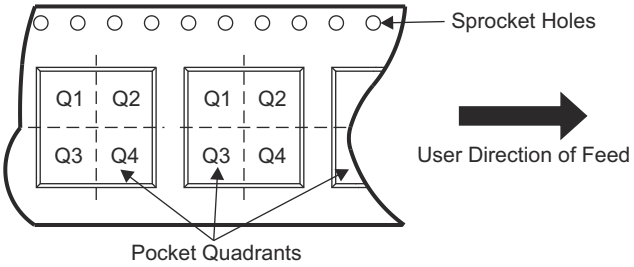


TAPE DIMENSIONS



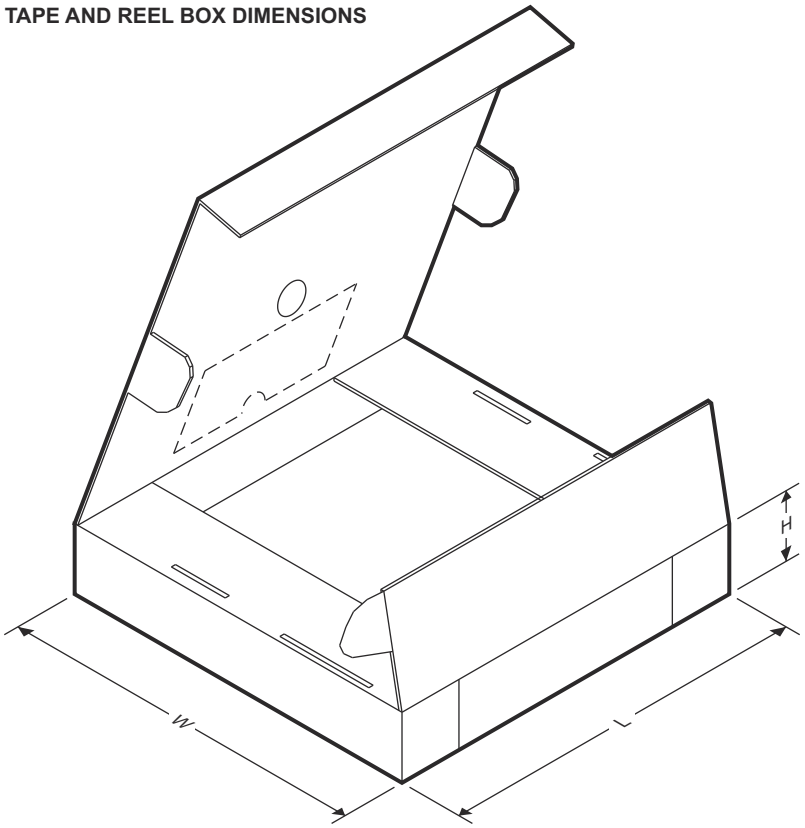
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD967201QVDKRQ1	WQFN-FCRLF	VDA	38	3000	330	12.4	5.30	6.30	1.20	8.00	12.00	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD967201QVDKRQ1	WQFN-FCRLF	VDA	38	3000	367	367	38

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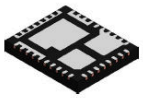
ADVANCE INFORMATION

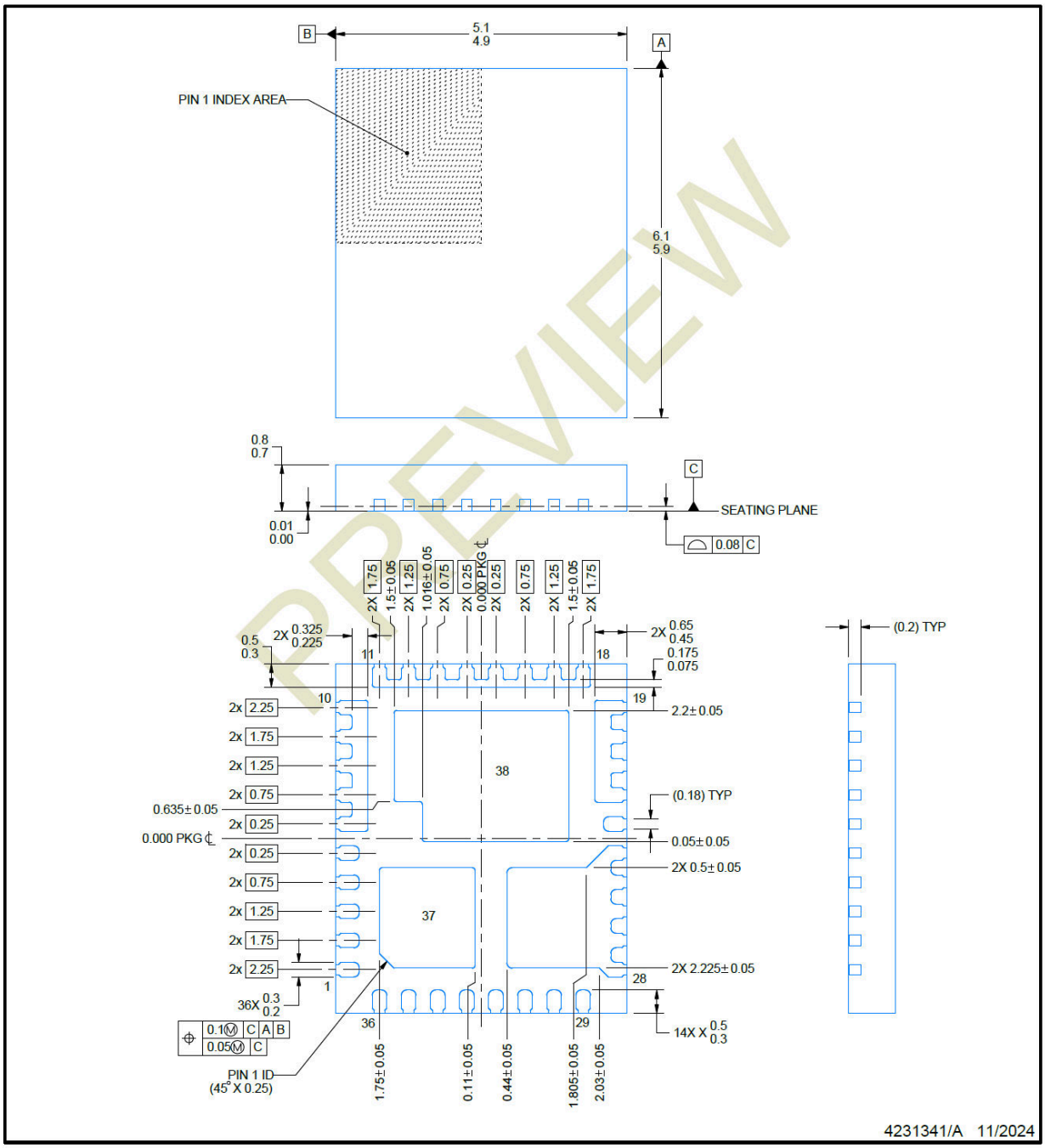
PACKAGE OUTLINE

VDK0038A



WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

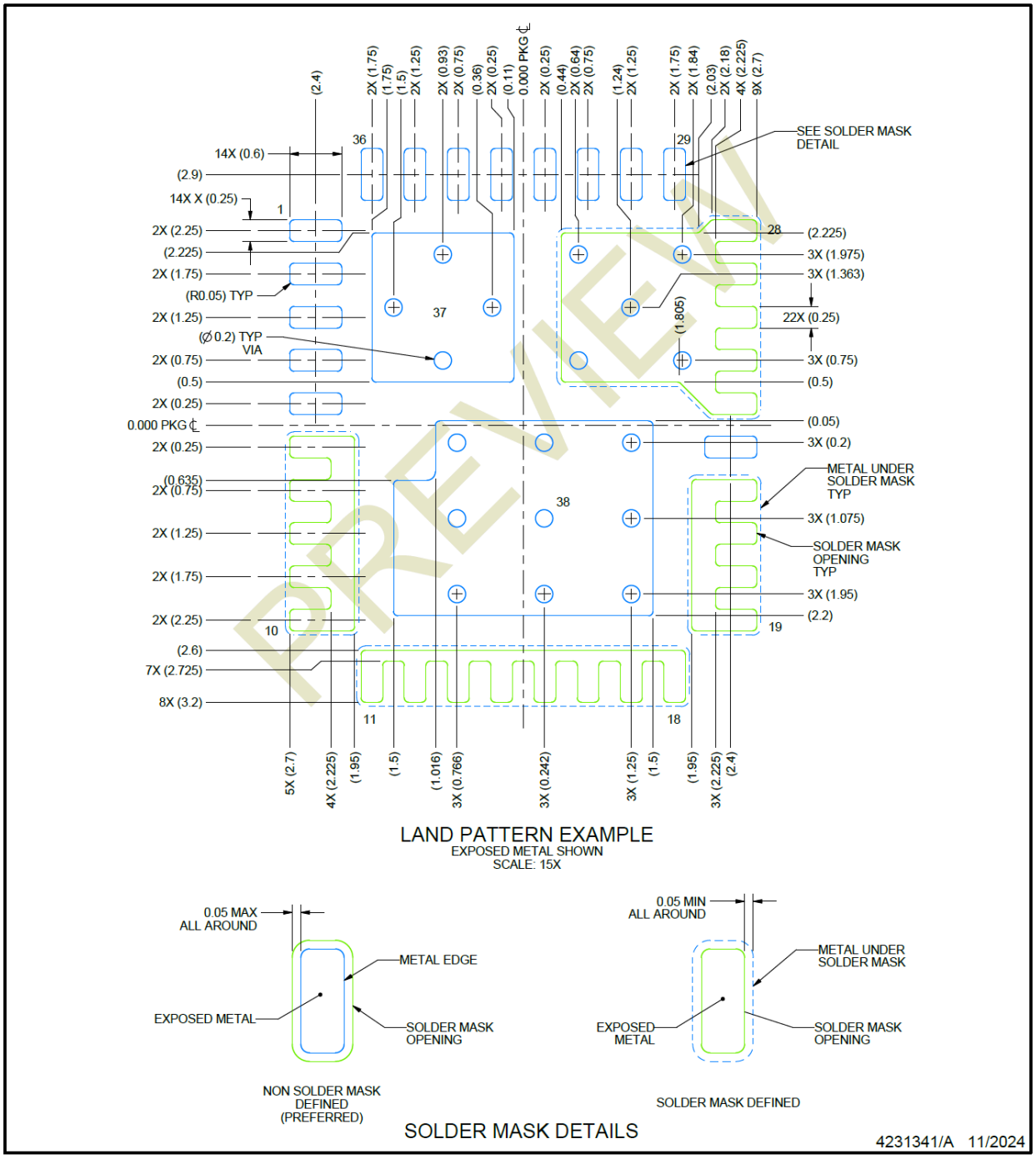
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VDK0038A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

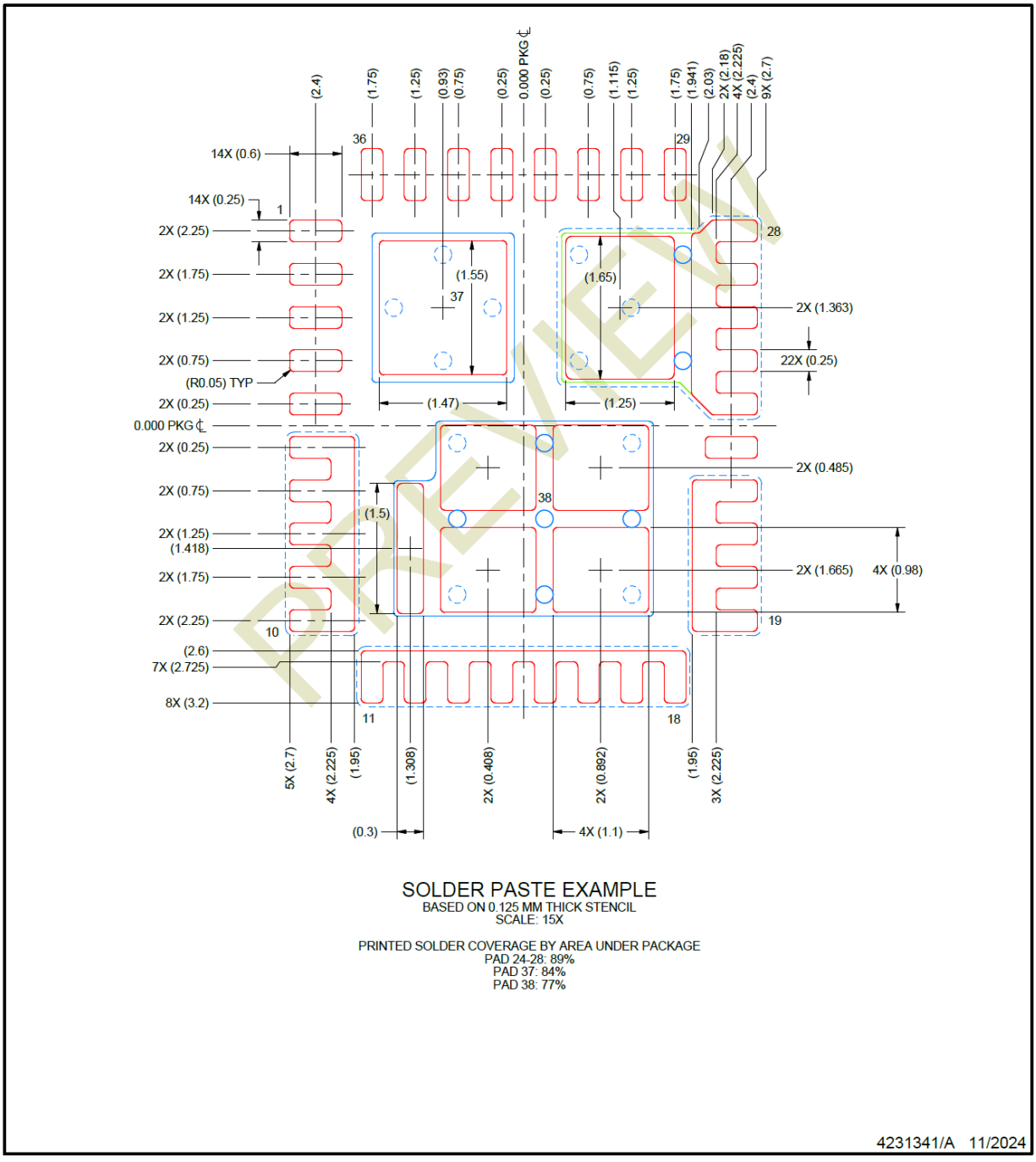
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

VDK0038A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSD967201QVDKRQ1	Active	Preproduction	WQFN-FCRLF (VDK) | 38	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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