TEXAS INSTRUMENTS

CSD97396Q4M

SLPS572 – DECEMBER 2015

CSD97396Q4M Synchronous Buck NexFET™ Power Stage

1 Features

- Over 93% System Efficiency at 15 A
- Max Rated Continuous Current 30 A, Peak 65 A
- High Frequency Operation (up to 2 MHz)
- High Density – SON 3.5 mm × 4.5 mm Footprint
- Ultra-Low Inductance Package
- System-Optimized PCB Footprint
- Ultra-Low Quiescent (ULQ) Current Mode
- 3.3 V and 5 V PWM Signal Compatible
- Diode Emulation Mode With FCCM
- Input Voltages up to 24 V
- Tri-State PWM Input
- Integrated Bootstrap Diode
- Shoot-Through Protection
- RoHS Compliant – Lead Free Terminal Plating
- Halogen Free

2 Applications

- Ultrabook/Notebook DC/DC Converters
- Multiphase Vcore and DDR Solutions
- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems

3 Description

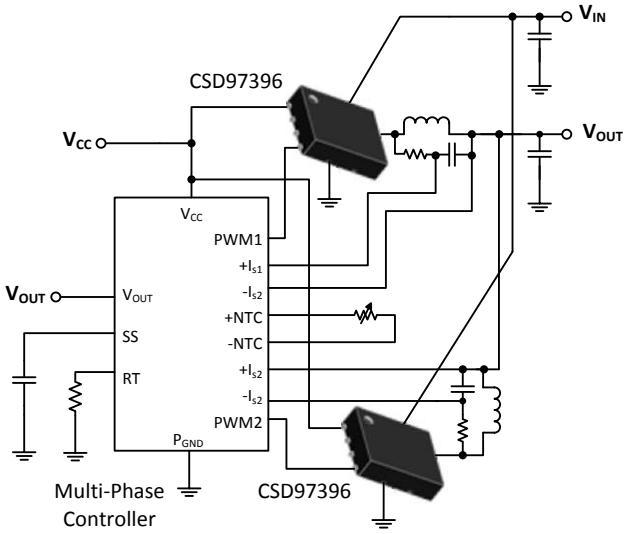
The CSD97396Q4M NexFET™ Power Stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and NexFET technology to complete the power stage switching function. The driver IC has a built-in selectable diode emulation function that enables DCM operation to improve light load efficiency. In addition, the driver IC supports ULQ mode that enables connected standby for Windows® 8. With the PWM input in tri-state, quiescent current is reduced to 130 µA, with immediate response. When SKIP# is held at tri-state, the current is reduced to 8 µA (typically 20 µs is required to resume switching). This combination produces a high current, high efficiency, and high speed switching device in a small 3.5 × 4.5 mm outline package. In addition, the PCB footprint is optimized to help reduce design time and simplify the completion of the overall system design.

Device Information(1)

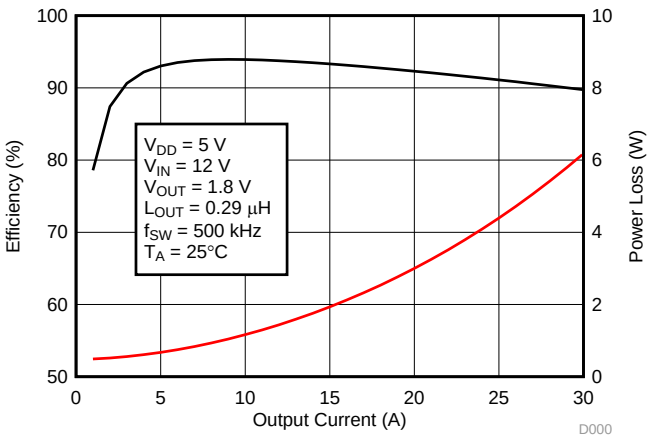
ORDER NUMBER	PACKAGE	MEDIA AND QTY	
CSD97396Q4M	SON 3.5 × 4.5 mm Plastic Package	13-inch reel	2500
CSD97396Q4MT		7-inch reel	250

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



Typical Power Stage Efficiency and Power Loss



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
7 Detailed Description ... 6
7.1 Overview ... 6
7.2 Functional Block Diagram ... 6
7.3 Feature Description ... 6
7.4 Device Functional Modes ... 8
8 Application and Implementation ... 9
8.1 Application Information ... 9
8.2 Typical Application ... 9
8.3 System Example ... 12
9 Layout ... 14
9.1 Layout Guidelines ... 14
9.2 Layout Example ... 14
9.3 Thermal Considerations ... 14
10 Device and Documentation Support ... 15
10.1 Community Resources ... 15
10.2 Trademarks ... 15
10.3 Electrostatic Discharge Caution ... 15
10.4 Glossary ... 15
11 Mechanical, Packaging, and Orderable Information ... 16
11.1 Mechanical Drawing ... 16
11.2 Recommended PCB Land Pattern ... 17
11.3 Recommended Stencil Opening ... 17

4 Revision History

DATE	REVISION	NOTES
December 2015	*	Initial release.

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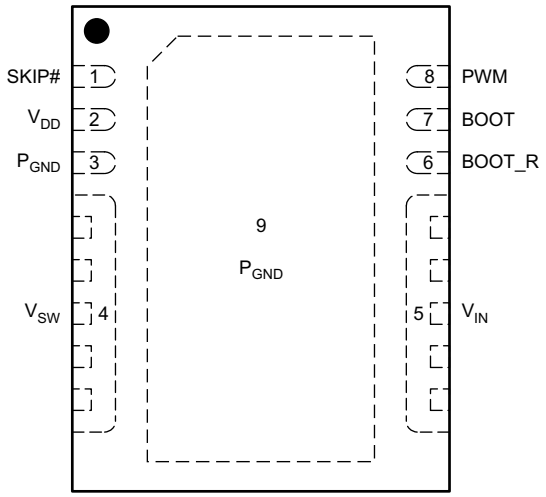
5 Pin Configuration and Functions

SON 3.5 × 4.5 mm
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	SKIP#	This pin enables the Diode Emulation function. When this pin is held low, diode emulation mode is enabled for the Sync FET. When SKIP# is high, the CSD97396Q4M operates in forced continuous conduction mode. A tri-state voltage on SKIP# puts the driver into a very low power state.
2	V_{DD}	Supply voltage to gate drivers and internal circuitry.
3	P_{GND}	Power ground, needs to be connected to Pin 9 and PCB
4	V_{SW}	Voltage switching node – pin connection to the output inductor.
5	V_{IN}	Input voltage pin. Connect input capacitors close to this pin.
6	BOOT_R	Bootstrap capacitor connection. Connect a minimum 0.1 µF 16 V X5R, ceramic cap from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the Control FET. The bootstrap diode is integrated. Boot_R is internally connected to V_{SW}.
7	BOOT	
8	PWM	Pulse width modulated 3-state input from external controller. Logic low sets Control FET gate low and Sync FET gate high. Logic high sets Control FET gate high and Sync FET gate Low. Open or High Z sets both MOSFET gates low if greater than the Tri-State Shutdown Hold-off Time (t_{3HT})
9	P_{GND}	Power Ground

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6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
	V_{IN} to P_{GND}	–0.3	30	V
	V_{SW} to P_{GND} , V_{IN} to V_{SW}	–0.3	30	V
	V_{SW} to P_{GND}, V_{IN} to V_{SW} (<10 ns)	–7	33	V
	V_{DD} to P_{GND}	–0.3	6	V
	PWM, SKIP# to P_{GND}	–0.3	6	V
	BOOT to P_{GND}	–0.3	35	V
	BOOT to P_{GND} (<10 ns)	–2	38	V
	BOOT to BOOT_R	–0.3	6	V
	BOOT to BOOT_R (duty cycle <0.2%)		8	V
P_D	Power dissipation		8	W
T_J	Operating temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)(1)	±1000	V
		Charged device model (CDM)(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage (1)			24	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH(2)		30	A
I_{OUT-PK}	Peak output current(3)			65	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		2000	kHz
	On-time duty cycle			85%	
	Minimum PWM on-time		40		ns
	Operating temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 2. Peak Output Current is applied for t_p = 10 ms, duty cycle ≤1%

6.4 Thermal Information

T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(1)			22.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(2)			2.5	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz (0.071 mm thick) Cu pad on a 1.5 inch x 1.5 inch, 0.06 inch (1.52 mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

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6.5 Electrical Characteristics

T_A = 25°C, V_{DD} = POR to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}						
Power Loss(1)		V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 15 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH, T_J = 25°C		1.9		W
Power Loss(2)		V_{IN} = 19 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 15 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH, T_J = 25°C		2.2		W
Power Loss(2)		V_{IN} = 19 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 15 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH, T_J = 125°C		2.6		W
V_{IN}						
I_Q	V_{IN} quiescent current	PWM = Floating, V_{DD} = 5 V, V_{IN}= 24 V			1	µA
V_{DD}						
I_{DD}	Standby supply current	PWM = Float, SKIP# = V_{DD} or 0 V		130		µA
		SKIP# = Float		8		µA
I_{DD}	Operating supply current	PWM = 50% Duty cycle, f_{SW} = 500 kHz		7.8		mA
POWER-ON RESET AND UNDERVOLTAGE LOCKOUT						
V_{DD} Rising	Power-on reset				4.15	V
V_{DD} Falling	UVLO		3.7			V
	Hysteresis			0.2		mV
PWM AND SKIP# I/O SPECIFICATIONS						
R_I	Input impedance	Pull up to V_{DD}		1700		kΩ
		Pull down (to GND)		800		
V_{IH}	Logic level high		2.65			V
V_{IL}	Logic level low				0.6	
V_{IH}	Hysteresis			0.2		
V_{TS}	Tri-state voltage		1.3		2	
$t_{THOLD(off1)}$	Tri-state activation time (falling) PWM(2)			60		ns
$t_{THOLD(off2)}$	Tri-state activation time (rising) PWM(2)			60		
t_{TSKF}	Tri-state activation time (falling) SKIP#(2)			1		µs
t_{TSKR}	Tri-state activation time (rising) SKIP# (2)			1		
$t_{3RD(PWM)}$	Tri-state exit time PWM(2)				100	ns
$t_{3RD(SKIP\#)}$	Tri-state exit time SKIP#(2)				50	µs
BOOTSTRAP SWITCH						
V_{FBST}	Forward voltage	I_F = 10 mA		120	240	mV
I_{RLEAK}	Reverse leakage(2)	V_{BST} – V_{DD} = 25 V			2	µA

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) Specified by design.

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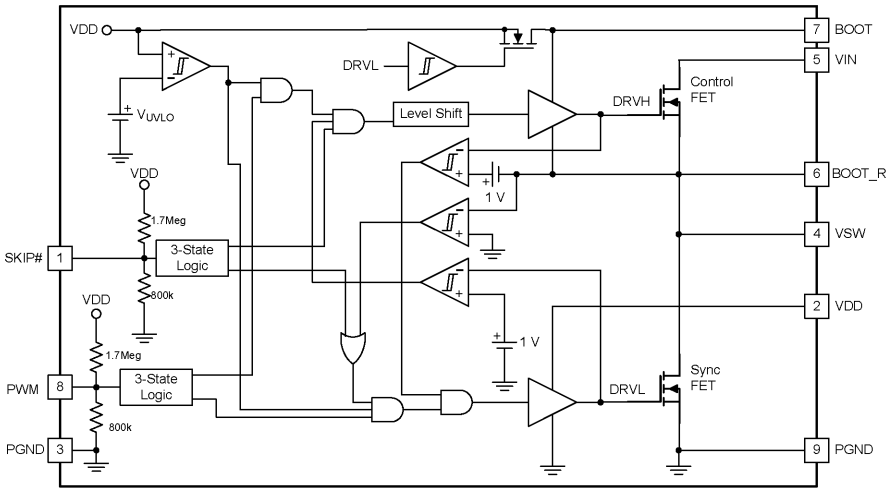
7 Detailed Description

7.1 Overview

The CSD97396Q4M NexFET™ Power Stage is a highly optimized design for use in a high-power, high-density synchronous buck converter.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Powering CSD97396Q4M and Gate Drivers

An external V_{DD} voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETs. A 1 µF 10 V X5R or higher ceramic capacitor is recommended to bypass V_{DD} pin to P_{GND}. A bootstrap circuit to provide gate drive power for the Control FET is also included. The bootstrap supply to drive the Control FET is generated by connecting a 100 nF 16 V X5R ceramic capacitor between BOOT and BOOT_R pins. An optional R_{BOOT} resistor can be used to slow down the turn on speed of the Control FET and reduce voltage spikes on the V_{SW} node. A typical 1 Ω to 4.7 Ω value is a compromise between switching loss and V_{SW} spike amplitude.

7.3.2 Undervoltage Lockout (UVLO) Protection

The UVLO comparator evaluates the VDD voltage level. As V_{VDD} rises, both the Control FET and Sync FET gates hold actively low at all times until V_{VDD} reaches the higher UVLO threshold (V_{UVLO_H})., Then the driver becomes operational and responds to PWM and SKIP# commands. If VDD falls below the lower UVLO threshold (V_{UVLO_L} = V_{UVLO_H} – Hysteresis), the device disables the driver and drives the outputs of the Control FET and Sync FET gates actively low. Figure 1 shows this function.

CAUTION

Do not start the driver in the very low power mode (SKIP# = Tri-state).

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Feature Description (continued)

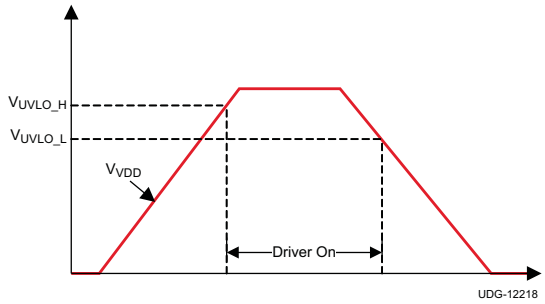

Figure 1. UVLO Operation

7.3.3 PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pull-up to maintain the voltage within the tri-state window during low-power modes. Operation into and out of tri-state mode follows the timing diagram outlined in Figure 2.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined the PWM voltage range between PWM logic high (V_{IH}) and logic low (V_{IL}) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3 V (typical) and 5 V (typical) PWM drive signals.

When the PWM exits tri-state, the driver enters CCM for a period of 4 µs, regardless of the state of the SKIP# pin. Normal operation requires this time period in order for the auto-zero comparator to resume.

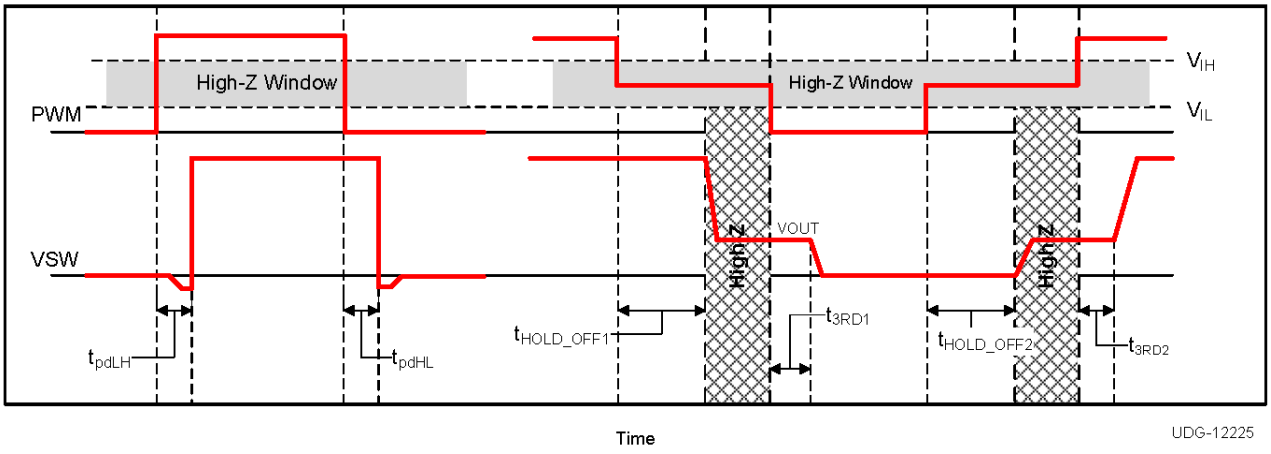

Figure 2. PWM Tri-State Timing Diagram

7.3.4 SKIP# Pin

The SKIP# pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When SKIP# is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When SKIP# is high, the ZX comparator disables, and the converter enters FCCM mode. When both SKIP# and PWM are tri-stated, normal operation forces the gate driver outputs low and the driver enters a low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When SKIP# is pulled low, the driver wakes up and is able to accept PWM pulses in less than 50 µs.

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Feature Description (continued)

Table 1 shows the logic functions of UVLO, PWM, SKIP#, the Control FET Gate and the Sync FET Gate.

Table 1. Logic Functions of the Driver IC

UVLO	PWM	SKIP#	SYNC FET GATE	CONTROL FET GATE	MODE
Active	—	—	Low	Low	Disabled
Inactive	Low	Low	High(1)	Low	DCM(1)
Inactive	Low	High	High	Low	FCCM
Inactive	High	H or L	Low	High	
Inactive	Tri-state	H or L	Low	Low	LQ(2)
Inactive	—	Tri-state	Low	Low	ULQ(3)

(1) Until zero crossing protection occurs.
(2) Low quiescent current (LQ)
(3) Ultra-low quiescent current (ULQ)

7.3.4.1 Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

7.3.5 Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and the BST pin is replaced by a FET which is gated by the DRVL signal.

7.4 Device Functional Modes

Table 1 shows the different functional modes of CSD97396. The diode emulation mode is enabled with SKIP# pulled low, which improves light load efficiency. With PWM in tri-state, Power Stage enters LQ mode and the quiescent current is reduced to 130 µA. When SKIP# is held in tri-state, ULQ mode is enabled and the current is decreased to 8 µA.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The Power Stage CSD97396Q4M is a highly optimized design for synchronous buck applications using NexFET devices with a 5 V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, SOA, and normalized graphs allow engineers to predict the product performance in the actual application.

8.2 Typical Application

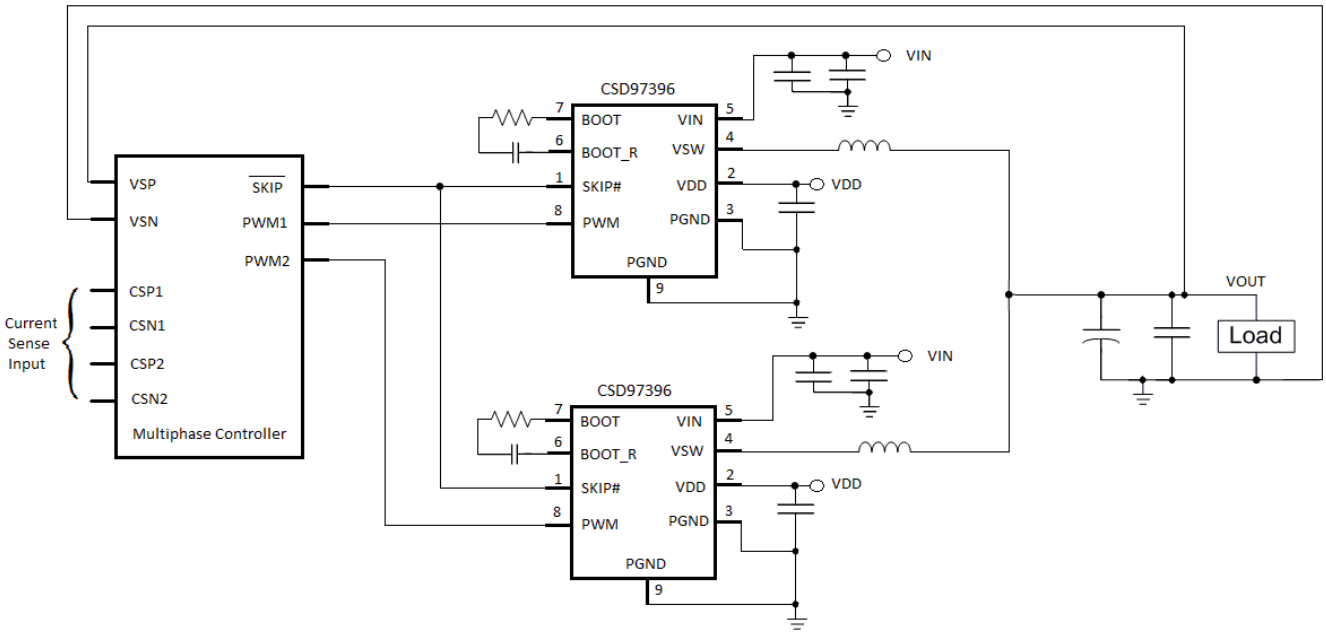
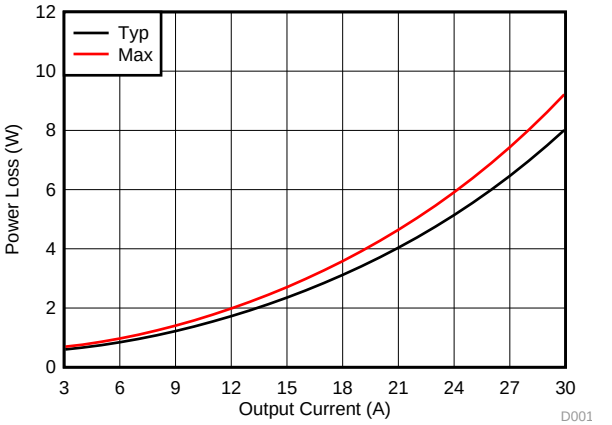


Figure 3. Application Schematic

Typical Application (continued)

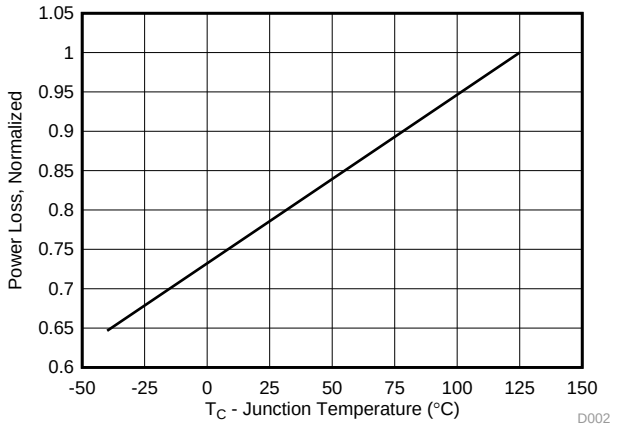
8.2.1 Application Curves

T_J = 125°C, unless stated otherwise. The Typical CSD97396Q4M System Characteristic curves (see Figure 6 and Figure 7) are based on measurements made on a PCB design with dimensions of 4.0" (W) × 3.5" (L) × 0.062" (T) and 6 copper layers of 1 oz. copper thickness. See *System Example* for detailed explanation.



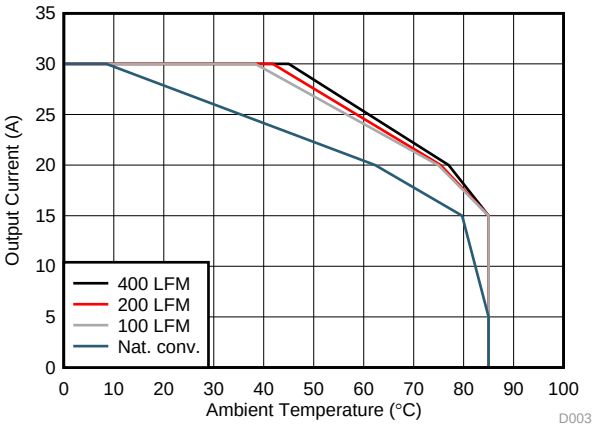
V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 4. Power Loss vs Output Current



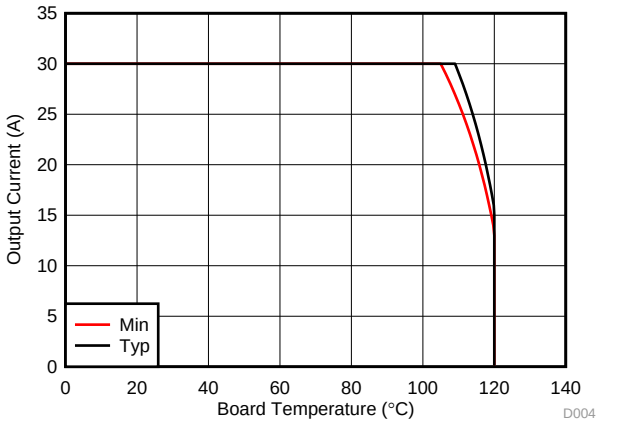
V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 5. Power Loss vs Temperature



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 6. Safe Operating Area – PCB Horizontal Mount



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 7. Typical Safe Operating Area

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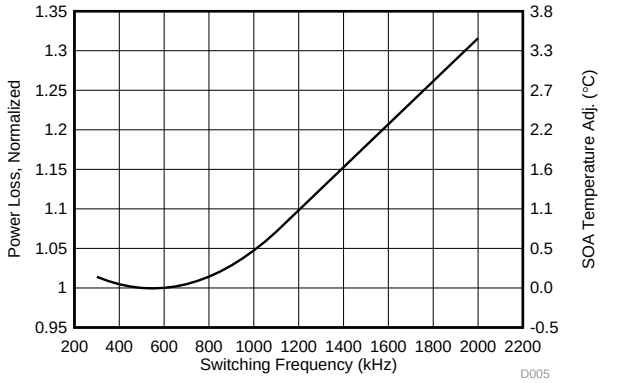
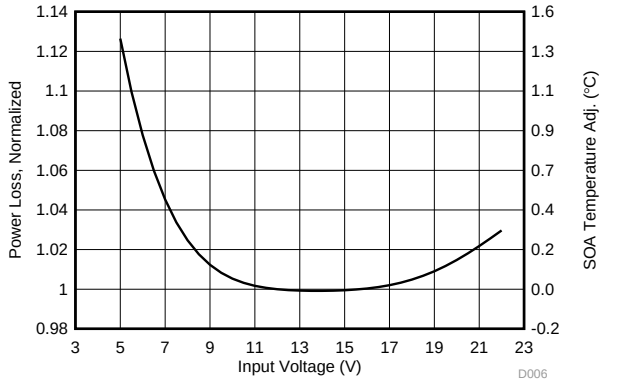
Typical Application (continued)

T_J = 125°C, unless stated otherwise. The Typical CSD97396Q4M System Characteristic curves (see Figure 6 and Figure 7) are based on measurements made on a PCB design with dimensions of 4.0" (W) × 3.5" (L) × 0.062" (T) and 6 copper layers of 1 oz. copper thickness. See *System Example* for detailed explanation.



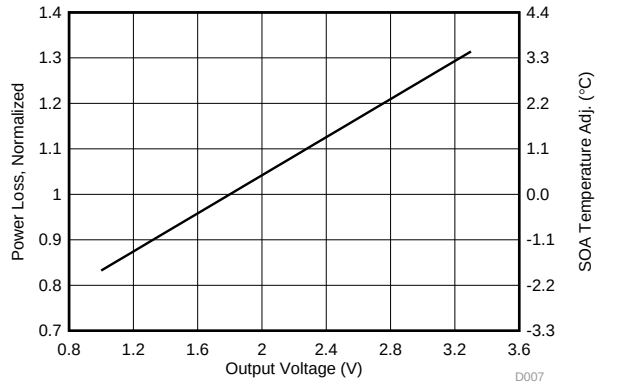
V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
I_{OUT} = 25 A L_{OUT} = 0.29 µH

Figure 8. Normalized Power Loss vs Frequency



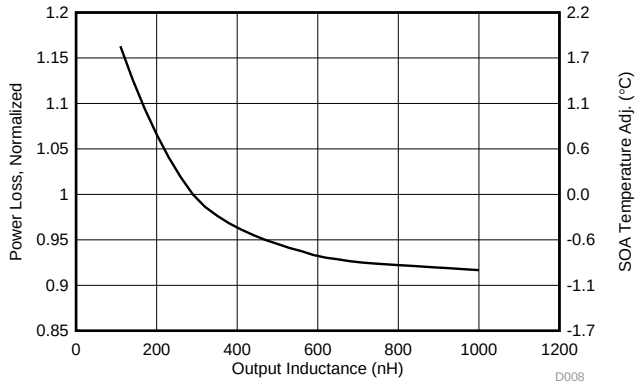
I_{OUT} = 25 A V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 9. Normalized Power Loss vs Input Voltage



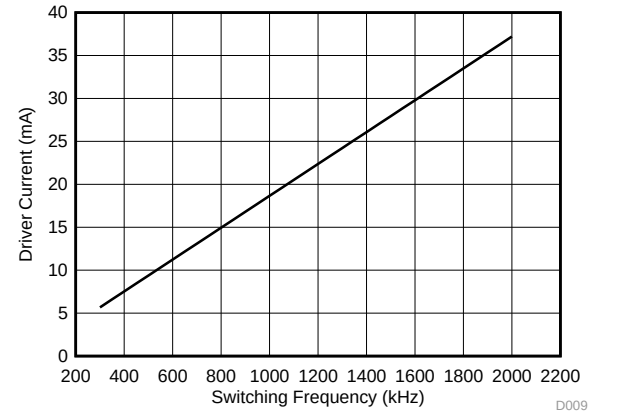
V_{IN} = 12 V V_{DD} = 5 V I_{OUT} = 25 A
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 10. Normalized Power Loss vs Output Voltage



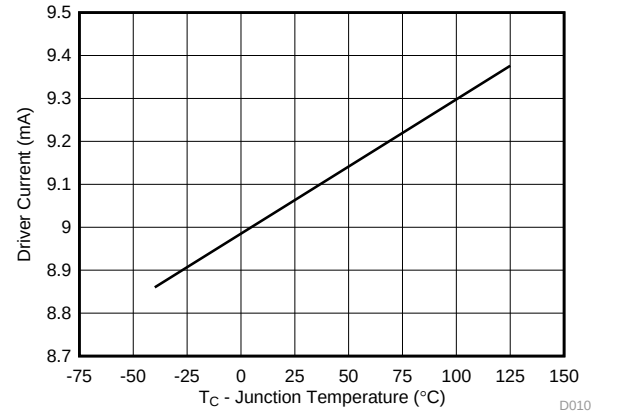
V_{IN} = 12 V V_{DD} = 5 V I_{OUT} = 25 A
f_{SW} = 500 kHz V_{OUT} = 1.8 V

Figure 11. Normalized Power Loss vs Output Inductance



V_{IN} = 12 V V_{DD} = 5 V I_{OUT} = 25 A
L_{OUT} = 0.29 µH V_{OUT} = 1.8 V

Figure 12. Driver Current vs Frequency



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
I_{OUT} = 25 A L_{OUT} = 0.29 µH

Figure 13. Driver Current vs Temperature

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8.3 System Example

8.3.1 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 4 plots the power loss of the CSD97396Q4M as a function of load current. This curve is measured by configuring and running the CSD97396Q4M as it would be in the final application (see Figure 14). The measured power loss is the CSD97396Q4M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\textbf{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 4 is measured at the maximum recommended junction temperature of T_J = 125°C under isothermal test conditions.

8.3.2 SOA Curves

The SOA curves in the CSD97396Q4M datasheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 6 and Figure 7 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness.

8.3.3 Normalized Curves

The normalized curves in the CSD97396Q4M data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

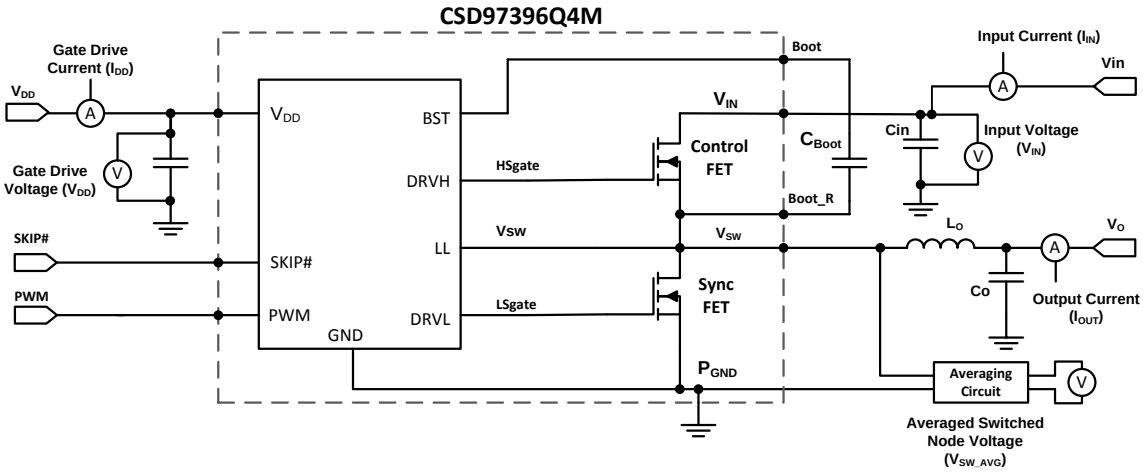

Figure 14. Power Loss Test Circuit

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System Example (continued)

8.3.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see the Design Example). Though the Power Loss and SOA curves in this datasheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

8.3.4.1 Design Example

Operating Conditions: Output Current (I_{OUT}) = 20 A, Input Voltage (V_{IN}) = 7 V, Output Voltage (V_{OUT}) = 2.0 V, Switching Frequency (f_{SW}) = 800 kHz, Output Inductor (L_{OUT}) = 0.2 µH

8.3.4.2 Calculating Power Loss

- Typical Power Loss at 20 A = 3.71 W (Figure 4)
- Normalized Power Loss for switching frequency ≈ 1.01 (Figure 8)
- Normalized Power Loss for input voltage ≈ 1.04 (Figure 9)
- Normalized Power Loss for output voltage ≈ 1.04 (Figure 10)
- Normalized Power Loss for output inductor ≈ 1.07 (Figure 11)
- **Final calculated Power Loss = 3.71 W × 1.01 × 1.04 × 1.04 × 1.07 ≈ 4.34 W**

8.3.4.3 Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ 0.16°C (Figure 8)
- SOA adjustment for input voltage ≈ 0.42°C (Figure 9)
- SOA adjustment for output voltage ≈ 0.46°C (Figure 10)
- SOA adjustment for output inductor ≈ 0.74°C (Figure 11)
- **Final calculated SOA adjustment = 0.16 + 0.42 + 0.46 + 0.74 ≈ 1.78°C**

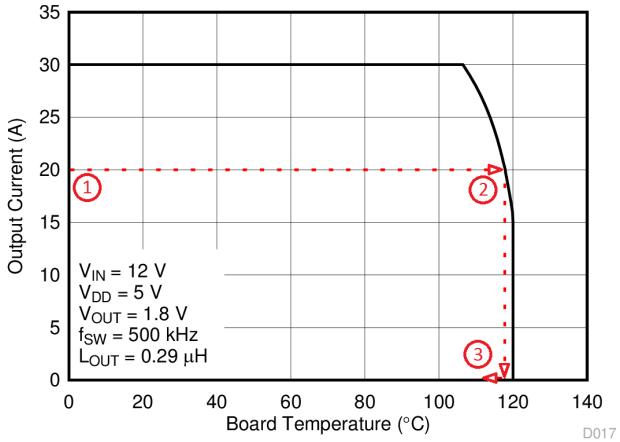

Figure 15. Power Stage CSD97396Q4M SOA

In the design example above, the estimated power loss of the CSD97396Q4M would increase to 4.23 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 1.78°C. Figure 15 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 1.78°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

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9 Layout

9.1 Layout Guidelines

9.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

9.1.2 Electrical Performance

The CSD97396Q4M has the ability to switch at voltage rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

- The placement of the input capacitors relative to V_{IN} and P_{GND} pins of CSD97396Q4M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 16). The example in Figure 16 uses 1 × 1 nF 0402 25 V and 3 × 10 µF 1206 25 V ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C5, C8 and C6, C19 should follow in order.
- The bootstrap cap C_{BOOT} 0.1 µF 0603 16 V ceramic capacitor should be closely connected between BOOT and BOOT_R pins
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD97396Q4M V_{SW} pins. Minimizing the V_{SW} node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. (1)

9.2 Layout Example

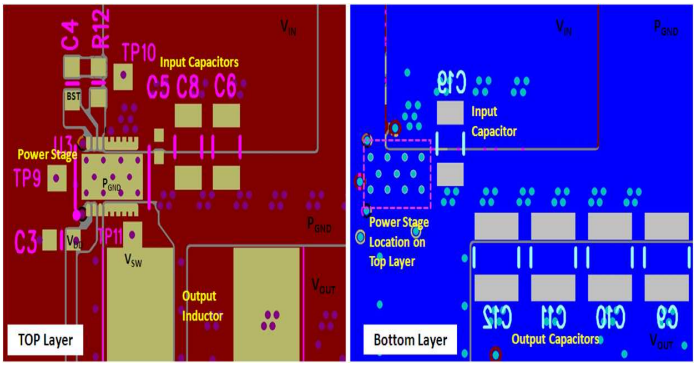

Figure 16. Recommended PCB Layout (Top Down View)

9.3 Thermal Considerations

The CSD97396Q4M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 16 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

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10 Device and Documentation Support

10.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.2 Trademarks

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10.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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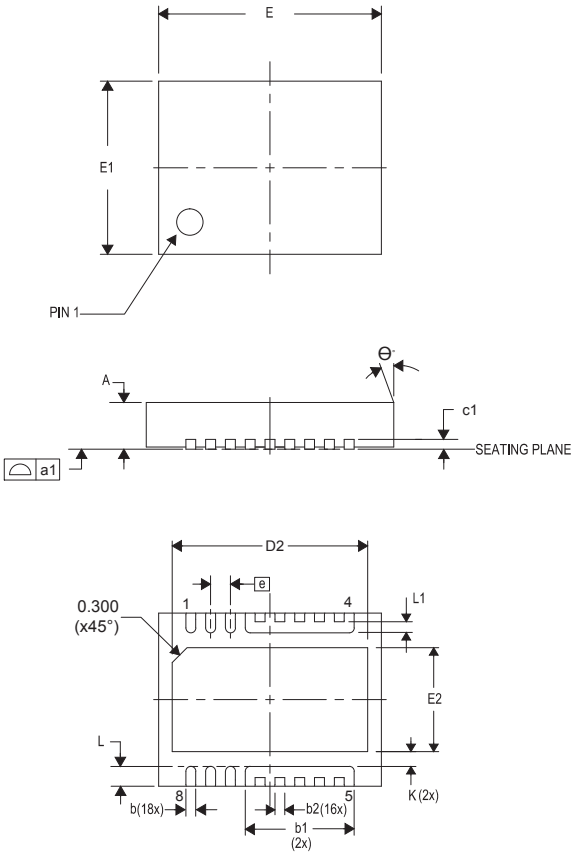
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Mechanical Drawing



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.800	0.900	1.000	0.031	0.035	0.039
a1	0.000	0.000	0.080	0.000	0.000	0.003
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	2.000	2.200	2.400	0.079	0.087	0.095
b2	0.150	0.200	0.250	0.006	0.008	0.010
c1	0.150	0.200	0.250	0.006	0.008	0.010
D2	3.850	3.950	4.050	0.152	0.156	0.160
E	4.400	4.500	4.600	0.173	0.177	0.181
E1	3.400	3.500	3.600	0.134	0.138	0.142
E2	2.000	2.100	2.200	0.079	0.083	0.087
e		0.400 TYP			0.016 TYP	
K		0.300 TYP			0.012 TYP	
L	0.300	0.400	0.500	0.012	0.016	0.020
L1	0.180	0.230	0.280	0.007	0.009	0.011
θ	0.00	—	—	0.00	—	—

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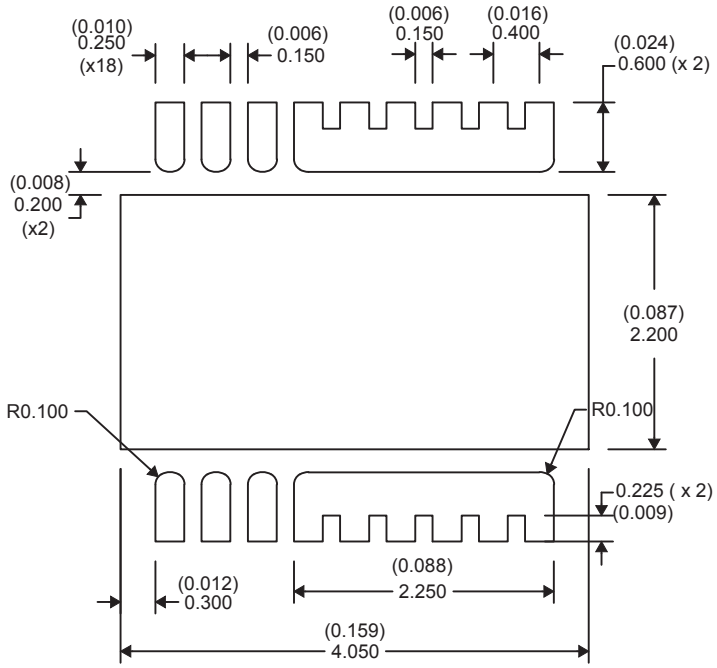
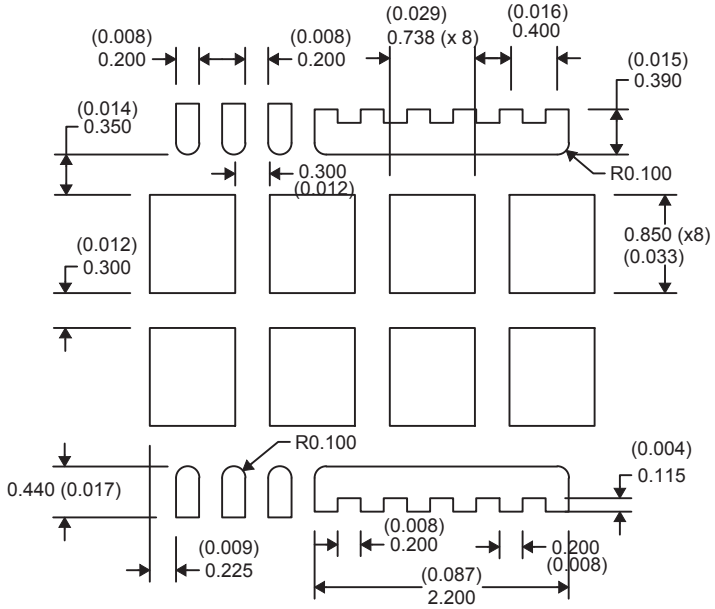
11.2 Recommended PCB Land Pattern



11.3 Recommended Stencil Opening



NOTE: Dimensions are in mm (inches).
Stencil is 100 µm thick.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD97396Q4M	Active	Production	VSON-CLIP (DPC) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	97396M
CSD97396Q4M.B	Active	Production	VSON-CLIP (DPC) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
CSD97396Q4MG4	Active	Production	VSON-CLIP (DPC) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	97396M
CSD97396Q4MG4.B	Active	Production	VSON-CLIP (DPC) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
CSD97396Q4MT	Active	Production	VSON-CLIP (DPC) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	97396M
CSD97396Q4MT.B	Active	Production	VSON-CLIP (DPC) | 8	250 | SMALL T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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