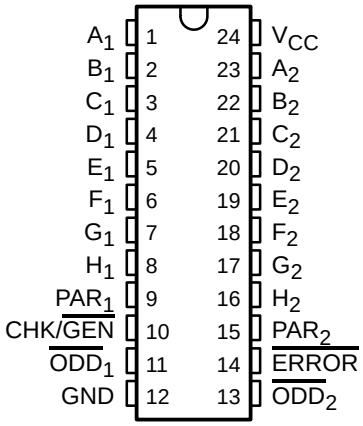
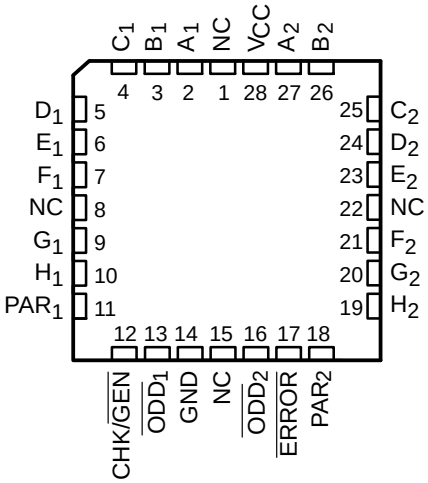
SCCS025B – MAY 1993 – REVISED OCTOBER 2001

- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **Two 8-Bit Parity Generators/Checkers**
- **Open-Drain Active-Low Parity-Error Output**
- **Expandable for Larger Word Widths**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **CY54FCT480T**
  - **32-mA Output Sink Current**
  - **12-mA Output Source Current**
- **CY74FCT480T**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**

CY74FCT480T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT480T . . . L PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’FCT480T devices are high-speed, dual, 8-bit parity generators/checkers. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a sum and parity-error ($\overline{\text{ERROR}}$) output. These devices can be used in odd-parity systems. $\overline{\text{ERROR}}$ is an open-drain output designed for easy expansion of the word width by a wired-OR connection of several ’FCT480T devices. Because no additional logic is needed, the parity-generation or parity-checking times remain the same as for an individual ’FCT480T device.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DIP – P	Tube	6.1	CY74FCT480BTPC	CY74FCT480BTPC
	QSOP – Q	Tape and reel	6.1	CY74FCT480BTQCT	FCT480B
	SOIC – SO	Tube	6.1	CY74FCT480BTSOC	FCT480B
		Tape and reel	6.1	CY74FCT480BTSOCT	
	DIP – P	Tube	7.5	CY74FCT480ATPC	CY74FCT480ATPC
	QSOP – Q	Tape and reel	7.5	CY74FCT480ATQCT	FCT480A
–55°C to 125°C	LCC – L	Tube	7	CY54FCT480BTLMB	

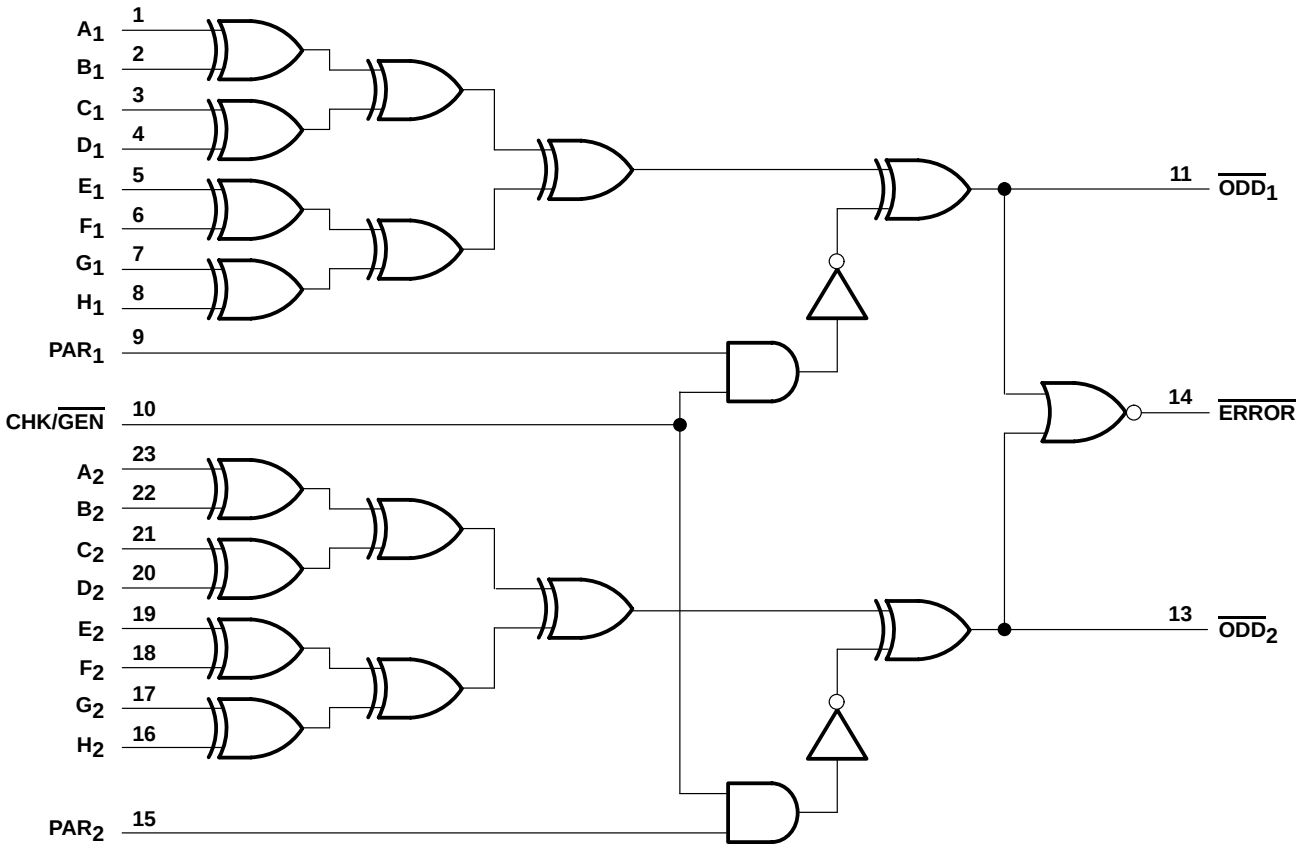
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS					OUTPUTS		
A_1–H_1	A_2–H_2	CHK/$\overline{GEN}$	PAR_1	PAR_2	$\overline{ODD}_1$	$\overline{ODD}_2$	$\overline{ERROR}$
Number of A_1–H_1 inputs, high is even	Number of A_2–H_2 inputs, high is even	H	H	H	L	L	H
		H	L	H	H	L	L
		H	H	L	L	H	L
		H	L	L	H	H	L
		L	X	X	H	H	L
	Number of inputs A_2–H_2, high is odd	H	H	H	L	H	L
		H	L	H	H	H	L
		H	H	L	L	L	H
		H	L	L	H	L	L
		L	X	X	H	L	L
Number of A_1–H_1 inputs, high is odd	Number of A_2–H_2 inputs, high is even	H	H	H	H	L	L
		H	L	H	L	L	H
		H	H	L	H	H	L
		H	L	L	L	H	L
		L	X	X	L	H	L
	Number of A_2–H_2 inputs, high is odd	H	H	H	H	H	L
		H	L	H	L	H	L
		H	H	L	H	L	L
		H	L	L	L	L	H
		L	X	X	L	L	H

H = High logic level, L = Low logic level, X = Don't care

logic diagram



Pin numbers shown are for the P, Q, and SO packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package	67°C/W
(see Note 2): Q package	61°C/W
(see Note 2): SO package	46°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		CY54FCT480T			CY74FCT480T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–32	mA
I_{OL}	Low-level output current			32			64	mA
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY54FCT480T			CY74FCT480T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = –18 mA		–0.7	–1.2				V
	V_{CC} = 4.75 V,	I_{IN} = –18 mA					–0.7	–1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –12 mA	2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = –15 mA				2.4	3.3		
		I_{OH} = –32 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.3	0.55	
V_{hys}	All inputs			0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}			5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}						5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						±1	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V			±1			±1	µA
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V	–60	–120	–225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V				–60	–120	–225	
I_{OZH}	V_{CC} = 5.5 V,	V_{OUT} = 2.7 V			10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V						10	
I_{OZL}	V_{CC} = 5.5 V,	V_{OUT} = 0.5 V			–10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V						–10	
I_{CC}	V_{CC} = 5.5 V,	V_{IN} ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2				mA
	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open			0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open						0.5	2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT480T			CY74FCT480T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CCD}¶	V_{CC} = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V				0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V							0.06	0.12	
I_C#	V_{CC} = 5.5 V, f_0 = 0 MHz, Outputs open	One bit switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1	2.4				
		16 bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		2.5	5‖				
			V_{IN} = 3.4 V or GND		6.5	21‖				
	V_{CC} = 5.25 V, f_0 = 0 MHz, Outputs open	One bit switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					0.7	1.4	
			V_{IN} = 3.4 V or GND					1	2.4	
		16 bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					2.5	5‖	
			V_{IN} = 3.4 V or GND					6.5	21‖	
C_i					5	10		5	10	pF
C_o					9	12		9	12	pF

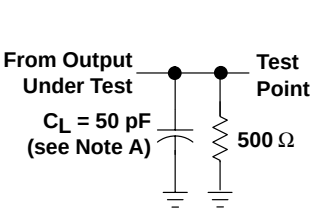
† Typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ This parameter is derived for use in total power-supply calculations.
# $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$
Where:
I_C= Total supply current
I_{CC}= Power-supply current with CMOS input levels
ΔI_{CC}= Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H= Duty cycle for TTL inputs high
N_T= Number of TTL inputs at D_H
I_{CCD}= Dynamic current caused by an input transition pair (HLH or LHL)
f_0= Clock frequency for registered devices, otherwise zero
f_1= Input signal frequency
N_1= Number of inputs changing at f_1
All currents are in milliamperes and all frequencies are in megahertz.
‖ Values for these conditions are examples of the I_{CC} formula.

switching characteristics over operating free-air temperature range (see Figure 1)

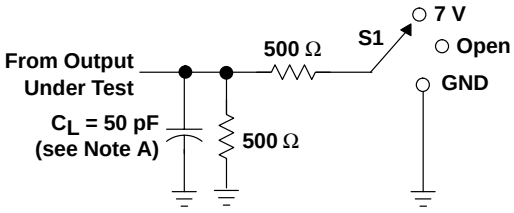
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT480AT		CY54FCT480BT		CY74FCT480BT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	$\overline{ODD}$ (see Figure 1)		7.5		7		6.1	ns
t_{PHL}				7		6.6		6.1	
t_{PLH}	CHK/$\overline{GEN}$	$\overline{ODD}$ (see Figure 1)		6.5		6.3		5.9	ns
t_{PHL}				7.5		7.4		5.9	
t_{PLH}†	A	$\overline{ERROR}$ (see Figure 2)		7		7		6.1	ns
t_{PHL}				8.5		8.1		6.5	
t_{PLH}	CHK/$\overline{GEN}$	$\overline{ERROR}$ (see Figure 2)		7.5		7.1		5.7	ns
t_{PHL}				7		6.9		5.5	

† t_{PLH} is measured up to $V_{OUT} = V_{OL} + 0.3$ V.

PARAMETER MEASUREMENT INFORMATION

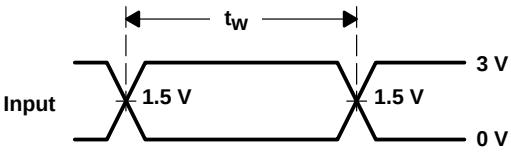


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

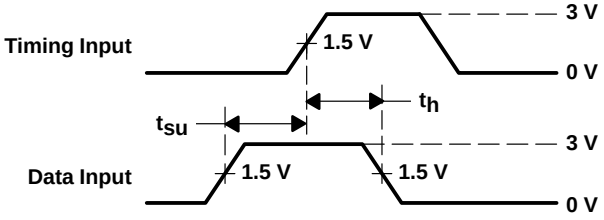


LOAD CIRCUIT FOR
3-STATE OUTPUTS

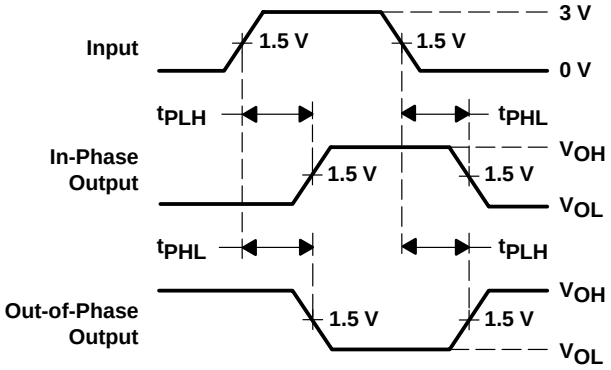
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



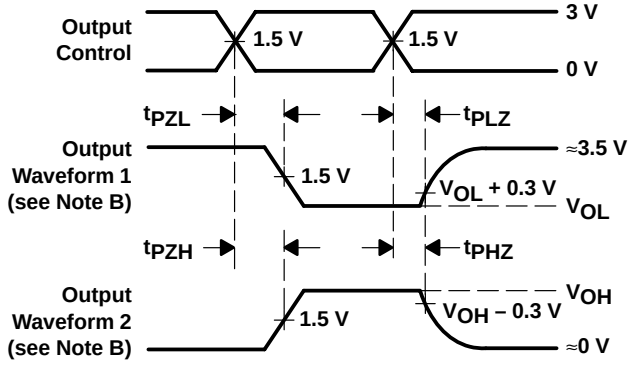
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

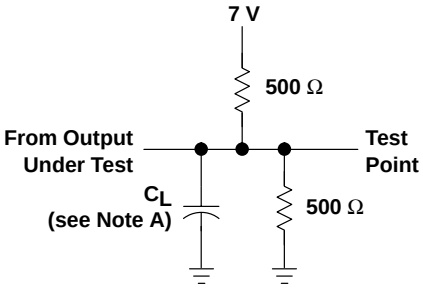


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

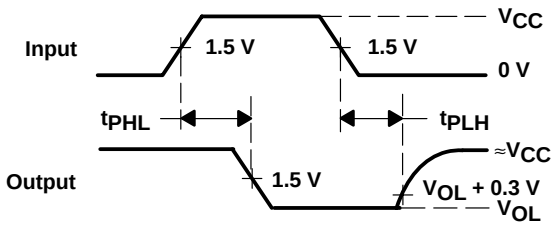
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
FOR OPEN-DRAIN OUTPUTS



LOAD CIRCUIT FOR
OPEN-DRAIN OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY54FCT480BTLMB	Active	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CY54FCT 480BTLMB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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