



## QUAD, 10-Bit, LOW-POWER, VOLTAGE OUTPUT, I<sup>2</sup>C INTERFACE DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- **Micropower Operation: 500  $\mu$ A at 3 V  $V_{DD}$**
- **Fast Update Rate: 188 kSPS**
- **Power-On Reset to Zero**
- **2.7-V to 5.5-V Analog Power Supply**
- **10-Bit Monotonic**
- **I<sup>2</sup>C™ Interface up to 3.4 Mbps**
- **Data Transmit Capability**
- **Rail-to-Rail Operation Output Buffer Amplifier**
- **Double-Buffered Input Register**
- **Address Support for up to Sixteen DAC6573s**
- **Synchronous Update for up to 64 Channels**
- **Voltage Translators for all Digital Inputs**
- **Operation From  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$**
- **Small 16 Lead TSSOP Package**

### APPLICATIONS

- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo Control**
- **PC Peripherals**
- **Portable Instrumentation**

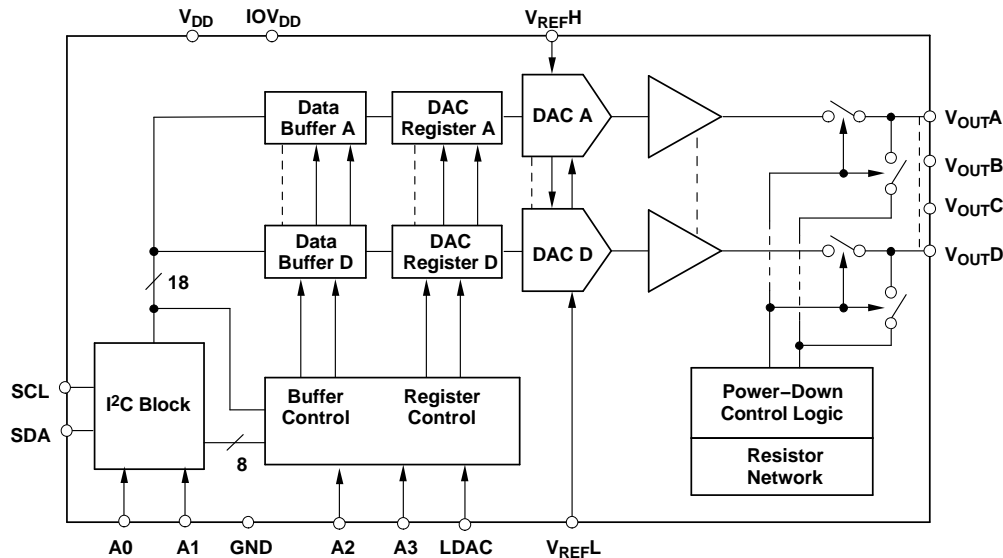
### DESCRIPTION

The DAC6573 is a low-power, quad channel, 10-Bit buffered voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail output swing. The DAC6573 utilizes an I<sup>2</sup>C compatible two wire serial interface supporting high-speed interface mode with address support of up to sixteen DAC6573s for a total of 64 channels on the bus.

The DAC6573 requires an external reference voltage to set the output range of the DAC. The DAC6573 incorporates a power-on-reset circuit that ensures that the DAC output powers up at zero volts and remains there until a valid write takes place in the device. The DAC6573 contains a power-down feature, accessed via the internal control register, that reduces the current consumption of the device to 200 nA at 5 V.

The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The power consumption is less than 3 mW at  $V_{DD}=5$  V reducing to 1  $\mu$ W in power-down mode.

The DAC6573 is available in a 16-lead TSSOP package.



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I<sup>2</sup>C is a trademark of Philips Corporation.



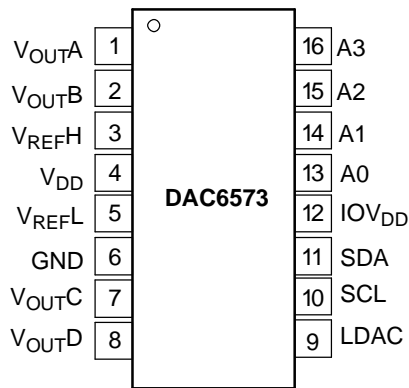
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PACKAGE/ORDERING INFORMATION**

| PRODUCT | PACKAGE  | PACKAGE DRAWING NUMBER | SPECIFICATION TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA          |
|---------|----------|------------------------|---------------------------------|-----------------|-----------------|--------------------------|
| DAC6573 | 16-TSSOP | PW                     | -40°C TO +105°C                 | D6573I          | DAC6573IPW      | 90 Piece Tube            |
|         |          |                        |                                 |                 | DAC6573IPWR     | 2000 Piece Tape and Reel |

**PW PACKAGE (TOPVIEW)**



**PIN DESCRIPTIONS**

| PIN | NAME              | DESCRIPTION  |
|-----|-------------------|--|
| 1   | V <sub>OUTA</sub> | Analog output voltage from DAC A                     |
| 2   | V <sub>OUTB</sub> | Analog output voltage from DAC B                     |
| 3   | V <sub>REFH</sub> | Positive reference voltage input                     |
| 4   | V <sub>DD</sub>   | Analog voltage supply input                          |
| 5   | V <sub>REFL</sub> | Negative reference voltage input                     |
| 6   | GND               | Ground reference point for all circuitry on the part |
| 7   | V <sub>OUTC</sub> | Analog output voltage from DAC C                     |
| 8   | V <sub>OUTD</sub> | Analog output voltage from DAC D                     |
| 9   | LDAC              | H/W synchronous V <sub>OUT</sub> update              |
| 10  | SCL               | Serial clock input                                   |
| 11  | SDA               | Serial data input                                    |
| 12  | IOV <sub>DD</sub> | I/O voltage supply input                             |
| 13  | A0                | Device address select - I <sup>2</sup> C             |
| 14  | A1                | Device address select - I <sup>2</sup> C             |
| 15  | A2                | Device address select - Extended                     |
| 16  | A3                | Device address select - Extended                     |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

|   |                                       |                                   |
|---|---------------------------------------|-----------------------------------|
| V <sub>DD</sub> to GND                          |                                       | -0.3 V to +6 V                    |
| Digital input voltage to GND                    |                                       | -0.3 V to V <sub>DD</sub> + 0.3 V |
| V <sub>OUT</sub> to GND                         |                                       | -0.3 V to V <sub>DD</sub> + 0.3 V |
| Operating temperature range                     |                                       | -40°C to +105°C                   |
| Storage temperature range                       |                                       | -65°C to +150°C                   |
| Junction temperature range (T <sub>J</sub> max) |                                       | +150°C                            |
| Power dissipation                               | Thermal impedance (R <sub>θJA</sub> ) | 161°C/W                           |
|   | Thermal impedance (R <sub>θJC</sub> ) | 29°C/W                            |
| Lead temperature, soldering                     | Vapor phase (60s)                     | 215°C                             |
|   | Infrared (15s)                        | 220°C                             |

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS**
 $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$  to GND;  $C_L = 200\text{ pF}$  to GND; all specifications  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise specified.

| PARAMETER  | TEST CONDITIONS                                       | MIN   | TYP       | MAX                   | UNITS                        |
|--|---|---|-----------|-----------------------|------------------------------|
| <b>STATIC PERFORMANCE<sup>(1)(2)</sup></b>               |   |   |           |                       |                              |
| Resolution   |   | 10  |           |                       | Bits                         |
| Relative accuracy  |   |   | $\pm 0.5$ | $\pm 2$               | LSB                          |
| Differential nonlinearity                                | Specified monotonic by design                         |   | $\pm 0.1$ | $\pm 0.5$             | LSB                          |
| Zero-scale error   |   |   | 5         | 20                    | mV                           |
| Full-scale error   |   |   | -0.15     | $\pm 1.0$             | % of FSR                     |
| Gain error   |   |   |           | $\pm 1.0$             | % of FSR                     |
| Zero code error drift                                    |   |   | $\pm 7$   |                       | $\mu\text{V}/^\circ\text{C}$ |
| Gain temperature coefficient                             |   |   | $\pm 3$   |                       | ppm of FSR/ $^\circ\text{C}$ |
| <b>OUTPUT CHARACTERISTICS<sup>(3)</sup></b>              |   |   |           |                       |                              |
| Output voltage range                                     |   | 0   |           | $V_{REFH}$            | V                            |
| Output voltage settling time (full scale)                | $R_L = \infty$ ; $0\text{ pF} < C_L < 200\text{ pF}$  |   | 7         | 9                     | $\mu\text{s}$                |
|  | $R_L = \infty$ ; $C_L = 500\text{ pF}$                |   | 12        |                       | $\mu\text{s}$                |
| Slew rate  |   |   | 1         |                       | V/ $\mu\text{s}$             |
| dc crosstalk (channel-to-channel)                        |   |   | 0.01      |                       | LSB                          |
| ac crosstalk (channel-to-channel)                        | 1 kHz Sine Wave                                       |   | -100      |                       | dB                           |
| Capacitive load stability                                | $R_L = \infty$  |   | 470       |                       | pF                           |
|  | $R_L = 2\text{ k}\Omega$                              |   | 1000      |                       | pF                           |
| Digital-to-analog glitch impulse                         | 1 LSB change around major carry                       |   | 12        |                       | nV-s                         |
| Digital feedthrough                                      |   |   | 0.3       |                       | nV-s                         |
| dc output impedance                                      |   |   | 1         |                       | $\Omega$                     |
| Short-circuit current                                    | $V_{DD} = 5\text{ V}$                                 |   | 50        |                       | mA                           |
|  | $V_{DD} = 3\text{ V}$                                 |   | 20        |                       | mA                           |
| Power-up time  | Coming out of power-down mode, $V_{DD} = +5\text{ V}$ |   | 2.5       |                       | $\mu\text{s}$                |
|  | Coming out of power-down mode, $V_{DD} = +3\text{ V}$ |   | 5         |                       | $\mu\text{s}$                |
| <b>REFERENCE INPUT</b>                                   |   |   |           |                       |                              |
| $V_{REFH}$ Input range                                   |   | 0   |           | $V_{DD}$              | V                            |
| $V_{REFL}$ Input range                                   | $V_{REFL} < V_{REFH}$                                 | 0   | GND       | $V_{DD}/2$            | V                            |
| Reference input impedance                                |   |   | 25        |                       | k $\Omega$                   |
| Reference current  | $V_{REF} = V_{DD} = +5\text{ V}$                      |   | 185       | 260                   | $\mu\text{A}$                |
|  | $V_{REF} = V_{DD} = +3\text{ V}$                      |   | 122       | 200                   | $\mu\text{A}$                |
| <b>LOGIC INPUTS<sup>(3)</sup></b>                        |   |   |           |                       |                              |
| Input current  |   |   |           | $\pm 1$               | $\mu\text{A}$                |
| $V_{IN\_L}$ , Input low voltage                          |   |   |           | $0.3 \times IOV_{DD}$ | V                            |
| $V_{IN\_H}$ , Input high voltage                         |   | $0.7 \times IOV_{DD}$                         |           |                       | V                            |
| Pin Capacitance  |   |   |           | 3                     | pF                           |
| <b>POWER REQUIREMENTS</b>                                |   |   |           |                       |                              |
| $V_{DD}$ , $IOV_{DD}$                                    |   | 2.7   |           | 5.5                   | V                            |
| $I_{DD}$ (normal operation), including reference current | Excluding load current                                |   |           |                       |                              |
|  | $I_{DD}$ @ $V_{DD} = +3.6\text{ V to }+5.5\text{ V}$  | $V_{IH} = IOV_{DD}$ and $V_{IL} = \text{GND}$ | 600       | 900                   | $\mu\text{A}$                |
|  | $I_{DD}$ @ $V_{DD} = +2.7\text{ V to }+3.6\text{ V}$  | $V_{IH} = IOV_{DD}$ and $V_{IL} = \text{GND}$ | 500       | 750                   | $\mu\text{A}$                |
| $I_{DD}$ (all power-down modes)                          |   |   |           |                       |                              |

(1) Linearity tested using a reduced code range of 12 to 1012; output unloaded.

 (2)  $V_{REFH} = V_{DD} - 0.1$ ,  $V_{REFL} = \text{GND}$ 

(3) Specified by design and characterization, not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega\text{ to GND}$ ;  $C_L = 200\text{ pF to GND}$ ; all specifications  $-40^\circ\text{C to }+105^\circ\text{C}$ , unless otherwise specified.

| PARAMETER                                     | TEST CONDITIONS                                 | MIN | TYP  | MAX  | UNITS            |
|---|---|-----|------|------|------------------|
| $I_{DD}@ V_{DD}=+3.6\text{V to }+5.5\text{V}$ | $V_{IH}= IOV_{DD}$ and $V_{IL}=GND$             |     | 0.2  | 1    | $\mu\text{A}$    |
| $I_{DD}@ V_{DD}=+2.7\text{V to }+3.6\text{V}$ | $V_{IH}= IOV_{DD}$ and $V_{IL}=GND$             |     | 0.05 | 1    | $\mu\text{A}$    |
| <b>POWER EFFICIENCY</b>                       |   |     |      |      |                  |
| $I_{OUT}/I_{DD}$                              | $I_{LOAD}= 2\text{ mA}$ , $V_{DD}= +5\text{ V}$ |     | 93%  |      |                  |
| <b>TEMPERATURE RANGE</b>                      |   |     |      |      |                  |
| Specified performance                         |   | -40 |      | +105 | $^\circ\text{C}$ |

**TIMING CHARACTERISTICS**

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega\text{ to GND}$ ; all specifications  $-40^\circ\text{C to }+105^\circ\text{C}$ , unless otherwise specified.

| SYMBOL            | PARAMETER   | TEST CONDITIONS                            | MIN | TYP           | MAX  | UNITS         |
|-------------------|---|--|-----|---------------|------|---------------|
| $f_{SCL}$         | SCL clock frequency   | Standard mode                              |     |               | 100  | kHz           |
|                   |   | Fast mode                                  |     |               | 400  | kHz           |
|                   |   | High-Speed mode, $C_B = 100\text{ pF max}$ |     |               | 3.4  | MHz           |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ |     |               | 1.7  | MHz           |
| $t_{BUF}$         | Bus free time between a STOP and START condition                                      | Standard mode                              |     | 4.7           |      | $\mu\text{s}$ |
|                   |   | Fast mode                                  |     | 1.3           |      | $\mu\text{s}$ |
| $t_{HD}; t_{STA}$ | Hold time (repeated) START condition  | Standard mode                              |     | 4.0           |      | $\mu\text{s}$ |
|                   |   | Fast mode                                  |     | 600           |      | ns            |
|                   |   | High-speed mode                            |     | 160           |      | ns            |
| $t_{LOW}$         | LOW period of the SCL clock   | Standard mode                              |     | 4.7           |      | $\mu\text{s}$ |
|                   |   | Fast mode                                  |     | 1.3           |      | $\mu\text{s}$ |
|                   |   | High-speed mode, $C_B = 100\text{ pF max}$ |     | 160           |      | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ |     | 320           |      | ns            |
| $t_{HIGH}$        | HIGH period of the SCL clock  | Standard mode                              |     | 4.0           |      | $\mu\text{s}$ |
|                   |   | Fast mode                                  |     | 600           |      | ns            |
|                   |   | High-Speed Mode, $C_B = 100\text{ pF max}$ |     | 60            |      | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ |     | 120           |      | ns            |
| $t_{SU}; t_{STA}$ | Setup time for a repeated START condition   | Standard mode                              |     | 4.7           |      | $\mu\text{s}$ |
|                   |   | Fast mode                                  |     | 600           |      | ns            |
|                   |   | High-speed mode                            |     | 160           |      | ns            |
| $t_{SU}; t_{DAT}$ | Data setup time   | Standard mode                              |     | 250           |      | ns            |
|                   |   | Fast mode                                  |     | 100           |      | ns            |
|                   |   | High-speed mode                            |     | 10            |      | ns            |
| $t_{HD}; t_{DAT}$ | Data hold time  | Standard mode                              |     | 0             | 3.45 | $\mu\text{s}$ |
|                   |   | Fast mode                                  |     | 0             | 0.9  | $\mu\text{s}$ |
|                   |   | High-speed mode, $C_B = 100\text{ pF max}$ |     | 0             | 70   | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ |     | 0             | 150  | ns            |
| $t_{RCL}$         | Rise time of SCL signal   | Standard mode                              |     |               | 1000 | ns            |
|                   |   | Fast mode                                  |     | $20 + 0.1C_B$ | 300  | ns            |
|                   |   | High-speed mode, $C_B = 100\text{ pF max}$ |     | 10            | 40   | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ |     | 20            | 80   | ns            |
| $t_{RCL1}$        | Rise time of SCL signal after a repeated START condition and after an acknowledge BIT | Standard mode                              |     |               | 1000 | ns            |
|                   |   | Fast mode                                  |     | $20 + 0.1C_B$ | 300  | ns            |
|                   |   | High-speed mode, $C_B = 100\text{ pF max}$ |     | 10            | 80   | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ |     | 20            | 160  | ns            |

**TIMING CHARACTERISTICS (continued)**
 $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$  to GND; all specifications  $-40^\circ\text{C to }+105^\circ\text{C}$ , unless otherwise specified.

| SYMBOL            | PARAMETER   | TEST CONDITIONS                            | MIN           | TYP | MAX  | UNITS         |
|-------------------|---|--|---------------|-----|------|---------------|
| $t_{FCL}$         | Fall time of SCL signal   | Standard mode                              |               |     | 300  | ns            |
|                   |   | Fast mode                                  | $20 + 0.1C_B$ |     | 300  | ns            |
|                   |   | High-speed mode, $C_B = 100\text{ pF max}$ | 10            |     | 40   | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ | 20            |     | 80   | ns            |
| $t_{RDA}$         | Rise time of SDA signal   | Standard mode                              |               |     | 1000 | ns            |
|                   |   | Fast mode                                  | $20 + 0.1C_B$ |     | 300  | ns            |
|                   |   | High-speed mode, $C_B = 100\text{ pF max}$ | 10            |     | 80   | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ | 20            |     | 160  | ns            |
| $t_{FDA}$         | Fall time of SDA signal   | Standard mode                              |               |     | 300  | ns            |
|                   |   | Fast mode                                  | $20 + 0.1C_B$ |     | 300  | ns            |
|                   |   | High-speed mode, $C_B = 100\text{ pF max}$ | 10            |     | 80   | ns            |
|                   |   | High-speed mode, $C_B = 400\text{ pF max}$ | 20            |     | 160  | ns            |
| $t_{SU}; t_{STO}$ | Setup time for STOP condition   | Standard mode                              | 4.0           |     |      | $\mu\text{s}$ |
|                   |   | Fast mode                                  | 600           |     |      | ns            |
|                   |   | High-speed mode                            | 160           |     |      | ns            |
| $C_B$             | Capacitive load for SDA and SCL   |  |               |     | 400  | pF            |
| $t_{SP}$          | Pulse width of spike suppressed   | Fast mode                                  |               |     | 50   | ns            |
|                   |   | High-speed mode                            |               |     | 10   | ns            |
| $V_{NH}$          | Noise margin at the HIGH level for each connected device (including hysteresis) | Standard mode                              | $0.2 V_{DD}$  |     |      | V             |
|                   |   | Fast mode                                  |               |     |      |               |
|                   |   | High-speed mode                            |               |     |      |               |
| $V_{NL}$          | Noise margin at the LOW level for each connected device (including hysteresis)  | Standard mode                              | $0.1 V_{DD}$  |     |      | V             |
|                   |   | Fast mode                                  |               |     |      |               |
|                   |   | High-speed mode                            |               |     |      |               |

### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

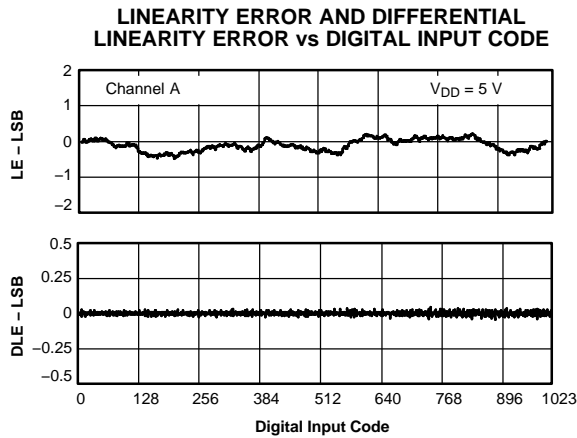


Figure 1.

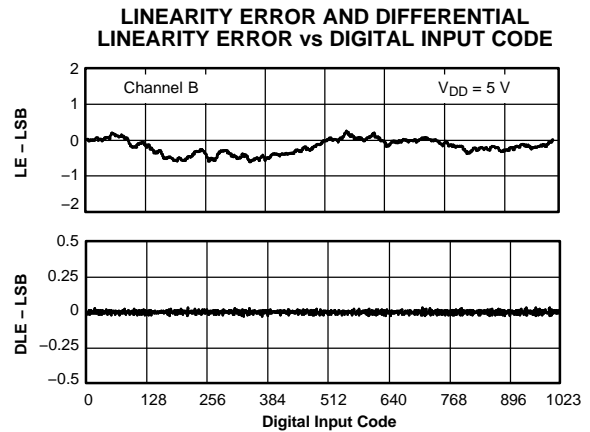


Figure 2.

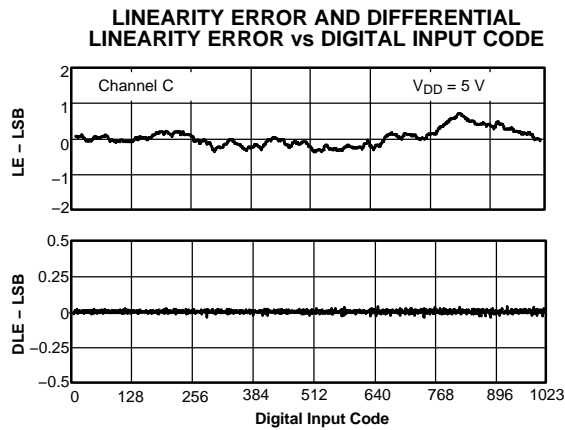


Figure 3.

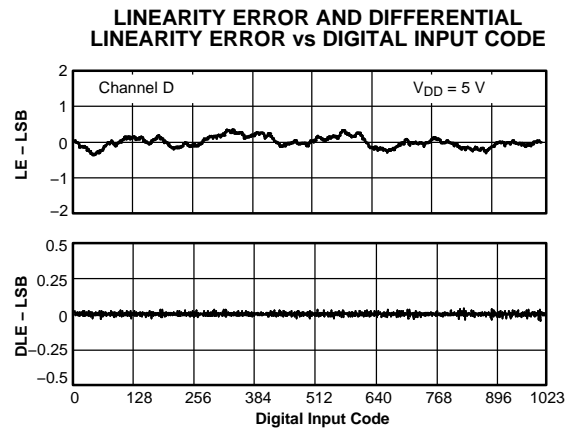


Figure 4.

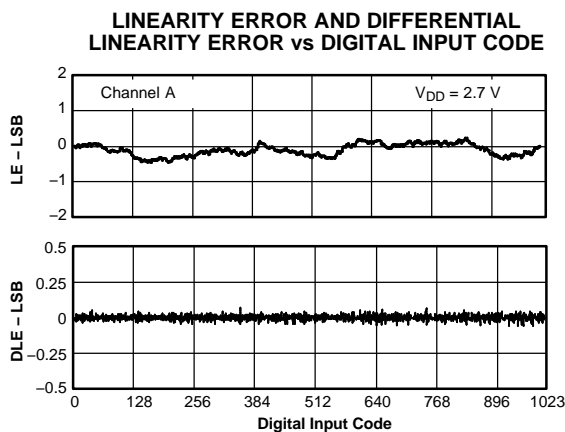


Figure 5.

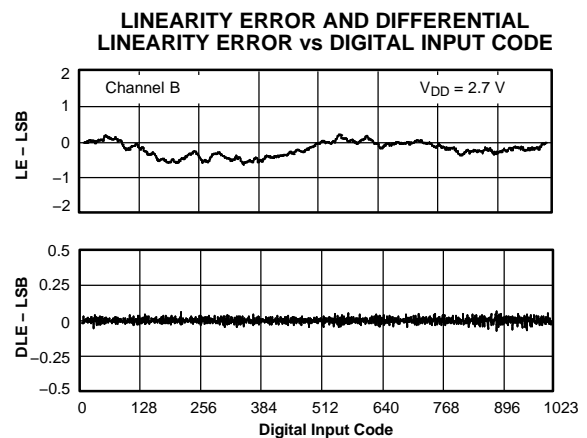


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

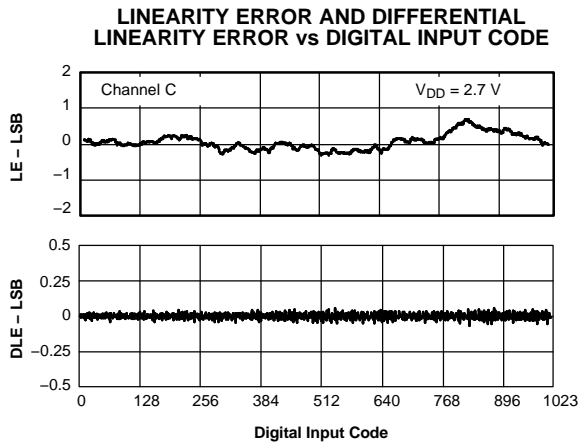


Figure 7.

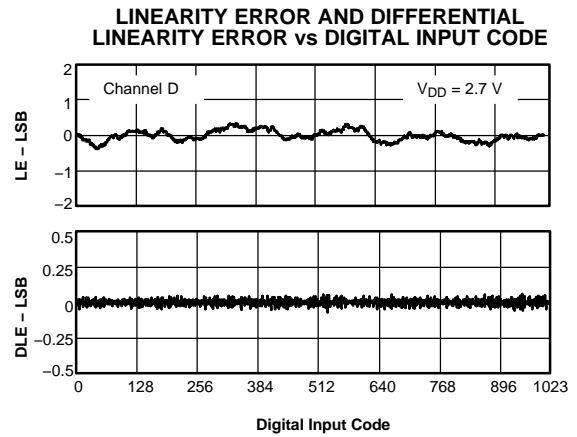


Figure 8.

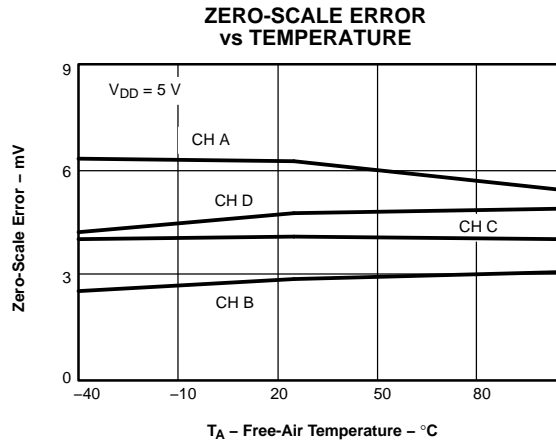


Figure 9.

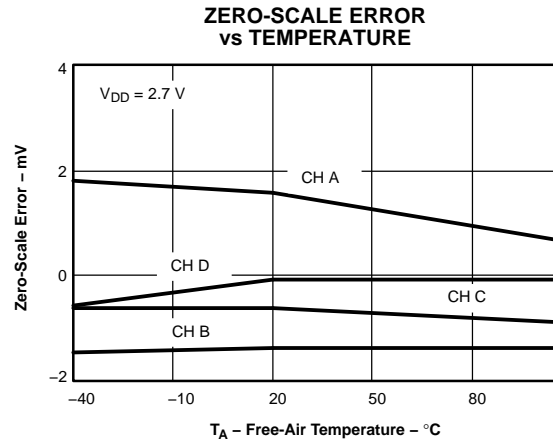


Figure 10.

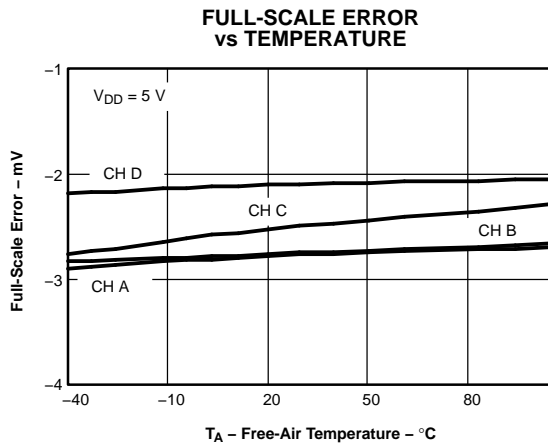


Figure 11.

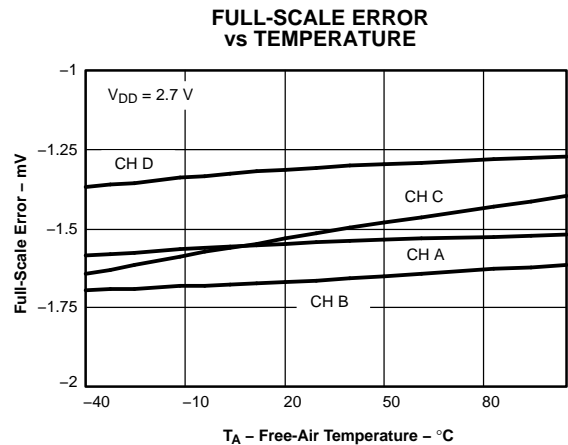


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

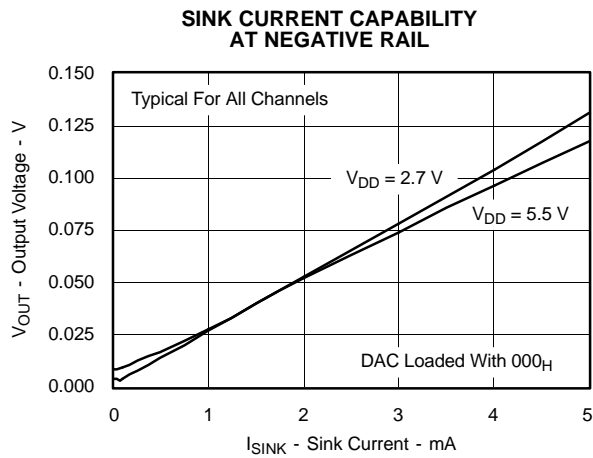


Figure 13.

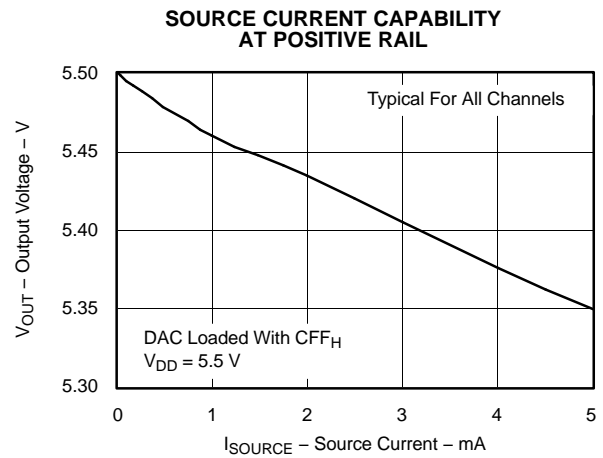


Figure 14.

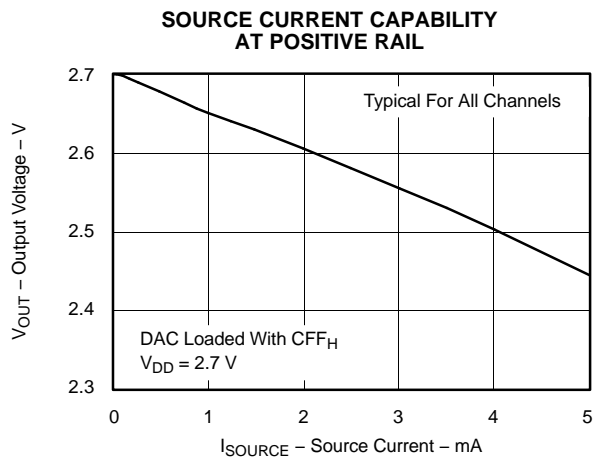


Figure 15.

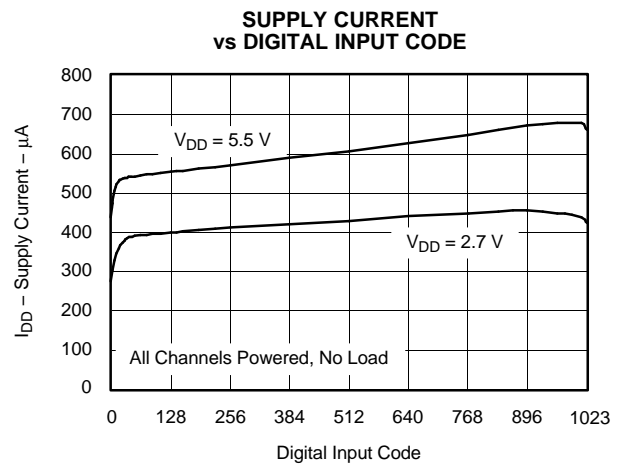


Figure 16.

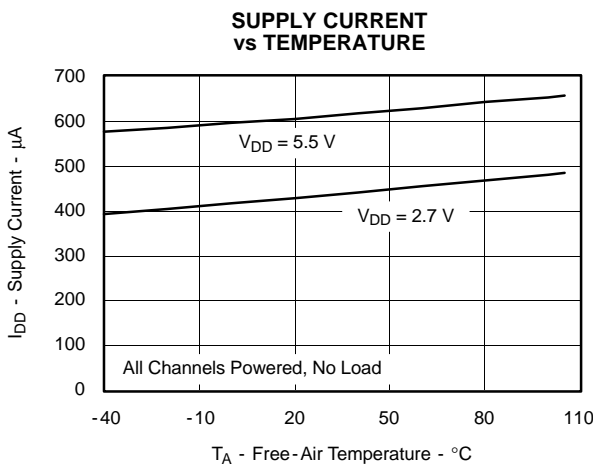


Figure 17.

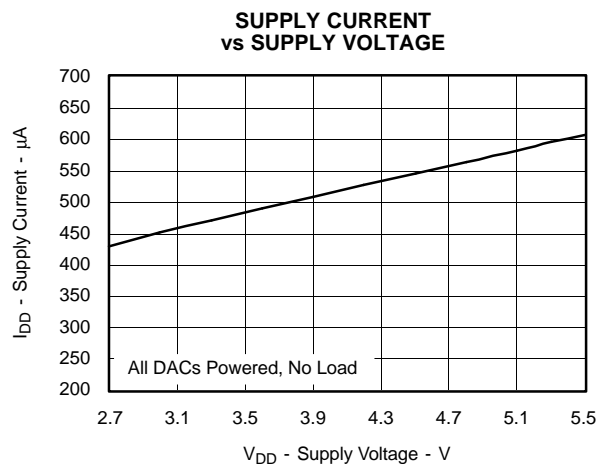
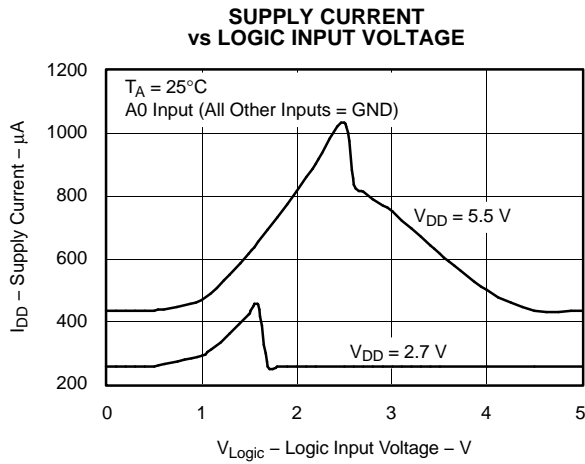


Figure 18.

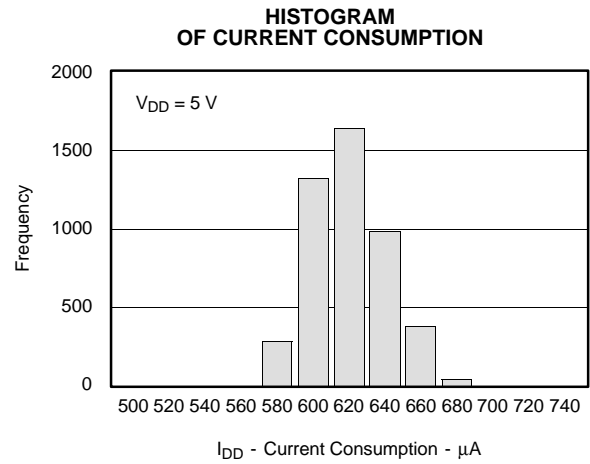


**TYPICAL CHARACTERISTICS (continued)**

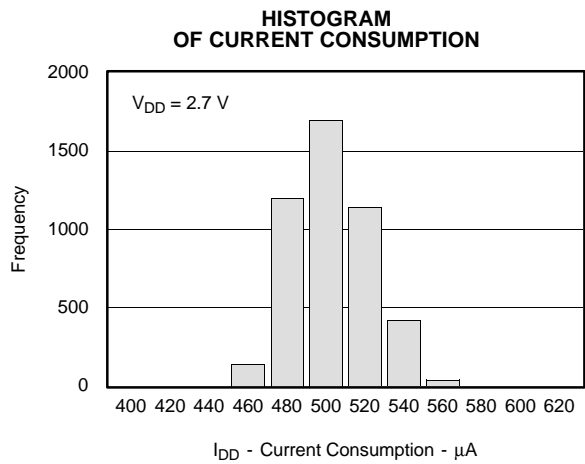
At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.



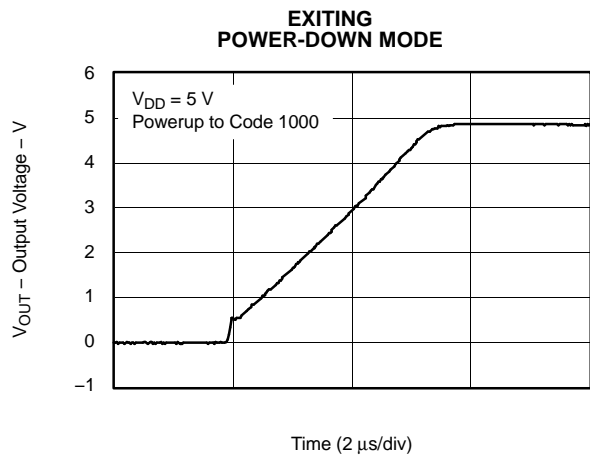
**Figure 19.**



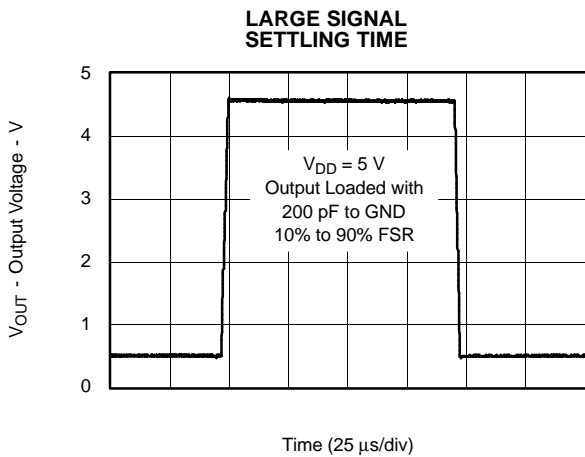
**Figure 20.**



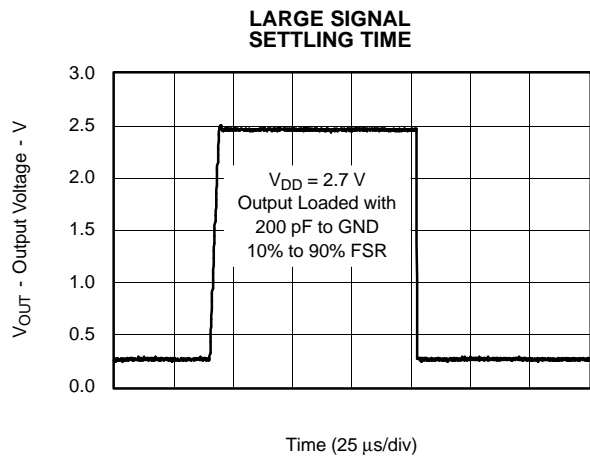
**Figure 21.**



**Figure 22.**



**Figure 23.**



**Figure 24.**

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

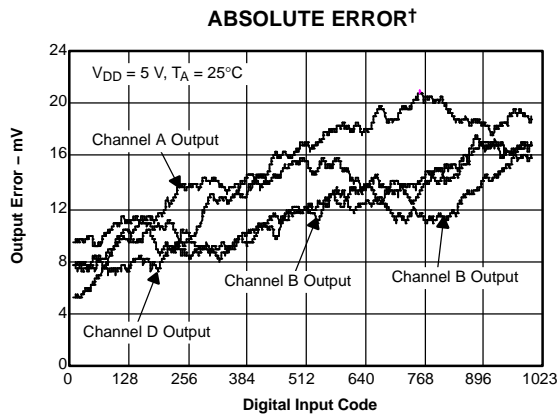


Figure 25.

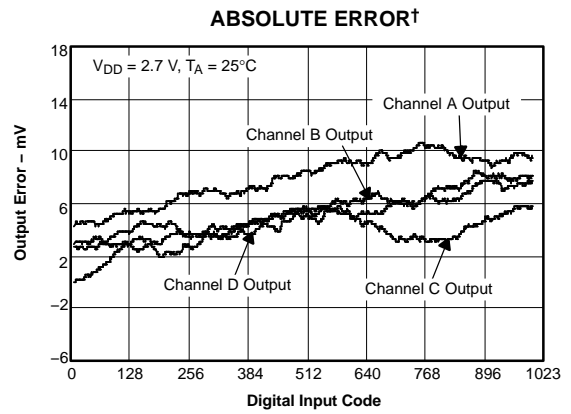


Figure 26.

<sup>†</sup>Absolute error is the deviation from ideal DAC characteristics. It includes affects of offset, gain, and integral linearity.

## THEORY OF OPERATION

### D/A SECTION

The architecture of the DAC6573 consists of a string DAC followed by an output buffer amplifier. Figure 27 shows a generalized block diagram of the DAC architecture.

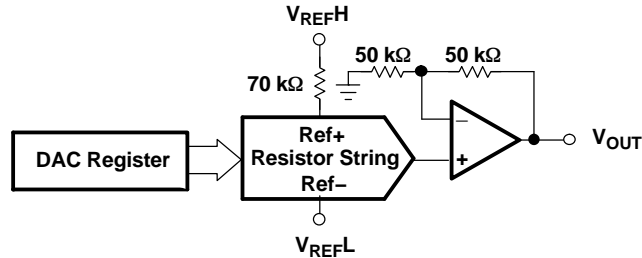


Figure 27. R-String DAC Architecture

The input coding to the DAC6573 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = 2 \times V_{REFL} + (V_{REFH} - V_{REFL}) \times \frac{D}{1024}$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 1023.

### RESISTOR STRING

The resistor string section is shown in Figure 28. It is basically a divide-by-2 resistor, followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Because the architecture consists of a string of resistors, it is specified monotonic.

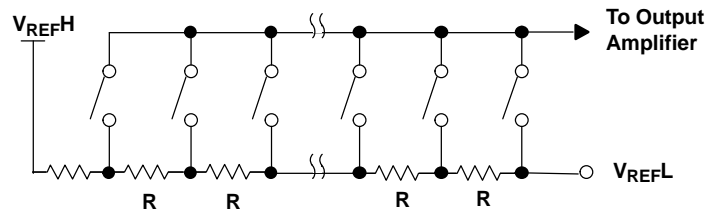


Figure 28. Typical Resistor String

### Output Amplifier

The output buffer is a gain-of-2 noninverting amplifier, capable of generating rail-to-rail voltages on its output, which gives an output range of 0V to  $V_{DD}$ . It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/μs with a half-scale settling time of 7 μs with the output unloaded.

### I<sup>2</sup>C Interface

I<sup>2</sup>C is a 2-wire serial interface developed by Philips Semiconductor (see I<sup>2</sup>C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

## THEORY OF OPERATION (continued)

The DAC6573 works as a slave and supports the following data transfer modes, as defined in the I<sup>2</sup>C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode. The DAC6573 supports 7-bit addressing; 10-bit addressing and general call address are *not* supported.

### F/S-Mode Protocol

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 29. All I<sup>2</sup>C-compatible devices recognize a *start condition*.
- The master then generates the SCL pulses, and transmits the 7-bit address and the *read/write direction bit*  $R/\overline{W}$  on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data condition* requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 30). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 31) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave ( $R/\overline{W}$  bit 1) or *receive* data from the slave ( $R/\overline{W}$  bit 0). In either case, the *receiver* must acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-Bit data and 1-bit acknowledge can continue as long as necessary.
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 29). This releases the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C-compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

### H/S-Mode Protocol

- When the bus is idle, both SDA and SCL lines are pulled high by the pullup devices.
- The master generates a start condition followed by a valid serial byte containing H/S master code 00001XXX. This transmission is made in F/S mode at no more than 400 Kbps. No device is allowed to acknowledge the H/S master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.
- The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the H/S-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in H/S-mode.

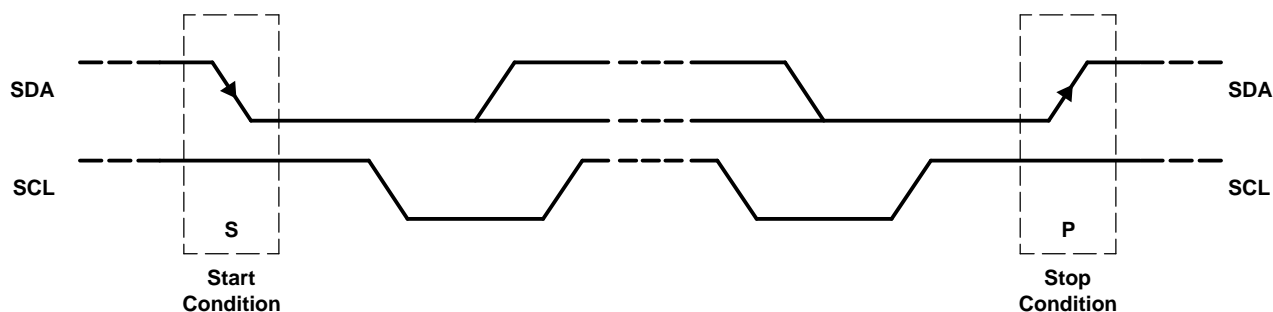


Figure 29. START and STOP Conditions

THEORY OF OPERATION (continued)

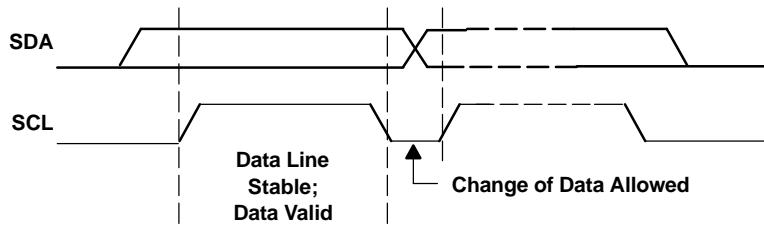


Figure 30. Bit Transfer on the I<sup>2</sup>C Bus

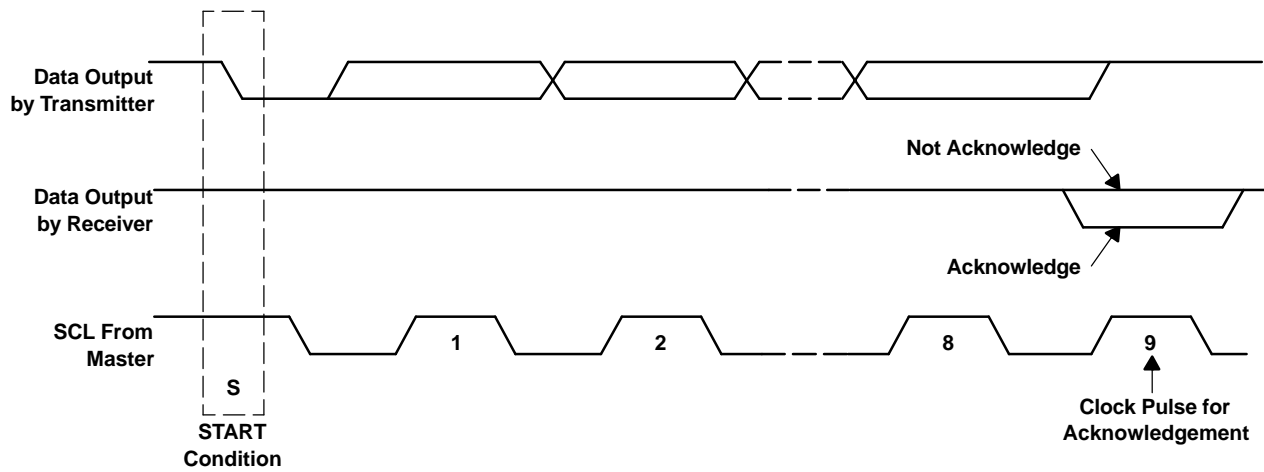


Figure 31. Acknowledge on the I<sup>2</sup>C Bus

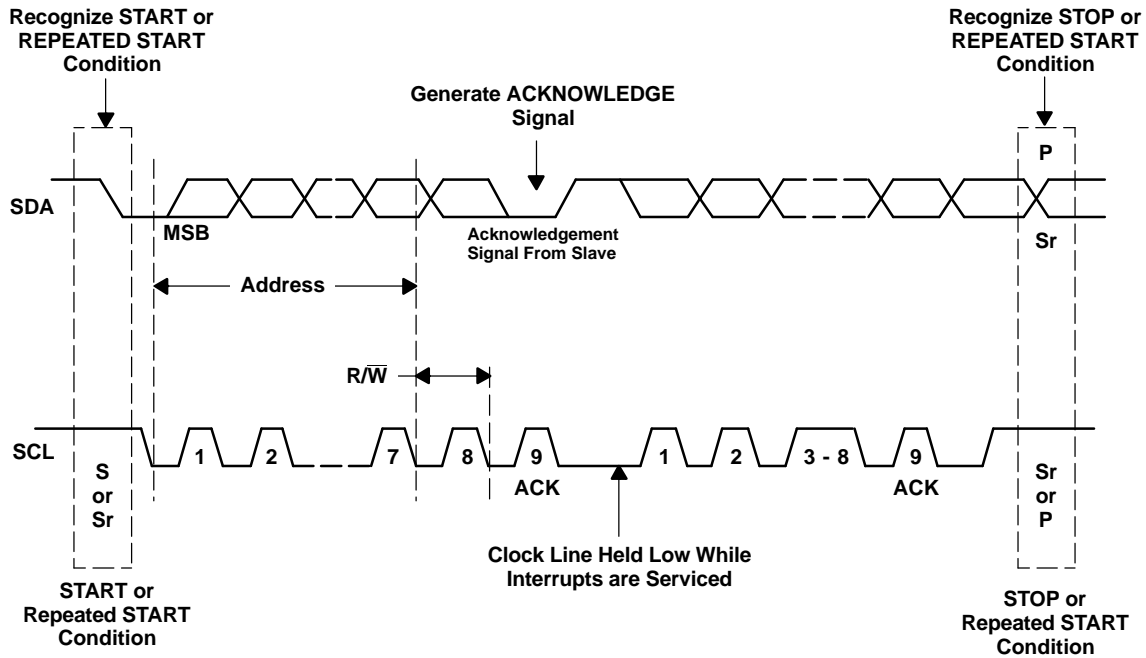


Figure 32. Bus Protocol

## DAC6573 I<sup>2</sup>C Update Sequence

The DAC6573 requires a start condition, a valid I<sup>2</sup>C address, a control byte, an MSB byte, and an LSB byte for a single update. After the receipt of each byte, DAC6573 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the DAC6573. The control byte sets the operational mode of the selected DAC6573. Once the operational mode is selected by the control byte, DAC6573 expects an MSB byte followed by an LSB byte for data update to occur. DAC6573 performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

The control byte needs not to be resent until a change in operational mode is required. The bits of the control byte continuously determine the type of update performed. Thus, for the first update, DAC6573 requires a start condition, a valid I<sup>2</sup>C address, a control byte, an MSB byte and an LSB byte. For all consecutive updates, DAC6573 needs an MSB byte, and an LSB byte as long as the control command remains the same.

Using the I<sup>2</sup>C high-speed mode ( $f_{sc1} = 3.4$  MHz), the clock running at 3.4 MHz, each 10-Bit DAC update other than the first update can be done within 18 clock cycles (MSB byte, acknowledge signal, LSB byte, acknowledge signal), at 188.88 kSPS. Using the fast mode ( $f_{sc1} = 400$  kHz), clock running at 400 kHz, maximum DAC update rate is limited to 22.22 kSPS. Once a stop condition is received, DAC6573 releases the I<sup>2</sup>C bus and awaits a new start condition.

### Address Byte

| MSB |   |   |   |   |    |    | LSB |
|-----|---|---|---|---|----|----|-----|
| 1   | 0 | 0 | 1 | 1 | A1 | A0 | R/W |

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the address are factory preset to 10011. The next two bits of the address are the device select bits A1 and A0. The A1, A0 address inputs can be connected to V<sub>DD</sub> or digital GND, or can be actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins during the power-up sequence of the DAC6573. Up to 16 devices (DAC6573) can still be connected to the same I<sup>2</sup>C-bus.

### Broadcast Address Byte

| MSB |   |   |   |   |   |   | LSB |
|-----|---|---|---|---|---|---|-----|
| 1   | 0 | 0 | 1 | 0 | 0 | 0 | 0   |

Broadcast addressing is also supported by DAC6573. Broadcast addressing can be used for synchronously updating or powering down multiple DAC6573 devices. DAC6573 is designed to work with other members of the DAC857x, DAC757x, and DAC557x families to support multichannel synchronous update. Using the broadcast address, DAC6573 responds regardless of the states of the address pins. Broadcast is supported only in write mode (master writes to DAC6573).

**Control Byte**

| MSB |    |    |    |   |      |      | LSB |
|-----|----|----|----|---|------|------|-----|
| A3  | A2 | L1 | L0 | X | Sel1 | Sel0 | PD0 |

**Table 1. Control Register Bit Descriptions**

| Bit Name | Bit Number/Description  |   |   |
|----------|-------------------------|---|---|
| A3       | Extended address bit    | The state of these bits must match the state of pins A3 and A2 in order for a proper DAC6573 data update, except in broadcast update mode.  |   |
| A2       | Extended address bit    |   |   |
| L1       | Load1 (mode select) bit | Are used for selecting the update mode.   |   |
| L2       | Load0 (mode select) bit |   |   |
|          | 00                      | Store I <sup>2</sup> C data. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register of a selected channel. This mode does not change the DAC output of the selected channel.  |   |
|          | 01                      | Update selected DAC with I <sup>2</sup> C data. Most commonly utilized mode. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register and in the DAC register of the selected channel. This mode changes the DAC output of the selected channel with the new data.                                  |   |
|          | 10                      | 4-channel synchronous update. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register and in the DAC register of the selected channel. Simultaneously, the other three channels get updated with previously stored data from the temporary register. This mode updates all four channels together. |   |
|          | 11                      | Broadcast update mode. This mode has two functions. In broadcast mode, DAC6573 responds regardless of local address matching, and channel selection becomes irrelevant as all channels update. This mode is intended to enable up to 64 channels simultaneous update, if used with the I <sup>2</sup> C broadcast address (1001 0000).          |   |
|          |                         | If Sel1=0   | All four channels are updated with the contents of their temporary register data. |
|          |                         | If Sel1=1   | All four channels are updated with the MS-BYTE and LS-BYTE data or powerdown.     |
| Sel1     | Buff Sel1 Bit           | Channel select bits   |   |
| Sel0     | Buff Sel0 Bit           |   |   |
|          | 00                      | Channel A   |   |
|          | 01                      | Channel B   |   |
|          | 10                      | Channel C   |   |
|          | 11                      | Channel D   |   |
| PD0      | Power Down Flag         |   |   |
|          | 0                       | Normal operation  |   |
|          | 1                       | Power-down flag (MSB7 and MSB6 indicate a power-down operation, as shown in Table 2).   |   |

**Table 2. Control Byte**

| C7   | C6 | C5    | C4    | C3                  | C2       | C1       | C0          | MSB7        | MSB6   | MSB5...  | DESCRIPTION |
|--|----|-------|-------|---------------------|----------|----------|-------------|-------------|--|--|-------------|
| A3   | A2 | Load1 | Load0 | Don't Care          | Ch Sel 1 | Ch Sel 0 | PD0         | MSB (PD1)   | MSB-1 (PD2)  | MSB-2 ...LSB   |             |
| <b>(Address Select)</b>  |    |       |       |                     |          |          |             |             |  |  |             |
| (A3 and A2 should correspond to the package address, set via pins A3 and A2) | 0  | 0     | X     | 0                   | 0        | 0        | 0           | Data        |  | Write to temporary register A (TRA) with data                |             |
|  | 0  | 0     | X     | 0                   | 1        | 0        | 0           | Data        |  | Write to temporary register B (TRB) with data                |             |
|  | 0  | 0     | X     | 1                   | 0        | 0        | 0           | Data        |  | Write to temporary register C (TRC) with data                |             |
|  | 0  | 0     | X     | 1                   | 1        | 0        | 0           | Data        |  | Write to temporary register D (TRD) with data                |             |
|  | 0  | 0     | X     | (00, 01, 10, or 11) |          | 1        | See Table 8 | 0           | Write to TRx (selected by C2 & C1 w/Powerdown Command)       |  |             |
|  | 0  | 1     | X     | (00, 01, 10, or 11) |          | 0        | Data        |             | Write to TRx (selected by C2 & C1 and load DACx w/data)      |  |             |
|  | 0  | 1     | X     | (00, 01, 10, or 11) |          | 1        | See Table 8 | 0           | Power-down DACx (selected by C2 and C1)                      |  |             |
|  | 1  | 0     | X     | (00, 01, 10, or 11) |          | 0        | Data        |             | Write to TRx (selected by C2 & C1 w/ data and load all DACs) |  |             |
|  | 1  | 0     | X     | (00, 01, 10, or 11) |          | 1        | See Table 8 | 0           | Power-down DACx (selected by C2 and C1) & load all DACs      |  |             |
| <b>Broadcast Modes (controls up to 4 devices on a single serial bus)</b>     |    |       |       |                     |          |          |             |             |  |  |             |
| X  | X  | 1     | 1     | X                   | 0        | X        | X           | X           |  | Update all DACs, all devices with previously stored TRx data |             |
| X  | X  | 1     | 1     | X                   | 1        | X        | 0           | Data        |  | Update all DACs, all devices with MSB[7:0] and LSB[7:0] data |             |
| X  | X  | 1     | 1     | X                   | 1        | X        | 1           | see Table 8 | 0  | Power-down all DACs, all devices                             |             |

**Most Significant Byte**

Most significant byte MSB[7:0] consists of eight most significant bits of 10-bit unsigned binary D/A conversion data. If C0=1, MSB[7], MSB[6] indicate a power-down operation as shown in Table 8.

**Least Significant Byte**

Least significant byte LSB[7:0] consists of the 2 least significant bits of the 10-Bit unsigned binary D/A conversion data, followed by 6 *don't care* bits. DAC6573 updates at the falling edge of the acknowledge signal that follows the LSB[0] bit.

**Default Readback Condition**

If the user initiates a readback of a specified channel without first writing data to that specified channel, the default readback is all zeros, since the readback register is initialized to 0 during the power on reset phase.



## LDAC Functionality

Depending on the control byte, DACs are synchronously updated on the falling edge of the acknowledge signal that follows LS byte. The LDAC pin is required only when an external timing signal is used to update all the channels of the DAC asynchronously. LDAC is a positive edge triggered asynchronous input that allows four DAC output voltages to be updated simultaneously with temporary register data. The LDAC trigger should only be used after the buffer's temporary registers are properly updated through software.

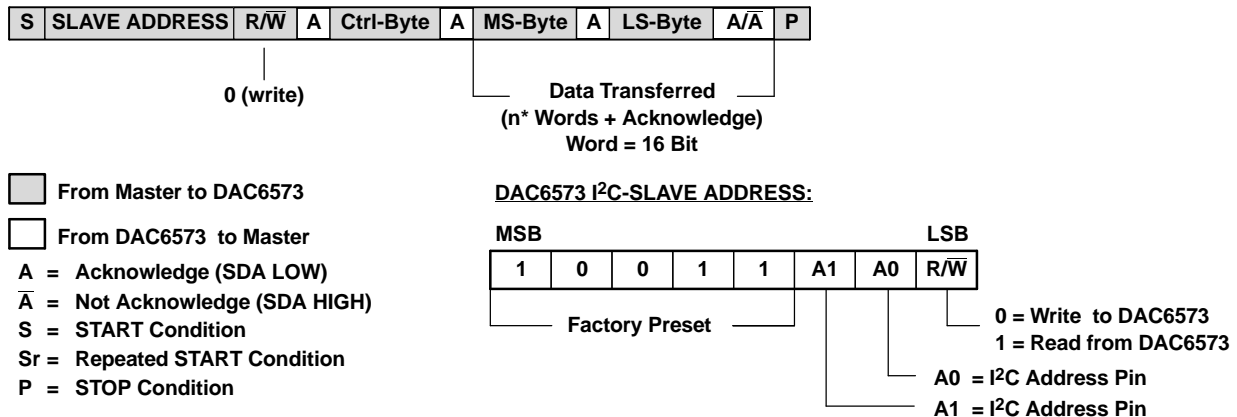
## DAC6573 Registers

**Table 3. DAC6573 Architecture Register Descriptions**

| REGISTER                                   | DESCRIPTION  |
|--|--|
| CTRL[7:0]                                  | Stores 8-Bit wide control byte sent by the master  |
| MSB[7:0]                                   | Stores the 8 most significant bits of unsigned binary data sent by the master. Can also store 2-bit power-down data.   |
| LSB[7:0]                                   | Stores the 2 least significant bits of unsigned binary data sent by the master (in LSB[7] and LSB[6]).   |
| TRA[11:0], TRB[11:0], TRC[11:0], TRD[11:0] | 12-bit temporary storage registers assigned to each channel. Two MSBs store power-down information, 10 LSBs store data.  |
| DRA[11:0], DRB[11:0], DRC[11:0], DRD[11:0] | 12-bit DAC registers for each channel. Two MSBs store power-down information, 10 LSBs store DAC data. An update of this register means a DAC update with data or power-down. |

## DAC6573 as a Slave Receiver—Standard and Fast Mode

Figure 33 shows the standard and fast mode master transmitter addressing a DAC6573 *Slave Receiver* with a 7-bit address.



**Figure 33. Standard and Fast Mode: Slave Receiver**

### DAC6573 as a Slave Receiver - High-Speed Mode

Figure 34 shows the high-speed mode master transmitter addressing a DAC6573 *Slave Receiver* with a 7-bit address.

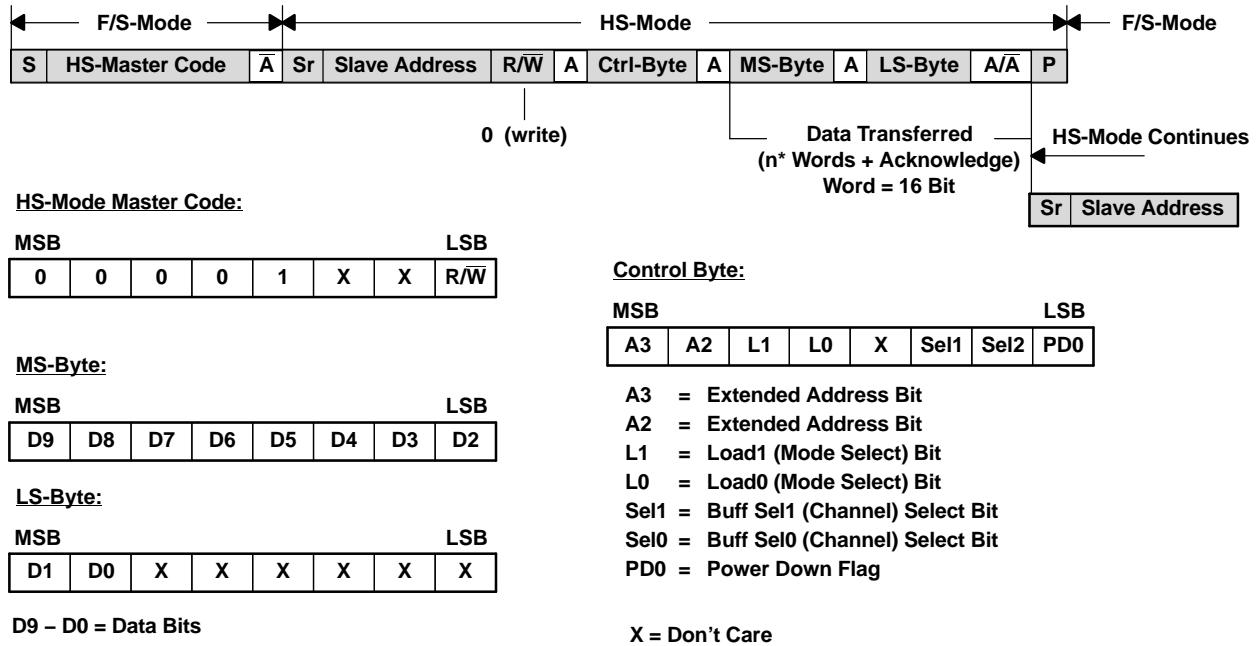


Figure 34. High-Speed Mode: Slave Receiver

## Master Transmitter Writing to a Slave Receiver (DAC6573) in Standard/Fast Modes

All write access sequences begin with the device address (with  $R/\overline{W} = 0$ ) followed by the control byte. This control byte specifies the operation mode of DAC6573 and determines which channel of DAC6573 is being accessed in the subsequent read/write operation. The LSB of the control byte (PD0-Bit) determines whether the following data is power-down data or regular data.

With (PD0-Bit = 0) the DAC6573 expects to receive data in the following sequence *HIGH-BYTE –LOW-BYTE – HIGH-BYTE – LOW-BYTE...*, until a STOP Condition or REPEATED START Condition on the I<sup>2</sup>C-bus is recognized (refer to the DATA INPUT MODE section of Table 4).

With (PD0-Bit = 1) the DAC6573 expects to receive 2 bytes of power-down data (refer to the POWER DOWN MODE section of Table 4).

**Table 4. Write Sequence in F/S Mode**

| DATA INPUT MODE |   |     |        |        |    |            |            |                   |   |
|-----------------|---|-----|--------|--------|----|------------|------------|-------------------|---|
| Transmitter     | MSB   | 6   | 5      | 4      | 3  | 2          | 1          | LSB               | Comment                                 |
| Master          | Start   |     |        |        |    |            |            |                   | Begin sequence                          |
| Master          | 1   | 0   | 0      | 1      | 1  | A1         | A0         | R/ $\overline{W}$ | Write addressing (R/ $\overline{W}$ =0) |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | A3  | A2  | Load 1 | Load 0 | x  | Buff Sel 1 | Buff Sel 0 | PD0               | Control byte (PD0=0)                    |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | D9  | D8  | D7     | D6     | D5 | D4         | D3         | D2                | Writing data word, high byte            |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | D1  | D0  | x      | x      | x  | x          | x          | x                 | Writing data word, low byte             |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | Data or Stop or Repeated Start <sup>(1)</sup> |     |        |        |    |            |            |                   | Data or done <sup>(2)</sup>             |
| POWER DOWN MODE |   |     |        |        |    |            |            |                   |   |
| Transmitter     | MSB   | 6   | 5      | 4      | 3  | 2          | 1          | LSB               | Comment                                 |
| Master          | Start   |     |        |        |    |            |            |                   | Begin sequence                          |
| Master          | 1   | 0   | 0      | 1      | 1  | A1         | A0         | R/ $\overline{W}$ | Write addressing (R/ $\overline{W}$ =0) |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | A3  | A2  | Load 1 | Load 0 | x  | Buff Sel 1 | Buff Sel 0 | PD0               | Control byte (PD0 = 1)                  |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | PD1   | PD2 | 0      | 0      | 0  | 0          | 0          | 0                 | Writing data word, high byte            |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | 0   | 0   | x      | x      | x  | x          | x          | x                 | Writing data word, low byte             |
| DAC6573         | DAC6573 Acknowledges                          |     |        |        |    |            |            |                   |   |
| Master          | Stop or Repeated Start <sup>(1)</sup>         |     |        |        |    |            |            |                   | Done                                    |

(1) Use repeated START to secure bus operation and loop back to the stage of write addressing for next Write.

(2) Once DAC6573 is properly addressed and control byte is sent, HIGH–BYTE–LOW–BYTE sequences can repeat until a STOP condition or repeated START condition is received.

### Master Transmitter Writing to a Slave Receiver (DAC6573) in HS Mode

When writing data to the DAC6573 in HS-mode, the master begins to transmit what is called the *HS-Master Code* (0000 1XXX) in F/S-mode. No device is allowed to acknowledge the *HS-Master Code*, so the *HS-Master Code* is followed by a NOT acknowledge.

The master then *switches* to HS-mode and issues a *repeated start* condition, followed by the address byte (with R/W = 0) after which the DAC6573 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6573. The LSB of the control byte (PD0-Bit) determines if the following data is *power-down data* or regular data.

With (PD0-Bit = 0) the DAC6573 expects to receive data in the following sequence HIGH-BYTE – LOW-BYTE – HIGH-BYTE – LOW-BYTE..., until a STOP condition or *repeated start* condition on the I<sup>2</sup>C-Bus is recognized (refer to Table 5 HS-MODE WRITE SEQUENCE - DATA).

With (PD0-Bit = 1) the DAC6573 expects to receive 2 bytes of power-down data (refer to Table 5 HS-MODE WRITE SEQUENCE - POWER DOWN).

**Table 5. Master Transmitter Writes to Slave Receiver (DAC6573) in HS-Mode**

| HS MODE WRITE SEQUENCE - DATA       |   |     |        |        |    |            |            |     |  |
|-------------------------------------|---|-----|--------|--------|----|------------|------------|-----|--|
| Transmitter                         | MSB   | 6   | 5      | 4      | 3  | 2          | 1          | LSB | Comment                                  |
| Master                              | Start   |     |        |        |    |            |            |     | Begin sequence                           |
| Master                              | 0   | 0   | 0      | 0      | 1  | X          | X          | X   | HS mode master code                      |
| NONE                                | Not acknowledge                               |     |        |        |    |            |            |     | No device may acknowledge HS master code |
| Master                              | Repeated start                                |     |        |        |    |            |            |     |  |
| Master                              | 1   | 0   | 0      | 1      | 1  | A1         | A0         | R/W | Write addressing (R/W=0)                 |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | 0   | 0   | Load 1 | Load 0 | 0  | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=0)                     |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | D9  | D8  | D7     | D6     | D5 | D4         | D3         | D2  | Writing data word, MSB                   |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | D1  | D0  | x      | x      | x  | x          | x          | x   | Writing data word, LSB                   |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | Data or stop or repeated start <sup>(1)</sup> |     |        |        |    |            |            |     | Data or done <sup>(2)</sup>              |
| HS MODE WRITE SEQUENCE - POWER DOWN |   |     |        |        |    |            |            |     |  |
| Transmitter                         | MSB   | 6   | 5      | 4      | 3  | 2          | 1          | LSB | Comment                                  |
| Master                              | Start   |     |        |        |    |            |            |     | Begin sequence                           |
| Master                              | 0   | 0   | 0      | 0      | 1  | X          | X          | X   | HS mode master code                      |
| NONE                                | Not acknowledge                               |     |        |        |    |            |            |     | No device may acknowledge HS master code |
| Master                              | Repeated start                                |     |        |        |    |            |            |     |  |
| Master                              | 1   | 0   | 0      | 1      | 1  | A1         | A0         | R/W | Write addressing (R/W = 0)               |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | 0   | 0   | Load 1 | Load 2 | 0  | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=1)                     |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | PD1   | PD2 | 0      | 0      | 0  | 0          | 0          | 0   | Writing data word, high byte             |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | 0   | 0   | x      | x      | x  | x          | x          | x   | Writing data word, low byte              |
| DAC6573                             | DAC6573 acknowledges                          |     |        |        |    |            |            |     |  |
| Master                              | Stop or repeated start <sup>(1)</sup>         |     |        |        |    |            |            |     | Done                                     |

(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

(2) Once DAC6573 is properly addressed and control byte is sent, high-byte-low-byte sequences can repeat until a stop or repeated start condition is received.

### DAC6573 as a Slave Transmitter—Standard and Fast Mode

Figure 35 shows the standard and fast mode master receiver addressing a DAC6573 *Slave Transmitter* with a 7-bit address.

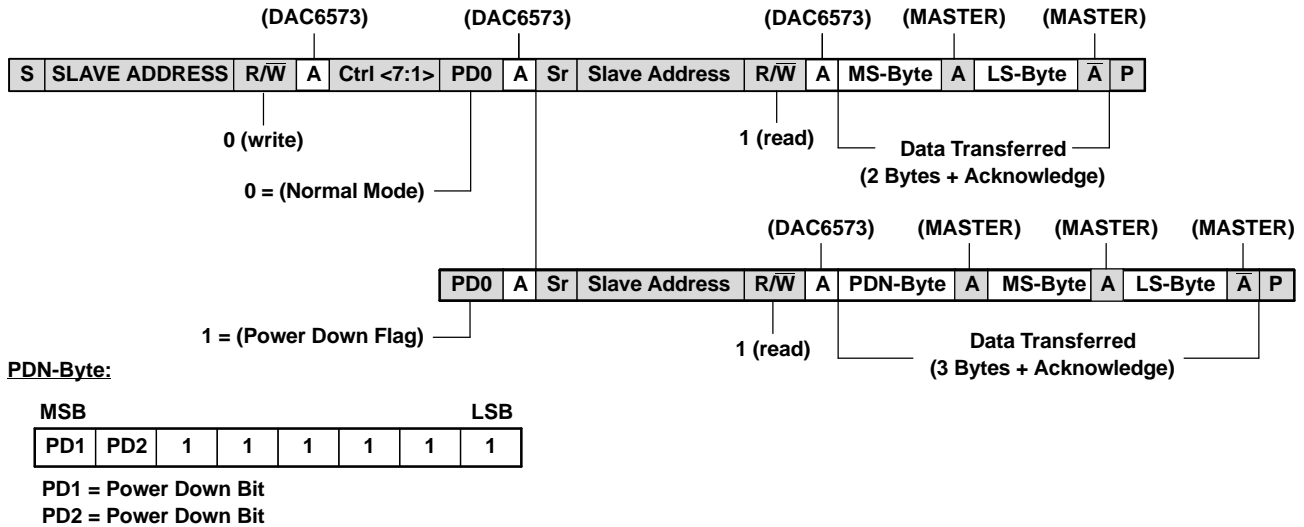


Figure 35. Standard and Fast Mode: Slave Transmitter

### DAC6573 as a Slave Transmitter - High-Speed Mode

Figure 36 shows an  $I^2C$ -Master addressing DAC6573 in high-speed mode (with a 7-bit address), as a *Slave Transmitter*.

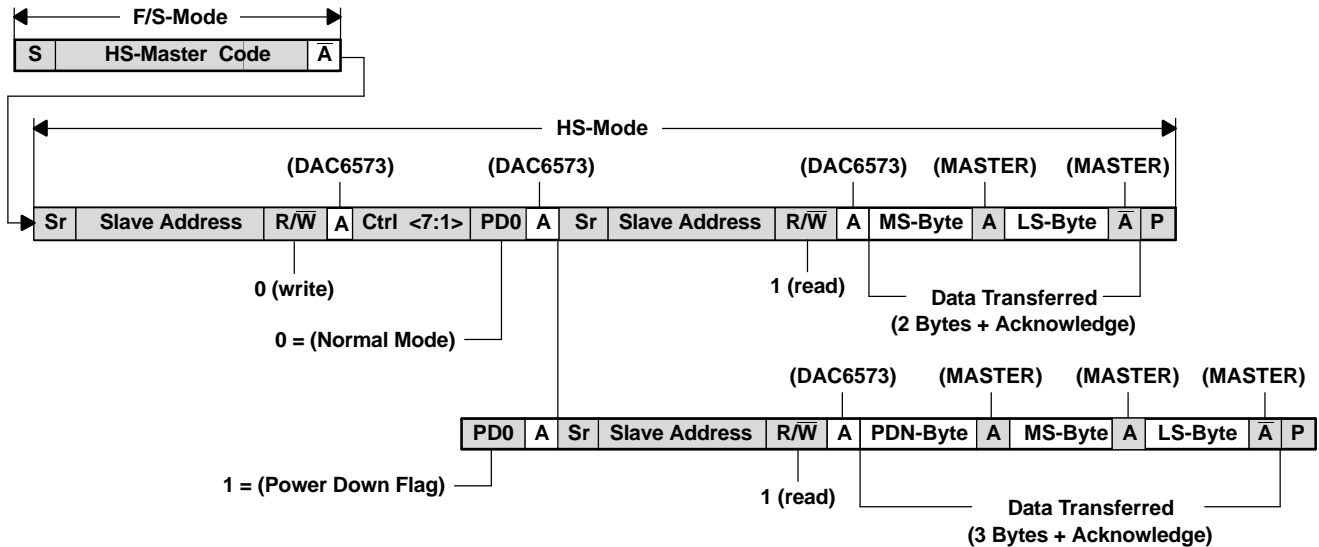


Figure 36. High-Speed Mode: Slave Transmitter

**Master Receiver Reading From a Slave Transmitter (DAC6573) in Standard/Fast Modes**

When reading data back from the DAC6573, the user begins with an address byte (with  $R/\bar{W} = 0$ ) after which the DAC6573 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6573. Following this there is a REPEATED START condition by the master and the address is resent with ( $R/\bar{W} = 1$ ). This is acknowledged by the DAC6573, indicating that it is prepared to transmit data. Two or three bytes of data are then read back from the DAC6573, depending on the (PD0-Bit). The value of *Buff-Sel1* and *Buff-Sel0* determines, which channel data is read back. A STOP Condition follows.

With the (PD0-Bit = 0) the DAC6573 transmits 2 bytes of data, *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 6. Data Readback Mode - 2 bytes).

With the (PD0-Bit = 1) the DAC6573 transmits 3 bytes of data, *POWER-DOWN-BYTE* followed by the *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 6. Data Readback Mode - 3 bytes).

**Table 6. Read Sequence in F/S Mode**

| DATA READBACK MODE - 2 BYTES |                                       |     |        |        |    |            |            |     |                              |
|------------------------------|---------------------------------------|-----|--------|--------|----|------------|------------|-----|------------------------------|
| Transmitter                  | MSB                                   | 6   | 5      | 4      | 3  | 2          | 1          | LSB | Comment                      |
| Master                       | Start                                 |     |        |        |    |            |            |     | Begin sequence               |
| Master                       | 1                                     | 0   | 0      | 1      | 1  | A1         | A0         | R/W | Write addressing (R/W=0)     |
| DAC6573                      | DAC6573 acknowledges                  |     |        |        |    |            |            |     |                              |
| Master                       | A3                                    | A2  | Load 1 | Load 0 | x  | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=0)         |
| DAC6573                      | DAC6573 acknowledges                  |     |        |        |    |            |            |     |                              |
| Master                       | Repeated start                        |     |        |        |    |            |            |     |                              |
| Master                       | 1                                     | 0   | 0      | 1      | 1  | A1         | A0         | R/W | Read addressing (R/W = 1)    |
| DAC6573                      | DAC6573 acknowledges                  |     |        |        |    |            |            |     |                              |
| DAC6573                      | D9                                    | D8  | D7     | D6     | D5 | D4         | D3         | D2  | Reading data word, high byte |
| Master                       | Master acknowledges                   |     |        |        |    |            |            |     |                              |
| DAC6573                      | D1                                    | D0  | x      | x      | x  | x          | x          | x   | Reading data word, low byte  |
| Master                       | Master not acknowledges               |     |        |        |    |            |            |     | Master signal end of read    |
| Master                       | Stop or repeated start <sup>(1)</sup> |     |        |        |    |            |            |     | Done                         |
| DATA READBACK MODE - 3 BYTES |                                       |     |        |        |    |            |            |     |                              |
| Transmitter                  | MSB                                   | 6   | 5      | 4      | 3  | 2          | 1          | LSB | Comment                      |
| Master                       | Start                                 |     |        |        |    |            |            |     | Begin sequence               |
| Master                       | 1                                     | 0   | 0      | 1      | 1  | A1         | A0         | R/W | Write addressing (R/W=0)     |
| DAC6573                      | DAC6573 acknowledges                  |     |        |        |    |            |            |     |                              |
| Master                       | A3                                    | A2  | Load 1 | Load 0 | x  | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=1)         |
| DAC6573                      | DAC6573 acknowledges                  |     |        |        |    |            |            |     |                              |
| Master                       | Repeated start                        |     |        |        |    |            |            |     |                              |
| Master                       | 1                                     | 0   | 0      | 1      | 1  | A1         | A0         | R/W | Read addressing (R/W = 1)    |
| DAC6573                      | DAC6573 acknowledges                  |     |        |        |    |            |            |     |                              |
| DAC6573                      | PD1                                   | PD2 | 1      | 1      | 1  | 1          | 1          | 1   | Read power down byte         |
| Master                       | Master acknowledges                   |     |        |        |    |            |            |     |                              |
| DAC6573                      | D9                                    | D8  | D7     | D6     | D5 | D4         | D3         | D2  | Reading data word, high byte |
| Master                       | Master acknowledges                   |     |        |        |    |            |            |     |                              |
| DAC6573                      | D1                                    | D0  | x      | x      | x  | x          | x          | x   | Reading data word, low byte  |
| Master                       | Master not acknowledges               |     |        |        |    |            |            |     | Master signal end of read    |
| Master                       | Stop or repeated start <sup>(1)</sup> |     |        |        |    |            |            |     | Done                         |

(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

## Master Receiver Reading From a Slave Transmitter (DAC6573) in HS-Mode

When reading data to the DAC6573 in HS-MODE, the master begins to transmit, what is called the *HS-Master Code* (0000 1XXX) in F/S mode. No device is allowed to acknowledge the *HS-Master Code*, so the *HS-Master Code* is followed by a NOT acknowledge.

The master then *switches* to HS-mode and issues a REPEATED START condition, followed by the address byte (with  $R/\overline{W} = 0$ ) after which the DAC6573 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6573.

Then there is a REPEATED START condition initiated by the master and the address is resent with ( $R/\overline{W} = 1$ ). This is acknowledged by the DAC6573, indicating that it is prepared to transmit data. Two or three bytes of data are then read back from the DAC6573, depending on the (PD0-Bit). The value of *Buff-Sel1* and *Buff-Sel0* determines, which channel data is read back. A STOP condition follows.

With the (PD0-Bit = 0) the DAC6573 transmits 2 bytes of data, *HIGH-BYTE* followed by *LOW-BYTE* (refer to Table 7 HS-Mode Readback Sequence).

With the (PD0-Bit = 1) the DAC6573 transmits 3 bytes of data, *POWER-DOWN-BYTE* followed by the *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 7 HS-Mode Readback Sequence).

**Table 7. Master Receiver Reading Slave Transmitter (DAC6573) in HS-Mode**

| HS MODE READBACK SEQUENCE |                         |     |        |        |    |            |            |                  |  |
|---------------------------|-------------------------|-----|--------|--------|----|------------|------------|------------------|--|
| Transmitter               | MSB                     | 6   | 5      | 4      | 3  | 2          | 1          | LSB              | Comment                                  |
| Master                    | Start                   |     |        |        |    |            |            |                  | Begin sequence                           |
| Master                    | 0                       | 0   | 0      | 0      | 1  | X          | X          | X                | HS mode master code                      |
| NONE                      | Not acknowledge         |     |        |        |    |            |            |                  | No device may acknowledge HS master code |
| Master                    | Repeated start          |     |        |        |    |            |            |                  |  |
| Master                    | 1                       | 0   | 0      | 1      | 1  | A1         | A0         | $R/\overline{W}$ | Write addressing ( $R/\overline{W}=0$ )  |
| DAC6573                   | DAC6573 acknowledges    |     |        |        |    |            |            |                  |  |
| Master                    | A3                      | A2  | Load 1 | Load 0 | X  | Buff Sel 1 | Buff Sel 0 | PD0              | Control byte (PD0 = 1)                   |
| DAC6573                   | DAC6573 acknowledges    |     |        |        |    |            |            |                  |  |
| Master                    | Repeated start          |     |        |        |    |            |            |                  |  |
| Master                    | 1                       | 0   | 0      | 1      | 1  | A1         | A0         | $R/\overline{W}$ | Read addressing ( $R/\overline{W}=1$ )   |
| DAC6573                   | DAC6573 acknowledges    |     |        |        |    |            |            |                  |  |
| DAC6573                   | PD1                     | PD2 | 1      | 1      | 1  | 1          | 1          | 1                | Power-down byte                          |
| Master                    | Master acknowledges     |     |        |        |    |            |            |                  |  |
| DAC6573                   | D9                      | D8  | D7     | D6     | D5 | D4         | D3         | D2               | Reading data word, high byte             |
| Master                    | Master acknowledges     |     |        |        |    |            |            |                  |  |
| DAC6573                   | D1                      | D0  | x      | x      | x  | x          | x          | x                | Reading data word, low byte              |
| Master                    | Master not acknowledges |     |        |        |    |            |            |                  | Master signal end of read                |
| Master                    | Stop or repeated start  |     |        |        |    |            |            |                  | Done                                     |

## Power-On Reset

The DAC6573 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC register is filled with zeros and the output voltage is 0 V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. Device pins must not be brought high before supply is applied.

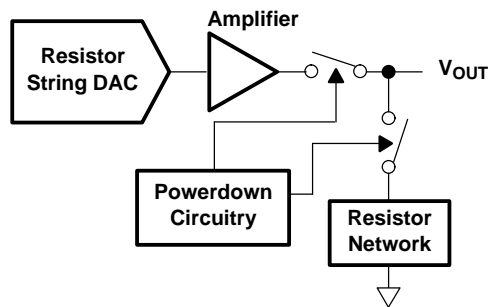
## Power-Down Modes

The DAC6573 contains four separate power-down modes of operation. The modes are programmable via two most significant bits of the MSB byte, while ( $CTRL[0] = PD0 = 1$ ). Table 8 shows how the state of these bits corresponds to the mode of operation of the device.

**Table 8. Power-Down Modes of Operation for the DAC6573**

| CTRL[0] | MSB[7] | MSB[6] | OPERATING MODE                 |
|---------|--------|--------|--------------------------------|
| 1       | 0      | 0      | PWD, high impedance DAC output |
| 1       | 0      | 1      | PWD, 1 kΩ to GND DAC output    |
| 1       | 1      | 0      | PWD, 100 kΩ to GND DAC output  |
| 1       | 1      | 1      | PWD, high impedance DAC output |

When (CTRL[0] = PD0 = 0), the device works normally with its normal power consumption of 150 μA at 5 V per channel. However, for the power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but also the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while in power-down mode. There are three different options: The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor or left open-circuit (high impedance). The output stage is illustrated in Figure 37.



**Figure 37. Output Stage During Power Down**

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power down is typically 2.5 μs for V<sub>DD</sub> = 5 V and 5 μs for V<sub>DD</sub> = 3 V. (See the Typical Curves section for additional information.)

The DAC6573 offers a flexible power-down interface based on channel register operation. A channel consists of a single 10-bit DAC with power-down circuitry, a temporary storage register (TR) and a DAC register (DR). TR and DR are both 12 bits wide. Two MSBs represent the power-down condition and the 10 LSBs represent data for TR and DR. By using bits 11 and 10 of TR and DR, a power-down condition can be temporarily stored and used just like data. Internal circuits ensure that MSB[7] and MSB[6] get transferred to TR[11] and TR[10] (DR[11] and DR[10]) when the power-down flag (CTRL[0] = PD0) is set. Therefore, DAC6573 treats power-down conditions like data and all the operational modes are still valid for power down. It is possible to broadcast a power-down condition to all the DAC6573s in the system, or it is possible to simultaneously power down a channel while updating data on other channels.

**CURRENT CONSUMPTION**

The DAC6573 typically consumes 150 μA at V<sub>DD</sub> = 5 V and 125 μA at V<sub>DD</sub> = 3 V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if V<sub>IH</sub> << V<sub>DD</sub>. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC. In power-down mode, typical current consumption is 200 nA.



## **IOV<sub>DD</sub> AND VOLTAGE TRANSLATORS**

IOV<sub>DD</sub> pin powers the digital input structures of the DAC6573. For single-supply operation, IOV<sub>DD</sub> can be tied to V<sub>DD</sub>. For dual-supply operation, the IOV<sub>DD</sub> pin provides interface flexibility with various CMOS logic families—connect it to the logic supply of the system. Analog circuits and internal logic of the DAC6573 use V<sub>DD</sub> as the supply voltage. The external logic high inputs get translated to V<sub>DD</sub> by level shifters. These level shifters use the IOV<sub>DD</sub> voltage as a reference to shift the incoming logic HIGH levels to V<sub>DD</sub>. IOV<sub>DD</sub> operates from 2.7 V to 5.5 V regardless of the V<sub>DD</sub> voltage, ensuring compatibility with various logic families. Although specified down to 2.7 V, IOV<sub>DD</sub> operates as low as 1.8 V with degraded timing and temperature performance. For lowest power consumption, ensure that logic V<sub>IH</sub> levels are as close as possible to IOV<sub>DD</sub>, and logic V<sub>IL</sub> levels as close as possible to GND voltages.

## **DRIVING RESISTIVE AND CAPACITIVE LOADS**

The DAC6573 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC6573 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2 k $\Omega$  can be driven by the DAC6573 while achieving a good load regulation. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20 mV of the DAC's digital input-to-voltage output transfer characteristic. The reference voltage applied to the DAC6573 may be reduced below the supply voltage applied to V<sub>DD</sub> in order to eliminate this condition if good linearity is a requirement at full scale (under resistive loading conditions).

## **CROSSTALK**

The DAC6573 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.01 LSBs. The ac crosstalk measured (for a full-scale, 1-kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under -100 dB.

## **OUTPUT VOLTAGE STABILITY**

The DAC6573 exhibits excellent temperature stability of  $\pm 3$  ppm/ $^{\circ}\text{C}$  typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a  $\pm 25$ - $\mu\text{V}$  window for a  $\pm 1^{\circ}\text{C}$  ambient temperature change. Combined with good dc noise performance and true 10-Bit differential linearity, the DAC6573 becomes a perfect choice for closed-loop control applications.

## **SETTLING TIME AND OUTPUT GLITCH PERFORMANCE**

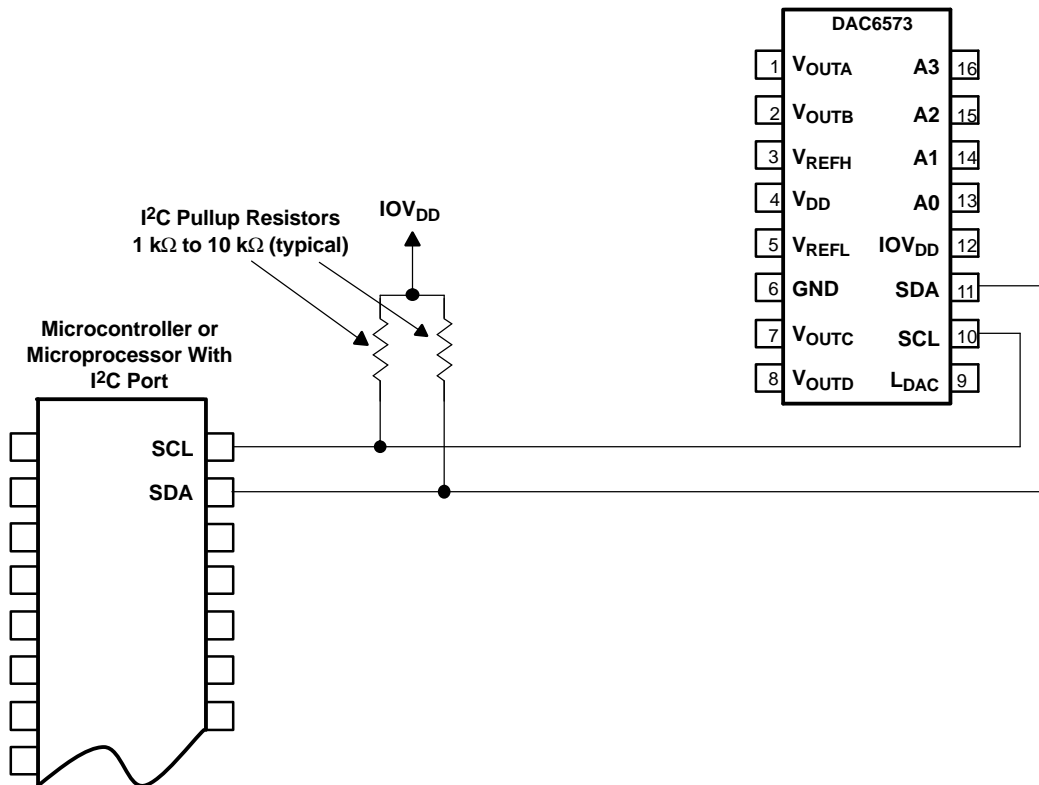
Settling time to within the 10-bit accurate range of the DAC6573 is achievable within 7  $\mu\text{s}$  for a full-scale code change at the input. Worst case settling times between consecutive code changes is typically less than 2  $\mu\text{s}$ . The high-speed serial interface of the DAC6573 is designed in order to support up to 188-kSPS update rate. For full-scale output swings, the output stage of each DAC6573 channel typically exhibits less than 100 mV of overshoot and undershoot when driving a 200 pF capacitive load. Code-to-code change glitches are extremely low ( $\sim 10$   $\mu\text{V}$ ) given that the code-to-code transition does not cross an Nx64 code boundary. Due to internal segmentation of the DAC6573, code-to-code glitches occur at each crossing of an Nx64 code boundary. These glitches can approach 100 mVs for N = 15, but settle out within  $\sim 2$   $\mu\text{s}$ .

## APPLICATION INFORMATION

The following sections give example circuits and tips for using the DAC6573 in various applications. For more information, contact your local TI representative, or visit the Texas Instruments website at <http://www.ti.com>.

### BASIC CONNECTIONS

For many applications, connecting the DAC6573 is extremely simple. A basic connection diagram for the DAC6573 is shown in Figure 38. The 0.1  $\mu\text{F}$  bypass capacitors provide the momentary bursts of extra current needed from the supplies.



NOTE: DAC6573 power and input/output connections are omitted for clarity, except I<sup>2</sup>C Inputs.

**Figure 38. Typical DAC6573 Connections**

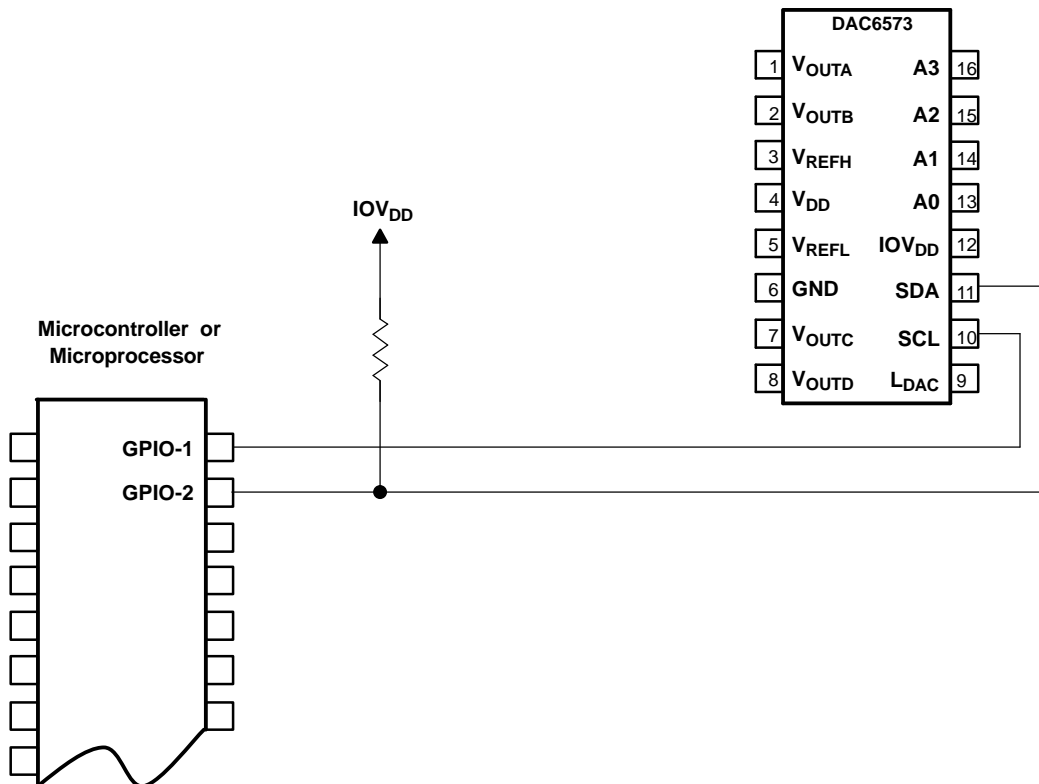
The DAC6573 interfaces directly to standard mode, fast mode and high-speed mode I<sup>2</sup>C controllers. Any microcontroller's I<sup>2</sup>C peripheral, including master-only and non-multiple-master I<sup>2</sup>C peripherals, work with the DAC6573. The DAC6573 does not perform clock-stretching (i.e., it never pulls the clock line low), so it is not necessary to provide for this unless other devices are on the same I<sup>2</sup>C bus.

Pullup resistors are necessary on both the SDA and SCL lines because I<sup>2</sup>C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance on the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. If the pullup resistors are too small the bus drivers may not be able to pull the bus line low.

### USING GPIO PORTS FOR I<sup>2</sup>C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I<sup>2</sup>C controller is not available, the DAC6573 can be connected to GPIO pins, and the I<sup>2</sup>C bus protocol simulated, or bit-banged, in software. An example of this for a single DAC6573 is shown in Figure 39.

**APPLICATION INFORMATION (continued)**



NOTE: DAC6573 power and input/output connections are omitted for clarity, except I<sup>2</sup>C inputs.

**Figure 39. Using GPIO With a Single DAC6573**

Bit-banging I<sup>2</sup>C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output a zero; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this reads as a zero in the port's input register.

Note that no pullup resistor is shown on the SCL line. In this simple case the resistor is not needed. The microcontroller can simply leave the line on output, and set it to one or zero as appropriate. It can do this because the DAC6573 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption due to the absence of a resistive pullup.

If there are any devices on the bus that may drive their clock lines low, do not use the above method. The SCL line must be high-Z or zero, and a pullup resistor must be provided as usual. Note also that this cannot be done on the SDA line in any case, because the DAC6573 drives the SDA line low from time to time, as all I<sup>2</sup>C devices do.

Some microcontrollers have selectable strong pullup circuits built in to their GPIO ports. In some cases, these can be switched on and used in place of an external pullup resistor. Weak pullups are also provided on some microcontrollers, but usually these are too weak for I<sup>2</sup>C communication. Test any circuit before committing it to production.

**USING REF02 AS A POWER SUPPLY FOR DAC6573**

Due to the extremely low supply current required by the DAC6573, a possible configuration is to use a REF02 +5-V precision voltage reference to supply the required voltage to the DAC6573 supply input as well as the reference input, as shown in Figure 40. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 outputs a steady supply voltage for the DAC6573. If the REF02 is used, the current it needs to supply to the DAC6573 is 600 μA typical and 900 μA max for

## APPLICATION INFORMATION (continued)

$V_{DD} = 5\text{ V}$ . When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5-k $\Omega$  load on a single DAC output) is:

$$600\ \mu\text{A} + (5\text{ V} / 5\text{ k}\Omega) = 1.6\text{ mA}$$

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 400  $\mu\text{V}$  for 1.6 mA of current drawn from it. This corresponds to a 0.08 LSB error for a 0 V to 5 V output range.

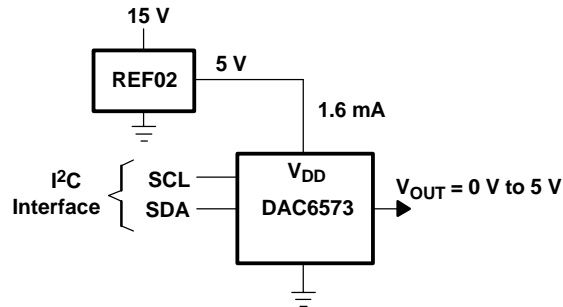


Figure 40. REF02 Power Supply

## LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

For best performance, the power applied to  $V_{DD}$  must be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection,  $V_{DD}$  must be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1- $\mu\text{F}$  to 10- $\mu\text{F}$  capacitor in parallel with a 0.1- $\mu\text{F}$  bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100  $\mu\text{F}$  electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the  $\pm 5\text{-V}$  supply, removing the high-frequency noise.

**PACKAGING INFORMATION**

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DAC6573IPW</a>  | Active        | Production           | TSSOP (PW)   16 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | D6573I              |
| DAC6573IPW.B                | Active        | Production           | TSSOP (PW)   16 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | D6573I              |
| <a href="#">DAC6573IPWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | D6573I              |
| DAC6573IPWR.B               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | D6573I              |
| DAC6573IPWRG4               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | D6573I              |
| DAC6573IPWRG4.B             | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | D6573I              |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC6573IPWR   | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| DAC6573IPWRG4 | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

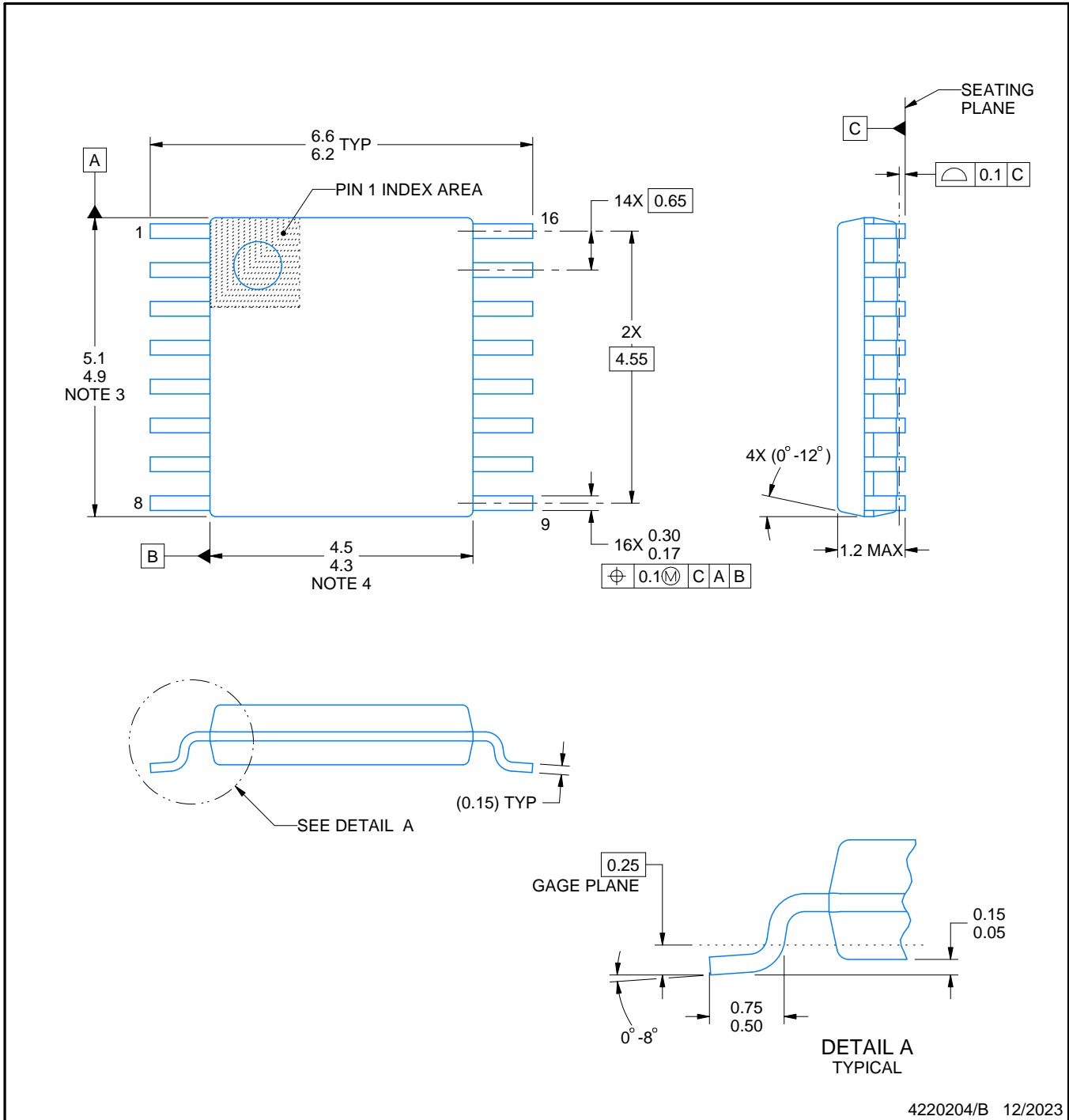
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC6573IPWR   | TSSOP        | PW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| DAC6573IPWRG4 | TSSOP        | PW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |



**TUBE**


\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DAC6573IPW   | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |
| DAC6573IPW.B | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

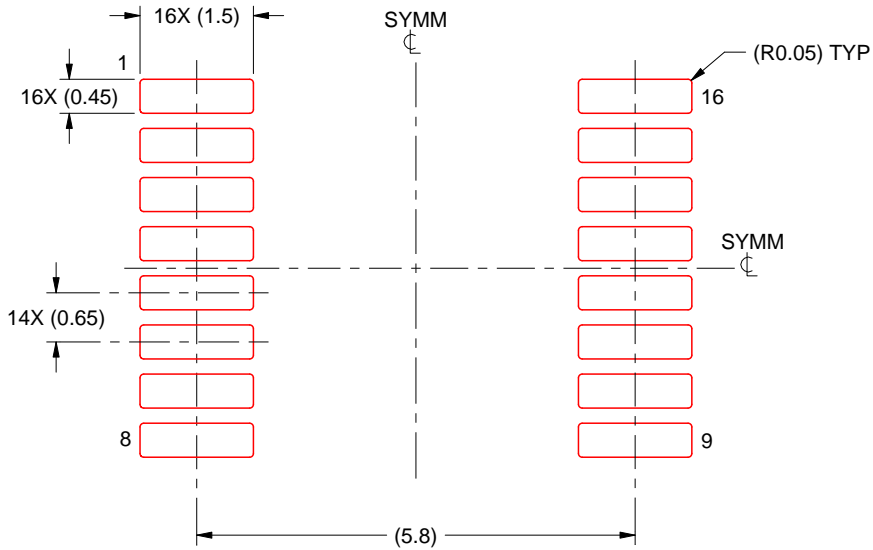
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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