DLP3940S-Q1 0.39-Inch 1080p FHD Digital Micromirror Device for Automotive Display Applications

1 Features

- Qualified for automotive applications –
  - –40°C to 105°C operating DMD array temperature range
- Functional Safety Quality-Managed
  - Documentation available to aid ISO 26262 functional safety system design up to ASIL-B
- The DLP3940S-Q1 automotive chipset includes:
  - DLP3940S-Q1 DMD
  - DLPC231S-Q1 DMD controller
  - TPS99002S-Q1 system management and illumination controller
- 0.39-inch diagonal micromirror array
  - 1080p FHD (1920 × 1080) display resolution at 120Hz
  - 4.5µm micromirror pitch
  - ±14.5° micromirror tilt (relative to flat surface)
  - Side illumination
  - Compatible with LED or laser illumination
- Up to 600MHz SubLVDS DMD interface for low power and emission
- 10kHz DMD refresh rate over temperature extremes
- Built-in self-test (BIST) of DMD memory cells

2 Applications

- Wide field of view and augmented reality head-up display (HUD)
- Digital cluster, navigation, and infotainment windshield displays

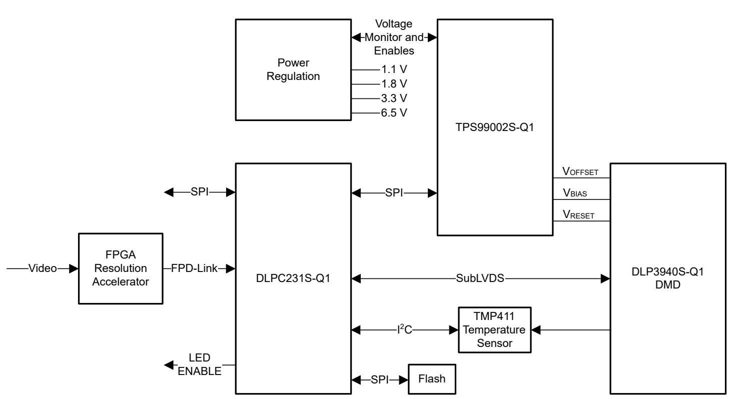
3 Description

The DLP3940S-Q1 digital micromirror device (DMD) is a digitally controlled micro-electro-mechanical system (MEMS) spatial light modulator (SLM) that enables bright 1080p FHD to achieve high-performance, high-resolution augmented reality head-up display (HUD). The 16:9 aspect ratio supports very wide aspect ratio designs, and the high resolution enables retinal limited displays to be achieved in HUD applications. The DLP3940S-Q1 offers a balance of optical throughput and resolution, enabling a wide field of view and a large driver eye box for enhanced user experience. This chipset, coupled with LEDs or lasers and an optical system, enables deep, saturated colors of 125% NTSC, high brightness of more than 15,000cd/m^2, high dynamic dimming ratio of more than 5000:1, and high solar load tolerance. The DLP3940S-Q1 automotive DMD micromirror array is configured for side illumination, which enables highly efficient and more compact optical engine designs. The DLP3940S-Q1 device is available in a panel package for optimized system cost. The package has low thermal resistance to the DMD array to enable efficient thermal solutions.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
DLP3940S-Q1	FSC (154)	18.35mm × 9.60mm

(1) For more information, see the addendum at the end of the data sheet.



Simplified Application

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4 Pin Configuration and Functions

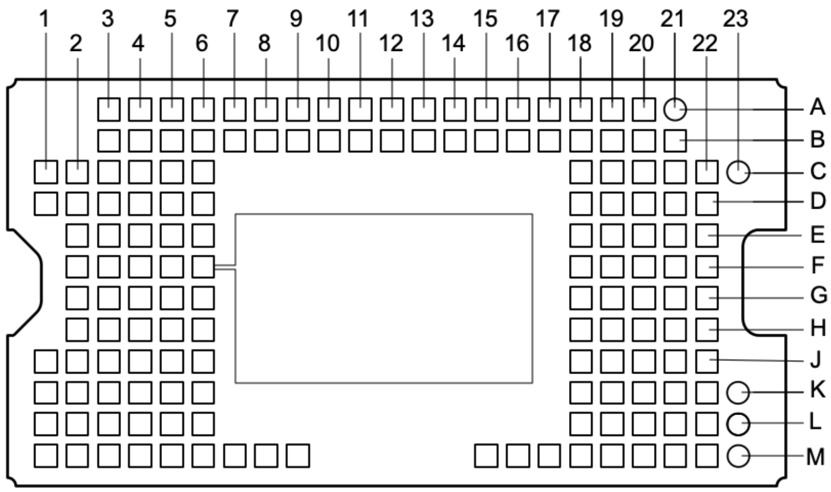

Figure 4-1. FSC Package 154-Pin LGA (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_CP(0)	G2	I	High-speed Differential Data Pair lane C0	Differential 100 Ω	1.052
D_CN(0)	G3	I	High-speed Differential Data Pair lane C0	Differential 100 Ω	1.112
D_CP(1)	M7	I	High-speed Differential Data Pair lane C1	Differential 100 Ω	6.519
D_CN(1)	M8	I	High-speed Differential Data Pair lane C1	Differential 100 Ω	6.611
D_CP(2)	H2	I	High-speed Differential Data Pair lane C2	Differential 100 Ω	0.921
D_CN(2)	H3	I	High-speed Differential Data Pair lane C2	Differential 100 Ω	1.376
D_CP(3)	M5	I	High-speed Differential Data Pair lane C3	Differential 100 Ω	5.196
D_CN(3)	M6	I	High-speed Differential Data Pair lane C3	Differential 100 Ω	5.318
D_CP(4)	K3	I	High-speed Differential Data Pair lane C4	Differential 100 Ω	1.579
D_CN(4)	K4	I	High-speed Differential Data Pair lane C4	Differential 100 Ω	1.648
D_CP(5)	M3	I	High-speed Differential Data Pair lane C5	Differential 100 Ω	3.414
D_CN(5)	M4	I	High-speed Differential Data Pair lane C5	Differential 100 Ω	3.857
D_CP(6)	L4	I	High-speed Differential Data Pair lane C6	Differential 100 Ω	2.460
D_CN(6)	L5	I	High-speed Differential Data Pair lane C6	Differential 100 Ω	2.566
D_CP(7)	K1	I	High-speed Differential Data Pair lane C7	Differential 100 Ω	1.114
D_CN(7)	L1	I	High-speed Differential Data Pair lane C7	Differential 100 Ω	1.707
DCLK_CP	K5	I	High-speed Differential Clock C	Differential 100 Ω	3.744
DCLK_CN	K6	I	High-speed Differential Clock C	Differential 100 Ω	3.883
D_DP(0)	J19	I	High-speed Differential Data Pair lane D0	Differential 100 Ω	4.189
D_DN(0)	J18	I	High-speed Differential Data Pair lane D0	Differential 100 Ω	4.435
D_DP(1)	M18	I	High-speed Differential Data Pair lane D1	Differential 100 Ω	6.588
D_DN(1)	M17	I	High-speed Differential Data Pair lane D1	Differential 100 Ω	6.867
D_DP(2)	H21	I	High-speed Differential Data Pair lane D2	Differential 100 Ω	1.754
D_DN(2)	H20	I	High-speed Differential Data Pair lane D2	Differential 100 Ω	1.936
D_DP(3)	J22	I	High-speed Differential Data Pair lane D3	Differential 100 Ω	1.339

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Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_DN(3)	J21	I	High-speed Differential Data Pair lane D3	Differential 100 Ω	1.634
D_DP(4)	L20	I	High-speed Differential Data Pair lane D4	Differential 100 Ω	3.329
D_DN(4)	L19	I	High-speed Differential Data Pair lane D4	Differential 100 Ω	3.436
D_DP(5)	M20	I	High-speed Differential Data Pair lane D5	Differential 100 Ω	3.631
D_DN(5)	M19	I	High-speed Differential Data Pair lane D5	Differential 100 Ω	3.738
D_DP(6)	M22	I	High-speed Differential Data Pair lane D6	Differential 100 Ω	2.420
D_DN(6)	M21	I	High-speed Differential Data Pair lane D6	Differential 100 Ω	2.573
D_DP(7)	K22	I	High-speed Differential Data Pair lane D7	Differential 100 Ω	1.406
D_DN(7)	K21	I	High-speed Differential Data Pair lane D7	Differential 100 Ω	1.881
DCLK_DP	K19	I	High-speed Differential Clock D	Differential 100 Ω	3.916
DCLK_DN	K18	I	High-speed Differential Clock D	Differential 100 Ω	4.022
TEMP_N	M2	I	Temp Diode N		1.133
TEMP_P	M1	I	Temp Diode P		1.237
LS_RDATA_D	B5	O	Low-speed Output		2.396
LS_RDATA_C	A4	O	Low-speed Output		2.255
LS_RDATA_B	A5	O	Low-speed Output		2.925
LS_RDATA_A	A3	O	Low-speed Output		2.045
LS_WDATA_N	B7	I	Low-speed Differential Input N		5.297
LS_WDATA_P	A7	I	Low-speed Differential Input P		5.253
LS_CLK_N	A8	I	Low-speed Differential Clock Input N		7.225
LS_CLK_P	A9	I	Low-speed Differential Clock Input P		6.962
DMD_DEN_ARSTZ	D1	I	Asynchronous Reset Active Low. Logic High Enables DMD	17.5kΩ pulldown	0.735
VDD	A6, A10, A12, A14, A16, A18, B4, B11, B13, B15, B19, B21, C21, D22, E21, G4, J1, J4, J6, L2, M15	P	Digital Core Supply Voltage		Plane
VBIAS	A20, B6	P	Supply Voltage for Positive Bias of Micromirror reset signal		Plane
VRESET	B8, B17	P	Supply Voltage for Negative Bias of Micromirror reset signal		Plane
VOFFSET	B9, M16	P	Supply voltage for HVCMOS logic, stepped up logic level		Plane
VDDI	C22, E4, F2, G20, J2, L22	P	Supply voltage for SubLVDS receivers		Plane

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
VSS	A11, A13, A15, A17, A19, B3, B10, B12, B14, B16, B18, B20,C1, C6, D4, D19, E22, F3, F6, G19, H4, H19, H22, J3, J5, J20, K2, K20,L3, L6, L18, L21, M9	G	Ground		Plane
N/C	A21, C18, C19, C2, C20, C23, C3, C4, C5, D18, D2, D20, D21, D3, D5, D6, E18, E19, E2, E20, E3, E5, E6, F18, F19, F20, F21, F22, F4, F5, G18, G21, G22, G5, G6, H18, H5, H6, K23, L23, M23	NC	No Connect Pin		N/A

(1) I=Input, O=Output, P=Power, G=Ground, NC=No Connect

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5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, and performance, and shorten the device's lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic and low speed interface (LSIF)[(1)]	-0.5	2.3	V
V_{DDI}	Supply voltage for SubLVDS receivers[(1)]	-0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[(1) (2)]	-0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode[(1)]	-0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode[(1)]	-15	0.5	V
$\| V_{DDI} - V_{DD} \|$	Supply voltage delta, absolute value[(3)]		0.3	V
$\| V_{BIAS} - V_{OFFSET} \|$	Supply voltage delta, absolute value[(4)]		11	V
$\| V_{BIAS} - V_{RESET} \|$	Supply voltage delta, absolute value[(5)]		34	V
INPUT VOLTAGE				
	Input voltage for other inputs -- LSIF and LVCMOS	-0.5	V_{DD} + 0.5	V
	Input voltage for other inputs -- SubLVDS[(1) (6)]	-0.5	V_{DDI} + 0.5	V
SUBLVDS INTERFACE				
$\| V_{ID} \|$	SubLVDS input differential voltage (absolute value)[(6)]		810	mV
I_{ID}	SubLVDS input differential current		10	mA
CLOCK FREQUENCY				
f_{clock}	Clock frequency for low speed interface LS_CLK	100	130	MHz
TEMPERATURE DIODE				
I_{TEMP_DIODE}	Max current source into temperature diode		120	µA
ENVIRONMENTAL[(8)]				
T_{ARRAY}	Temperature, operating[(7)]	-40	105	°C
T_{ARRAY}	Temperature, non-operating[(7)]	-40	125	°C

(1) All voltage values are concerning the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw and permanent damage to the device.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw and permanent damage to the device.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw and permanent damage to the device.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage to the internal termination resistors may result.
(7) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), as shown in Figure 6-5 using the Micromirror Array Temperature Calculation.
(8) Refer to the *Reliability Lifetime Estimates for RDP DMDs in Automotive Applications* Application Report (DLPA146) for reliability data for the digital micromirror device (DMD) when operated at high temperature.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD temperature	-40	125	°C

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM)[1]	±1000	V
		Charged device model (CDM)[2]	±250	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted).

		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE RANGE					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface (1) (2)	1.71	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers (1) (2)	1.71	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (1) (2) (3)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode (1) (2)	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode (1) (2)	–14.5	–14	–13.5	V
$\| V_{DDI}$ - VDD $\|$	Supply voltage delta (absolute value) (1) (2) (4)			0.3	V
$\| V_{BIAS}-V_{OFFSET} \|$	Supply voltage delta (absolute value) (1) (2) (5)			10.5	V
$\| V_{BIAS} - V_{RESET} \|$	Supply voltage delta (absolute value) (1) (2) (6)			33	V
LPSDR INTERFACE					
V_{IH}	High-level input voltage	0.7 x V_{DD}			V
V_{IL}	Low-level input voltage			0.3 x V_{DD}	V
V_{IH}(AC)	AC input high voltage	0.8 × V_{DD}		V_{DD} + 0.3	V
V_{IL}(AC)	AC input low voltage	–0.3		0.2 × V_{DD}	V
V_{Hyst}	Input Hysteresis	0.1 × V_{DD}		0.4 × V_{DD}	V
f_{max_LS}	Clock frequency for low speed interface LS_CLK (7)	108	120	130	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK) (7)	44		56	%
SUBLVDS INTERFACE					
f_{max_HS}	Clock frequency for high-speed interface DCLK (8)		600	720	MHz
DCD_{IN}	LVDS duty cycle distortion (DCLK)	48		52	%
$\| V_{ID} \|$	LVDS differential input voltage magnitude (8)	150	250	350	mV
V_{CM}	Common mode voltage (8)	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage (8)	525		1275	mV
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
TEMPERATURE DIODE					
I_{TEMP_DIODE}	Max current source into Temperature Diode			120	µA
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operation (9) (10) (11)	-40		105	°C
Q_{AP-ILL}	Window aperture illumination overfill (12) (13) (14)			80	mW/mm^2
ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410 nm (9) (15)			10	mW/cm^2

(1) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) All voltage values are concerning the ground pins (V_{SS}).
(3) V_{OFFSET} supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(7) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(8) Refer to the SubLVDS timing requirements in Timing Requirements.
(9) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination reduces the device's lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at the test point (TP1) shown in Figure 6-5 and the package thermal resistance using the Micromirror Array Temperature Calculation.
(11) Long-term is defined as the usable life of the device.
(12) Applies to region defined in Figure 5-1.
(13) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly for normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area

outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Minimizing the light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system the amount of overfill light on the outside of the active array may cause system performance degradation.

(14) To calculate, see Window Aperture Illumination Overfill Calculation.
(15) To calculate, see Micromirror Power Density Calculation.

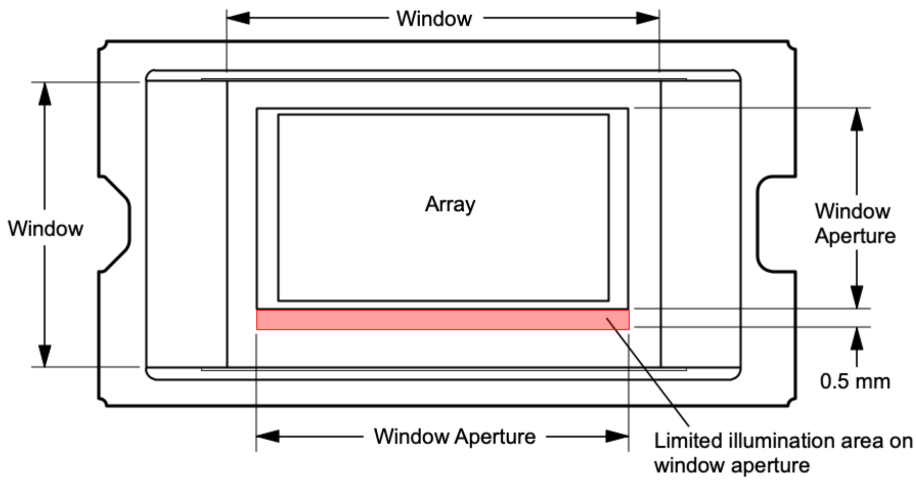

Figure 5-1. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

THERMAL METRIC		DLP3940S-Q1 FSC 154 PIN	UNIT
Thermal resistance	Active area-to-test point 1 (TP1)(1)	2.6	°C/W
	Active area-to-temperature sense diode(1)	0.1	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the Recommended Operating Conditions. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window's clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

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5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER (6)		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD} (3) (4)	Typical			140	mA
I_{DDI}	Supply current: V_{DDI} (3) (4)	Typical			45	mA
I_{OFFSET}	Supply current: V_{OFFSET} (5)	Typical			6	mA
I_{BIAS}	Supply current: V_{BIAS} (5)	Typical			0.6	mA
I_{RESET}	Supply current: V_{RESET}	Typical			1.8	mA
POWER						
P_{DD}	Supply power dissipation: V_{DD} (3) (4)	Typical			252	mW
P_{DDI}	Supply power dissipation: V_{DDI} (3) (4)	Typical			81	mW
P_{OFFSET}	Supply power dissipation: V_{OFFSET} (5)	Typical			60	mW
P_{BIAS}	Supply power dissipation: V_{BIAS} (5)	Typical			1.08	mW
P_{RESET}	Supply power dissipation: V_{RESET}	Typical			25.2	mW
P_{TOTAL}	Supply power dissipation Total	Typical			419.28	mW
LPSDR INPUT						
I_{IL}	Low level input current	V_{DD} = 1.95V, V_I = 0V	-100			nA
I_{IH}	High level input current	V_{DD} = 1.95V, V_I = 1.95V			135	uA
LPSDR OUTPUT						
V_{OH}	DC output high voltage (7) (8) (9)	I_{OH} = -2 mA	0.8 x V_{DD}			V
V_{OL}	DC output low voltage (7) (8) (9)	I_{OL} = 2 mA			0.2 x V_{DD}	V
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	F = 1 MHz			10	pF
C_{IN}	Input capacitance SubLVDS	F = 1 MHz			20	pF
C_{OUT}	Output capacitance	F = 1 MHz			10	pF
C_{TEMP}	Temperature sense diode capacitance	F = 1 MHz			20	pF

(1) Device electrical characteristics are over Section 5.4 unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta | V_{DDI} – V_{DD} | must be less than the specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than the specified limit.
(6) All power supply connections are required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(7) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(8) The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209-2F, Low-Power Double Data Rate (LPDDR) JESD209-2F.
(9) LPSDR output specification is for pins LS_RDATA_A, LS_RDATA_B, LS_RDATA_C, and LS_RDATA_D.

5.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output. (1)	C_L = 15pF			15	ns
	Slew rate, LS_RDATA		0.3			V/ns
	Output duty cycle distortion, LS_RDATA		40		60	%

(1) Device electrical characteristics are over Section 5.4 unless otherwise noted.

5.8 Timing Requirements

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
LVCMOS						
LPSDR						
t_r	Rise slew rate (2)	(20% to 80%) × VDD(6)	0.25			V/ns
t_f	Fall slew rate (2)	(80% to 20%) × VDD(6)	0.25			V/ns
t_r	Rise slew rate (1)	(30% to 80%) × VDD(6)	1		3	V/ns
t_f	Fall slew rate (1)	(70% to 20%) × VDD(6)	1		3	V/ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points(5)	4.2			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points(5)	4.2			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK(5)			1.5	ns
t_h	Hold time	LS_WDATA valid after LS_CLK(5)			1.5	ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points(7)	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points(7)	0.7	1		V/ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points(8)	0.7			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points(8)	0.7			ns
t_{WINDOW}	Window time (1) (3)	Setup time + Hold time(5)	0.25			ns
t_{su}	Setup time	HS_DATA valid before HS_CLK(8)			0.17	ns
t_h	Hold time	HS_DATA valid after HS_CLK(8)			0.17	ns
t_{POWER}	Power-up receiver(4)				200	ns

(1) The specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 5-3.
(2) The specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise and fall slew rate in Figure 5-3.
(3) Window time derating example: 0.5V/ns slew rate increases the window time by 0.7ns, from 3ns to 3.7ns. See Figure 5-5.
(4) The specification is for the SubLVDS receiver time only and does not take into account commanding and latency after commanding.
(5) See Figure 5-2.
(6) See Figure 5-3.
(7) See Figure 5-4.
(8) See Figure 5-6.

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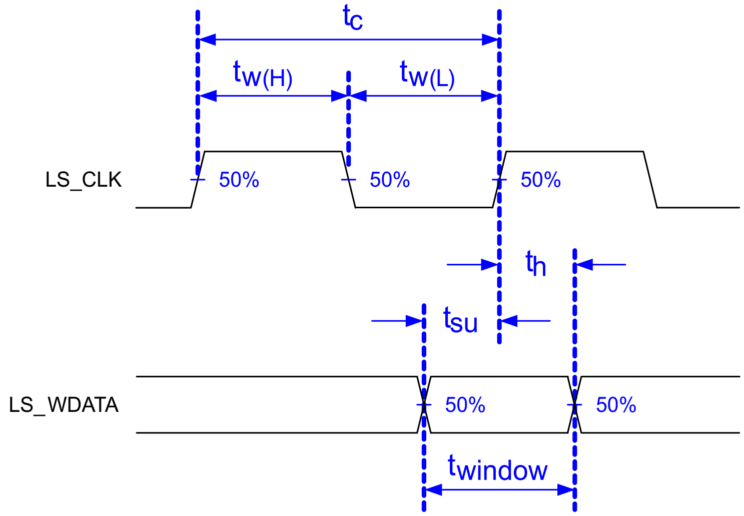

The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209-2F, *Low Power Double Data Rate (LPDDR)* JESD209-2F.

Figure 5-2. LPSDR Switching Parameters

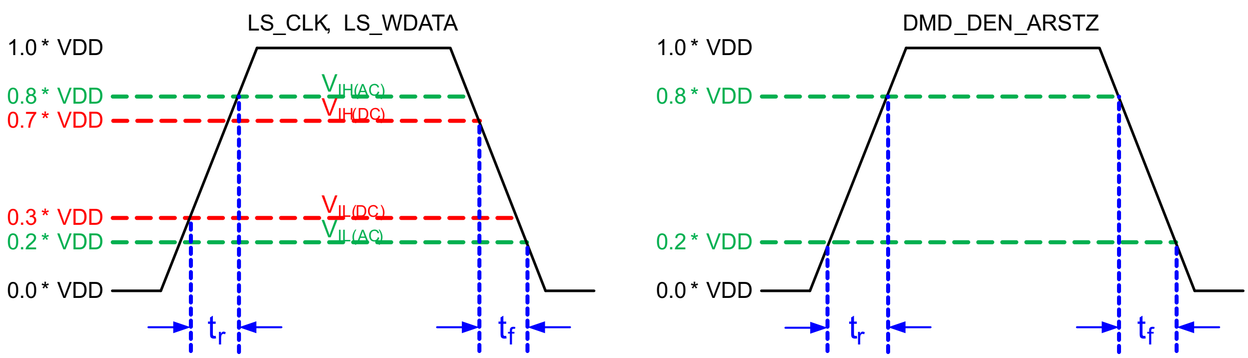

Figure 5-3. LPSDR Input Rise and Fall Slew Rate

Not to Scale

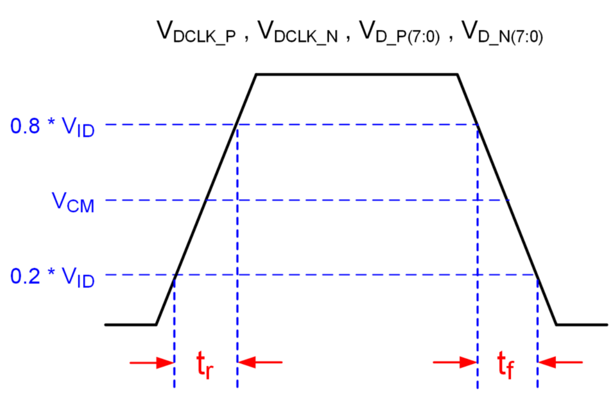

Figure 5-4. SubLVDS Input Rise and Fall Slew Rate

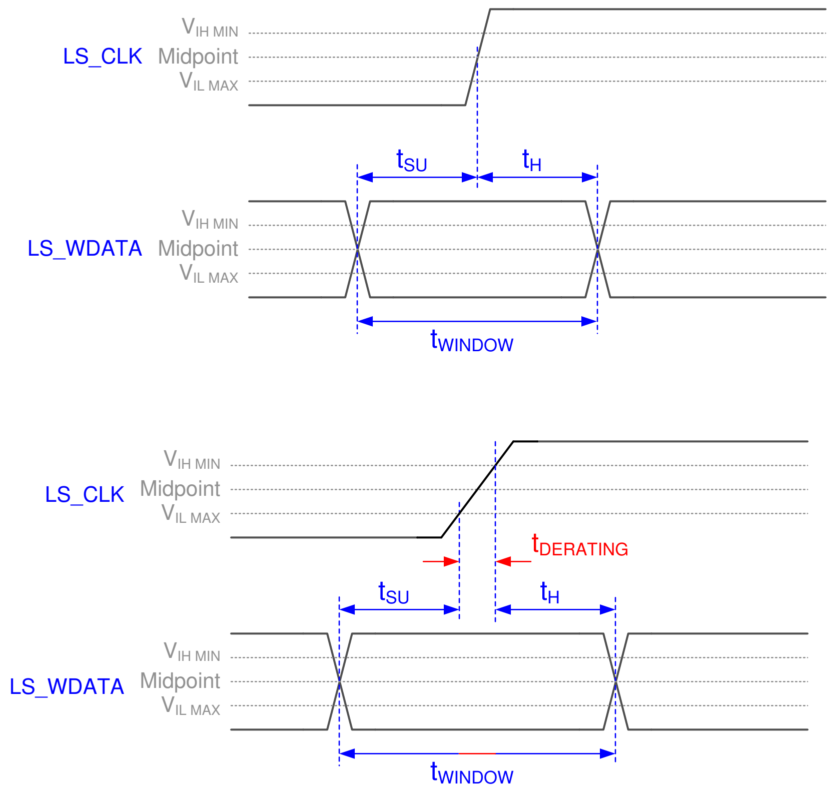

Figure 5-5. Window Time Derating Concept

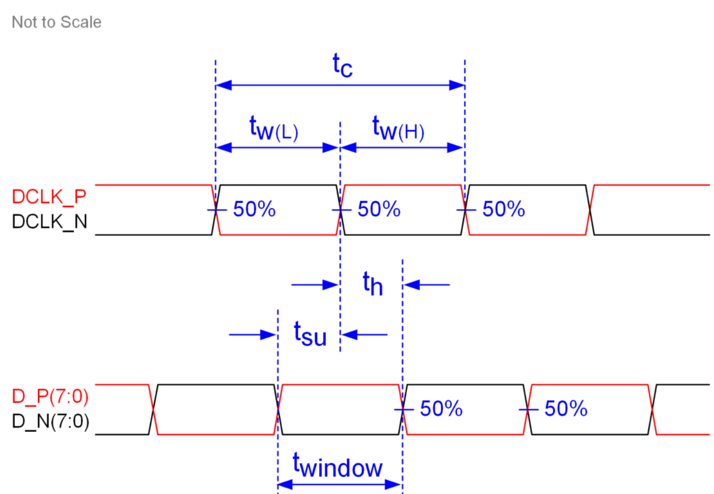

Figure 5-6. SubLVDS Switching Parameters

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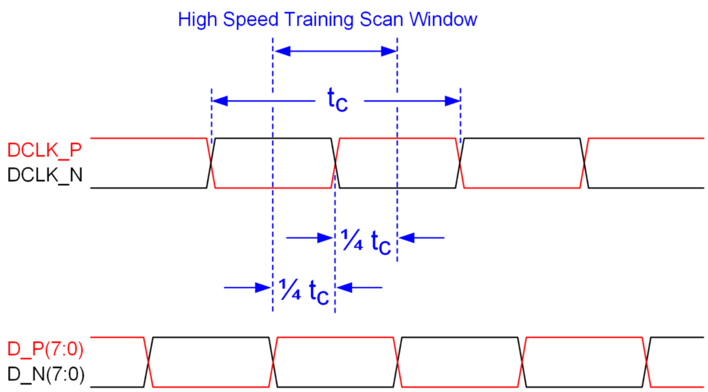


Note: Refer to Section 5.8 for details.

Figure 5-7. High-Speed Training Scan Window

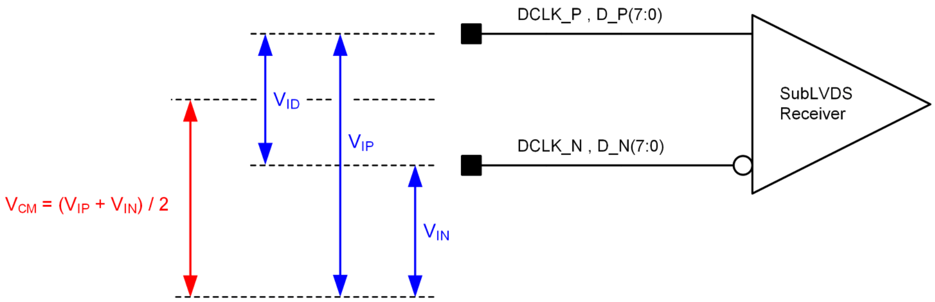


Figure 5-8. SubLVDS Voltage Parameters

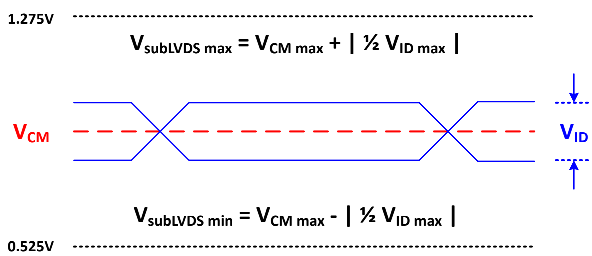


Figure 5-9. SubLVDS Waveform Parameters

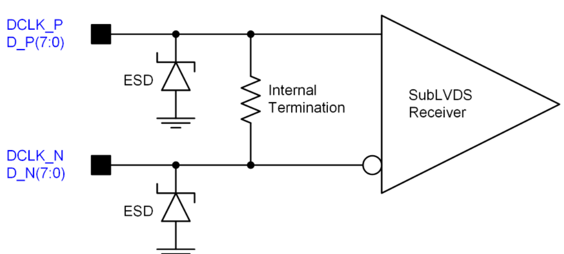


Figure 5-10. SubLVDS Equivalent Input Circuit

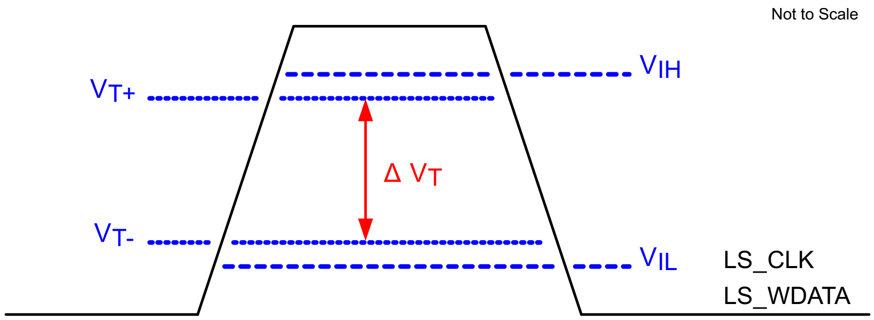


Figure 5-11. LPSDR Input Hysteresis

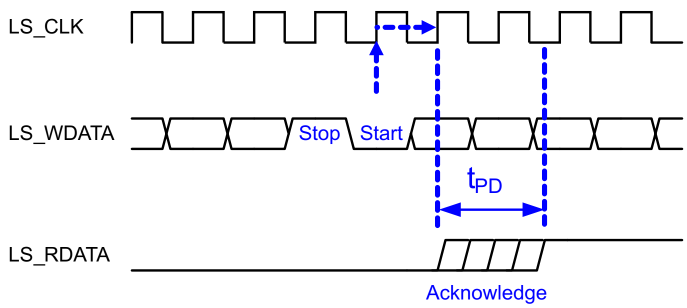
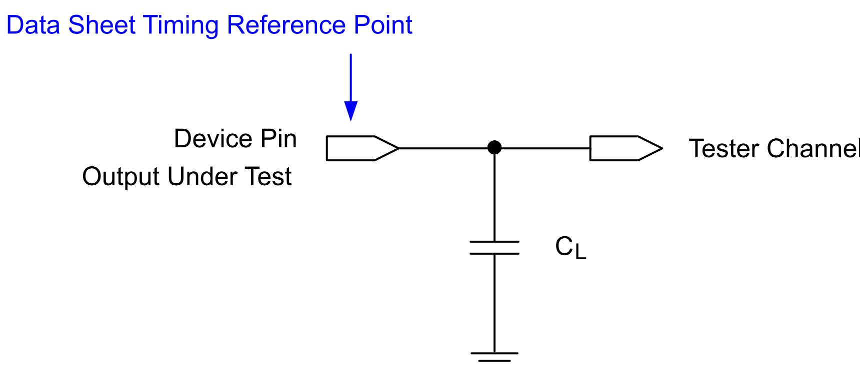


Figure 5-12. LPSDR Read Out



See Section 5.6 for more information.

Figure 5-13. Test Load Circuit for Output Propagation Measurement

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5.9 System Mounting Interface Loads

PARAMETER	Condition	MIN	NOM	MAX	UNIT
Thermal Interface Area	Maximum load evenly distributed within each area [(1)]			50	N
Electrical Interface Area	Maximum load evenly distributed within each area [(1)]			143	N

(1) See Figure 5-14.

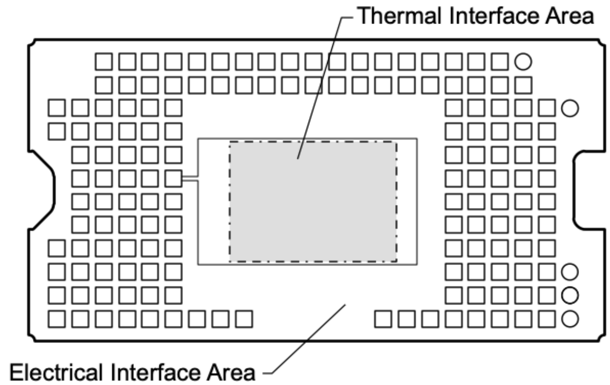

Figure 5-14. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION			VALUE	UNIT
M	Number of active columns [1] [2]		1360	micromirrors
N	Number of active rows [1] [2]		1536	micromirrors
Ɛ	Micromirror pitch, diagonal[1]		4.525	µm
P	Micromirror pitch, vertical and horizontal [1]		6.4	µm
	Micromirror active array width [1]	(P × M) + (P / 2)	8.7072	mm
	Micromirror active array height [1]	(P × N) / 2 + (P / 2)	4.9184	mm
	Micromirror active border [3]	Pond of micromirror (POM)	15	micromirrors/side

(1) See Figure 5-15.
(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display one distinct pixel on the screen during every frame, resulting in a full 1920 x 1080 pixel image being displayed.
(3) The structure and qualities of the border or borders around the active array include a band of partially functional micromirrors referred to as the *Pond of Micromirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

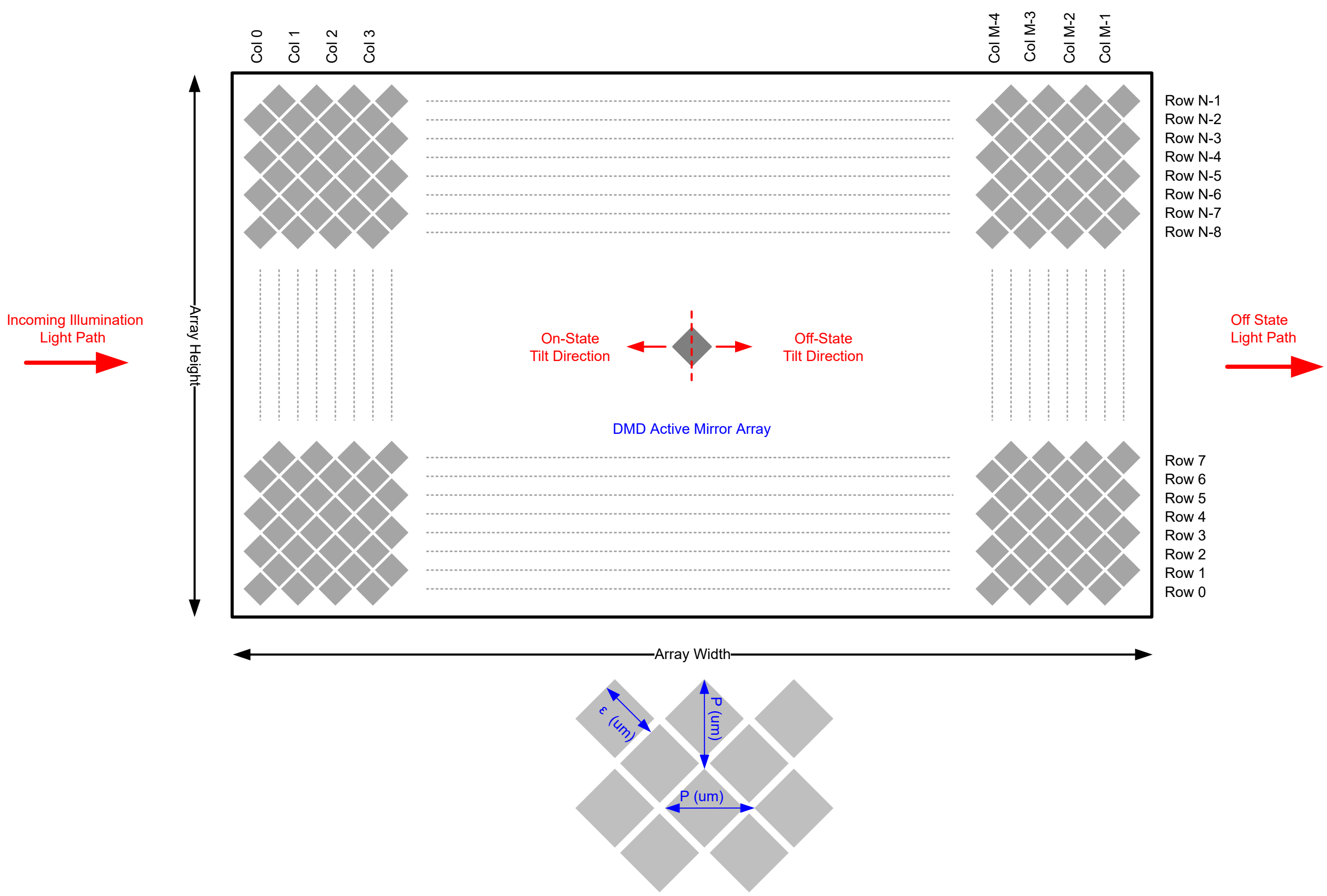

Figure 5-15. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state [1] [2] [3] [4]	13.5	14.5	15.5	degrees
Micromirror crossover time[5]				1	3	μs
Micromirror switching time[6]			6			μs
Image Performance[7]	Bright pixel(s) in active area[8]	Gray 10 Screen[9]			0	Micromirrors
	Bright pixel(s) in the POM[10]	Gray 10 Screen[9]			1	
	Dark pixel(s) in the active area[11]	White Screen			4	
	Adjacent pixel(s)[12]	Any Screen			0	
	Unstable pixel(s) in active area[13]	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the variation that can occur between any two individual micromirrors, located on the same device or on different devices.
(4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(6) The minimum time between successive transitions of a micromirror.
(7) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
• Test set degamma shall be linear.
• Test set brightness and contrast shall be set to nominal.
• The diagonal size of the projected image shall be a minimum of 20 inches.
• The projections screen shall be unity gain.
• The projected image shall be inspected from a 38-inch minimum viewing distance.
• The image shall be in focus during all image quality tests.
(8) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
(9) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(10) POM definition: Rectangular border of off-state mirrors surrounding the active area.
(11) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

5.12 Window Characteristics

PARAMETER		MIN	NOM	MAX
Window material			Corning Eagle XG	
Window refractive index	at wavelength 546.1 nm		1.5119	
Window aperture [1]				
Illumination overfill			See Section 6.5.	

(1) See the mechanical package ICD for details regarding the size and location of the window aperture.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP3940S-Q1 DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement Texas Instruments (TI) DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

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6 Detailed Description

6.1 Overview

The DLP3940S-Q1 digital micromirror device (DMD) is a 0.39-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors, combined with advanced DLP image processing algorithms, enables each micromirror to display one distinct pixel on the screen during every frame, resulting in a full 1920 × 1080 pixel image being displayed. The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to Section 6.2. The deflection of the micromirrors (positive or negative) is individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.39” 1080p FHD chipset is comprised of the DLP3940S-Q1 DMD, DLPC231S-Q1 display controller, and the TPS99002S-Q1 PMIC and the LED driver. To ensure reliable operation, the DLP3940S-Q1 DMD must always be used with the DLP display controller and the PMIC specified in the chipset.

6.2 Functional Block Diagram

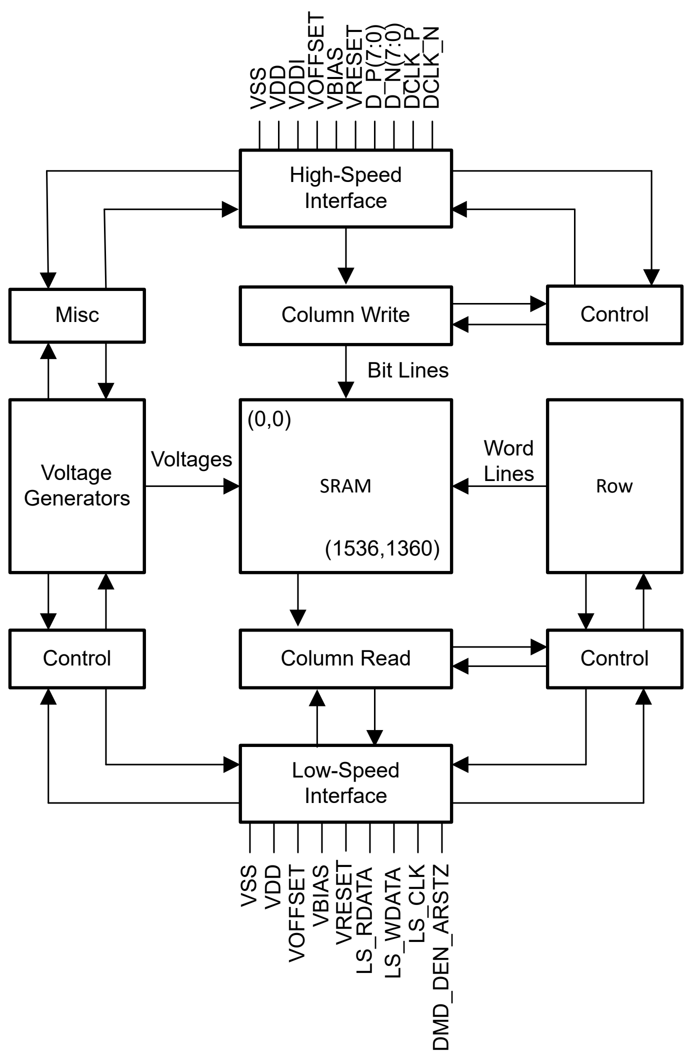

Figure 6-1. Functional Block Diagram

6.3 Feature Description

The DLP3940S-Q1 consists of a two-dimensional array of 1-bit CMOS memory cells driven by a SubLVDS bus from the DLPC231S-Q1 and powered by the TPS99002S-Q1. The temperature sensing diode is used to continuously monitor the DMD array temperature.

To ensure reliable operation, the DLP3940S-Q1 must be used with the DLPC231S-Q1 DMD display controller and the TPS99002S-Q1 system management and illumination controller.

6.3.1 SubLVDS Data Interface

The SubLVDS signaling protocol was designed to enable very fast DMD data refresh rates while simultaneously maintaining low power and low emission. The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high-speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

Data is loaded into the SRAM under each micromirror using the SubLVDS interface from the DLPC231S-Q1. This interface consists of 16 pairs of differential data signals plus two clock pairs into two separate buses C and D loading the left and right half of the SRAM array. The data is latched on both transitions creating a double data rate (DDR) interface. The SubLVDS interface also implements a continuous training algorithm to optimize the data and clock timing to allow for a more robust interface.

The entire DMD array of 2.1 million pixels can be updated at a rate of less than 130µs as a result of the high-speed SubLVDS interface.

6.3.2 Low Speed Interface for Control

The Low-Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low-speed clock, and LS_WDATA is the low-speed data input.

The purpose of the low speed interface is to configure the DMD at power up and power down and to control the micromirror reset voltage levels that are synchronized with the data loading. The micromirror reset voltage controls the time when the mirrors are mechanically switched. The low speed differential interface includes two pairs of signals for write data and clock, and two single-ended signals for output (C and D).

6.3.3 Power Interface

The DMD requires four DC voltages: 1.8V source (for V_{DD} and V_{DDI}), V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical LED-based system, 1.8V, V_{OFFSET}, V_{RESET}, and V_{BIAS} are managed by the TPS99002S-Q1 PMIC and LED driver.

6.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Figure 5-13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for the characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC231S-Q1 display controller. See the DLPC231S-Q1 display controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trade-offs. Although it is not possible to anticipate every conceivable application, projector image quality and

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optical performance are contingent on compliance with the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same or smaller as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. This is commonly referred to as “illumination overdrive.” The DLP3940S-Q1 has a 14.5° tilt angle which corresponds to the f/2.0 numerical aperture. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture angle of the illumination optics or the projection optics exceeds the micromirror tilt angle, contrast degradation and objectionable artifacts in the display border or active area are possible.

6.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light on the window aperture may have to be further reduced below the suggested 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

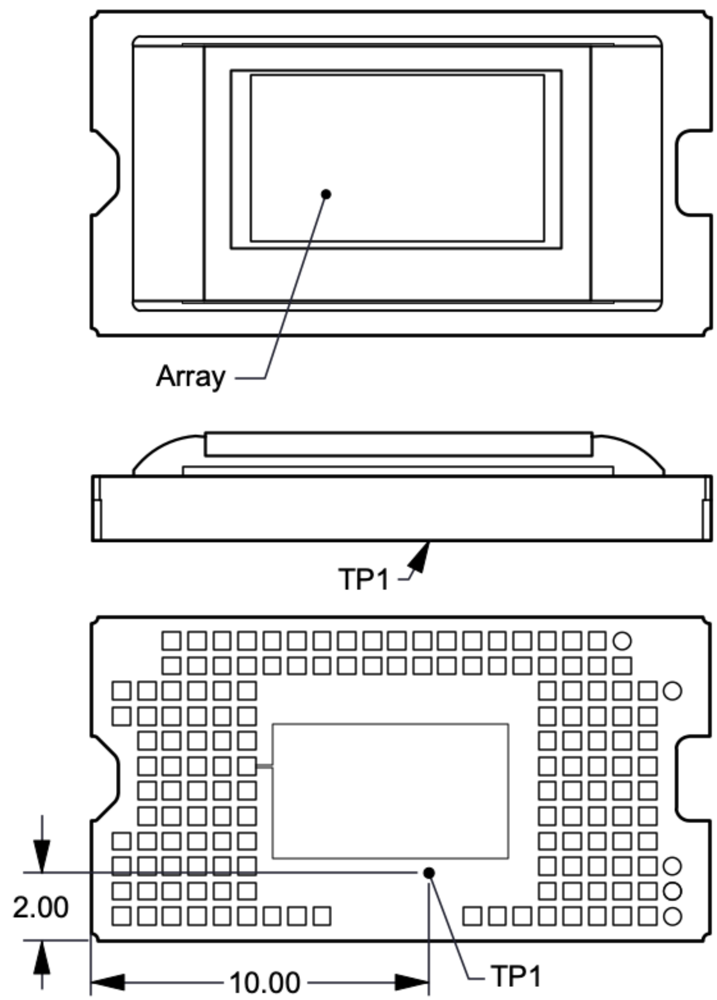

Figure 6-2. DMD Thermal Test Points

The active array temperature can be computed analytically from the thermal measurement point on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations provide the relationship between the array temperature and the reference ceramic temperature (TP1) in Figure 6-2:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ILLUMINATION} = Q_{INCIDENT} \times \text{DMD Absorption Constant} \quad (2)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (3)$$

where

- T_{ARRAY} = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature at the TP1 location in Figure 6-2 (°C)
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to thermal test point TP1 (°C/W)
- Q_{ARRAY} = total power (electrical plus absorbed) on the DMD array (W)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)

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- $Q_{ILLUMINATION}$ = absorbed illumination heat load (W)
- $Q_{INCIDENT}$ = incident power on the DMD (W)

The DMD absorption constant is a function of illumination distribution on the active array and the array border, angle of incidence (AOI), f number of the system, and operating state of the mirrors. The absorption constant is higher in the OFF state than in the ON state. Equations to calculate the absorption constant are provided for both ON and OFF mirror states. They assume an AOI of 29 degrees, an f/2.0 system, and they account for the distribution of light on the active array, POM, and array border.

$$\text{DMD Absorption Constant (OFF state)} = 1.004 - 0.005235 \times (\text{\% of light on ActiveArray} + \text{POM}) \quad (4)$$

$$\text{DMD Absorption Constant (ON state)} = 1.004 - 0.007776 \times (\text{\% of light on ActiveArray} + \text{POM}) \quad (5)$$

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies.

The following sample calculations assume 10% of the total incident light falls outside of the active array and POM, and the mirrors are in the OFF state.

1. $T_{CERAMIC}$ = 50°C (measured)
2. $Q_{INCIDENT}$ = 10W (measured)
3. DMD Absorption Constant = 1.004 – 0.005235 × 90 = 0.533
4. $Q_{ELECTRICAL}$ = 0.5W
5. $R_{ARRAY–TO–CERAMIC}$ = 2.6°C/W
6. Q_{ARRAY} = 0.5W + (0.533 x 10 W) = 5.83W
7. T_{ARRAY} = 50°C × (5.83W × 2.6°C/W) = 65.2°C

When designing the DMD heatsink solution, the package thermal resistance from array to reference ceramic temperature (thermocouple location TP1 can be used to determine the temperature rise through the package as given by the following equations:

$$T_{ARRAY\text{-}TO\text{-}CERAMIC} = Q_{ARRAY} \times R_{ARRAY–TO–CERAMIC} \quad (6)$$

6.6.1 Monitoring Array Temperature Using the Temperature Sense Diode

The active array temperature can be computed analytically from the temperature sense diode measurement, the thermal resistance from array to diode, the electrical power, and the illumination heat load. The relationship between array temperature and the temperature sense diode is provided by the following equations:

$$T_{ARRAY} = T_{DIODE} + (Q_{ARRAY} \times R_{ARRAY–TO–DIODE}) \quad (7)$$

$$Q_{ILLUMINATION} = (Q_{INCIDENT} \times \text{DMD Absorption Constant}) \quad (8)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (9)$$

where

- T_{ARRAY} = computed array temperature (°C)
- T_{DIODE} = measured temperature sense diode temperature (°C)
- $R_{ARRAY–TO–DIODE}$ = package thermal resistance from array to diode (°C/W)
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (W)
  Refer to Section 6.6 for details.
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)
- $Q_{ILLUMINATION}$ = absorbed illumination heat load (W)
- $Q_{INCIDENT}$ = incident power on the DMD (W)

The following sample calculations assume 10% of the total incident light falls outside of the active array and POM, and the mirrors are in the OFF state.

1. T_{DIODE} = 55°C
2. $Q_{INCIDENT}$ = 10W (measured)
3. DMD Absorption Constant = 1.004 – 0.005235 × 90 = 0.533
4. $Q_{ELECTRICAL}$ = 0.5W
5. $R_{ARRAY–TO–DIODE}$ = 0.1°C/W
6. Q_{ARRAY} = 0.5W + (0.533 × 10W) = 5.83W
7. T_{ARRAY} = 55°C + (5.83W × 0.1°C/W) = 55.6°C

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

$$ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000\text{mW/W} \div A_{ILL}\ (\text{mW/cm}^2) \quad (10)$$

$$A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})\ (\text{cm}^2) \quad (11)$$

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm ^{2}) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on

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the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 12.1 W (measured)

A_{ARRAY} = ((8.7072 mm × 4.9184 mm) ÷ 100mm^2/cm^2) = 0.4283 cm^2 (data sheet)

OV_{ILL} = 16.3% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00021 (spectral measurement)

A_{ILL} = 0.4283 cm^2 ÷ (1 - 0.163) = 0.5117 cm^2

ILL_{UV} = [0.00021 × 12.1 W] × 1000mW/W ÷ 0.5117 cm^2 = 4.966 mW/cm^2

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

- $Q_{AP\text{-}ILL} = [Q_{INCIDENT} \times OP_{AP\_ILL\_RATIO}] \div A_{AP\_ILL}$ (W/cm^2)

where:

- $Q_{AP\text{-}ILL}$ = window aperture illumination overfill (W/cm^2)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP\_ILL\_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- $A_{AP\text{-}ILL}$ = size of the window aperture critical area (cm^2) (data sheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

Sample calculation:

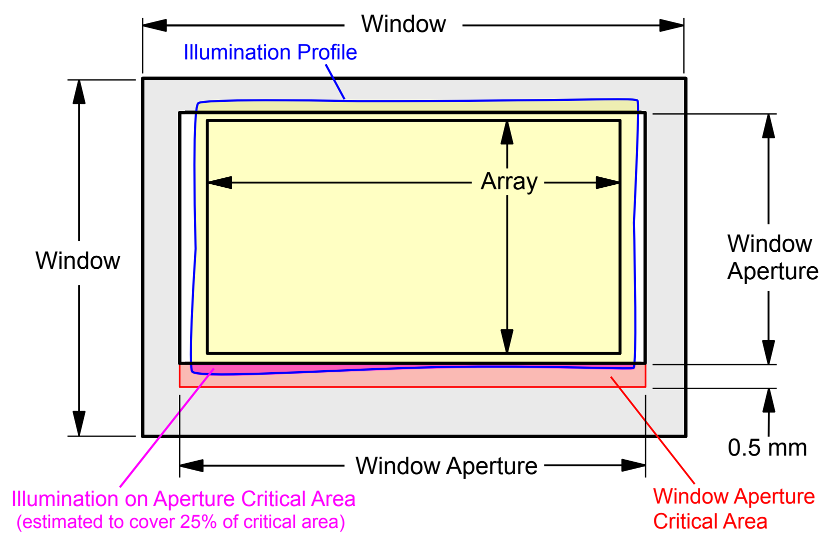

Figure 6-3. Window Aperture Overfill Example

See the above figure for the length of the critical aperture.

$$Q_{INCIDENT} = 12.1\ W\ \text{(measured)} \quad (12)$$

$$OP_{AP\_ILL\_RATIO} = 0.312\%\ \text{(optical model)} \quad (13)$$

$$OV_{CA\_RATIO} = 25\%\ \text{(optical model)} \quad (14)$$

$$\text{Length of the window aperture for critical area} = 0.9802\ cm\ \text{(data sheet)} \quad (15)$$

$$\text{Width of critical area} = 0.050\ cm\ \text{(data sheet)} \quad (16)$$

$$A_{AP\text{-}ILL} = 0.9802\ cm \times 0.050\ cm = 0.04901\ cm^2 \quad (17)$$

$$Q_{AP\text{-}ILL} = (12.1\ W \times 0.00312) \div (0.04901\ cm^2 \times 0.25) = 3.08\ W/cm^2\ (W/cm^2) \quad (18)$$

6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time); whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

DMDs are spatial light modulators that reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC231S-Q1 controller. The high tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Typical applications using the DLP3940S-Q1 include automotive applications such as head-up display systems.

DMD power-up and power-down sequencing is strictly controlled by the TPS99002S-Q1 . Refer to Section 8 for power-up and power-down specifications. To ensure reliable operation, the DLP3940S-Q1 DMD must always be used with the DLPC231S-Q1 controller and a TPS99002S-Q1 PMIC.

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7.2 Typical Application

The chipset consists of three components—the DLP3940S-Q1 automotive DMD, the DLPC231S-Q1, and the TPS99002S-Q1. The DMD is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC231S-Q1 is a controller for the DMD; it formats incoming video and controls the timing of the DMD illumination sources and the DMD in order to display the incoming video. The TPS99002S-Q1 is a high-performance voltage regulator for the DMD, a controller for the illumination sources (for example, LEDs or lasers), and a management IC for the entire chipset. In conjunction, the DLPC231S-Q1 and the TPS99002S-Q1 can be used for system-level monitoring, diagnostics, and failure detection features. Figure 7-1 is a system-level block diagram with these devices in the DLP Augmented Reality Heads-Up Display configuration and displays the primary features and functions of each device.

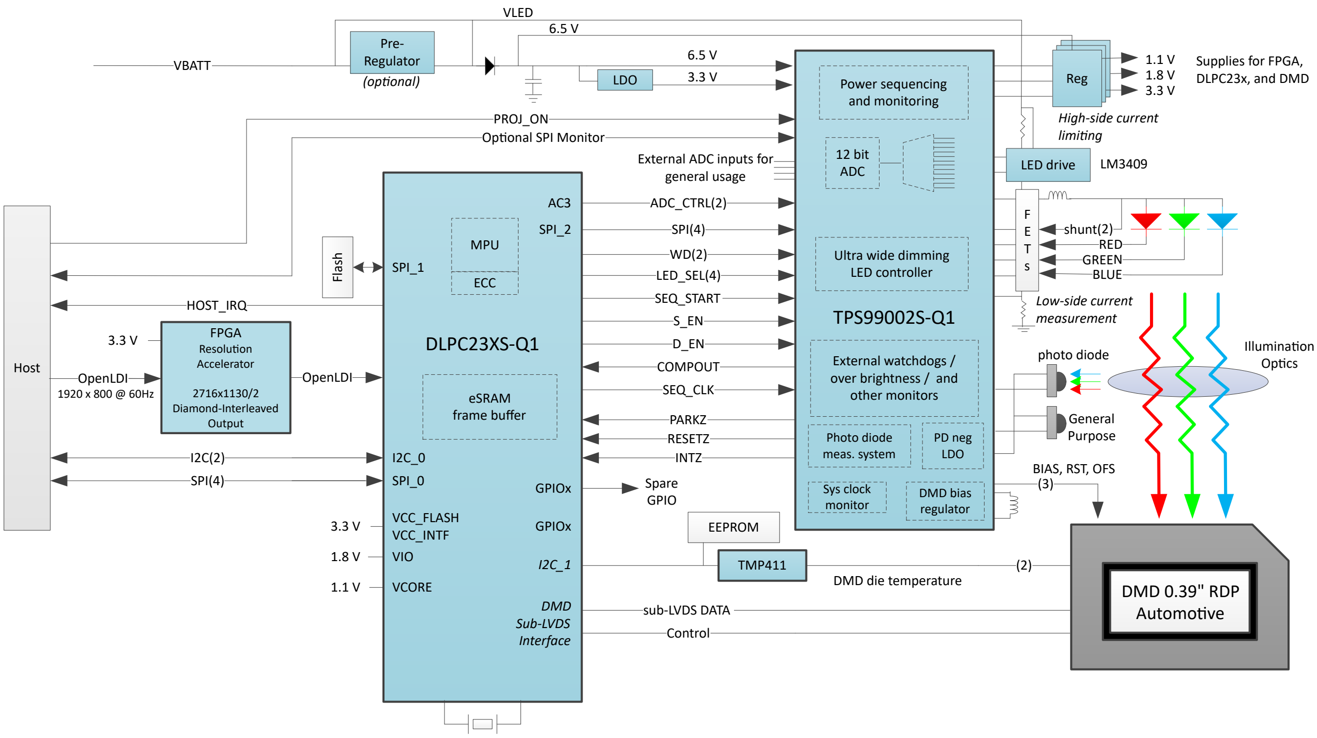

Figure 7-1. Augmented Reality Heads-Up Display System Block Diagram

7.2.1 Application Overview

Figure 7-1 shows the system block diagram for a DLP module. The system uses the DLPC231S-Q1, TPS99002S-Q1, and the DLP3940S-Q1 automotive DMD. The combination of the DLPC231S-Q1 and TPS99002S-Q1 removes the need for external SDRAM and a dedicated microprocessor. The chipset manages the illumination control of LED sources, power sequencing functions, and system management functions. Additionally, the chipset supports numerous system diagnostic and built-in self-test (BIST) features.

The DLPC231S-Q1 is a controller for the DMD and the light sources in the DLP module. It receives input video from the host and synchronizes DMD and light source timing to achieve the desired video. The DLPC231S-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing to create a video with grayscale shading and multiple colors, if applicable.

The DLPC231S-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. Host commands can be sent using either the I2C bus or the SPI bus. The bus that is not being used for host commands can be used as a read-only bus for diagnostic purposes. The input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The 24-bit bus can be limited to only 8-bits or 16-bits of data for single light source or dual light source systems depending on the system design. The SPI flash memory provides the embedded software for the DLPC231S-Q1's ARM core, any calibration data, and default settings. The TPS99002S-Q1 provides diagnostic and monitoring information to the DLPC231S-Q1 using a SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411A-Q1 uses an I2C interface to provide the DMD array temperature to the DLPC231S-Q1.

The outputs of the DLPC231S-Q1 are configuration and monitoring commands to the TPS99002S-Q1, timing controls to the LED or laser driver, control and data signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC231S-Q1 communicates with the TPS99002S-Q1 over an SPI bus. It uses this to configure the TPS99002S-Q1 and to read monitoring and diagnostics information from the TPS99002S-Q1. The DLPC231S-Q1 sends drive-enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a SubLVDS interface.

The TPS99002S-Q1 is a highly integrated mixed-signal IC that controls DMD power and provides monitoring and diagnostics information for the DLP system. The power sequencing and monitoring blocks of the TPS99002S-Q1 properly power up the DMD and provide accurate DMD voltage rails (–14V, 10V, and 18V), and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99002S-Q1 also has several output signals that can be used to control a variety of LED or laser driver topologies. The TPS99002S-Q1 has several general-purpose ADCs that designers can use for system-level monitoring, such as over-brightness detection.

The TPS99002S-Q1 receives inputs from the DLPC231S-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC231S-Q1 sends configuration and control commands to the TPS99002S-Q1 over an SPI bus and several other control signals. The DLPC231S-Q1's clocks are also monitored by the watchdogs in the TPS99002S-Q1 to detect any errors. The power rails are monitored by the TPS99002S-Q1 to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99002S-Q1 using a dedicated SPI bus, which enables independent monitoring. Additionally, the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99002S-Q1 has several general-purpose ADCs that can be used to implement system-level monitoring functions.

The outputs of the TPS99002S-Q1 are diagnostic information and error alerts to the DLPC231S-Q1, and control signals to the LED or laser driver. The TPS99002S-Q1 can output diagnostic information to the host and the DLPC231S-Q1 over two SPI buses. In case of critical system errors, such as power loss, it outputs signals to the DLPC231S-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as input (video data) and produces a mechanical output (mirror position). The electrical interface to the DMD is a SubLVDS

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interface with the DLPC231S-Q1. The mechanical output is the state of more than 2.1 million mirrors in the DMD array that can be tilted ±14.5°. In a projection system, the mirrors are used as pixels to display an image.

7.2.2 Input Image Resolution

The DLP3940S-Q1 together with the DLPC231S-Q1 supports different display resolutions up to 1920 × 800.

The DLPC231S-Q1 is limited to a display frame buffer size of 1,536,000 pixels or an equivalent resolution of 1920 × 800. As a result, the DLPC231S-Q1 will sub-image 1920 × 800 frame data onto the 1920 × 1080 micro-mirror array, resulting in 280 unused rows of mirrors. A front-end FPGA resolution accelerator is used to convert and format the 1920 × 800 orthogonal display input received at the FPD-Link interface to a diamond compatible format. The FPGA enables the DLPC231S-Q1 to drive the DLP3940S-Q1 without the need to apply additional diamond downsampling or decimation at the DMD. The resulting output of the FPGA accelerator is a diamond formatted frame resolution of 2716 × 1130 / 2 or 1,534,540 pixels transferred to the DLPC231S-Q1 through an FPD-Link interface.

The FPGA resolution accelerator applies de-gamma, a diamond anti-aliasing filter, diamond translation, an inverse filter, and inverse gamma. Alternatively, this resolution accelerator routine can be offloaded from the FPGA to be performed as a pre-processed step at a high-bandwidth host processor to bypass and eliminate the need for an FPGA.

For information on how the input image is displayed onto the DLP3940S-Q1, refer to the DLPC230-Q1 / DLPC230S-Q1 / DLPC231S-Q1 Programmer's Guide for Display Applications.

Future controllers will support the full HD resolution of 1920 × 1080 when paired with the DLP3940S-Q1.

7.2.3 Reference Design

For information about connecting together the DLP3940S-Q1 DMD, DLPC231S-Q1 controller, and TPS99002S-Q1, contact the TI Application Team for additional information about the DLP3940S-Q1 evaluation module (EVM). TI has optical-mechanical reference designs available; contact TI at the TI E2E™ design support forums for more information.

7.2.4 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles or number of operating hours at different temperatures. To assist in evaluation an Application Report may be provided in the future. Contact TI at the TI E2E™ design support forums for more information.

7.2.5 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and the desired brightness have a major effect on the overall system design and size.

The display system uses the DLP3940S-Q1 as the core imaging device and contains a 0.39-inch array of micromirrors. The DLPC231S-Q1 controller is the digital interface between the DMD and the rest of the system, taking digital input from frontend receiver and driving the DMD over a high-speed interface. The TPS99002S-Q1 PMIC serves as a voltage regulator for the DMD, controller, and LED illumination functionality.

7.2.6 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP3940S-Q1 DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with DLPC231S-Q1 display controller and TPS99002S-Q1 PMIC driver.

7.3 Temperature Sensing

The software application provides functions to configure the TMP411A-Q1 to read the DLP3940S-Q1 DMD temperature sensor diode. Use this data to incorporate additional functionality in the overall system design, such as adjusting illumination, fan speeds, and so on. All communication between the TMP411A-Q1 and the DLPC231S-Q1 controller is completed using the I^2C interface. The TMP411A-Q1 connects to the DMD through the pins outlined in Section 4.

7.3.1 Temperature Sensing Diode

The DMD includes a temperature-sensing diode designed to be used with the TMP411-Q1 temperature monitoring device. The DLPC231S-Q1 monitors the temperature sense diode through the TMP411A-Q1. The DLPC231S-Q1 operation of the DMD timing can be adjusted based on the DMD array temperature, therefore this connection is essential to ensure reliable operation of the DMD.

Figure 7-2 shows the typical connection between the DLPC231S-Q1, TMP411A-Q1, and the DMD.

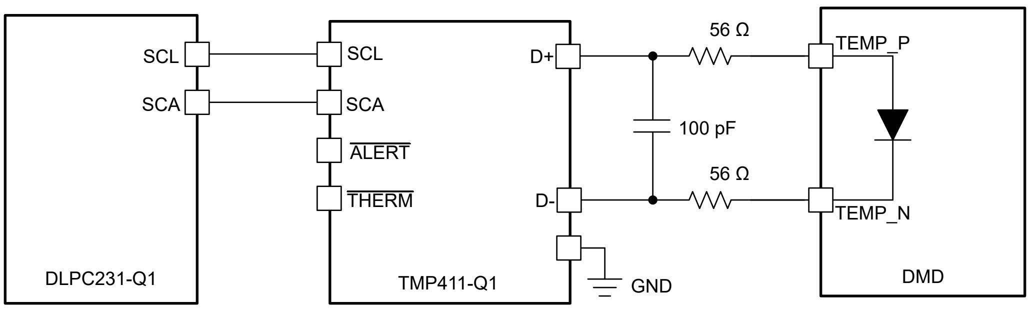

Figure 7-2. Temperature Sense Diode Typical Circuit Configuration

7.3.1.1 Temperature Sense Diode Theory

A temperature-sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Three different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in their base-emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the TMP411A-Q1 data sheet for detailed information about temperature diode theory and measurement. Figure 7-3 and Figure 7-4 illustrate the relationships between the current and voltage through the diode.

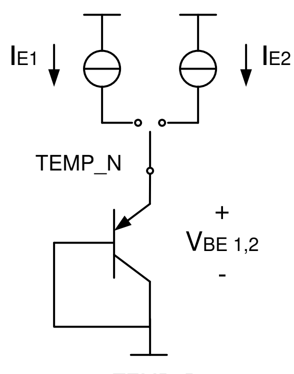

Figure 7-3. Temperature Measurement Theory

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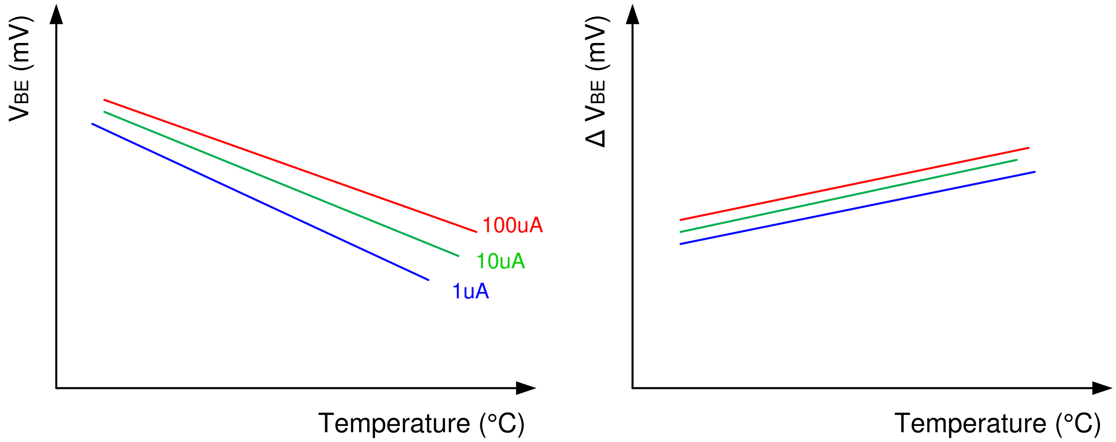

Figure 7-4. Example of Delta VBE Versus Temperature

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{DDI}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in DMD Power Supply Requirements.

V_{BIAS}, V_{DD}, V_{DDI}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

Table 8-1. DMD Power Supply Sequence Requirements

SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY1} (1)	Power up delay requirement	from V_{OFFSET} settled at recommended operating voltage to V_{BIAS} and V_{RESET} power up	2			ms
t_{DELAY3} (1)	Power down delay requirement	Delay V_{DD} must be held high from V_{OFFSET}, V_{BIAS} and V_{RESET} powering down	50			us
V_{OFFSET}	Supply voltage level	at beginning of power-up sequence delay			6	V
V_{BIAS}	Supply voltage level	at end of power-up sequence delay			6	V

(1) See DMD Power Supply Requirements.

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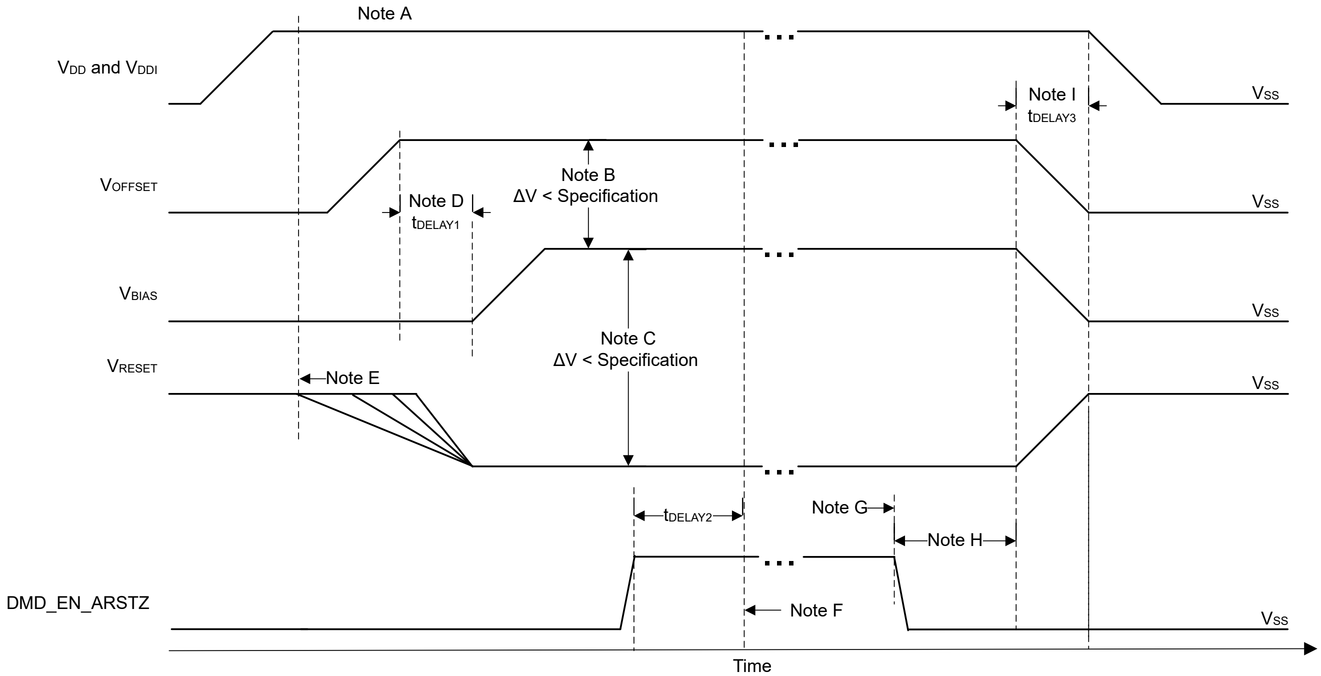
8.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET} plus t_{DELAY1}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Recommended Operating Conditions.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in Absolute Maximum Ratings, Recommended Operating Conditions, and in DMD Power Supply Requirements.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} have settled at the operating voltages listed in Recommended Operating Conditions.

8.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Recommended Operating Conditions.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the Absolute Maximum Ratings, Recommended Operating Conditions, and DMD Power Supply Requirements.
- During power-down, LVCMOS input pins must be less than specified in the Recommended Operating Conditions.

8.3 DMD Power Supply Sequencing Requirements



A. See Pin Configuration and Functions for the *Pin Functions Table*.
B. To prevent excess current, the supply voltage difference $|V_{OFFSET} – V_{BIAS}|$ must be less than the specified limit in the Recommended Operating Conditions.
C. To prevent excess current, the supply difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit in Recommended Operating Conditions.
D. V_{BIAS} should power up after V_{OFFSET} has powered up, per the t_{DELAY1} specification.
E. DLP controller software initiates the global V_{BIAS} command.
F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET}, and V_{OFFSET}.
G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, DMD_EN_ARSTZ will go low.
H. V_{DD} must remain high until after V_{OFFSET}, V_{BIAS}, V_{RESET} go low, per t_{DELAY3} specification.
I. To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit in Recommended Operating Conditions.

Figure 8-1. DMD Power Supply Requirements

9 Layout

9.1 Layout Guidelines

Refer to the DLPC231S-Q1 and TPS99002S-Q1 data sheets for specific PCB layout and routing guidelines. For specific DMD PCB guidelines, use the following:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals.
- Minimum of two 220nF decoupling capacitors close to V_{BIAS}.
- Minimum of two 220nF decoupling capacitors close to V_{RESET}.
- Minimum of three 4.7μF decoupling capacitors close to V_{OFFSET}.
- Minimum of four 100nF decoupling capacitors close to V_{DDI} and V_{DD}.
- Temperature diode pins: The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411A-Q1 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411A-Q1 are sensitive to noise. See the *TMP411 ±1°C Remote and Local Temperature Sensor with N-Factor and Series Resistance Correction Data Sheet* for specific routing recommendations.

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

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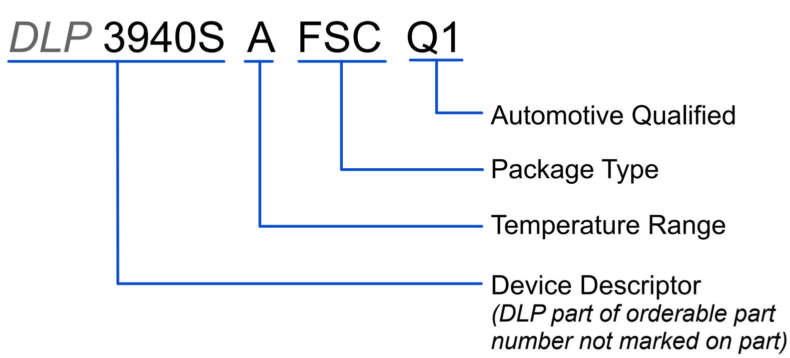
10.2 Device Support

10.2.1 Device Nomenclature

Figure 10-1. Part Number Description

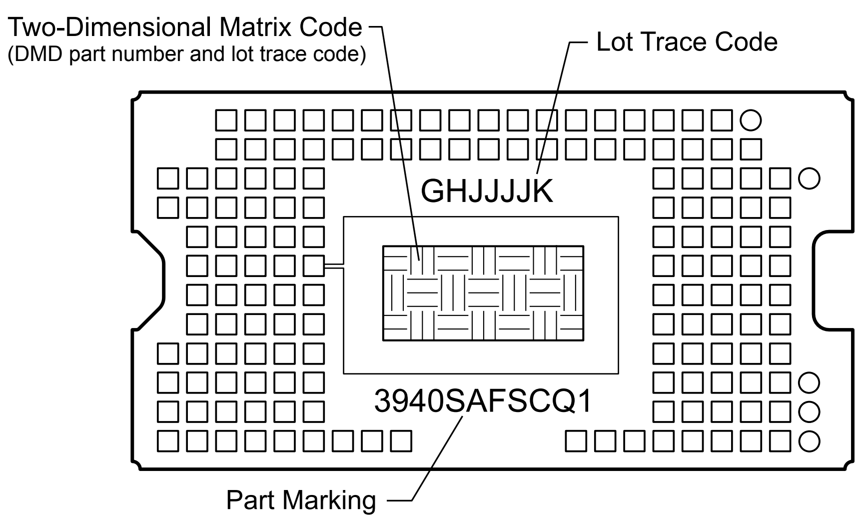


10.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 10-2 and includes the legible character string GHJJJJK 3940SAFSCQ1. GHJJJJK is the lot trace code and 3940SAFSCQ1 is the device marking.

Example: GHJJJJK 3940SAFSCQ1

Figure 10-2. DMD Marking Locations



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10.3 Documentation Support

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XDLP394SAFSCQ1	Active	Preproduction	CLGA (FSC) | 154	96 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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