DLP991U Industrial Digital Micromirror Device

1 Features

- High resolution 4096 × 2176 micromirror array
  - > 8.9 million micromirrors
  - 5.4µm micromirror pitch
  - 0.99" micromirror array diagonal
  - ±12° micromirror tilt relative to flat S
  - Designed for corner illumination
  - Integrated micromirror driver circuitry
- Designed for visible light use (400nm to 800nm)
  - 97% window transmission (single pass, through two window surfaces)
  - 89% micromirror reflectivity
  - 79% average photopic weighted diffraction and 80% unweighted (410nm–800nm) efficiency (f/2.4) per photopic luminous efficiency—CIE 086-1990
  - 90% on-state array fill factor

2 Applications

- Industrial
  - Direct imaging lithography
  - 3D printing
  - Machine vision and quality control
  - Laser marking and repair
- Medical
  - Ophthalmology
  - 3D scanners for limb and skin measurement
  - HyperSpectral imaging/scanning
- Displays
  - 3D imaging microscopes
  - Augmented reality and information overlay

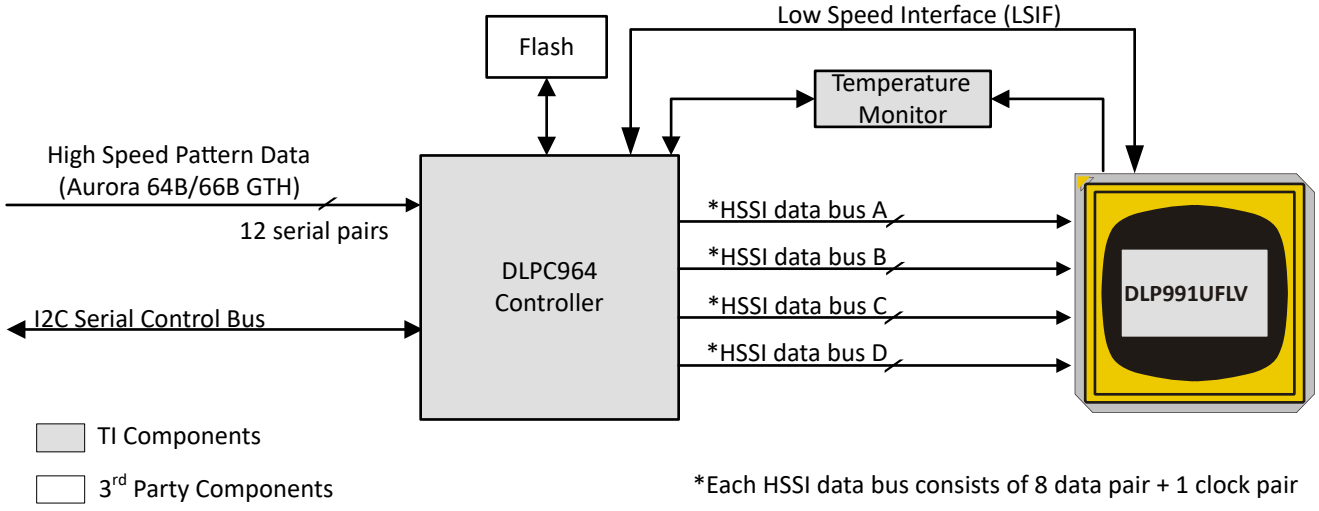
3 Description

Featuring over 8.9 million micromirrors, the high-resolution DLP991U digital micromirror device (DMD) is a spatial light modulator (SLM) that modulates the amplitude, direction, or phase of incoming light. This advanced light control technology has numerous applications in the industrial, medical, and consumer markets. The streaming nature of the DLP991U and its DLPC964 controller make it ideally suited for exceptionally high-speed continuous data streaming for direct imaging (LDI) applications. The DMD enables large 3D print build sizes and ultra-fine resolutions for various 3D printing applications. The high resolution provides a direct benefit to the scanning of larger objects in 3D machine vision applications.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
DLP991UFLV	FLV (321)	42.16mm × 42.16mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



Simplified Application

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4 Pin Configuration and Functions

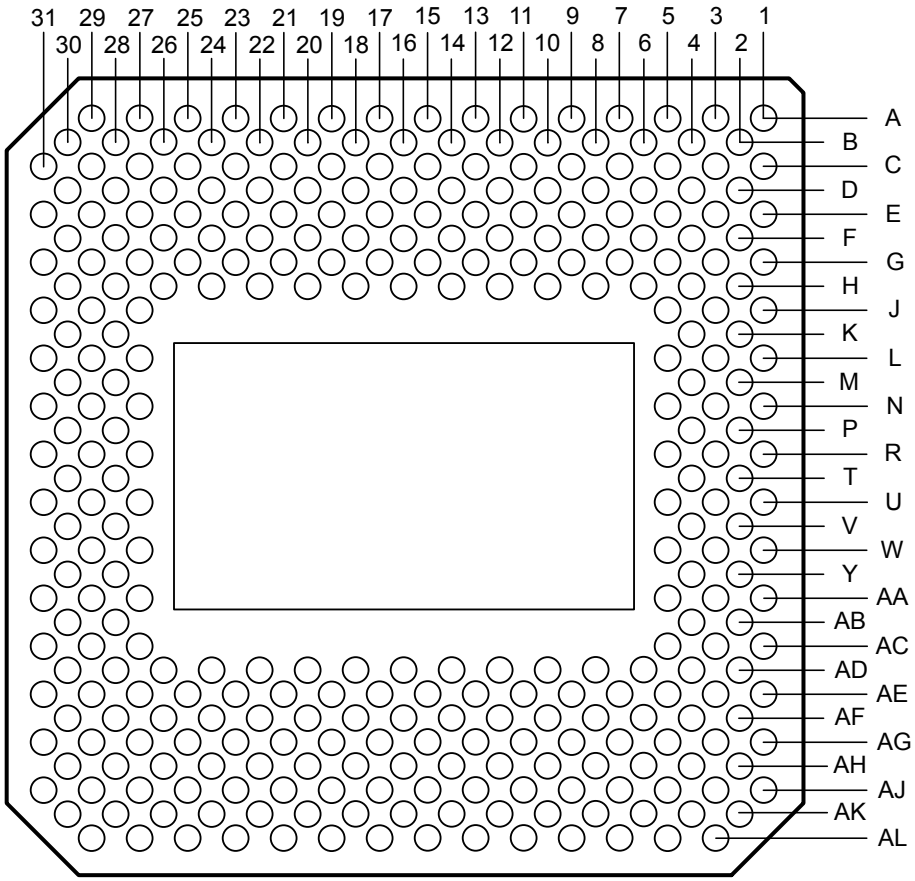


Figure 4-1. FLV Package 321-Pin LGA Bottom View

CAUTION

To ensure reliable, long-term operation of the DLP991U DMD, it is critical to properly manage the layout and operation of the signals identified in the table below. For specific details and guidelines, refer to the *PCB Design Requirements for TI DLP® Standard SST Digital Micromirror Devices*.

Table 4-1. Package Pinout

PIN		INPUT-OUTPUT[1]	PIN DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_AP(0)	E1	I	High-Speed Differential Data Pair lane A0	Differential 100Ω	10.79289
D_AN(0)	F2	I	High-Speed Differential Data Pair lane A0	Differential 100Ω	10.7718
D_AP(1)	J1	I	High-Speed Differential Data Pair lane A1	Differential 100Ω	13.77059
D_AN(1)	G1	I	High-Speed Differential Data Pair lane A1	Differential 100Ω	13.75662
D_AP(2)	A5	I	High-Speed Differential Data Pair lane A2	Differential 100Ω	10.33756
D_AN(2)	B6	I	High-Speed Differential Data Pair lane A2	Differential 100Ω	10.3464
D_AP(3)	K2	I	High-Speed Differential Data Pair lane A3	Differential 100Ω	12.35641
D_AN(3)	L1	I	High-Speed Differential Data Pair lane A3	Differential 100Ω	12.33238
D_AP(4)	B8	I	High-Speed Differential Data Pair lane A4	Differential 100Ω	9.64012
D_AN(4)	A7	I	High-Speed Differential Data Pair lane A4	Differential 100Ω	9.64824
D_AP(5)	A11	I	High-Speed Differential Data Pair lane A5	Differential 100Ω	11.96008
D_AN(5)	A9	I	High-Speed Differential Data Pair lane A5	Differential 100Ω	11.95453
D_AP(6)	R1	I	High-Speed Differential Data Pair lane A6	Differential 100Ω	17.77003
D_AN(6)	T2	I	High-Speed Differential Data Pair lane A6	Differential 100Ω	17.73406
D_AP(7)	W1	I	High-Speed Differential Data Pair lane A7	Differential 100Ω	21.44439
D_AN(7)	U1	I	High-Speed Differential Data Pair lane A7	Differential 100Ω	21.43676
DCLK_AP	P2	I	High-Speed Differential Clock A	Differential 100Ω	16.02177
DCLK_AN	N1	I	High-Speed Differential Clock A	Differential 100Ω	16.01225
D_BP(0)	A13	I	High-Speed Differential Data Pair lane B0	Differential 100Ω	8.39128
D_BN(0)	B12	I	High-Speed Differential Data Pair lane B0	Differential 100Ω	8.39933
D_BP(1)	P30	I	High-Speed Differential Data Pair lane B1	Differential 100Ω	30.30779

Table 4-1. Package Pinout (continued)

PIN		INPUT-OUTPUT[1]	PIN DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_BN(1)	R31	I	High-Speed Differential Data Pair lane B1	Differential 100Ω	30.30599
D_BP(2)	B14	I	High-Speed Differential Data Pair lane B2	Differential 100Ω	9.53143
D_BN(2)	A15	I	High-Speed Differential Data Pair lane B2	Differential 100Ω	9.52732
D_BP(3)	A17	I	High-Speed Differential Data Pair lane B3	Differential 100Ω	11.23296
D_BN(3)	B16	I	High-Speed Differential Data Pair lane B3	Differential 100Ω	11.23915
D_BP(4)	B20	I	High-Speed Differential Data Pair lane B4	Differential 100Ω	13.82456
D_BN(4)	A21	I	High-Speed Differential Data Pair lane B4	Differential 100Ω	13.82794
D_BP(5)	N31	I	High-Speed Differential Data Pair lane B5	Differential 100Ω	26.98275
D_BN(5)	L31	I	High-Speed Differential Data Pair lane B5	Differential 100Ω	26.99587
D_BP(6)	G31	I	High-Speed Differential Data Pair lane B6	Differential 100Ω	24.55442
D_BN(6)	J31	I	High-Speed Differential Data Pair lane B6	Differential 100Ω	24.51977
D_BP(7)	B22	I	High-Speed Differential Data Pair lane B7	Differential 100Ω	16.27286
D_BN(7)	A23	I	High-Speed Differential Data Pair lane B7	Differential 100Ω	16.29733
DCLK_BP	A19	I	High-Speed Differential Clock B	Differential 100Ω	12.98251
DCLK_BN	B18	I	High-Speed Differential Clock B	Differential 100Ω	12.98727
D_CP(0)	AL7	I	High-Speed Differential Data Pair lane C0	Differential 100Ω	18.55831
D_CN(0)	AL5	I	High-Speed Differential Data Pair lane C0	Differential 100Ω	18.57877
D_CP(1)	AG1	I	High-Speed Differential Data Pair lane C1	Differential 100Ω	23.81943
D_CN(1)	AF2	I	High-Speed Differential Data Pair lane C1	Differential 100Ω	23.79686
D_CP(2)	AC1	I	High-Speed Differential Data Pair lane C2	Differential 100Ω	26.31612
D_CN(2)	AE1	I	High-Speed Differential Data Pair lane C2	Differential 100Ω	26.32655

Table 4-1. Package Pinout (continued)

PIN		INPUT-OUTPUT[1]	PIN DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_CP(3)	AA1	I	High-Speed Differential Data Pair lane C3	Differential 100Ω	24.97633
D_CN(3)	AB2	I	High-Speed Differential Data Pair lane C3	Differential 100Ω	24.98848
D_CP(4)	AK10	I	High-Speed Differential Data Pair lane C4	Differential 100Ω	17.76946
D_CN(4)	AL9	I	High-Speed Differential Data Pair lane C4	Differential 100Ω	17.75209
D_CP(5)	AL15	I	High-Speed Differential Data Pair lane C5	Differential 100Ω	14.23357
D_CN(5)	AK14	I	High-Speed Differential Data Pair lane C5	Differential 100Ω	14.22774
D_CP(6)	AK18	I	High-Speed Differential Data Pair lane C6	Differential 100Ω	12.92082
D_CN(6)	AL17	I	High-Speed Differential Data Pair lane C6	Differential 100Ω	12.93366
D_CP(7)	AL19	I	High-Speed Differential Data Pair lane C7	Differential 100Ω	12.23762
D_CN(7)	AL21	I	High-Speed Differential Data Pair lane C7	Differential 100Ω	12.21188
DCLK_CP	AL13	I	High-Speed Differential Clock C	Differential 100Ω	14.80911
DCLK_CN	AL11	I	High-Speed Differential Clock C	Differential 100Ω	14.80629
D_DP(0)	AL23	I	High-Speed Differential Data Pair lane D0	Differential 100Ω	8.81383
D_DN(0)	AK22	I	High-Speed Differential Data Pair lane D0	Differential 100Ω	8.81029
D_DP(1)	AL25	I	High-Speed Differential Data Pair lane D1	Differential 100Ω	10.2057
D_DN(1)	AK24	I	High-Speed Differential Data Pair lane D1	Differential 100Ω	10.21071
D_DP(2)	AK26	I	High-Speed Differential Data Pair lane D2	Differential 100Ω	11.97626
D_DN(2)	AL27	I	High-Speed Differential Data Pair lane D2	Differential 100Ω	11.97857
D_DP(3)	V30	I	High-Speed Differential Data Pair lane D3	Differential 100Ω	17.09379
D_DN(3)	U31	I	High-Speed Differential Data Pair lane D3	Differential 100Ω	17.05432
D_DP(4)	AF30	I	High-Speed Differential Data Pair lane D4	Differential 100Ω	12.2472

Table 4-1. Package Pinout (continued)

PIN		INPUT-OUTPUT[1]	PIN DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_DN(4)	AE31	I	High-Speed Differential Data Pair lane D4	Differential 100Ω	12.23151
D_DP(5)	W31	I	High-Speed Differential Data Pair lane D5	Differential 100Ω	14.32509
D_DN(5)	Y30	I	High-Speed Differential Data Pair lane D5	Differential 100Ω	14.32262
D_DP(6)	AB30	I	High-Speed Differential Data Pair lane D6	Differential 100Ω	11.15985
D_DN(6)	AA31	I	High-Speed Differential Data Pair lane D6	Differential 100Ω	11.15796
D_DP(7)	AD30	I	High-Speed Differential Data Pair lane D7	Differential 100Ω	13.11281
D_DN(7)	AC31	I	High-Speed Differential Data Pair lane D7	Differential 100Ω	13.11248
DCLK_DP	AG31	I	High-Speed Differential Clock D	Differential 100Ω	13.93058
DCLK_DN	AH30	I	High-Speed Differential Clock D	Differential 100Ω	13.92796
LS_WDATA_P	B26	I	LVDS Data	Differential 100Ω	10.90213
LS_WDATA_N	A27	I	LVDS Data	Differential 100Ω	10.90334
LS_CLK_P	B24	I	LVDS CLK	Differential 100Ω	11.06614
LS_CLK_N	A25	I	LVDS CLK	Differential 100Ω	11.02884
LS_RDATA_A	F24	O	LVCMOS Output		2.03585
LS_RDATA_B	D26	O	LVCMOS Output		5.2634
LS_RDATA_C	F30	O	LVCMOS Output		9.57426
LS_RDATA_D	C27	O	LVCMOS Output		7.1452
AMUX_OUT	E17	O	Analog Test Mux		6.35517
DMUX_OUT	E29	O	Digital Test Mux		7.21573
DMD_EN_ARSTZ	AE23, E27, Y4	I	ARSTZ	17.5kΩ Pulldown	63.74499
TEMP_N	E23	I	Temp Diode N		3.21385
TEMP_P	F22	I	Temp Diode P		2.85542
VDD	A29, A3, AA29, AB4, AD10, AD12, AD28, AD8, AE13, AE15, AF10, AF12, AF18, AF22, AF24, AF26, AF28, AF6, AH10, AH12, AH14, AH16, AH18, AJ1, AJ11, AJ21, AJ29, AJ31, AJ5, AK2, AL29, B4, C1, C13, C21, C29, C31, D12, D16, D18, D20, D24, D8, F10, F12, F16, F18, F20, F8, H16, H18, H20, H22, H24, H28, K4, L3, M4, N29, P28, P4, T28, T4, V28, V4, Y28	P	Digital Core Supply Voltage		Plane

Table 4-1. Package Pinout (continued)

PIN		INPUT-OUTPUT[1]	PIN DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
VDDA	AB28, AD14, AD16, AD18, AD22, AD24, AE19, AE27, AF20, AH20, AH24, D10, D14, F6, G11, G15, H10, H12, H14, H26, H8, K28	P	HSSI Supply Voltage		Plane
VRESET	AF4, AG5, D6, E5	P	Supply Voltage for Negative Bias of Micromirror reset signal		Plane
VBIAS	AD4, AE3, D4	P	Supply Voltage for Positive Bias of Micromirror reset signal		Plane
VOFFSET	AD26, AE5, F26, F4, H4	P	Supply voltage for HVCMOS logic, stepped up logic level		Plane
VSS	A1, AA3, AC29, AC3, AD20, AD6, AE11, AE17, AE21, AE25, AE29, AE7, AE9, AF14, AF16, AF8, AG11, AG13, AG15, AG17, AG19, AG21, AG23, AG25, AG27, AG29, AG3, AH2, AH26, AH4, AH6, AK30, AK4, AK8, AL3, C3, D2, D22, D28, D30, E11, E13, E15, E19, E21, E25, E3, E31, E7, F14, G13, G17, G19, G21, G23, G25, G27, G29, G3, G5, G7, G9, H2, H30, H6, J29, J3, K30, L29, M2, M28, M30, N3, R29, R3, T30, U29, U3, V2, W29, W3, Y2	G	Ground		Plane
VSSA	AD2, AH22, AH28, AJ13, AJ15, AJ17, AJ19, AJ23, AJ25, AJ27, AJ3, AJ7, AJ9, AK12, AK16, AK20, AK28, AK6, B10, B2, B28, B30, C11, C15, C17, C19, C23, C25, C5, C7, C9, E9	G	Ground		Plane
N/C	AA5, AA27, AC5, AC27, AG7, AG9, AH8, F28, J5, J27, L5, L27, N27, R27, N5, R5, U5, U27, W5, W27	NC	No Connect		

(1) I = Input, O = Output, P = Power, G = Ground, NC = No Connect

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Supply Voltage				
V_{DD}	Supply voltage for LVCMOS core logic and LVCMOS low speed interface (LSIF)(1)	–0.5	2.3	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers(1)	–0.3	2.2	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(1) (2)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(1)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(1)	–15	0.5	V
$\lvert V_{DDA} - V_{DD} \rvert$	Supply voltage delta (absolute value)(3)		0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(4)		11	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value)(5)		34	V
Input Voltage				
	Input voltage for other inputs – LVDS and LVCMOS(1)	–0.5	2.45	V
	Input voltage for other inputs – HSSI(1) (6)	–0.2	V_{DDA}	V
Low speed interface (LSIF)				
f_{CLOCK}	LSIF clock frequency (LS_CLK)		130	MHz
$\lvert V_{ID} \rvert$	LSIF differential input voltage magnitude(6)		810	mV
I_{ID}	LSIF differential input current(7)		10	mA
High speed serial interface (HSSI)				
f_{CLOCK}	HSSI clock frequency (DCLK)		1.65	GHz
$\lvert V_{ID} \rvert$	HSSI differential input voltage magnitude Data Lane		700	mV
$\lvert V_{ID} \rvert$	HSSI differential input voltage magnitude Clock Lane		700	mV
Environmental				
T_{ARRAY}	Temperature, operational(8)	0	90	°C
	Temperature, non-operational(8)	-40	90	°C
T_{WINDOW}	Temperature, operational(8)	0	70	°C
	Temperature, non-operational (8)	–40	90	°C
T_{DELTA_MAX}	[maximum of TP2 or TP3] minus T_{MIN_ARRAY} (9)		5	°C
T_{DELTA_MIN}	[minimum of TP2 or TP3] minus T_{MAX_ARRAY} (9)	–30		°C
RH	Relative humidity, operational and non-operational		95%	

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDA} and V_{DD} may result in excessive current draw.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) Differential inputs must not exceed the specified limit or damage may result to the internal termination resistors. Specification applies to both the high speed serial interface (HSSI) and the low speed interface (LSI).
(8) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at the test point (TP1) shown in Figure 6-1 and the package thermal resistances using the calculation in Section 6.6.
(9) Refer to Section 6.6 for the calculation.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_{DMD}	DMD Storage Temperature	–40	80	C
RH	Relative Humidity (non-condensing)		95	%

5.3 ESD Ratings

SYMBOL	PARAMETER	DESCRIPTION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted)(1)

PARAMETER		MIN	TYP	MAX	UNIT
Supply Voltages					
V_{DD}	Supply voltage for LVCMOS core logic and low speed interface (LSIF)(2)	1.85	1.9	1.95	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers(2)	1.85	1.9	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(2) (3) (4)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for micromirror electrode(2)	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode(2)	–14.5	–14	–13.5	V
$\lvert V_{DDA} - V_{DD} \rvert$	Supply voltage delta, absolute value(5)			0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta, absolute value(6)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta, absolute value			33	V
LVCMOS Input					
V_{IH}	High level input voltage(2) (7)	0.7 × V_{DD}			V
V_{IL}	Low level input voltage(2) (7)			0.3 × V_{DD}	V
Low Speed Interface (LSIF)					
f_{CLOCK}	LSIF clock frequency (LS_CLK)(9)	108	120	130	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK)	44%		56%	
$\lvert V_{ID} \rvert$	LSIF differential input voltage magnitude (9)	150	350	440	mV
V_{LVDS}	LSIF voltage(9)	575		1520	mV
V_{CM}	Common mode voltage(9)	700	900	1300	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
High Speed Serial Interface (HSSI)					
f_{CLOCK}	HSSI clock frequency (DCLK)(8)	1.8	1.8	1.8	GHz
DCD_{IN}	HSSI duty cycle distortion (DCLK)	44%	50%	56%	
$\lvert V_{ID} \rvert$ Data	HSSI differential input voltage magnitude Data Lane(8)	100	400	600	mV
$\lvert V_{ID} \rvert$ CLK	HSSI differential input voltage magnitude Clock Lane(8)	300	400	600	mV
VCM_{DC} Data	Input common mode voltage (DC) Data Lane(8)	200	600	800	mV
VCM_{DC} CLK	Input common mode voltage (DC) Clk Lane(8)	200	600	800	mV
VCM_{ACp-p}	AC peak to peak (ripple) on common mode voltages of Data Lane and Clock Lane(8)			100	mV

5.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)(1)

PARAMETER		MIN	TYP	MAX	UNIT
Z_{LINE}	Line differential impedance (PWB/trace)		100		Ω
Z_{IN}	Internal differential termination resistance (R_{Xterm})	80	100	120	Ω
Environmental 410nm – 800nm (Visible Wavelengths)					
T_{ARRAY}	Array temperature, long-term operational(10) (11) (13) (16)	45		70(12)	°C
	Array temperature, short-term operational 500 hour maximum(11) (14)	10		45	°C
T_{WINDOW}	Window temperature, operational, TP2 and TP3	15		75	°C
T_{DELTA_MAX}	[maximum of TP2 or TP3] minus T_{MIN_ARRAY} (16)			5	°C
T_{DELTA_MIN}	[minimum of TP2 or TP3] minus T_{MAX_ARRAY} (16)	–30			°C
RH	Relative humidity (non-condensing)			95%	
Solid State Illumination 410nm – 800nm (Visible Wavelengths)					
ILL_{UV}	Illumination power at wavelengths < 410nm(10) (17)			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ≥ 410nm and ≤ 800nm(15) (17)			60	W/cm^2
ILL_{IR}	Illumination power at wavelengths > 800nm(17)			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths ≥ 410nm and ≤ 475nm(15) (17)			20	W/cm^2
ILL_{BLU1}	Illumination power at wavelengths ≥ 410nm and ≤ 440nm(15) (17)			3.1	W/cm^2
Environmental(18) For Illumination Source 400nm – 420nm					
T_{ARRAY}	Array temperature, long-term operational(10) (11) (12) (13) (16)	20		30	°C
T_{WINDOW}	Window temperature, operational, TP2 and TP3	10		30	°C
T_{DELTA_MAX}	[maximum of TP2 or TP3] minus T_{MIN_ARRAY} (16)			5	°C
T_{DELTA_MIN}	[minimum of TP2 or TP3] minus T_{MAX_ARRAY} (16)	–10			°C
RH	Relative humidity (non-condensing)			95%	
Duty Cycle	Operating Landed Duty Cycle(20)		50%		
Illumination 400nm – 420nm(19)					
ILL_{UV}	Illumination power at wavelengths < 400nm(10) (17)			10	mW/cm^2
ILL_{BLU2}	Illumination power at wavelengths ≥ 400nm and ≤ 420nm(15) (17)			22.5	W/cm^2

(1) Section 5.4 are applicable after the DMD is installed in the final product.
(2) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(3) All voltage values are with respect to the V_{SS} ground pins.
(4) V_{OFFSET} supply transients must fall within specified max voltages.
(5) To prevent excess current, the supply voltage delta | $V_{DDA} – V_{DD}$ | must be less than specified limit.
(6) To prevent excess current, the supply voltage delta | $V_{BIAS} – V_{OFFSET}$ | must be less than specified limit.
(7) LVCMOS input pin is DMD_DEN_ARSTZ.
(8) See the high-speed serial interface (HSSI) timing requirements in Section 5.8.
(9) See the low-speed interface (LSIF) timing requirements in Section 5.8.
(10) Simultaneous exposure of the DMD to the maximum Section 5.4 for temperature and UV illumination will reduce device lifetime.
(11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 6-1, and the package thermal resistances using the calculation.
(12) The maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to Section 6.8.1 for a definition of micromirror landed duty cycle.
(13) Long-term is defined as the usable life of the device.
(14) Short-term is defined as the cumulative time over the usable life of the device.
(15) The maximum optical power that can be incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature T_{ARRAY}.
(16) Refer to Section 6.6 for calculation examples.
(17) Refer to Section 6.7 for calculation examples.

(18) Optimal, long-term performance and optical efficiency of the digital micromirror device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty-cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.

(19) This is the illumination power density and illumination total power on the DMD and does not include illumination overfill of the DMD device outside the active array.

(20) Landed Duty Cycle refers to the percentage of time an individual micromirror spends landed in one state (12° or –12°) versus the opposite state (–12° or 12°). 50% equates to a 50/50 duty cycle where the mirror has been landed 50% in the on-state and 50% in the off-state. See Section 7.8 for more information on landed duty cycle.

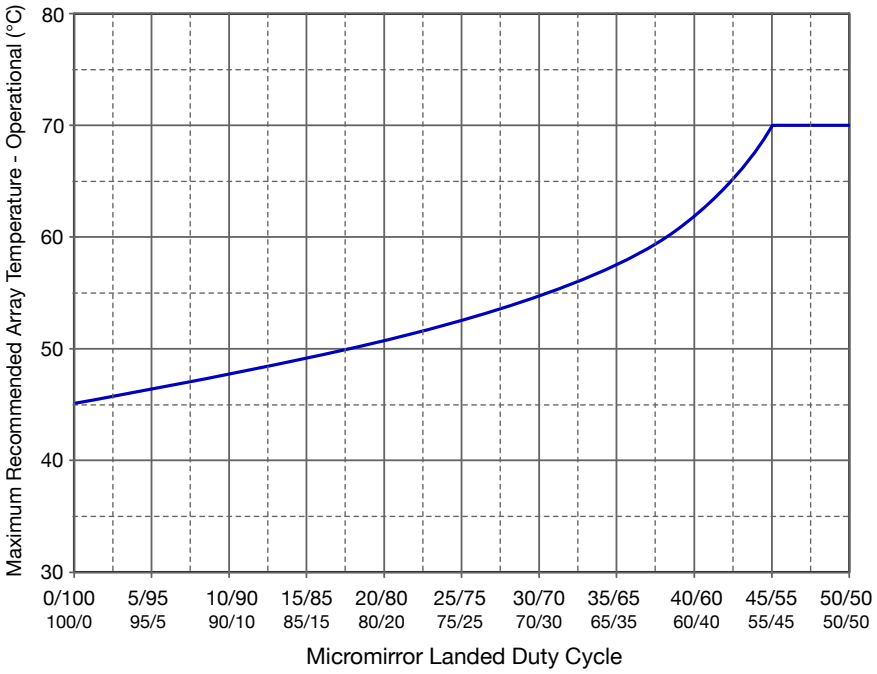


Figure 5-1. Maximum Recommended Array Temperature—Derating Curve for 410nm–800nm (Visible Wavelengths)

5.5 Thermal Information

THERMAL METRIC		DLP991U FLV PACKAGE 321 PINS	UNIT
$R_{MAX\_ARRAY\_TO\_CERAMIC}$	Thermal Resistance, active area Maximum to test point 1 (TP1) (1)	0.55	°C/W
$R_{MIN\_ARRAY\_TO\_CERAMIC}$	Thermal Resistance, active area Minimum to test point 1 (TP1) (1)	0.30	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device. Refer to Figure 6-1 for TP1 location.

5.6 Electrical Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER (2) (3)	TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
Current — Typical						
I_{DD}	Supply current V_{DD} (4)			1.5	1.9	A
I_{DDA}	Supply current V_{DDA} (4)			1.4	1.9	A
I_{OFFSET}	Supply current V_{OFFSET} (5) (6)			37	50	mA

5.6 Electrical Characteristics (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER (2) (3)	TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
I_{BIAS}	Supply current V_{BIAS} (5) (6)			12.0	50	mA
I_{RESET}	Supply current V_{RESET} (6)		–50	–25		mA
Power — Typical						
P_{DD}	Supply power dissipation V_{DD} (4)			2710	3710	mW
P_{DDA}	Supply power dissipation V_{DDA} (4)			2500	3600	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} (5) (6)			370	525	mW
P_{BIAS}	Supply power dissipation V_{BIAS} (5) (6)			216	925	mW
P_{RESET}	Supply power dissipation V_{RESET} (6)			350	725	mW
P_{TOTAL}	Supply power dissipation Total			6146	9485	mW
LVCMOS Input						
I_{IL}	Low level input current (7)	V_{DD} = 1.95V, V_I = 0V	–100			nA
I_{IH}	High level input current (7)	V_{DD} = 1.95V, V_I = 1.95V			135	µA
LVCMOS Output						
V_{OH}	DC output high voltage (8)	I_{OH} = –2mA	0.8 × V_{DD}			V
V_{OL}	DC output low voltage (8)	I_{OL} = 2mA			0.2 × V_{DD}	V
Receiver Eye Characteristics						
A1	Minimum eye opening for Data Lane(9)		100			mV
	Minimum eye opening for CLK Lane(9)		300			mV
A2	Maximum signal swing (9) (10)				600	mV
X1	Maximum eye closure (9)				0.275	UI
X2	Maximum eye closure (9)				0.4	UI
| t_{DRIFT} |	Drift between Clock and Data between Training Patterns				20	ps
Capacitance						
C_{IN}	Input capacitance LVCMOS	f = 1MHz			30	pF
C_{IN}	Input capacitance LSIF (low speed interface)	f = 1MHz			20	pF
C_{IN}	Input capacitance HSSI (high speed serial interface) - Differential - Clock and Data pins	f = 1MHz			5	pF
C_{OUT}	Output capacitance	f = 1MHz			10	pF

(1) Device electrical characteristics are over Recommended Operating Conditions unless otherwise noted.
(2) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(3) All voltage values are with respect to the ground pins (V_{SS}).
(4) To prevent excess current, the supply voltage delta | V_{DDA} – V_{DD} | must be less than specified limit.
(5) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than specified limit.
(6) Power dissipation based upon 1 Phased reset, 1 array load, and 1 global reset in 90µs
(7) The LVCMOS input specification is for pin DMD_DEN_ARSTZ.
(8) The LVCMOS output specification is for pins LS_RDATA_A and LS_RDATA_B.
(9) Refer to Figure 5-11, Receiver Eye Mask (1e-12 BER).
(10) Defined in Section 5.4.

5.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Output propagation, Clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. (1)	C_L = 5pF			11.1	ns

5.7 Switching Characteristics (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Output propagation, Clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. (1)	C_L = 10pF			11.3	ns
	Slew rate, LS_RDATA	20%–80%, C_L <10p	0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) See Figure 5-2.

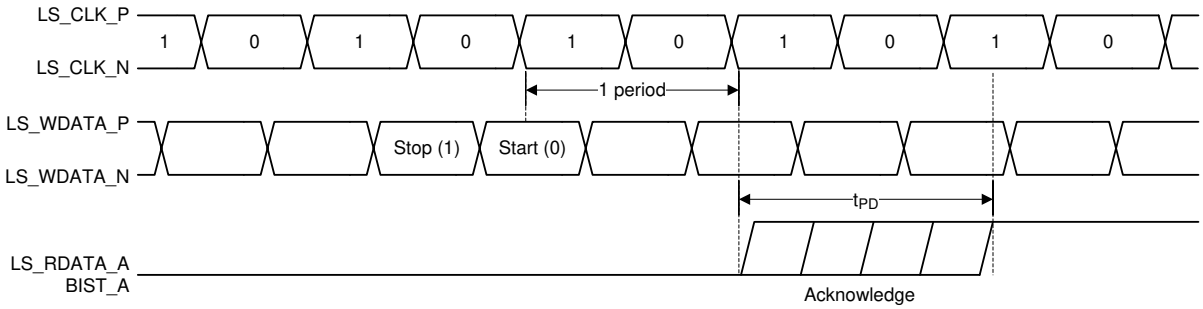


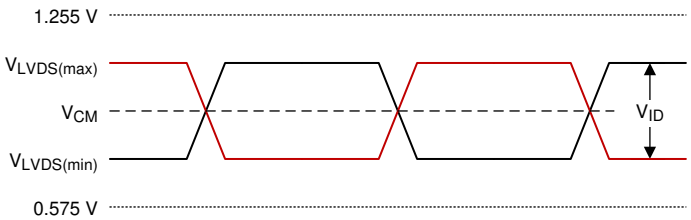
Figure 5-2. Switching Characteristics

5.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS						
t_r	Rise time (1)	20% to 80% reference points			25	ns
t_f	Fall time (1)	80% to 20% reference points			25	ns
Low Speed Interface (LSIF)						
t_r	Rise time (2)	20% to 80% reference points			450	ps
t_f	Fall time (2)	80% to 20% reference points			450	ps
t_{su}	Setup time(3)	LS_WDATA valid before rising edge of LS_CLK (differential)	1.5			ns
t_h	Hold time (3)	LS_WDATA valid after rising edge of LS_CLK (differential)	1.5			ns
High Speed Serial Interface (HSSI)						
t_r	Rise time (4)	from -A1 to A1 minimum eye height specification	50		100	ps
t_f	Fall time (4)	from A1 to -A1 minimum eye height specification	50		100	ps

(1) See Figure 5-9 for rise time and fall time for LVCMOS.
(2) See Figure 5-5 for rise time and fall time for LSIF.
(3) See Figure 5-4 for setup and hold time for LSIF.
(4) See Figure 5-10 for rise time and fall time for HSSI.



$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (1)$$

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (2)$$

Figure 5-3. LSIF Waveform Requirements

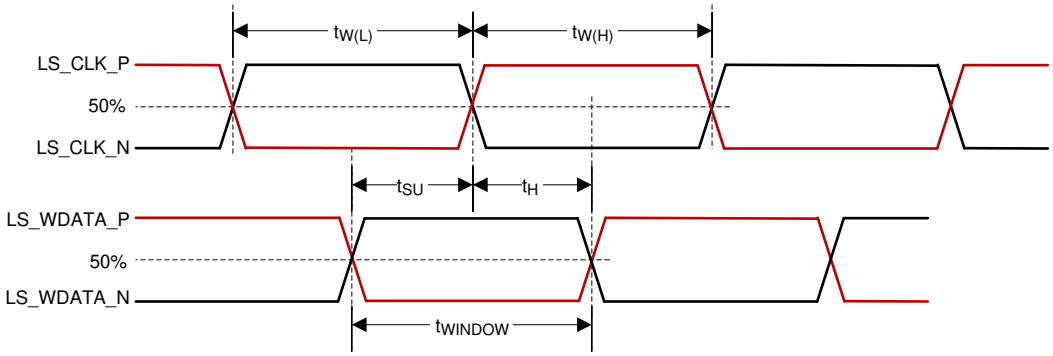


Figure 5-4. LSIF Timing Requirements

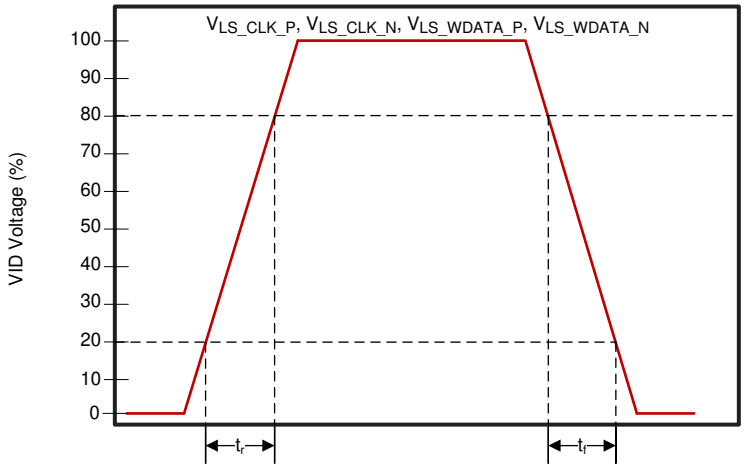


Figure 5-5. LSIF Rise, Fall Time Slew

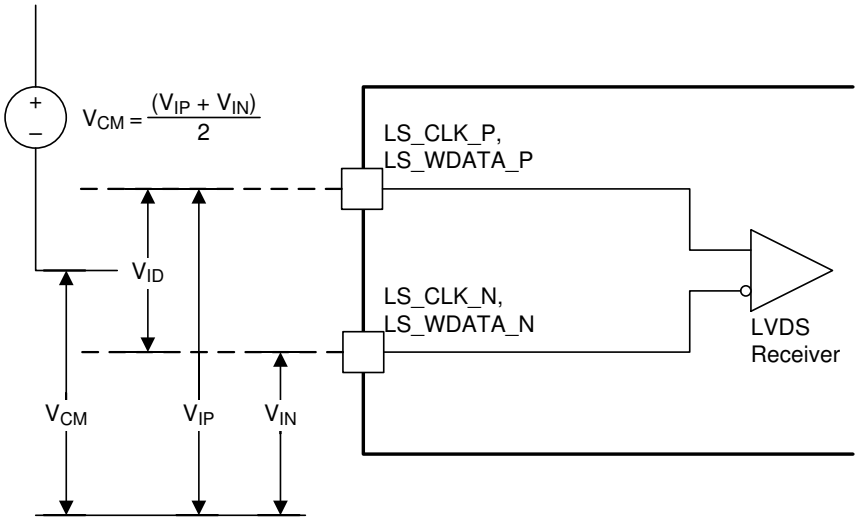


Figure 5-6. LSIF Voltage Requirements

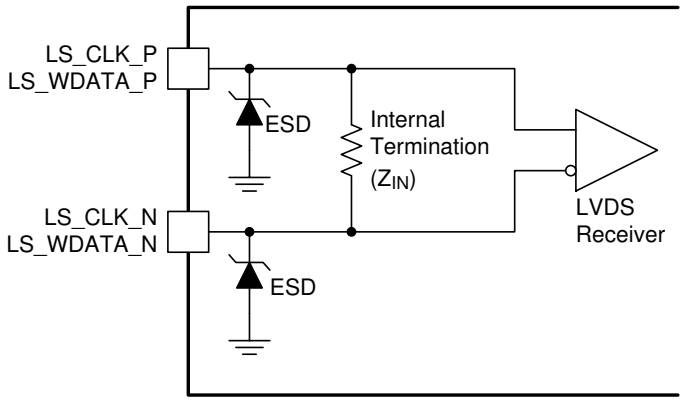


Figure 5-7. LSIF Equivalent Input

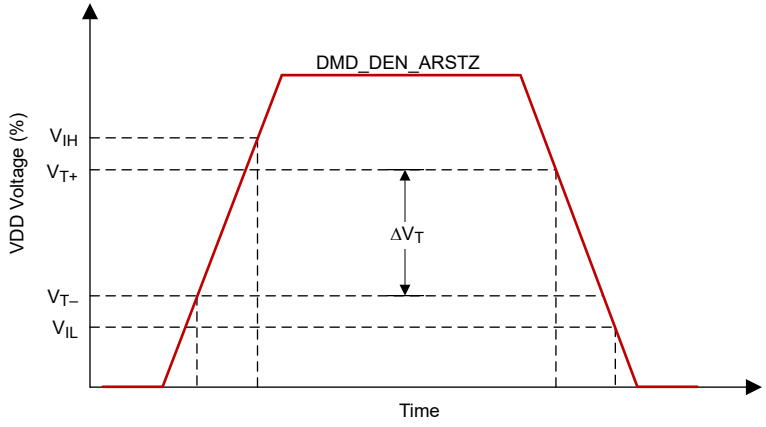


Figure 5-8. LVCMOS Input Hysteresis

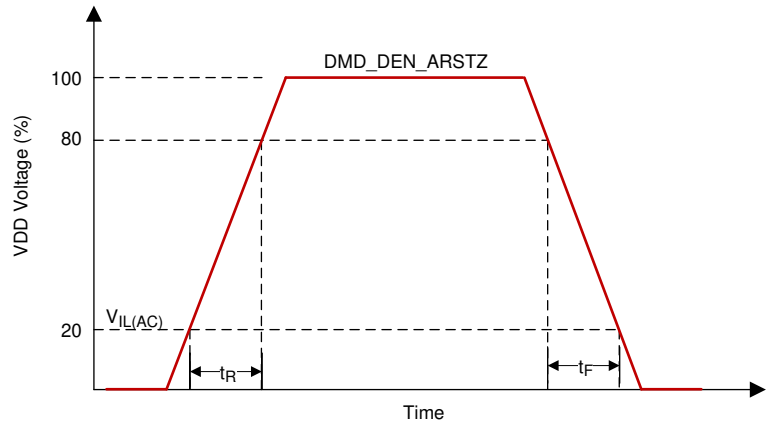
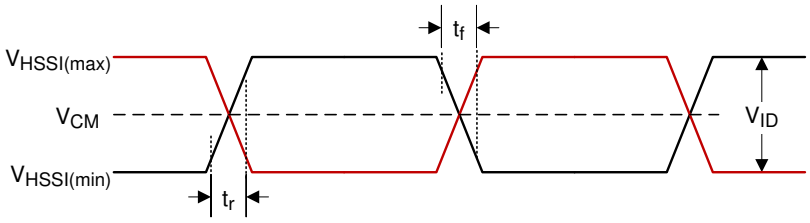


Figure 5-9. LVCMOS Rise, Fall Time Slew Rate



$$V_{HSSI\,(max\,)} = V_{CM\,(max\,)} + \left|\frac{1}{2} \times V_{ID\,(max\,)}\right| \quad (3)$$

$$V_{HSSI\,(min\,)} = V_{CM\,(min\,)} - \left|\frac{1}{2} \times V_{ID\,(max\,)}\right| \quad (4)$$

Figure 5-10. HSSI Waveform Requirements

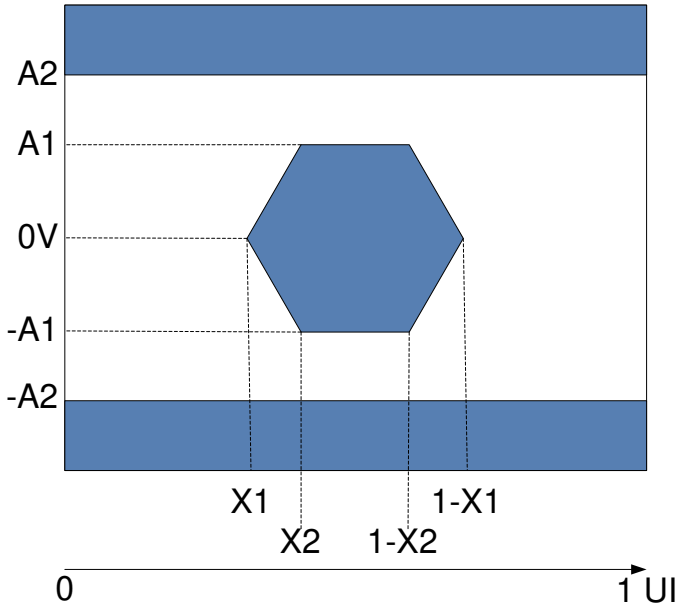


Figure 5-11. HSSI Eye Characteristics

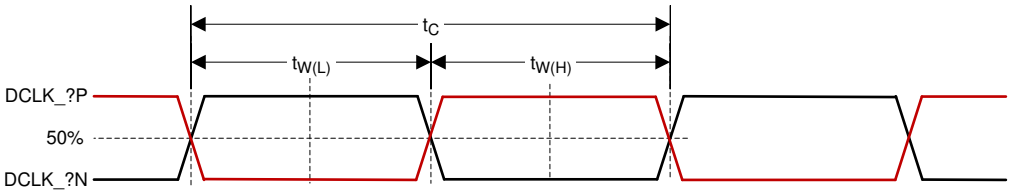


Figure 5-12. HSSI CLK Characteristics

5.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
Maximum load to be applied to the electrical interface area(2)			1334	N
Maximum load to be applied to the Datum A interface area(1) (2)			712	N
Maximum load to be applied to the thermal interface area(2)			200	N

(1) Combined loads of the thermal and electrical interface areas in excess of the Datum A load shall be evenly distributed outside the Datum A area (1334+200 – Datum A), or the combined loads of the thermal and electrical areas reduced.
(2) Uniformly distributed within area shown in Figure 5-13.

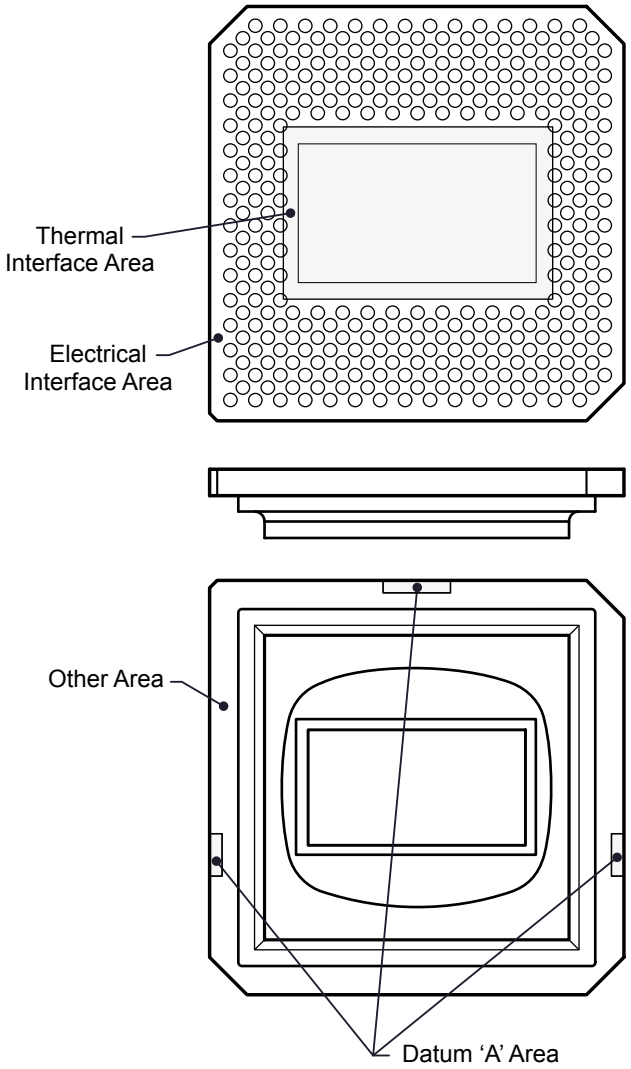


Figure 5-13. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

PARAMETER	DESCRIPTION	VALUE	UNIT
M	Number of active columns (1)	4096	micromirrors
N	Number of active rows (1)	2176	micromirrors
P	Micromirror (pixel) pitch(1)	5.4	µm
Micromirror active array width(1)	Micromirror pitch × number of active columns	22.1184	mm
Micromirror active array height(1)	Micromirror pitch × number of active rows	11.7504	mm
Micromirror active border (top and bottom)(2)	Pond of micromirror (POM)	20	micromirrors/side
Micromirror active border (right and left)(2)	Pond of micromirror (POM)	20	micromirrors/side

(1) See Figure 5-14.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

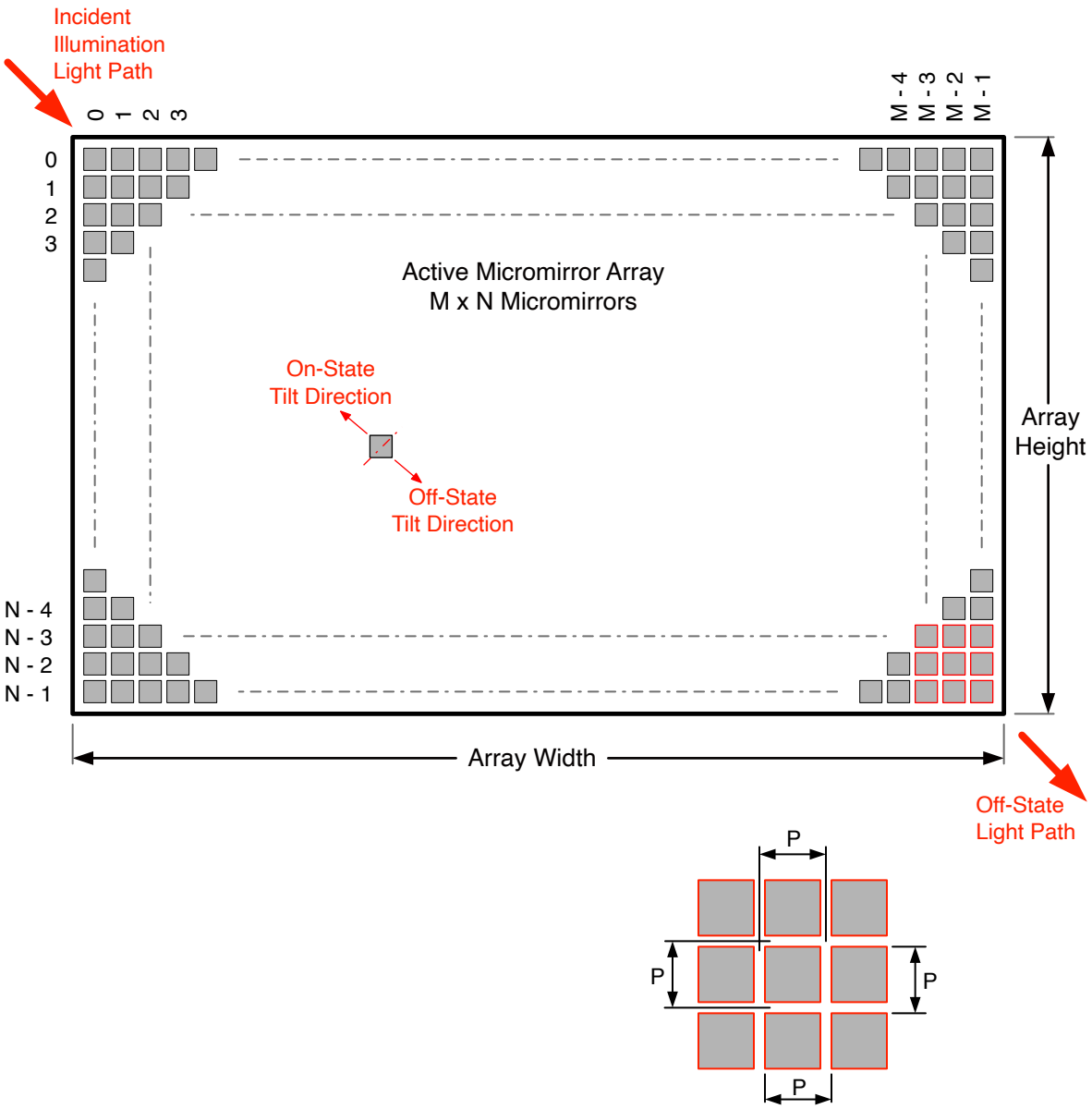


Figure 5-14. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Micromirror tilt angle(2) (3) (4) (5)	landed state(1)	11		13	Degrees
COT	Micromirror crossover time(6)	typical performance		1	3	µs
	Micromirror switching time(7)	typical performance	4			µs
	Orientation of the micromirror axis-of-rotation(8)		44		46	Degrees
	Micromirror array optical efficiency(9) (10)	400nm to 420nm, with all micromirrors in the ON state		66%		
	Micromirror array optical efficiency(9) (10)	410nm to 800nm, with all micromirrors in the ON state		63%		
	Non-operating micromirrors(11)	Non-adjacent micromirrors			10	micromirrors
		Adjacent micromirrors			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(7) The minimum time between successive transitions of a micromirror at the end of a Mirror Clocking Pulse to the beginning of the next Mirror Clocking Pulse.
(8) Measured relative to the package datums 'B' and 'C'.
(9) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:

- Illumination wavelength, bandwidth/line-width, degree of coherence
- Illumination Angle, plus angle tolerance
- Illumination and projection aperture size, and location in the system optical path
- Illumination overfill of the DMD micromirror array
- Aberrations present in the illumination source and/or illumination path
- Aberrations present in the projection path

The specified nominal DMD optical efficiency is based on the following use conditions:

- Visible illumination (400 to 800 nm)
- Input illumination optical axis oriented at 24° relative to the window normal
- Projection optical axis oriented at 0° relative to the window normal
- f / 3 illumination aperture
- f / 2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- Micromirror array fill factor: nominally 90%
- Micromirror array diffraction efficiency: nominally 86%
- Micromirror surface reflectivity: nominally 88%
- Window transmission: nominally 97% (single pass, through two surface transitions)

(10) Does not account for the effect of micromirror switching duty cycle, which is application dependent. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.
(11) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the "OFF" position to the "ON" position or vice versa.

5.12 Window Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Window material			Corning 7056		
Window refractive index	at wavelength 589nm		1.487		
Window transmittance, minimum within the wavelength range 400nm–800nm	Applies to all angles 0–30 AOI (1) (2)	97			%
Window transmittance, average over the wavelength range 400nm–800nm	Applies to all angles 30–45 AOI (1) (2)	97			%

(1) Single-pass through both surfaces and glass
(2) AOI—The angle of incidence is the angle between an incident ray and the normal to a reflecting or refracting surface.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLPC991U DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

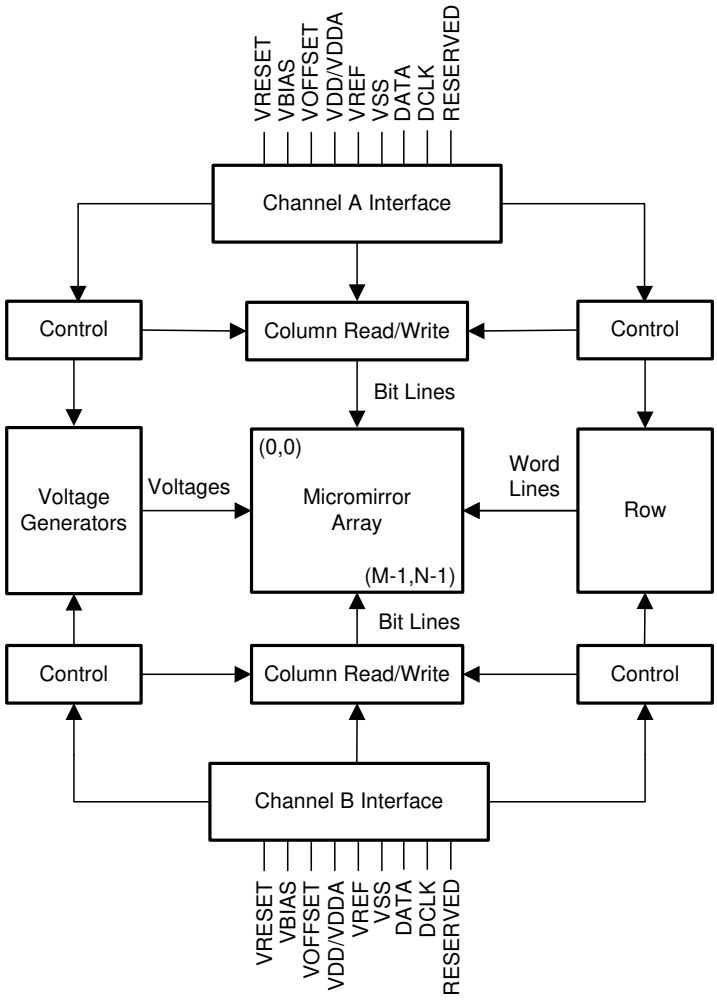
6 Detailed Description

6.1 Overview

The DLP991U DMD is a 0.99-inch diagonal spatial light modulator that consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The input electrical data interface is a differential high-speed serial interface (HSSI). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to Figure 5-14. The positive or negative deflection angle of the micromirrors can be individually controlled by writing a '1' or a '0' to each memory cell thereby changing the address voltage of underlying CMOS addressing circuitry.

To ensure reliable operation, the DLP991U DMD must always be used with the TI-provided DLPC964 industrial controller.

6.2 Functional Block Diagram



For pin details on Channels A, B, C, and D, refer to Section 4 and HSSI Interface section of Section 5.8.
Channels C and D are connected identically as A and B, but were omitted from this image for clarity.

6.3 Feature Description

6.3.1 Power Interface

The DLP991U DMD requires five DC voltages for proper operation: V_{DD}, V_{DDA}, V_{OFFSET}, V_{RESET}, and V_{BIAS}. VDD/VDDA power inputs require a 1.9V power supply. V_{OFFSET} (10V), V_{RESET} (–14V), and V_{BIAS} (18V) are supplied to the DMD to enable micromirror actuation control.

6.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the display controller. See the *DLPC964 Digital Micromirror Device Controller Data Sheet* or contact a TI applications engineer for more information.

6.5 Optical Interface and System Image Quality Considerations

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to have zero light flux incident anywhere on the window aperture. Depending on the

particular system's optical architecture, overfill light may have to be further reduced below the maximum 10% level in order to be acceptable.

6.6 DMD Temperature Calculation

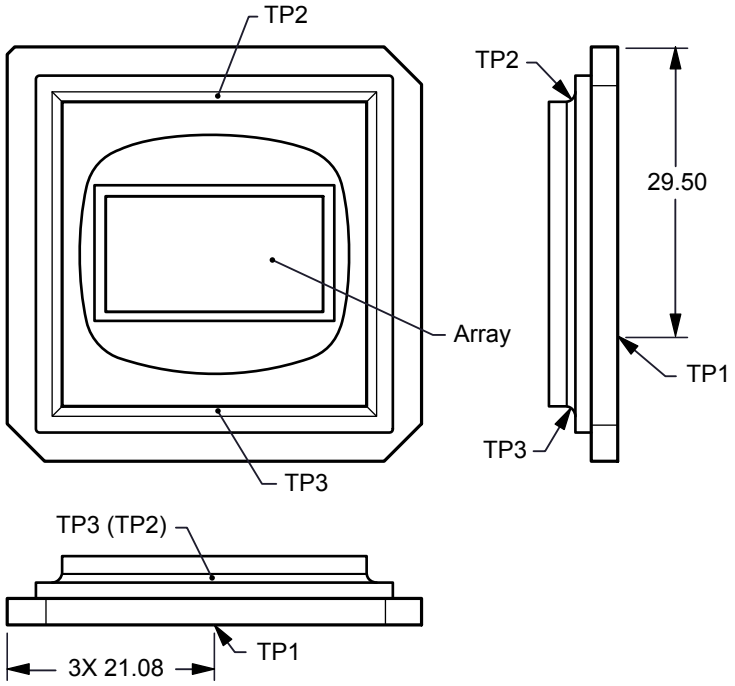


Figure 6-1. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{MAX\_ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{MAX\_ARRAY\text{-}TO\text{-}CERAMIC})$$

$$T_{MIN\_ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{MIN\_ARRAY\text{-}TO\text{-}CERAMIC})$$

$$T_{DELTA\_MIN} = [\text{minimum of TP2 or TP3}] - T_{MAX\_ARRAY}$$

$$T_{DELTA\_MAX} = [\text{maximum of TP2 or TP3}] - T_{MIN\_ARRAY}$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (Watts) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power
- $Q_{INCIDENT}$ = Total incident optical power to DMD
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$)
- DMD average thermal absorptivity on-state = 0.25
- DMD average thermal absorptivity off-state = 0.40

The electrical power dissipation of the DMD ($Q_{ELECTRICAL}$) is variable and depends on the voltages, data rates and operating frequencies of each specific application system. $Q_{ELECTRICAL}$ should be measured in each specific application to determine the proper value of $Q_{ELECTRICAL}$ to use in the equations below. To calculate array temperature, the value for electrical power dissipation of the DMD ($Q_{ELECTRICAL}$) used in the example calculations below is 6.2 Watts (Typ). The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for each DMD chip in a system. It assumes an illumination distribution of 91.0% on the active array, and 9.0% on the array border.

Sample calculations for off-state and on-state are shown below.

6.6.1 Off-State Thermal Differential (T_{DELTA_MIN})

TP1 (ceramic) = 25.0°C (measured)

TP2 (window) = 50.0°C (measured)

TP3 (window) = 47.0°C (measured)

$Q_{INCIDENT}$ = 150W (measured)

$Q_{ELECTRICAL}$ = 6.2W

$R_{MAX\_ARRAY\text{-}TO\text{-}CERAMIC}$ = 0.55°C/W

Q_{ARRAY} = 6.2W + (150W × 0.40) = 66.2W

T_{MAX_ARRAY} = 25.0°C + (66.2W × 0.55°C/W) = 61.4°C

T_{DELTA_MIN} = [minimum of TP2 or TP3] –T_{MAX_ARRAY} = 47.0°C – 61.4°C = –14.4°C

6.6.2 On-State Thermal Differential (T_{DELTA_MAX})

TP1 (ceramic) = 22.0°C (measured)

TP2 (window) = 38.0°C (measured)

TP3 (window) = 35.0°C (measured)

$Q_{INCIDENT}$ = 150W (measured)

$Q_{ELECTRICAL}$ = 6.2W

$R_{MIN\_ARRAY\text{-}TO\text{-}CERAMIC}$ = 0.30°C/W

Q_{ARRAY} = 6.2W + (150W × 0.25) = 43.7W

T_{MIN_ARRAY} = 22.0°C + (43.7W × 0.30°C/W) =35.1°C

T_{DELTA_MAX} = [maximum of TP2 or TP3] –T_{MIN_ARRAY} = 38.0°C – 35.1°C = 2.9°C

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000$ (mW/W) ÷ A_{ILL} (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000$ (mW/W) ÷ A_{ILL} (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU2} = [OP_{BLU2\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 – OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- ILL_{BLU2} = BLU2 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤440nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU2\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥400nm and ≤420nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample Calculation—Illumination 410nm – 800nm (Visible Wavelengths)

$Q_{INCIDENT}$ = 150W (measured)

A_{ARRAY} = (22.1184mm × 11.7504mm) ÷ 100 (mm/cm) = 2.599cm^2 (data sheet)

OV_{ILL} = 9% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00017 (spectral measurement)

$OP_{VIS\text{-}RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR\text{-}RATIO}$ = 0.00006 (spectral measurement)

$OP_{BLU\text{-}RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1\text{-}RATIO}$ = 0.03200 (spectral measurement)

A_{ILL} = 2.599cm^2 ÷ (1 – 0.09) = 2.8560cm^2

ILL_{UV} = [0.00017 × 150W] × 1000 (mW/W) ÷ 2.8560cm^2 = 8.928mW/cm^2

ILL_{VIS} = [0.99977 × 150W] ÷ 2.8560cm^2 = 52.51W/cm^2

ILL_{IR} = [0.00006 × 150W] × 1000 (mW/W) ÷ 2.8560cm^2 = 3.151mW/cm^2

ILL_{BLU} = [0.28100 × 150W] ÷ 2.8560cm^2 = 14.76W/cm^2

ILL_{BLU1} = [0.03200 × 150W] ÷ 2.8560cm^2 = 1.68W/cm^2

Sample Calculation—Illumination 400nm – 420nm

$Q_{INCIDENT}$ = 33W (measured)

A_{ARRAY} = (22.1184mm × 11.7504mm) ÷ 100 (mm/cm) = 2.599cm^2 (data sheet)

OV_{ILL} = 9% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00076 (spectral measurement)

$OP_{BLU2\text{-}RATIO}$ = 0.99924 (spectral measurement)

A_{ILL} = 2.599cm^2 ÷ (1 – 0.09) = 2.8560cm^2

ILL_{UV} = [0.00076 × 33W] × 1000 (mW/W) ÷ 2.8560cm^2 = 8.782mW/cm^2

ILL_{BLU2} = [0.99924 × 33W] ÷ 2.8560cm^2 = 11.546W/cm^2

6.8 Micromirror Landed-On/Landed-Off Duty Cycle

6.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the On state 75% of the time (and in the Off state 25% of the time); whereas 25/75 would indicate that the pixel is in the Off state 75% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

6.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 5-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a given long-term average Landed Duty Cycle.

6.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 6-1.

Table 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70

Table 6-1. Grayscale Value and Landed Duty Cycle (continued)

GRAYSCALE VALUE	LANDED DUTY CYCLE
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). DMDs vary in resolution and size and can contain over 8.9 million micromirrors. Each micromirror of a DMD is independently controlled and can be synchronized with illuminators and cameras to enable a wide range of applications. DLP technology enables a wide variety of Industrial products worldwide, from digital imaging engines embedded in large lithography machines to high-resolution 3D Printing machines.

The most recent class of chipsets from Texas Instruments is based on a breakthrough micromirror technology, called SST. With a smaller pixel pitch of 5.4µm and a tilt angle of 12 degrees, SST chipsets enable higher resolution in a smaller form factor and enhanced image processing features while maintaining high optical efficiency. DLP chipsets are a great fit for any system that values high-resolution projection at high-modulation speeds.

7.2 Typical Application

The DLP991U DMD is a 4096 × 2176 resolution DLP digital micromirror device. When combined with the TI DLPC964 industrial controller and other electrical, optical and mechanical components the DLP991U DMD provides a superior solution for industrial direct imaging and 3D printer applications. Figure 7-1 shows a typical single-chip system application using the DLP991U DMD.

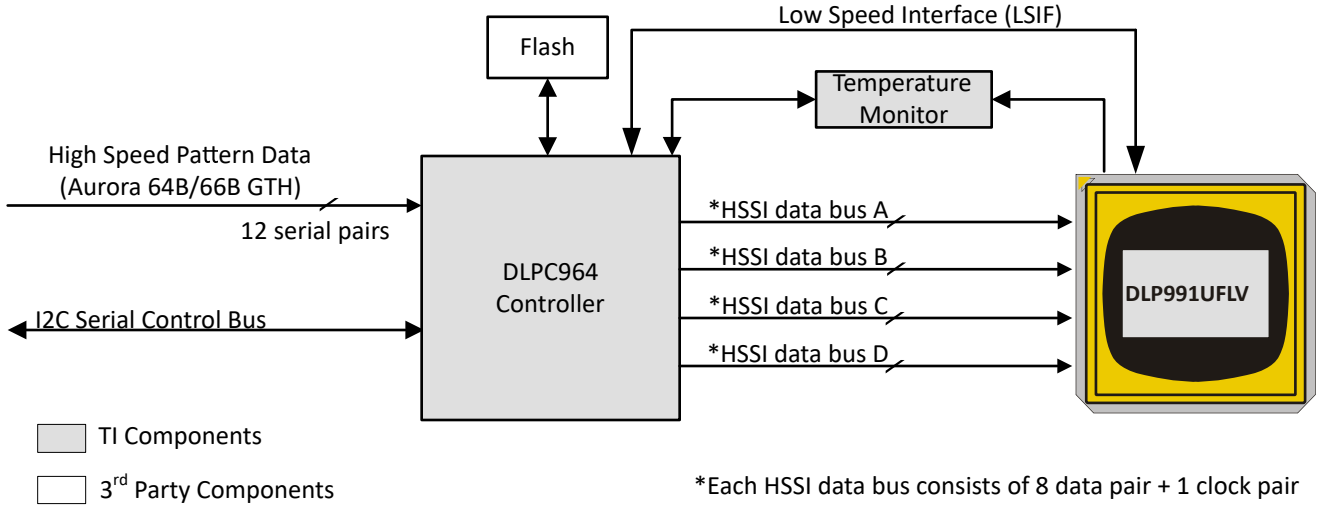


Figure 7-1. Typical DLP991U Application Diagram

Table 7-1. DMD Overview

DMD	ARRAY	SINGLE ROW LOAD TIME (ns)	SINGLE BLOCK LOAD TIME (µs)	GLOBAL RESET MODE FULL ARRAY (PATTERNS/ SECOND)	QUAD BLOCK RESET MODE FULL ARRAY (PATTERNS/ SECOND)
DLP991U	4096 × 2176	37.09	5.04	11,273	12,390

7.2.1 Design Requirements

At a high level, DLP991U DMD systems include an illumination source, a light engine, electronic components, and software. The designer must first choose an illumination source and design the optical engine taking into consideration the relationship between the optics and the illumination source. The designer must then understand the electronic components of a DMD system. The application PCB board supports all of the required electronic components to power and control the DLP991U DMD, which can include the DLPC964 industrial controller, power supplies, and the DMD device.

7.2.2 Detailed Design Procedure

For customer assistance in designing the electrical connections between the DLPC964 Industrial Controller and the DLP991U DMD, TI provides a reference design schematic and layout guidelines which are recommended to be followed to achieve a reliable projection subsystem. To complete the DLP system an optical module or light engine is required that contains the DMD, associated illumination sources, optical elements, necessary mechanical components, and recommended thermal design concepts and guidelines.

7.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP461 temperature sensor, as shown in Figure 7-2. The serial bus from the TMP461 can be connected to the DLPC964 industrial controller to enable its temperature sensing features. See the *DLPC964 Digital Micromirror Device Controller Data Sheet* for more information about how to query the temperature readings.

The DLPC964 industrial controller can configure the TMP461 to read the DMD temperature sensor diode. This data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination power, fan speeds, active cooling temperatures, or flow rates, and so on. All communication between the TMP461 and the DLPC964 industrial controller are completed using the I^2C interface. The TMP461 connects to the DMD via pins E23 and F22, as outlined in Pin Configuration and Functions.

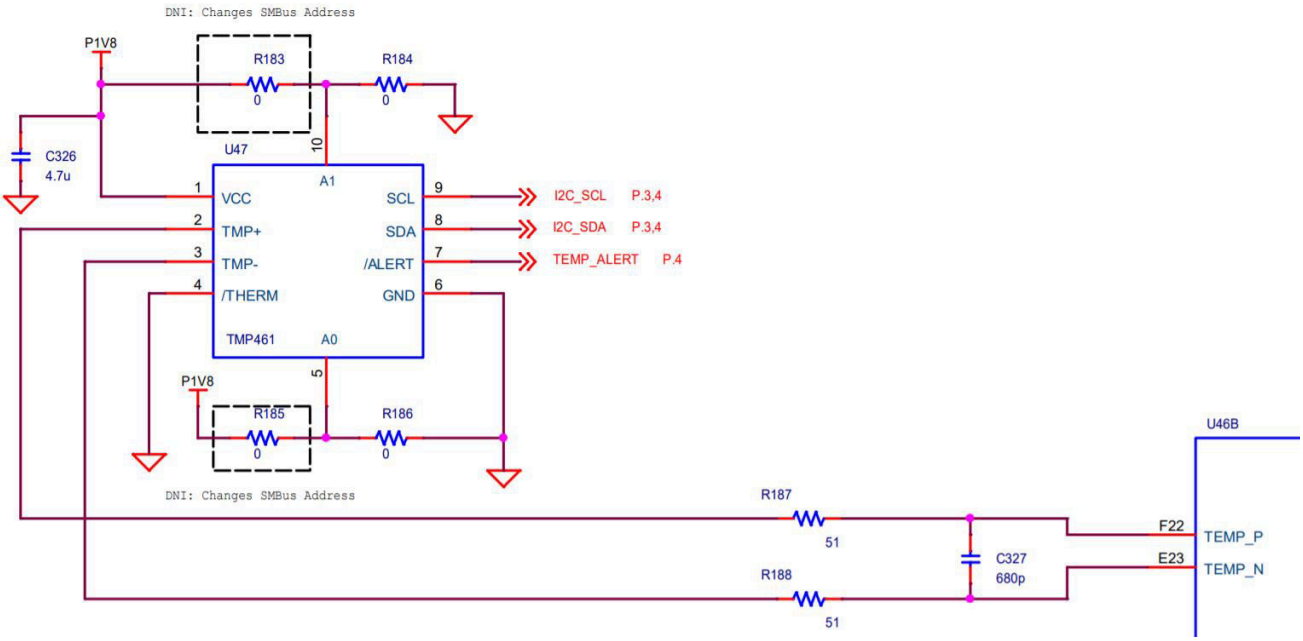


Figure 7-2. System Board Routing Example for Temperature Sensor

1. Details are omitted for clarity. See the TI reference design for connections to the DLPC964 industrial controller.
2. See the TMP461 Data Sheet for system board layout recommendations.

3. See the TMP461 Data Sheet and the TI Reference Design for suggested component values for R1, R2, R3, R4, and C1.
4. R5 = 0Ω. R6 = 0Ω. Zero ohm resistors should be located close to the DMD package pins.

7.4 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{DD}, V_{DDA}, V_{BIAS}, V_{OFFSET}, and V_{RESET}. DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

Note

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See Figure 7-3 DMD Power Supply Sequencing Requirements.

V_{DD}, V_{DDA}, V_{BIAS}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD's reliability and lifetime. Common ground VSS must also be connected.

Table 7-2. Power Supply Sequence Requirements

SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY}	Delay requirement	from V_{OFFSET} power up to V_{BIAS} power up	2			ms
V_{OFFSET}	Supply voltage level	at beginning of power-up sequence delay(1)			6	V
V_{BIAS}	Supply voltage level	at end of power-up sequence delay(1)			6	V

(1) See Sequence Delay Requirement.

7.4.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDA} must always start and settle before V_{OFFSET} plus Delay1 specified in Table 7-3, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Section 5.4.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in Section 5.1, in Section 5.4, and in Figure 7-3.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} and V_{DDA} have settled at operating voltages listed in Section 5.4.

7.4.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} and V_{DDA} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See Table 7-3.
- During power-down, it is a strict requirement that the voltage delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Section 5.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in Section 5.1, in Section 5.4, and in Figure 7-3.
- During power-down, LVCMOS input pins must be less than specified in Section 5.4.

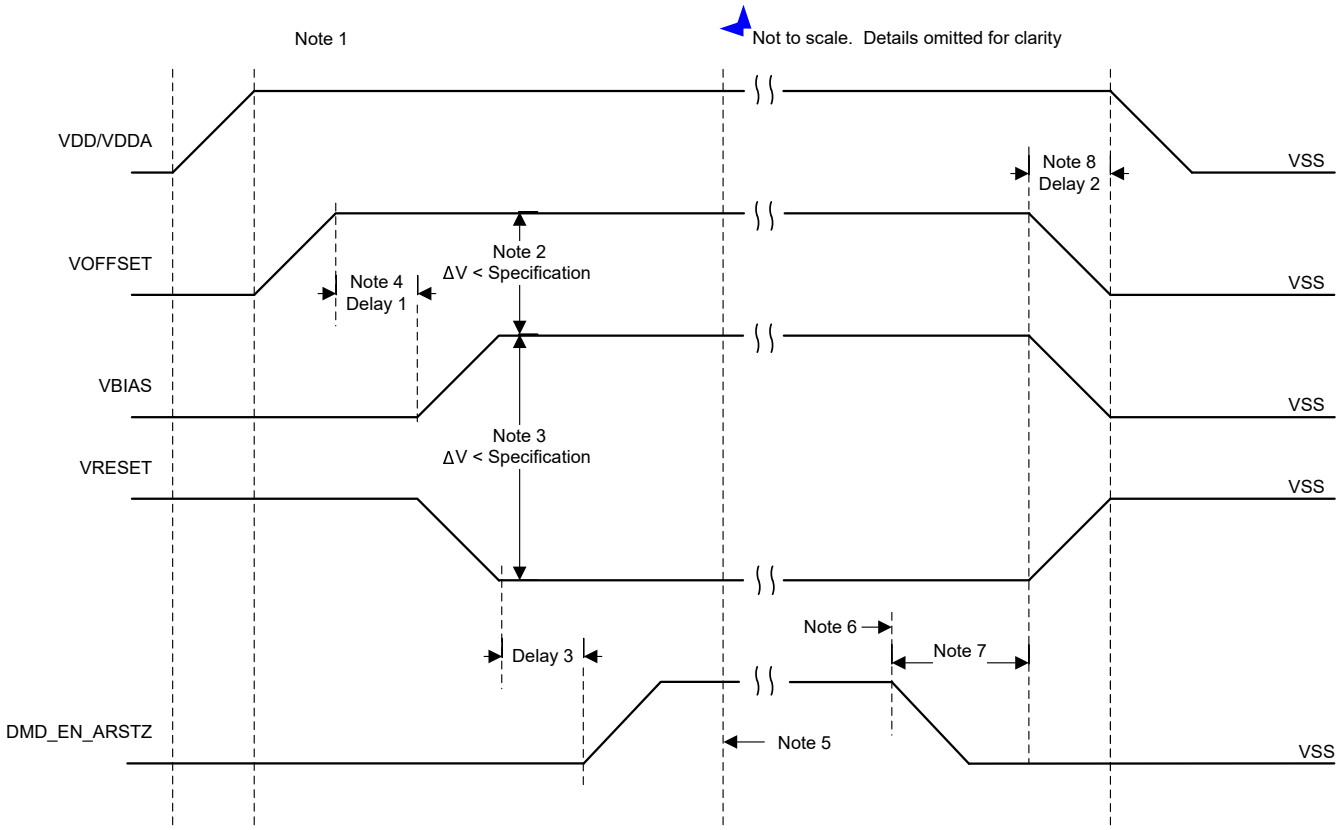


Figure 7-3. DMD Power Supply Requirements

1. See Section 4.
2. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified in Section 5.4.
3. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than specified limit in Section 5.4.
4. V_{BIAS} should power up after V_{OFFSET} has powered up, per the Delay1 specification in Table 7-3.
5. DLP controller software initiates the global V_{BIAS} command.
6. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET}, and V_{OFFSET}.
7. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware DMD_EN_ARSTZ will go low.
8. V_{DD} / V_{DDA} must remain above the minimum values specified in Section 6.4 until after V_{OFFSET}, V_{BIAS}, V_{RESET} go low, per Delay2 specification in Table 7-3.
9. To prevent excess current, the supply voltage delta $|V_{DDA} – V_{DD}|$ must be less than specified limit in Section 5.4.

Table 7-3. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1	Delay from V_{OFFSET} settled at recommended operating voltage to V_{BIAS} and V_{RESET} power up.	1	2		ms
Delay2	Delay V_{DD} must be held high from V_{OFFSET}, V_{BIAS} and V_{RESET} powering down.	50			µs
Delay3	Delay from V_{BIAS} and V_{RESET} settled at recommended operating voltage to DMD_EN_ARSTZ being asserted.	20			µs

7.5 Layout

7.5.1 Layout Guidelines

These guidelines are targeted at designing a PCB board with the DLP991U DMD. The DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic including 3.6Gbps differential data buses run to the DMD. Use full or mini power planes for V_{OFFSET}, V_{RESET}, and V_{BIAS}. Solid planes are required for ground. The target impedance for single-ended traces on the PCB is 50Ω ±10% and 100Ω ±10% for differential traces, as outlined in Table 7-5. Manufacture the PCB with a high-quality FR-4 material.

7.5.1.1 PCB Design Standards

PCBs must be designed and built in accordance with the industry specifications shown in Industry Design Specifications.

Table 7-4. Industry Design Specifications

INDUSTRY SPECIFICATION	APPLICABLE TO
IPC-2221 and IPC-2222, Class 2, at Level B producibility	Board Design
IPC-6011 and IPC-6012, Class 2	PWB fabrication
IPC-SM-840, Class 3	Finished PWB solder mask
UL94V-0 Flammability Rating and Marking	Finished PWB
UL796 Rating and Marking	Finished PWB

7.5.1.2 General PCB Routing

7.5.1.2.1 Trace Impedance and Routing Priority

For best performance, TI recommends a target impedance for the PCB of 50Ω ±10% for single-ended signals. The differential signals that are 100Ω ±10% are described in Trace Impedance.

Table 7-5. Trace Impedance

SIGNALS	DIFFERENTIAL IMPEDANCE
HSSI DMD Interface—DMD_D_(A,B,C,D)[7:0], DMD_DCLK_(A,B,C,D)	100Ω differential
DMD LS Interface—DMD_LS_CLK, DMD_LS_WDATA	100Ω differential

Table 7-6 lists the routing priority of the signals.

Table 7-6. Routing Priority

SIGNALS	PRIORITY
HSSI DMD Interface - DMD_D_(A,B,C,D)[7:0], DMD_DCLK_(A,B,C,D)	1
DMD LS Interface - DMD_LS_CLK, DMD_LS_WDATA	2
All other signals	3

7.5.1.2.2 Example PCB Layer Stack-Up

Careful attention to the PCB layer design is required to meet system design requirements. Table 7-7 shows an example PCB stack-up. To maximize signal integrity of the high-speed differential signals that make up the HSSI DMD input interface, the differential signals are routed on the internal layers and referenced to solid ground planes. To further improve the signal integrity of the DMD board, Nelco N4000-13 SI is used as the dielectric material to improve the signal slew rate for better performance of the HSSI DMD Input Interface.

Table 7-7. Example PCB Layer Stack-Up

LAYER NUMBER	LAYER NAME	COPPER WEIGHT	COMMENTS
1	Side A—Primary Components	½ oz (before plating)	Top components, including power generation and data input connectors. Low frequency signals routing. Need copper fill (GND) plated up to 1oz. Impedance reference for layer #2
2	Signal (High-Frequency)	½ oz	High-speed signal layer, high-speed differential data buses from input connector to DMD. Data lines are kept underneath ground pour on layer #1.
3	Ground	½ oz	Solid ground plane (net GND) reference for signal layer #2, #4
4	Signal (High-Frequency)	½ oz	High-speed signal layer, high-speed differential data buses from input connector to DMD
5	Ground	½ oz	Solid ground plane (net GND) reference for signal layers #4, #6
6	Signal (High-Frequency)	½ oz	High-speed signal layer, high-speed differential data buses from input connector to DMD
7	Ground	½ oz	Solid ground plane (net GND) reference for signal layer #6, 8
8	Side B—DMD, Power Planes and Secondary Components	½ oz (before plating)1	DMD and escapes. Data input connectors. Primary split power planes for 1.8V, 3.3V, 10V, –14V, 18V. Discrete components if necessary. Low-frequency signals routing. Need copper fill plated up to 1oz.

1. As noted in the DLP991U DMD mechanical ICD drawing, the DMD device pads are plated with 50–100 micro-inches electrolytic nickel under 30 micro-inches minimum electrolytic gold.

7.5.1.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005"/0.0015" (Trace-Width/Spacing) design rule. Use an analysis of impedance and stack-up requirements to determine and calculate actual trace widths.

Maximize the width of all voltage signals as space permits.

Follow the width and spacing requirements listed in Table 7-8 and Table 7-9.

Table 7-8. Trace Minimum Spacing

SIGNAL	PWR	GND	SINGLE-ENDED	DIFFERENTIAL PAIRS	UNIT
				PAIR-TO-PAIR	
PWR	15	5	15	15	mils
GND	5		5	5	mils
HSSI DMD Interface —DMD_D_(A,B,C,D)[7:0], DMD_DCLK_(A,B,C,D),	15	5	3x intra-pair (P-to-N) spacing	3x intra-pair (P-to-N) spacing	mils
DMD LS Interface— DMD_LS_CLK, DMD_LS_WDATA, DMD_LS_RDATA_(A,B,C,D)	15	5	3x trace width spacing	3x intra-pair (P-to-N) spacing	mils
All other signals	15	5	3x trace width spacing	3x intra-pair (P-to-N) spacing	mils

Table 7-9. Voltage Trace Widths and Spacing Recommendations

SIGNAL NAME	MIN. TRACE WIDTH (mils)	MIN. TRACE SPACING (mils)	LAYOUT REQUIREMENTS
GND	Maximize	5	Maximize trace width to connecting pin as a minimum.
P3P3V	40	15	Create mini planes on layer 8 as needed. Connect to devices on layers 1 and 8 as necessary with multiple vias.
P1P9V	40	15	Create mini planes on layer 8 as needed. Connect to devices on layers 1 and 8 as necessary with multiple vias. Feedback resistor divider must be placed close to P1P9V load pins on DMD.
V_OFFSET (10V)	40	15	Create mini planes on layer 8 as needed. Connect to devices on layers 1 and 8 as necessary.
V_RESET (–14V)	40	15	Create mini planes on layer 8 as needed. Connect to devices on layers 1 and 8 as necessary.
V_BIAS (18V)	40	15	Create mini planes on layer 8 as needed. Connect to devices on layers 1 and 8 as necessary.

7.5.1.2.4 Power and Ground Planes

TI strongly discourages signal routing on power planes or on planes adjacent to power planes. If signals must be routed on layers adjacent to power planes, they must not cross splits in power planes to prevent EMI and preserve signal integrity.

Connect all internal digital ground (GND) planes in as many places as possible. Connect all internal ground planes with a minimum distance between connections of 0.5”. Extra vias may not be required if there are sufficient ground vias due to normal ground connections of devices.

Connect power and ground pins of each component to the power and ground planes with at least one via for each pin. Minimize trace lengths for component power and ground pins. (ideally, less than 0.100”).

Ground plane slots are strongly discouraged.

7.5.1.2.5 Trace Length Matching

7.5.1.2.5.1 HSSI Input Bus Skew

High-Speed Serial DMD Interface Routing Constraints lists the high-speed serial DMD interface routing constraints.

Table 7-10. High-Speed Serial DMD Interface Routing Constraints

SIGNAL	REFERENCE SIGNAL	ROUTING SPEC	UNIT
DMD_D_A{0…7}_P, DMD_D_A{0…7}_N	DMD_DCLK_A_P, DMD_DCLK_A_N	± 45	ps
DMD_D_B{0…7}_P, DMD_D_B{0…7}_N	DMD_DCLK_B_P, DMD_DCLK_B_N	± 45	ps
DMD_D_C{0…7}_P, DMD_D_C{0…7}_N	DMD_DCLK_C_P, DMD_DCLK_C_N	± 45	ps
DMD_D_D{0…7}_P, DMD_D_D{0…7}_N	DMD_DCLK_D_P, DMD_DCLK_D_N	± 45	ps

Table 7-10. High-Speed Serial DMD Interface Routing Constraints (continued)

SIGNAL	REFERENCE SIGNAL	ROUTING SPEC	UNIT
DMD_D_A bus	DMD_D_B bus	± 45	ps
DMD_D_C bus	DMD_D_D bus	± 45	ps
DMD_D_A bus	DMD_D_C bus	± 45	ps
Intra-pair P	Intra-pair N	± 2	ps

7.5.1.2.5.2 Other Timing Critical Signals

Other Timing Critical Signals lists the routing constraints for other timing critical signals.

Table 7-11. Other Timing Critical Signals

SIGNAL	CONSTRAINTS
DMD_LS_CLK_P DMD_LS_CLK_N DMD_LS_WDATA_P DMD_LS_WDATA_N DMD_LS_RDATA_{A,B,C,D}	Intra-pair (P-to-N) matched within ± 2ps. Differential pairs matched within ± 45ps of one another

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

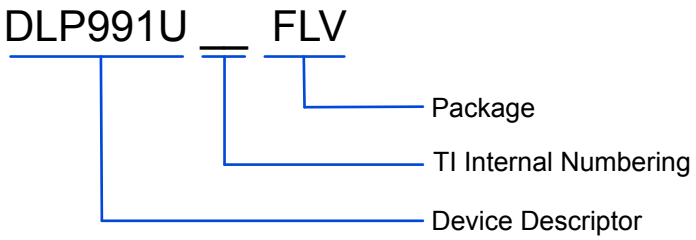


Figure 8-1. Part Number Description

8.1.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 8-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, part 1 of the serial number, and part 2 of the serial number. The first character of the DMD serial number (part 1) is the manufacturing year. The second character of the DMD serial number (part 1) is the manufacturing month.

Example: DLP991UFLV GHXXXXX LLLLLLM

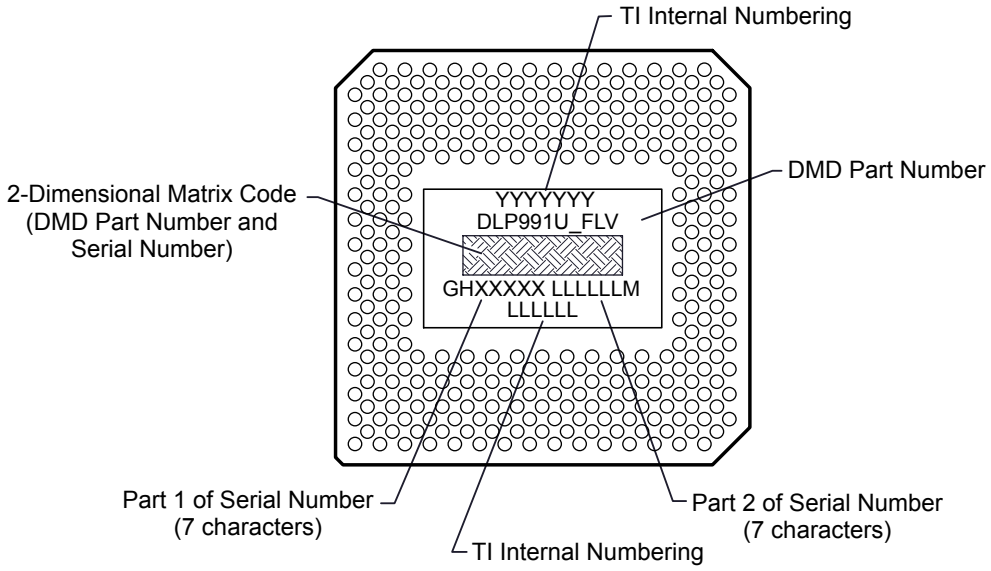


Figure 8-2. DMD Marking Locations

8.2 Documentation Support

8.2.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP991UFLV DMD.

- *DLPC964 Digital Micromirror Device Controller Data Sheet*
- *DLPLCRC964 Evaluation Module Quick Start Guide*
- *DLP DLPC964 Apps FPGA User's Guide*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Package Option Addendum

10.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4) (5)
DLP991UFLV	PREVIEW	CLGA	FLV	321	1	RoHS & Green	NI-PD-AU	N/A for Pkg Type		Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP991UFLV	ACTIVE	CLGA	FLV	321	12	RoHS & Green	NI-PD-AU	N / A for Pkg Type	45 to 90		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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