DP83TD530-Q1 Automotive 10BASE-T1S Multidrop OA PMD Transceiver with TC10

1 Features

- IEEE 802.3cg compliant 10Mbps 10BASE-T1S
  - Multidrop or point-to-point half-duplex
  - Supports >25m cable and >16 nodes depending on channel
- Host controller interface: OA compliant 3-pin interface
- AEC-Q100 qualified for automotive applications:
  - Temperature: –40 to 125°C, T_A (grade 1)
- Single supply operation from 3.3V with 1.8/2.5/3.3V options for I/O voltage
- OA TC10 local and remote wake-up support
- Support OA TC14 PHY features when paired with appropriate external host
  - Topology discovery
  - Signal Quality Indicator (SQI)
  - Harness Defect Detection (HDD)
- Robust PHY architecture with protection and fault detection features
  - Bus wires short to GND or 48V VBAT protection
  - Overtemperature, undervoltage detection
  - ±8kV HBM ESD for MDI pins
  - ±8kV ISO10605 /IEC61000-4-2 ESD contact discharge on MDI pins
  - Extended CMV support for MDI pins
  - OA PMA, and EMC compliant

2 Applications

- Automotive:
  - Body electronics and lighting
  - Automotive gateway
  - Short range radars
  - Robotics
  - Hybrid, electric, and powertrain systems
- Industrial:
  - Factory automation
  - HVAC systems
  - Motor drives

3 Description

The DP83TD530-Q1 is 10BASE-T1S OA TC-14 compliant PMD transceiver. This device provides full analog front end functionality while relying on the host system for MAC, digital PHY, and management functions. This solution, similar to the CAN transceiver approach, features a simple and cost effective 3-pin clock-less interface between the host controller and the PMD transceiver chip. The device supports 10Mbps multi-drop or point-to-point half-duplex communication over unshielded twisted pair cables with extended common mode voltage (CMV) tolerance. The device communicates to a host controller or switch using OA-3pin interface. The host must have the 10BASE-T1S digital PHY incorporated.

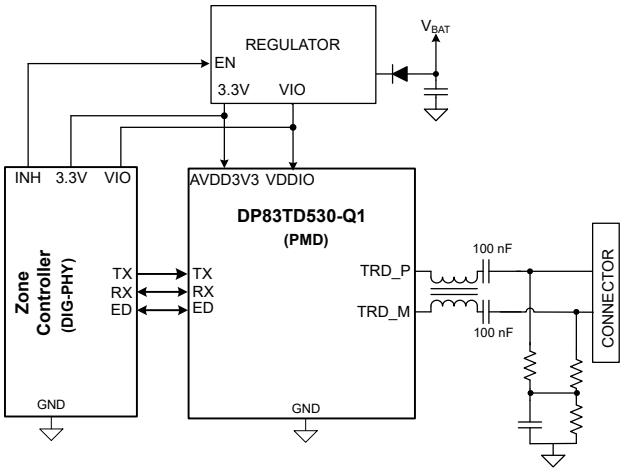
The DP83TD530-Q1 incorporates TC10 wake/sleep features to enable efficient system-level power consumption. The device supports remote wake-up over the Ethernet data line.

The DP83TD530-Q1 is equipped with diagnostic features such as cable fault detection, undervoltage and overtemperature monitoring to streamline system development and maintenance.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DP83TD530-Q1	VSON (DRB) (8)	3mm x 3mm

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

ADVANCE INFORMATION

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ADVANCE INFORMATION

4 Related Products

PART NUMBER	PACKAGE	10BASE-T1S PHY TYPE
DP83TD555J-Q1	QFN-20, 4mm × 4mm	OA SPI MAC-PHY transceiver
DP83TD535-Q1	VSON-14, 4.5mm × 3mm	OA PMD transceiver with MDIO and TC10 pins
DP83TD530-Q1	VSON-8, 3mm × 3mm	OA PMD transceiver

ADVANCE INFORMATION

5 Pin Configuration and Functions

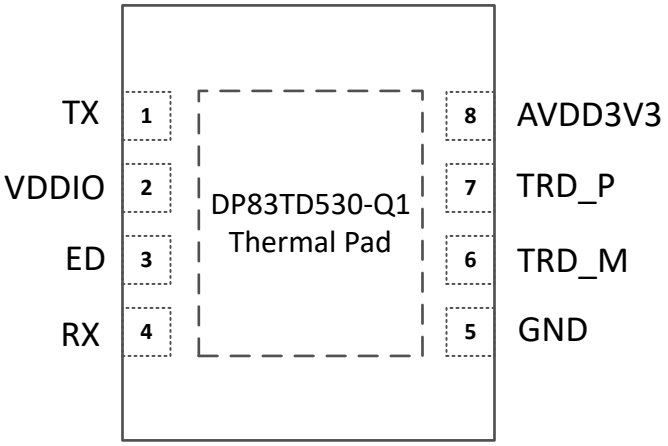

Figure 5-1. DP83TD530-Q1 Pinout (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	Internal R_{PU}/R_{PD}	DESCRIPTION
NAME	NO.			
Media Dependent Differential Interface				
TRD_P	7	I/O	-	Positive terminal differential of transmit and receive: bidirectional differential signaling configured for 10BASE-T1S
TRD_M	6	I/O	-	Negative terminal of differential transmit and receive: bidirectional differential signaling configured for 10BASE-T1S
3-PIN Interface/Serial Management Interface Pins				
TX	1	I	R_{PU} = 15kΩ	**TX** is Ethernet Transmit Data Input
ED	3	I/O	R_{PU} = 15kΩ	**ED (Energy Detect):**Energy Detect for line activity/ collision detection **MDIO (Management Data Input and Output):**In configuration mode, this pin behaves as an MDIO bidirectional management data signal, this pin is connected to the host controller.
RX	4	I/O	R_{PU} / R_{PD}= 15kΩ	**RX:**Ethernet Receive Data Output when in non-configuration operating mode. This pin has internal a pull up resistor (15kΩ) when this pin is not used as MDC for device configuration. **MDC (Management Data Clock):**In configuration mode, this pin behaves as an MDC synchronous clock to the MDIO serial management input and output data. This pin has internal pull down (15kΩ) during configuration mode.
Power/Ground				
AVDD3V3	8	P	-	3.3V Device Supply Voltage
VDDIO	2	P	-	Input/output Supply Voltage (1.8V, 2.5V or 3.3V)
GND	5	G	-	Ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

Table 5-2. Pin Voltage Domain

PIN NAME	VOLTAGE DOMAIN	OUTPUT VOLTAGE RANGE
TRD_P	AVDD3V3	0.5xAVD3V3 ±(0.4V - 0.6V)
TRD_M	AVDD3V3	0.5xAVD3V3 ±(0.4V - 0.6V)
TX	VDDIO	0V - VDDIO
RX	VDDIO	0V - VDDIO
ED	VDDIO	0V - VDDIO

ADVANCE INFORMATION

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

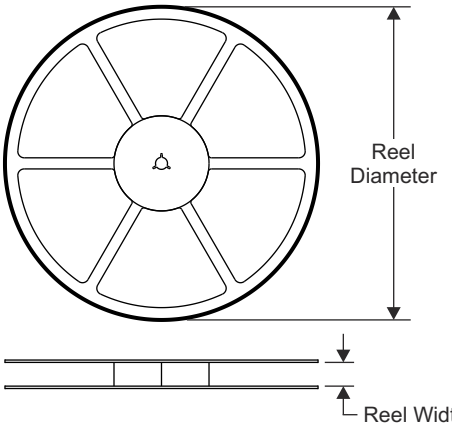
PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
PDP83TD530DRBTC	Active	Preproduction	VSON(DRB)|8	250 | small T&R	-	Call TI	Call TI	-40 to 125°C	P530T4

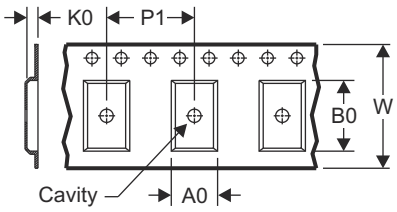
(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

7.1 Tape and Reel Information

REEL DIMENSIONS

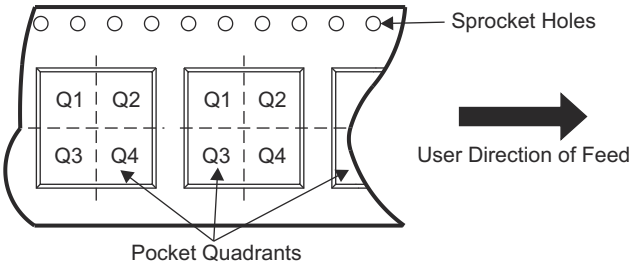


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDP83TD530DRBTC	DRB	VSON	8	250	180	12.4	3.3	3.3	1.1	8.0	12.0	1

ADVANCE INFORMATION

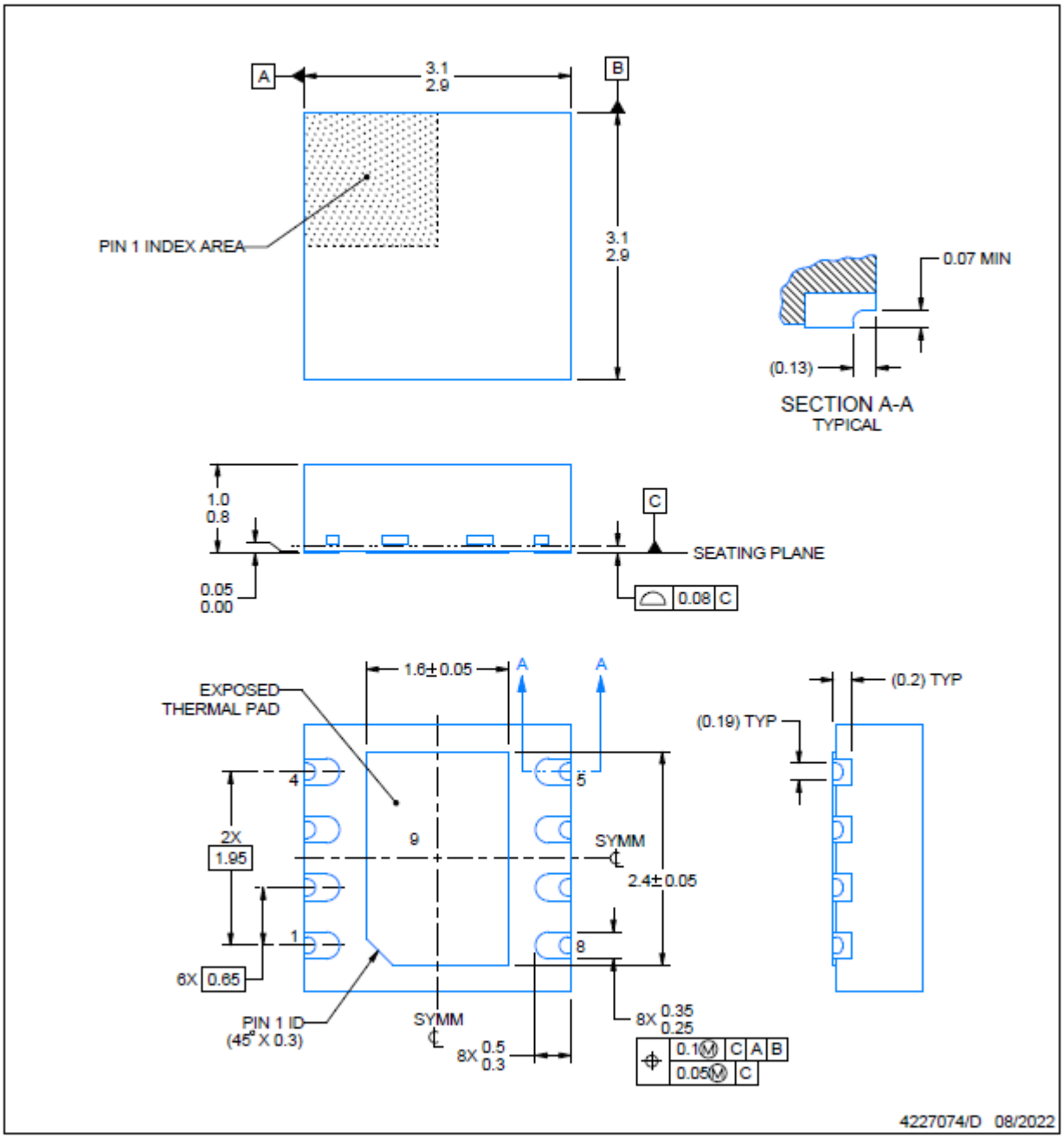
7.2 Mechanical Data

DRB0008K

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

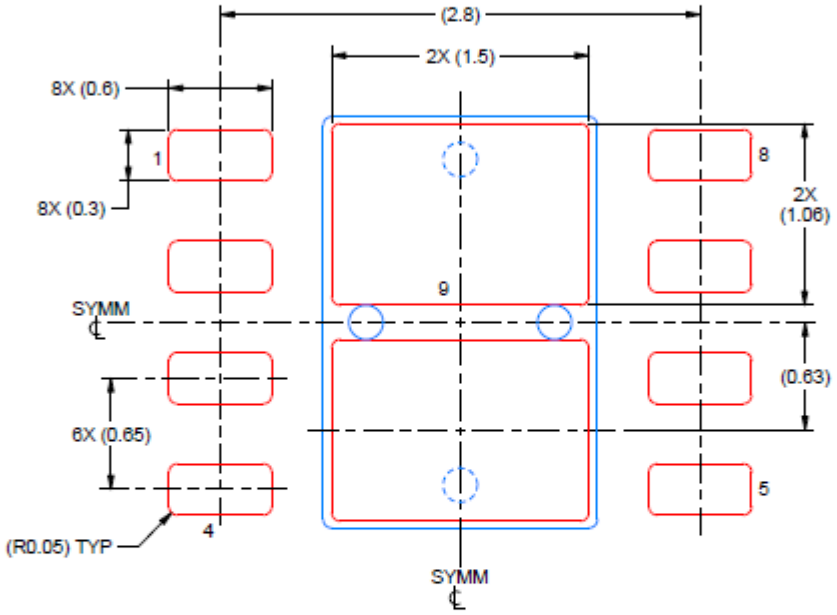
EXAMPLE BOARD LAYOUT

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DRB0008K — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDP83TD530DRBTC	Active	Preproduction	SON (DRB) | 8	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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