

# DRV3263-Q1 48V Battery 3-Phase Gate Driver Unit with Integrated Cutoff Drivers

## 1 Features

- AEC-Q100 Test Guidance for automotive applications
  - Device ambient temperature:  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$
- **Functional Safety-Compliant**
  - Developed for functional safety applications
  - Documentation to aid ISO 26262 system design will be available upon production release
  - Systematic capability up to ASIL D targeted
- Three phase half-bridge gate driver
  - Drives six N-channel MOSFETs (NMOS)
  - 8 to 85V wide operating voltage range
  - Bootstrap architecture for high-side gate driver
  - 50mA average gate switching current enables driving 400nC MOSFETs at 20kHz
  - Trickle charge pump to support 100% PWM duty cycle and to generate overdrive supply
- Cutoff driver
  - Drive N-channel MOSFET cutoff switches in multiple topologies
  - Two SPI-controllable channels (DRV3263A) or
  - One channel with SPI or HW pin control (DRV3263B)
- Smart Gate Drive architecture
  - 15-level configurable peak gate drive current up to 1000 / 2000mA (source / sink)
  - Independently configurable pre-charge and pre-discharge regions
  - Configurable soft shutdown to minimize inductive voltage spikes during overcurrent shutdown
- Low-side Current Sense Amplifier
  - Sub-1mV low input offset across temperature
  - 8-level adjustable gain
- SPI-based detailed configuration and diagnostics with OTP memory to store default configuration settings
- DRVOFF independent driver disable pin
- High voltage wake up pin (nSLEEP)
- 6x, 3x, 1x, and Independent PWM modes
- Supports 3.3V and 5V logic inputs
- Integrated protection features
  - Battery and power supply voltage monitors
  - MOSFET  $V_{DS}$  and  $R_{sense}$  over current monitors
  - MOSFET  $V_{GS}$  gate fault monitors
  - Analog Built-In Self-Test (ABIST)
  - Device thermal warning and shutdown
  - Fault condition indicator pin

## 2 Applications

- 48V automotive motor control applications
  - Electrical Power Steering and Steer-by-Wire
  - Electro-Mechanical Brake and Electro-Hydraulic Brake
  - Shifter, Transmission, Suspension Control

## 3 Description

The DRV3263-Q1 is an integrated smart gate driver for 48V automotive three-phase BLDC applications. The device provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV3263-Q1 generates the correct gate drive voltages using an external 12V supply and an integrated bootstrap diode for the high-side MOSFETs. A trickle charge pump allows for the gate drivers to support 100% PWM duty cycle control and provides overdrive gate drive voltage for driving external switches, which can be controlled through dedicated cutoff driver pins.

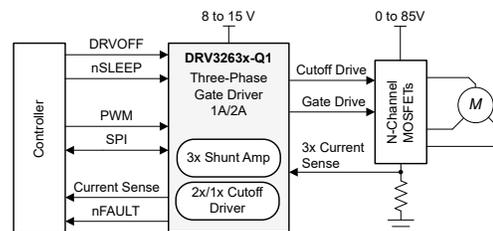
The DRV3263-Q1 provides low-side current sense amplifiers to support resistor based low-side current sensing. The low offset and low gain error of the amplifiers enable the system to obtain precise motor current measurements.

A wide range of diagnostics and protection features are integrated with the DRV3263-Q1, enabling a robust motor drive system design and reduce external components. The highly configurable device response allows the device to be integrated seamlessly into a variety of system designs.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
DRV3263-Q1	QFN (48)	7mm × 7mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Simplified Schematic**



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ADVANCE INFORMATION

## 4 Device and Documentation Support

### 4.1 Documentation Support

#### 4.1.1 Related Documentation

- Texas Instruments, [Understanding Smart Gate Drive \(Rev. D\) application report](#)
- Texas Instruments, [Brushless-DC Motor Driver Considerations and Selection Guide \(Rev. A\) application report](#)
- Texas Instruments, [Designing High-Side and 3-Phase Isolator MOSFET Circuits in Motor Apps application note](#)
- Texas Instruments, [Best Practices for Board Layout of Motor Drivers \(Rev. B\) application note](#)
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package application report](#)
- Texas Instruments, [PowerPAD™ Made Easy application report](#)
- Texas Instruments, [Sensored 3-Phase BLDC Motor Control Using MSP430 application report](#)
- Texas Instruments, [Hardware Design Considerations for an Electric Bicycle Using a BLDC Motor application report](#)

### 4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 4.3 Support Resources

### 4.4 Trademarks

All trademarks are the property of their respective owners.

### 4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial release.

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## 6.1 Package Option Addendum

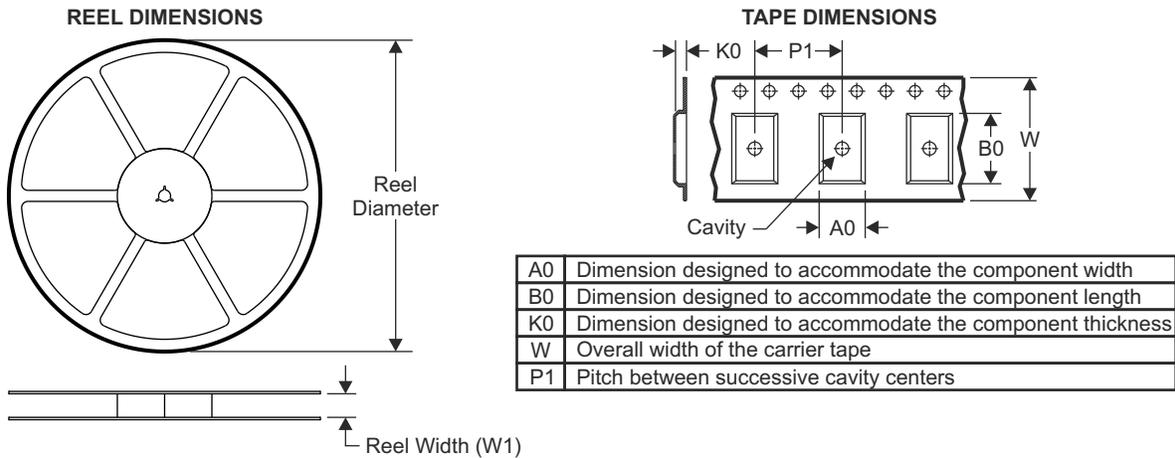
### Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
DRV3263RGZR Q1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NiPdAu	Level-3-260C-1 68 HR	-40 to 125	DRV8334

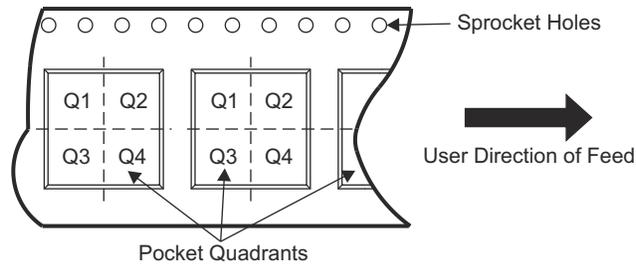
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## 6.2 Tape and Reel Information



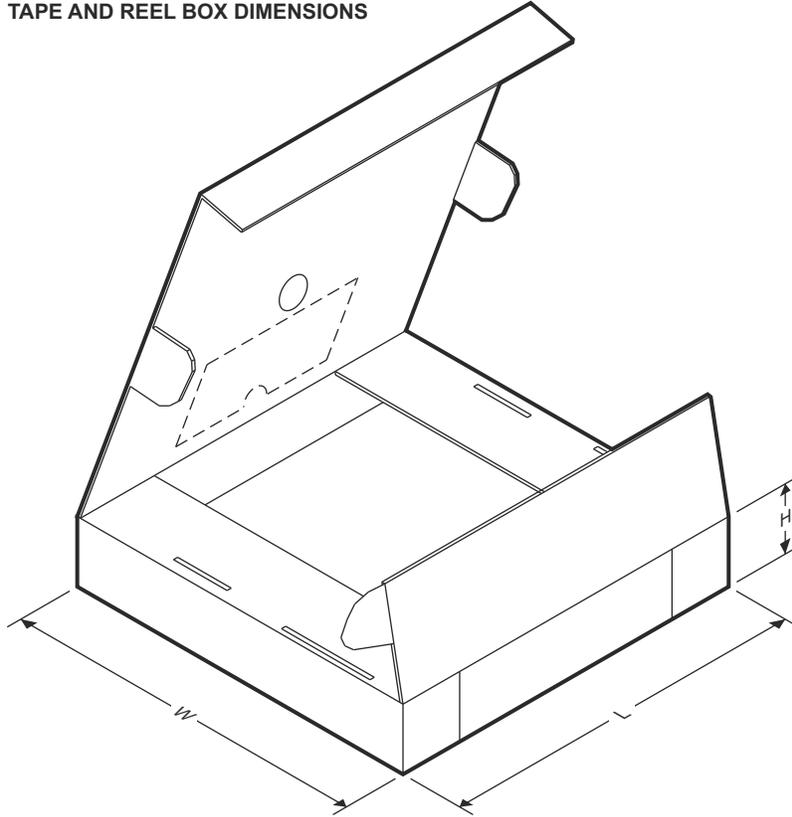
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3263RGZRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	2

ADVANCE INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3263RGZRQ1	VQFN	RGZ	48	1000	336.6	336.6	31.8

**ADVANCE INFORMATION**



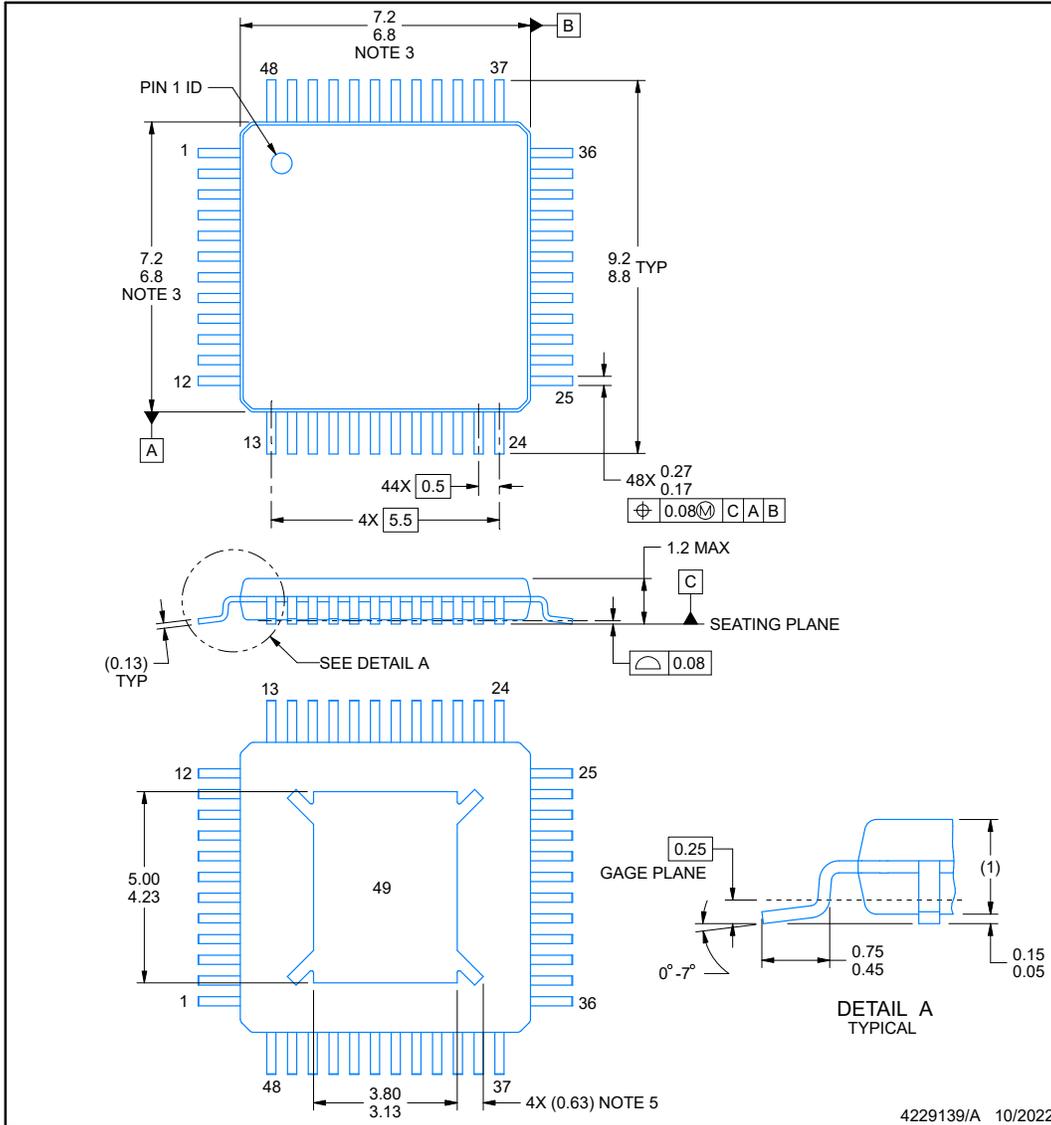
**PACKAGE OUTLINE**

**PHP0048P**

**PowerPAD™ HTQFP - 1.2 mm max height**

FPLASSTIC:QJLWAD/FPLAHTFPACKK

**ADVANCE INFORMATION**



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

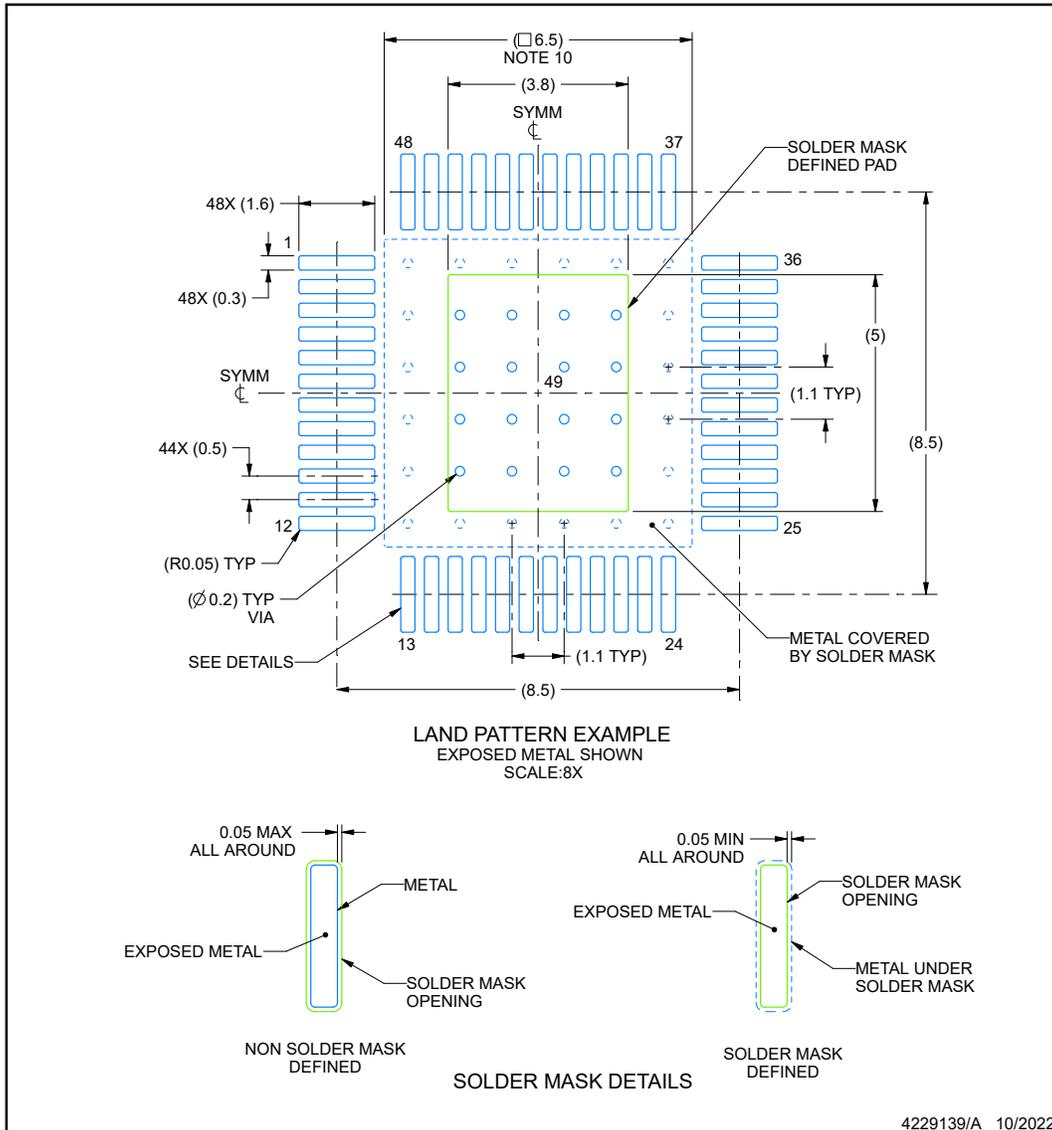
4229139/A 10/2022  
PowerPAD is a trademark of Texas Instruments.

**EXAMPLE BOARD LAYOUT**

**PHP0048P**

**PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

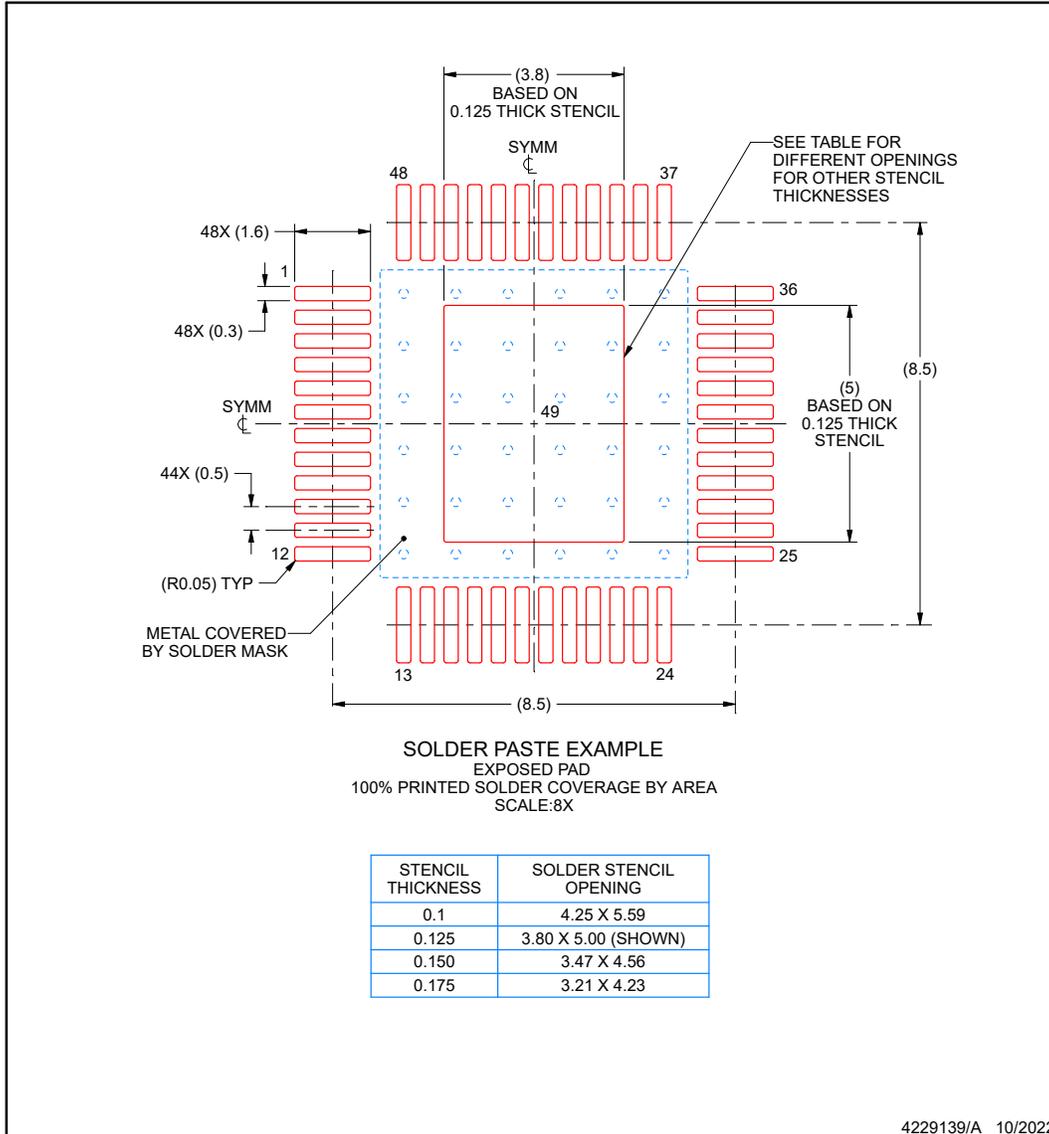
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

**EXAMPLE STENCIL DESIGN**

**PHP0048P**

**PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">PDRV3263AERGZRQ1</a>	Active	Preproduction	VQFN (RGZ)   48	4000   LARGE T&R	-	Call TI	Call TI	-40 to 150	
<a href="#">PDRV3263BERGZRQ1</a>	Active	Preproduction	VQFN (RGZ)   48	4000   LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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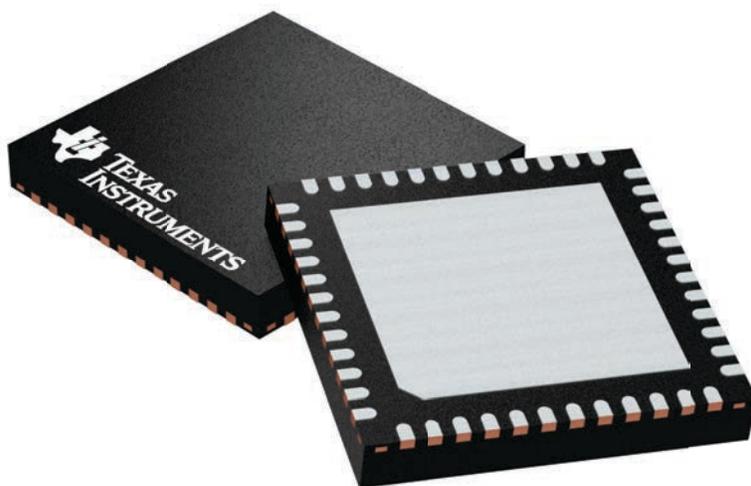
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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