DS100BR410 Low Power Quad Channel Repeater with 10.3125 Gbps Equalizer and De-Emphasis Driver

Check for Samples: DS100BR410

FEATURES

- **Quad channel repeater for up to 10.3125 Gbps**
- **Low power consumption, with option to power down unused channels**
- **Adjustable receive equalization**
- **Adjustable transmit de-emphasis**
- **Adjustable transmit V_{OD} (up to 1200 mVp-p)**
- **IDLE detection — squelch function auto mutes the output for SATA/SAS OOB signal**
- **<0.22 UI of residual DJ at 10.3125 Gbps with 12 meters cable**
- **Programmable via pin selection or SMBus interface**
- **Single supply operation at 2.5 V ±5%**
- **-40°C to +85°C Operation**
- **≥7 kV HBM ESD Rating**
- **High speed signal flow–thru pinout package: 48-pin WQFN (7 mm x 7 mm, 0.5 mm pitch)**

APPLICATIONS

- **High-speed active copper cable modules**
- **FR-4 Backplanes**
- **10GE, 8GFC, 10GFC, 10G SONET, SAS, SATA, and InfiniBand**

DESCRIPTION

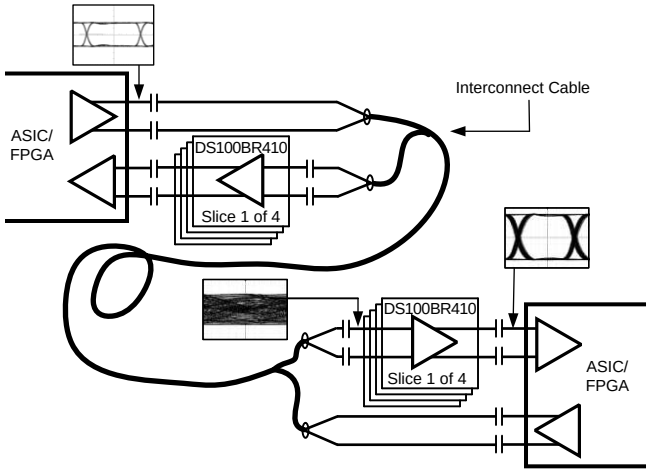
The DS100BR410 is an extremely low power, high performance quad-channel repeater for high-speed serial links with data rates up to 10.3125 Gbps. The device performs both receive equalization and transmit de-emphasis on each of its 4 channels to compensate for channel loss, allowing maximum flexibility of physical placement within a system.

The receiver's continuous time linear equalizer (CTLE) is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium such as backplane trace or cable. The transmitter features adjustable V_{OD} (output amplitude voltage level) and de-emphasis driver to compensate for PCB trace lost.

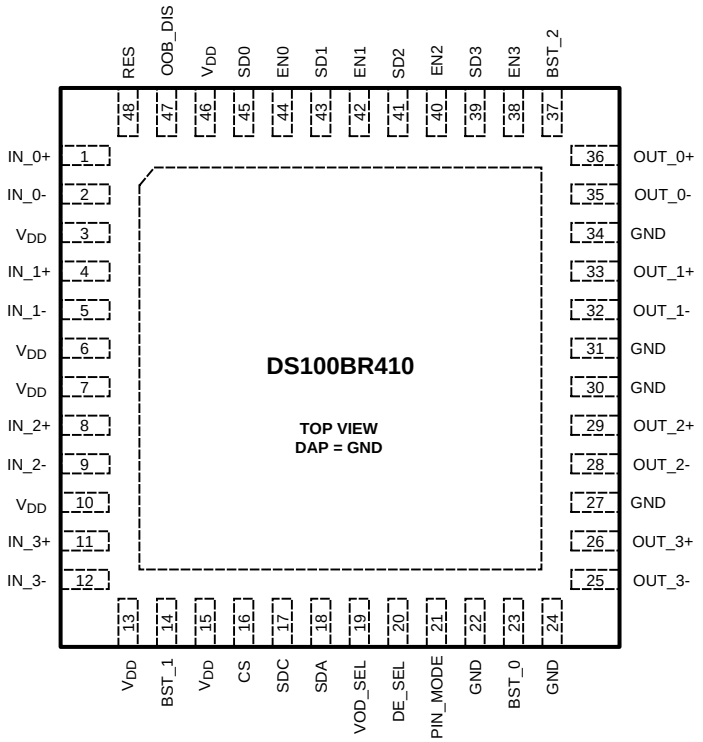
With a low power consumption and control to turn-off unused channels, the DS100BR410 is part of TI's PowerWise family of energy efficient devices.

The programmable settings can be applied via pin mode or SMBus mode interface.

Typical Application Diagram



Connection Diagram



Pin Descriptions

Pin Name	Pin #	I/O, Type[1]	Description
HIGH SPEED DIFFERENTIAL I/O			
IN_0+ IN_0–	1 2	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_0+ to IN_0-.
IN_1+ IN_1–	4 5	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_1+ to IN_1-.
IN_2+ IN_2–	8 9	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_2+ to IN_2-.
IN_3+ IN_3–	11 12	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor connects IN_3+ to IN_3-.
OUT_0+ OUT_0–	36 35	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_0+ to OUT_0-.
OUT_1+ OUT_1–	33 32	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_1+ to OUT_1-.
OUT_2+ OUT_2–	29 28	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_2+ to OUT_2-.
OUT_3+ OUT_3–	26 25	O, CML	Inverting and non-inverting CML differential outputs from the driver. An on-chip 100Ω terminating resistor connects OUT_3+ to OUT_3-.
2.5V LVCMOS CONTROL PINS			
BST_2 BST_1 BST_0	37 14 23	I, LVCMOS	BST_2, BST_1, and BST_0 select the equalizer boost level for all channels. BST_2 and BST_1 are internally pulled high. BST_0 is internally pulled low. See Table 1
EN0 EN1 EN2 EN3	44 42 40 38	I, LVCMOS	Enable channel n input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.

(1) **Note:** I = Input O = Output, LVCMOS pins are 2.5 V levels only, **only SMBus pins SDA, SDC and CS are 3.3V tolerant.**

Pin Descriptions (continued)

Pin Name	Pin #	I/O, Type[1]	Description
PIN_MODE	21	I, LVCMOS	Pin mode control input. When held High, device is in Pin control mode. When held Low, device is in SMBus Control Mode PIN_MODE is internally pulled High.
SD0 SD1 SD2 SD3	45 43 41 39	O, LVCMOS	Signal detect n output. Output is High when signal is detected. Output is Low when signal is NOT detected.
OOB_DIS	47	I, LVCMOS	OOB disable control input. When held High, OOB is disabled. When held Low, OOB is enabled. Out Of Band (OOB) for SATA/SAS applications is active. OOB_DIS is internally pulled Low.
Analog Input Pins (4–level Inputs)			
VOD_SEL	19	I, analog	Differential Output Voltage Select Input Tie to V_{DD}, V_{OD} = 1.2 Vp-p Leave Open, V_{OD} = 1.0 Vp-p Resistor (20 kΩ) to GND, V_{OD} = 800 mVp-p Tie to GND, V_{OD} = 600 mVp-p
DE_SEL	20	I, analog	De-Emphasis Select Input Tie to V_{DD} = -9 dB Leave Open = -6 dB Resistor (20 kΩ) to GND = -3 dB Tie to GND = 0 dB
SERIAL MANAGEMENT BUS (SMBus) INTERFACE			
SDA	18	I/O, LVCMOS	Data Input / Open Drain Output External pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
SDC	17	I, LVCMOS	Clock Input Pin is 3.3 V LVCMOS tolerant.
CS	16	I, LVCMOS	Chip Select When high, access to the SMBus registers are enabled. When low, access to the SMBus registers are disabled. Please refer to “SMBus configuration Registers” section for detail information. Pin is 3.3 V LVCMOS tolerant.
POWER			
V_{DD}	3, 6, 7, 10, 13, 15, 46	Power	V_{DD} = 2.5 V ± 5%
GND	22, 24, 27, 30, 31, 34	Power	Ground reference.
DAP	PAD	Power	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board with at least 4 via to lower the ground impedance and improve the thermal performance of the package.
RES	48	NC	***Reserved*** – Do not connect

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{DD})		-0.5V to +2.75V
2.5 I/O Voltage (LVCMOS and Analog Input)		-0.5V to +2.75V
3.3 LVCMOS I/O Voltage (SDA, SDC, CS)		-0.5V to +4.0V
CML Input Voltage (IN_n+/-)		-0.5V to +2.75V
CML Output Voltage (OUT_n+/-)		-0.5V to +2.75V
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
ESD Rating	HBM, STD - JESD22-A114F	≥7 kV
	MM, STD - JESD22-A115-A	≥200 V
	CDM, STD - JESD22-C101-D	≥1250 V
Thermal Resistance θ_{JA}, No Airflow, 4 layer JEDEC, 9 thermal vias		27.6 °C/W
For soldering specifications: see product folder at www.ti.com http://www.ti.com/lit/SNOA549		

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied.

Recommended Operating Conditions(1)

	Min	Typ	Max	Units
Supply Voltage				
V_{DD} to GND	2.375	2.5	2.625	V
Ambient Temperature	-40	25	+85	°C

(1) The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless other specified. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
POWER						
PD	Power Supply Consumption	Device Output Enabled (EN[3:0] = High), VOD_SEL = open (1.0 Vp-p)		220	275	mW
		Device Output Disable (EN[3:0] = Low)		25	40	mW
PS_{NT}	Supply Noise Tolerance(2)	50 Hz to 100 Hz		100		mV_{P-P}
		100 Hz to 10 MHz		40		mV_{P-P}
		10 MHz to 5.0 GHz		10		mV_{P-P}
2.5 LVCMOS DC Specifications						
V_{IH}	High Level Input Voltage		1.75		V_{DD}	V
V_{IL}	Low Level Input Voltage		-0.3		0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -3mA	2.0			V
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA			0.4	V
I_{IN}	Input Leakage Current	$V_{IN} = V_{DD}$			+10	µA
		V_{IN} = GND	-10			µA

(1) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(2) Specification is ensured by characterization at optimal boost setting and is not tested in production.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
I_{IN-P}	Input Leakage Current with Internal Pull-Down/Up Resistors	$V_{IN} = V_{DD}$, with internal pull-down resistors			+65	µA
		V_{IN} = GND, with internal pull-up resistors	-50			µA
Signal Detect						
SDH	Signal Detect ON Threshold Level	Default input signal level to assert SD pin, 10.3125 Gbps		130		mV_{p-p}
SDL	Signal Detect OFF Threshold Level	Default input signal level to de-assert SD, 10.3125 Gbps		60		mV_{p-p}
CML Receiver Inputs (IN_n+, IN_n-)						
V_{TX}	Source Transmit Launch Signal Level (IN diff)	AC-Coupled Requirement, Differential measurement at point A. Figure 1	600		1600	mV_{P-P}
R_{LI}	Differential Input Return Loss - SDD11	100 MHz – 6 GHz, with fixture's effect de-embedded		-15		dB
CML Driver Outputs (OUT_n+, OUT_n-)						
V_{OD}	Output Differential Voltage Level(3), Figure 2	Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled, VOD_SEL = open (1.0 Vp-p), DE_SEL = GND	750	970	1150	mV_{P-P}
		Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled, VOD_SEL = V_{DD} (1.2 Vp-p), DE_SEL = GND		1140		mV_{P-P}
V_{OD_DE}	De-Emphasis Levels(4) (5)	DE_SEL = 20kΩ to GND, VOD_SEL = V_{DD} (1.2 Vp-p)		-3		dB
		DE_SEL = open, VOD_SEL = V_{DD} (1.2 Vp-p)		-6		dB
		DE_SEL = V_{DD}, VOD_SEL = V_{DD} (1.2 Vp-p)		-9		dB
t_R, t_F	Transition Time	20% to 80% of differential output voltage, measured within 1" from output pins. Figure 2	30	38	45	ps
R_{LO}	Differential Output Return Loss - SDD22	100 MHz – 6 GHz, with fixture's effect de-embedded. IN+ = static high.		-15		dB
t_{PLHD}	Differential Low to High Propagation Delay	Propagation delay measurement at 50% crossing between input to output, 100 Mbps. Figure 3		240		ps
t_{PHLD}	Differential High to Low Propagation Delay			240		ps
t_{CCSK}	Inter Pair Channel to Channel Skew	Difference in 50% crossing between channels		7		ps
t_{PPSK}	Part to Part Output Skew	Difference in 50% crossing between outputs		20		ps
RJ	Random Jitter	V_{TX} = 1.0 Vp-p, BST_[2:0] = 000, (4) (6)		0.3		ps_{rms}

(3) Measured with clock-like {11111 00000} pattern.
(4) Measured with clock-like {11111 00000} pattern.
(5) The de-emphasis level of −3 dB, −6 dB, −9 dB are for V_{OD} = 1.2 Vp-p. At lower V_{OD} level, the de-emphasis levels are reduced.
(6) Random jitter contributed by the equalizer is defined as sqrt ($J_{OUT}^2 - J_{IN}^2$). J_{OUT} is the random jitter at equalizer outputs in ps-rms, see point C of Figure 1; J_{IN} is the random jitter at the input of the equalizer in ps-rms, see point B of Figure 1.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
Equalization						
DJ1	Residual Deterministic Jitter at 10.3125 Gbps	V_{TX} = 1.0 V_{P-P}, 12 meter 30 AWG cable, EQ = 03F'h (BST[2:0] = 111), PRBS-7 (2^7-1) pattern. (7)		0.10	0.22	UI_{P-P}
DJ2	Residual Deterministic Jitter at 6.0 Gbps	V_{TX} = 1.0 V_{P-P}, 12 meter 30 AWG cable, EQ = 07F'h, PRBS-7 (2^7-1) pattern. (7)		0.07	0.12	UI_{P-P}
Signal DETECT and ENABLE Timing						
t_{ZISD}	Input OFF to ON detect — SD Output High Response Time	Response time measurement at V_{IN} to SD output, V_{IN} = 800 mV_{P-P}, 100 Mbps, 40" of 6 mil microstrip FR4. Figure 4		35		ns
t_{IZSD}	Input ON to OFF detect — SD Output Low Response Time			400		ns
t_{OZOED}	EN High to Output ON Response Time	Response time measurement at EN input to V_O, V_{IN} = 800 mV_{P-P}, 100 Mbps, 40" of 6 mil microstrip FR4. Figure 5		150		ns
t_{ZOED}	EN Low to Output OFF Response Time			5		ns

(7) Deterministic jitter is measured at the differential outputs (point C of Figure 1), minus the deterministic jitter before the test channel (point A of Figure 1). Random jitter is removed through the use of averaging or similar means.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
Serial Bus Interface DC Specifications						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		V_{DD}	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	See (2)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SDC	See (2) (3)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	$V_{DD3.3}$, (2) (3)		2000		Ω
		$V_{DD2.5}$, (2) (3)		1000		Ω
Serial Bus Interface Timing Specifications – (See Figure 6) (4)(5)						
F_{SMB}	Bus Operating Frequency		10		100	kHz
T_{BUF}	Bus Free Time Between Stop and Start Condition		4.7			µs
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	4.0			µs
$T_{SU:STA}$	Repeated Start Condition Setup Time		4.7			µs
$T_{SU:STO}$	Stop Condition Setup Time		4.0			µs
$T_{HD:DAT}$	Data Hold Time		300			ns

(1) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(2) Maximum termination voltage should be identical to the device supply voltage.
(3) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(4) Recommended value. Parameter not tested in production.
(5) Recommended maximum capacitance load per bus segment is 400pF.

Electrical Characteristics — Serial Management Bus Interface (continued)

Over recommended operating supply and temperature ranges unless other specified. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
$T_{SU:DAT}$	Data Setup Time		250			ns
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period		4.0		50	µs
t_F	Clock/Data Fall Time				300	ns
t_R	Clock/Data Rise Time				1000	ns
t_{POR}	Time in which a device must be operational after power-on reset				500	ms

AC WAVEFORMS AND TEST CIRCUITS

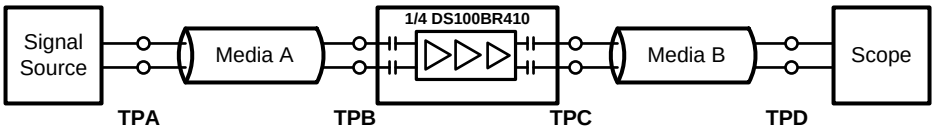


Figure 1. Test Setup Diagram

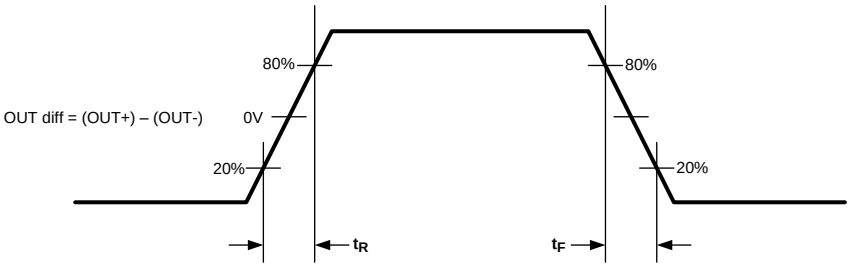


Figure 2. Output Transition Times

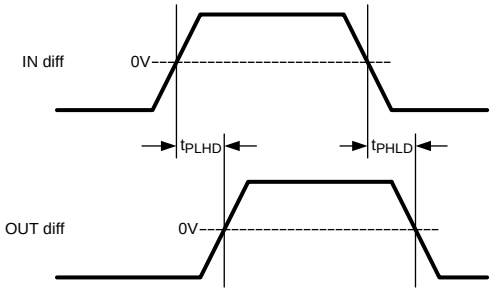


Figure 3. Propagation Delay Timing Diagram

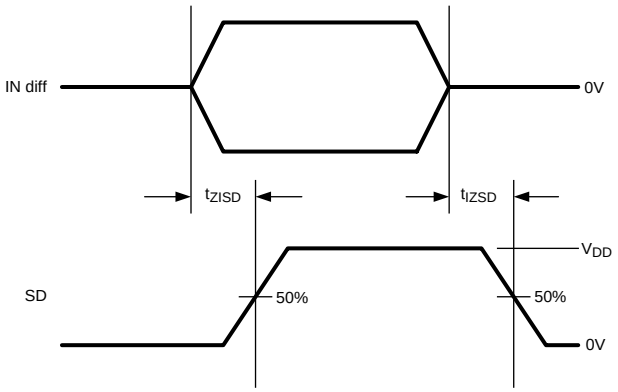


Figure 4. Signal Detect (SD) Delay Timing Diagram

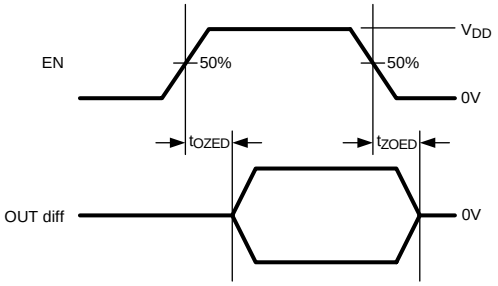


Figure 5. Enable (EN) Delay Timing Diagram

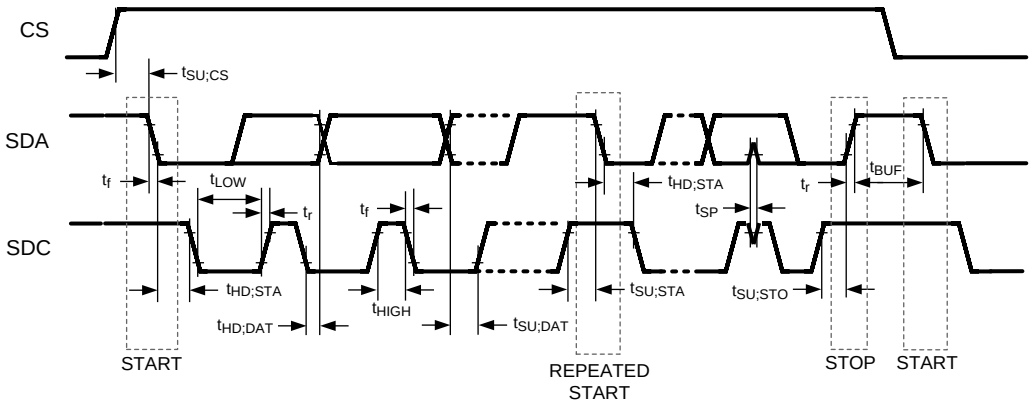


Figure 6. SMBus Timing Parameters

FUNCTIONAL DESCRIPTION

DS100BR410 Functional Descriptions

The DS100BR410 is a Low Power Quad Channel Repeater with Equalizer and De-Emphasis Driver optimized for operation up to 10.3125 Gbps for backplane and cable applications.

DATA CHANNELS

The DS100BR410 provides four data channels. Each data channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a CML driver as shown in Figure 7.

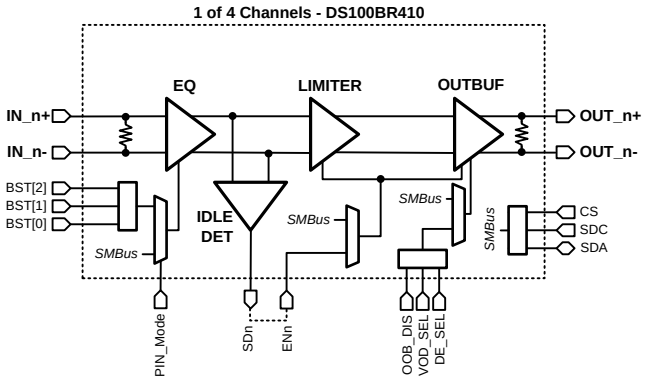


Figure 7. Simplified Block Diagram

EQUALIZER BOOST CONTROL

Each data channel support eight programmable levels of equalization boost. The state of the PIN_MODE control input determines how the boost settings are controlled. If PIN_MODE is held High, then the equalizer boost setting is controlled by the Boost Set pins (BST_[2:0]) in accordance with Table 1. If this programming method is chosen, then the boost setting selected on the Boost Set pins is applied to all channels. When PIN_MODE is held Low, the equalizer boost level is controlled through the SMBus. This programming method is accessed via the appropriate SMBus registers (see Table 4). Using this approach, equalizer boost settings can be programmed for each channel individually. PIN_MODE is internally pulled High, therefore if left open, the boost settings are controlled by the Boost Set pins (BST_[2:0]). The eight levels of boost settings enables the DS100BR410 to address a wide range of media loss and data rates.

Table 1. Boost / EQ Pin Mode Configuration

Inputs			SMBus Register Bits	Result @ 5 GHz
BST_2	BST_1	BST_0	[8:0]	
0	0	0	000000000	2.7 dB
0	0	1	000000001	7.3 dB
0	1	0	000000011	12.2 dB
0	1	1	000000111	16.6 dB
1	0	0	000001111	20.6 dB
1	0	1	000011111	24.8 dB
1	1	0	000101111	27.6 dB (default)
1	1	1	000111111	28.9 dB

SIGNAL DETECT

The DS100BR410 features a signal detect circuit on each data channel. The status of the signal of each channel can be determined by either reading the Signal Detect bit (SDn) in the SMBus registers (see Table 4) or by the state of each SDn pin. An output logic high indicates the presence of a signal that has exceeded the ON threshold value (called SDH). An output logic Low means that the input signal has fallen below the OFF threshold value (called SDL). These values are programmed via the SMBus. If not programmed via the SMBus, the thresholds take on the default values. The Signal Detect threshold values can be changed through the SMBus. All threshold values specified are DC peak-to-peak differential signals (positive signal minus negative signal) at the input of the device.

OUTPUT LEVEL CONTROL

The output amplitude of the CML drivers can be controlled via the 4–level analog input VOD_SEL pin or via SMBus (see Table 4). The default V_{OD} level is 1.0 Vp-p.

Table 2. VOD_SEL Pin Configuration

VOD_SEL Pin	Result
Tie High - V_{DD}	1.2 Vp-p
Open* (default)	1.0 Vp-p
20 kΩ resistor to GND	800 mVp-p
Tie to GND	600 mVp-p

OUTPUT DE-EMPHASIS CONTROL

The output De-Emphasis may be controled via the 4–level analog input DE_SEL pin or via SMBus (see Table 4).

Table 3. DE_SEL Pin Configuration

DE_SEL Pin	Result
Tie High - V_{DD}	-9 dB
Open* (default)	-6 dB
20 kΩ resistor to GND	-3 dB
Tie to GND	0 dB

AUTOMATIC ENABLE FEATURE

It may be desirable to place unused channels in power-saving Standby mode. This can be accomplished by connecting the Signal detect (SDn) pin to the Enable (ENn) pin for each channel (See Figure 7).

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. The use of the Chip Select signal is **required**. Holding the CS pin High enables the SMBus port allowing access to the configuration registers. Holding the CS pin Low disables the device's SMBus allowing communication from the host to other slave devices on the bus. In the STANDBY state, the System Management Bus remains active. When communication to other devices on the SMBus is active, the CS signal for the DS100BR410s must be driven Low.

The address byte for all DS100BR410s is AC'h. Based on the SMBus 2.0 specification, the DS100BR410 has a 7-bit slave address of 1010110'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 1100'b or AC'h.

The SDA, SDC and CS pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SDC and CS may also require an external pull-up resistor and it depends on the Host that drives the bus.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SDC is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SDC is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SDC is High indicates a message STOP condition.

IDLE: If SDC and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus Transactions

The device supports WRITE, Burst WRITE, READ. and Burst READ transactions. See Table 4 for register address, type (Read/Write, Read Only), default value and function information.

Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drive the 8-bit data byte.
7. The Device drives an ACK bit (“0”).
8. The Host drives a STOP condition.
9. The Host de-selects the device by driving its SMBus CS signal Low.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drives a START condition.
7. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
8. The Device drives an ACK bit “0”.
9. The Device drives the 8-bit data value (register contents).
10. The Host drives a NACK bit “1”indicating end of the READ transfer.
11. The Host drives a STOP condition.
12. The Host de-selects the device by driving its SMBus CS signal Low.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Information on the Registers

The status registers 01'h to 03'h provide information of the channel that is selected. The information provided are the OOB_DIS, EN, EQ Boost, VOD and DEM bits of the selected channel. By default, channel 0 is selected. In order to change the selected channel, write to reg_07 bit[5:4]. Write a 1 to reg_07 bit[0] is also needed to allow the registers 13'h to 1A'h to control the channel EN and EQ boost bits of each of the channels. Each channel can be individually enabled (EN) and set to a desired boost level with these registers. Please refer to Table 4 for additional information.

Table 4. DS100BR410 Register Map

ADD (hex)	REG Name	Bit(s)	Field	Type	Default (binary)	Description
00	Device ID	7:4	Device ID	R	0010	Device ID Value
		3	SD_CH3	R		1: Signal detected on CH3 0: No signal
		2	SD_CH2	R		1: Signal detected on CH2 0: No signal
		1	SD_CH1	R		1: Signal detected on CH1 0: No signal
		0	SD_CH0	R		1: Signal detected on CH0 0: No signal
01	Status Register for OOB_DIS, EN and Boost_bit[8]	7	***Reserved***	R		
		6	OOB_DIS	R		OOB_DIS 1: OOB Disabled 0: OOB Enabled
		5	***Reserved***	R		
		4	EN	R		EN 1: Channel Enabled 0: Channel Disabled
		3:1	***Reserved***	R		
		0	Boost_bit[8]	R		Boost_bit[8]
02	Status Register for Boost_bit[7:0]	7:0	Boost_bit[7:0]	R		Boost_bit[7:0]
03	Status Register for VOD[5:4] and DEM[1:0]	7:6	***Reserved***	R		
		5:4	VOD[5:4]	R		VOD[5:4] 00 = 0.6 Vp-p 01 = 0.8 Vp-p 10 = 1.0 Vp-p 11 = 1.2 Vp-p
		3:2	***Reserved***	R		
		1:0	DEM[1:0]	R		DEM[1:0] 00 = 0 dB 01 = -3 dB 10 = -6 dB 11 = -9 dB
04	***Reserved***	7:0	***Reserved***	R	00	
05	Signal Detect Assert Threshold	7:6	SD_ON_CH3	R/W	00	Signal Detect ON Threshold 00 = 130 mV 01 = 125 mV 10 = 150 mV 11 = 140 mV
		5:4	SD_ON_CH2	R/W	00	
		3:2	SD_ON_CH1	R/W	00	
		1:0	SD_ON_CH0	R/W	00	
06	Signal Detect De-assert Threshold	7:6	SD_OFF_CH3	R/W	00	Signal Detect OFF Threshold 00 = 60 mV 01 = 40 mV 10 = 105 mV 11 = 90 mV
		5:4	SD_OFF_CH2	R/W	00	
		3:2	SD_OFF_CH1	R/W	00	
		1:0	SD_FF_CH0	R/W	00	

Table 4. DS100BR410 Register Map (continued)

ADD (hex)	REG Name	Bit(s)	Field	Type	Default (binary)	Description
07	Port/Channel Select and Enable SMBus Registers	7:6	***Reserved***	R/W	00	
		5:4	Port/Channel Select for Status	R/W	00	Select port/channel [1:0] to report status in REG_01 to REG_03 00 = port0 (CH0) 01 = port1 (CH1) 10 = port2 (CH2) 11 = port3 (CH3)
		3:1	***Reserved***	R/W	000	
		0	SMBUS Channel EN and EQ boost	R/W	0	Channel EN and EQ Boost through pins or smbus REG_13 to REG_1A 0 = Channel EN[3:0] and EQ BST[2:0] boost set by external pins 1 = Allow channel EN and EQ boost to be set by SMBus Register bits: REG_13 to REG_1A
08	Driver V_{OD} Control	7	***Reserved***	R/W	0	
		6:4	***Reserved***	R/W	111	
		3:2	VOD Control	R/W	10	00 = 0.6 Vp-p 01 = 0.8 Vp-p 10 = 1.0 Vp-p 11 = 1.2 Vp-p
		1:0	***Reserved***	R/W	00	
09 – 10	***Reserved***	7:0	***Reserved***	R/W	00000000	
11	De-Emphasis Control	7:6	DEM_CH3	R/W	00	00 = 0 dB 01 = -3 dB 10 = -6 dB 11 = -9 dB
		5:4	DEM_CH2	R/W	00	
		3:2	DEM_CH1	R/W	00	
		1:0	DEM_CH0	R/W	00	
12	OOB Signal Detect Control	7:3	***Reserved***	R/W	00000	
		2:1	***Reserved***	R/W	11	
		0	OOB Signal Detect Control	R/W	0	0 = OOB signal detect enabled 1 = OOB signal detect disabled
13	Channel 3 EN and EQ Control	7:5	***Reserved***	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	***Reserved***	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
14	EQ Control Channel 3	7:0	Boost[7:0]	R/W	00000000	See Table 5
15	Channel 2 EN and EQ Control	7:5	***Reserved***	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	***Reserved***	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
16	EQ Control Channel 2	7:0	Boost[7:0]	R/W	00000000	See Table 5
17	Channel 1 EN and EQ Control	7:5	***Reserved***	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	***Reserved***	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
18	EQ Control Channel 1	7:0	Boost[7:0]	R/W	00000000	See Table 5

Table 4. DS100BR410 Register Map (continued)

ADD (hex)	REG Name	Bit(s)	Field	Type	Default (binary)	Description
19	Channel 0 EN and EQ Control	7:5	***Reserved***	R/W	000	
		4	Channel Enable	R/W	1	0 = Disabled 1 = Enabled
		3:1	***Reserved***	R/W	000	
		0	Boost[8]	R/W	0	See Table 5
1A	EQ Control Channel 0	7:0	Boost[7:0]	R/W	00000000	See Table 5

Table 5. Boost / EQ SMBus Register: 16 levels - recommended settings

Boost Register Bits									Result
bit[8]	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	@ 5.5 GHz
0	0	0	0	0	0	0	0	0	000'h - 2.7 dB (BST_[2:0]=000)
0	0	0	0	0	0	0	0	1	001'h - 7.3 dB (BST_[2:0]=001)
0	0	0	0	0	0	0	1	0	002'h - 10.3 dB
0	0	0	0	0	0	0	1	1	003'h - 12.2 dB (BST_[2:0]=010)
0	0	0	0	0	0	1	1	1	007'h - 16.6 dB (BST_[2:0]=011)
0	0	0	0	1	0	1	0	1	015'h - 17 dB
0	0	0	0	0	1	0	1	1	00B'h - 19.2 dB
0	0	0	0	0	1	1	1	1	00F'h - 20.6 dB (BST_[2:0]=100)
0	0	1	0	1	0	1	0	1	055'h - 21.9 dB
0	0	0	0	1	1	1	1	1	01F'h - 24.8 dB (BST_[2:0]=101)
0	0	0	1	0	1	1	1	1	02F'h - 27.6 dB (BST_[2:0]=110)
0	0	0	1	1	1	1	1	1	03F'h - 28.9 dB (BST_[2:0]=111)
0	1	0	1	0	1	0	1	0	0AA'h - 31.3 dB
0	0	1	1	1	1	1	1	1	07F'h - 33.3 dB
0	1	0	1	1	1	1	1	1	0BF'h - 35.7 dB
0	1	1	1	1	1	1	1	1	0FF'h - 37 dB

Applications Information

GENERAL RECOMMENDATIONS

The DS100BR410 is a high performance circuit capable of delivering excellent performance up to 10.3125 Gbps. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

UNUSED CHANNEL

It is recommended to disable the unused channel (EN[3:0] = LOW). The power consumption of the device is reduced when the channel is disabled.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The high speed CML inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the differential signals away from other signals and noise sources on the printed circuit board. See *AN-1187* (SNOA401) for additional information on WQFN packages.

Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each via hole. To further improve the signal quality, a ground via placed close to the signal via for a low inductance return current path is recommended. When the via structure is associated with stripline trace and a thick board, further optimization such as back drilling is often used to reduce the high frequency effects of via stubs on the signal path. To minimize cross-talk coupling, it is recommended to have >3X gap spacing between the differential pairs. For example, if the trace width is 5 mils with 5 mils spacing – 100Ω differential impedance (closely coupled). The gap spacing between the differential pairs should be >15 mils.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS100BR410 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1uF or 0.01 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS100BR410. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

Typical Performance Curves Characteristics

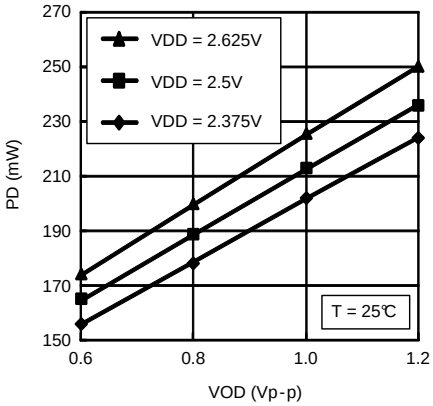


Figure 8. Power Dissipation (PD) vs. Output Differential Voltage (VOD)

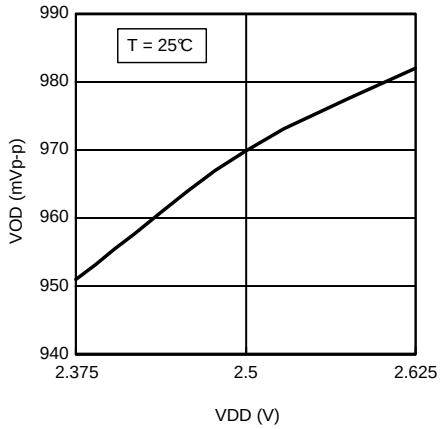


Figure 9. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Supply Voltage (VDD)

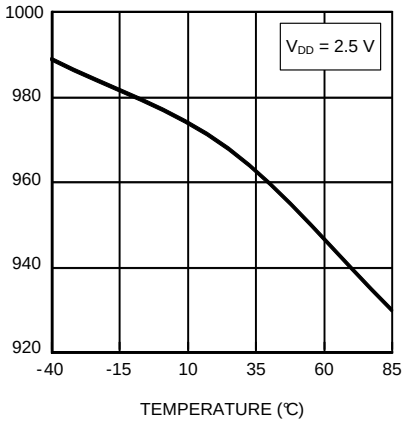


Figure 10. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature

Typical Performance Eye Diagrams Characteristics

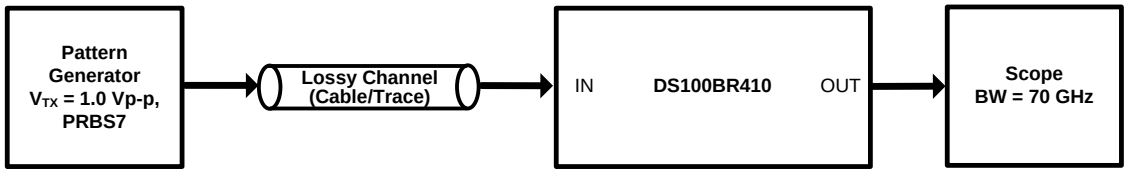


Figure 11. Test Setup Connections Diagram

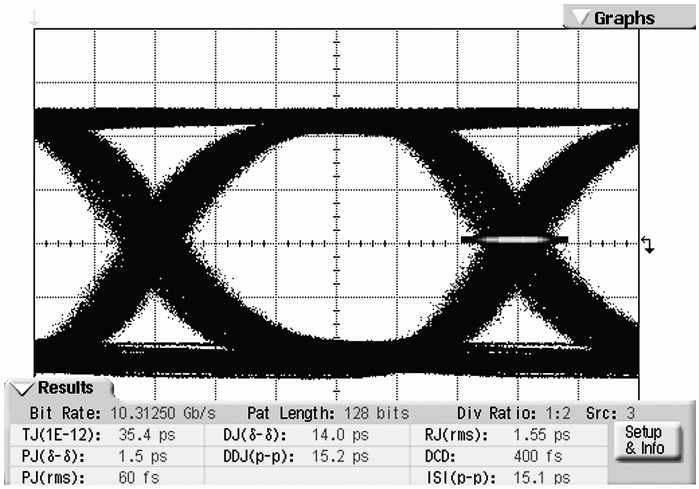


Figure 12. 12 meters, 30–AWG Cable at 10.3125 Gbps, BST[2:0] = 111, DE_SEL = 0 dB

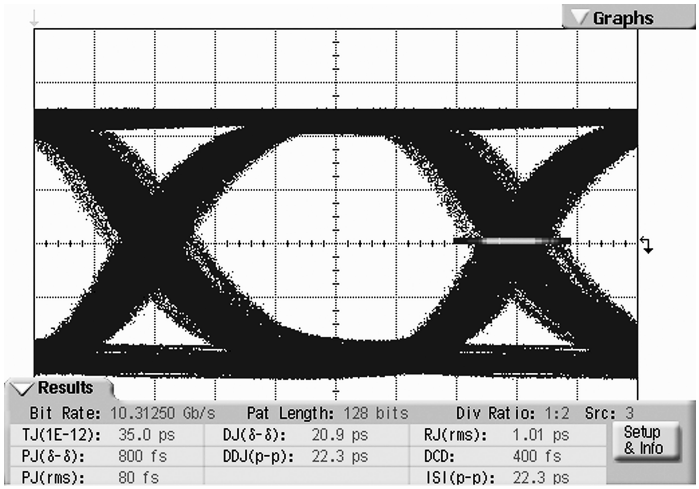


Figure 13. 40 inches, 6–mil FR4 Trace at 10.3125 Gbps, BST[2:0] = 101, DE_SEL = 0 dB

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS100BR410SQ/NOPB	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	100BR410
DS100BR410SQ/NOPB.A	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	100BR410
DS100BR410SQE/NOPB	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	100BR410
DS100BR410SQE/NOPB.A	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	100BR410
DS100BR410SQX/NOPB	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	100BR410
DS100BR410SQX/NOPB.A	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	100BR410
DS100BR410SQX/NOPB.B	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

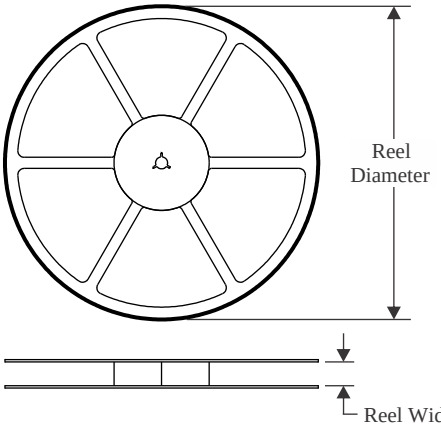
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

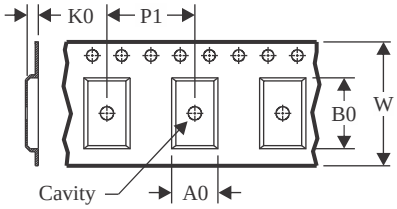
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

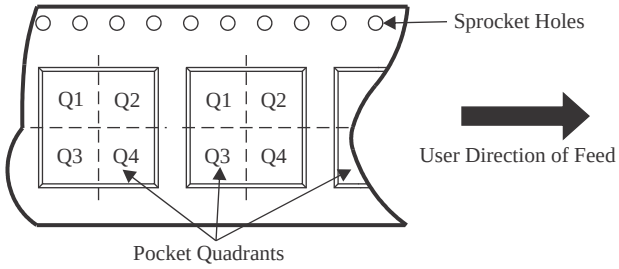


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

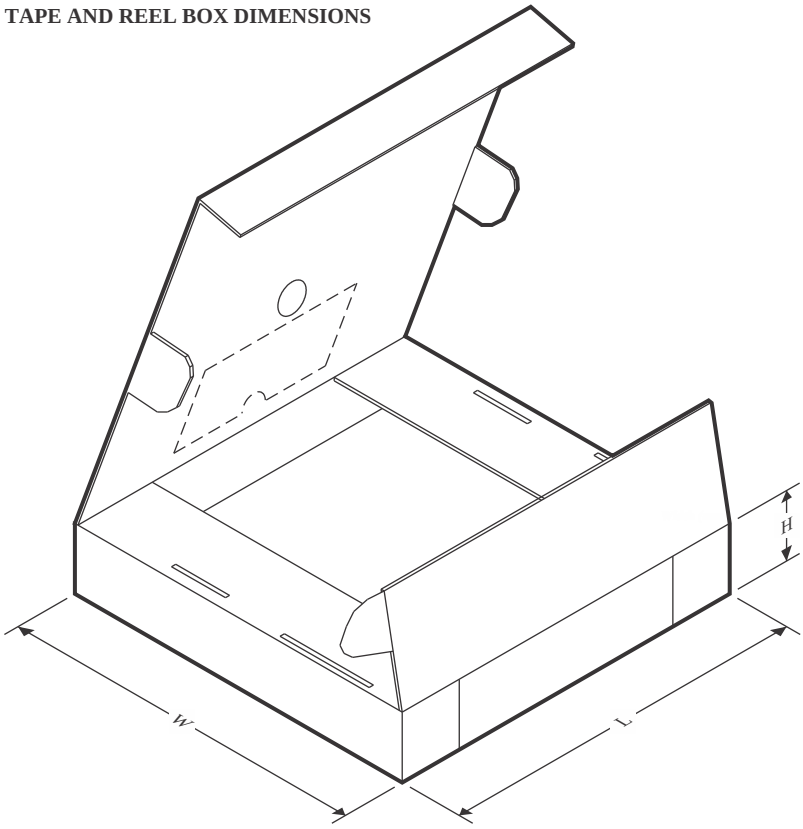
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS100BR410SQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS100BR410SQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS100BR410SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

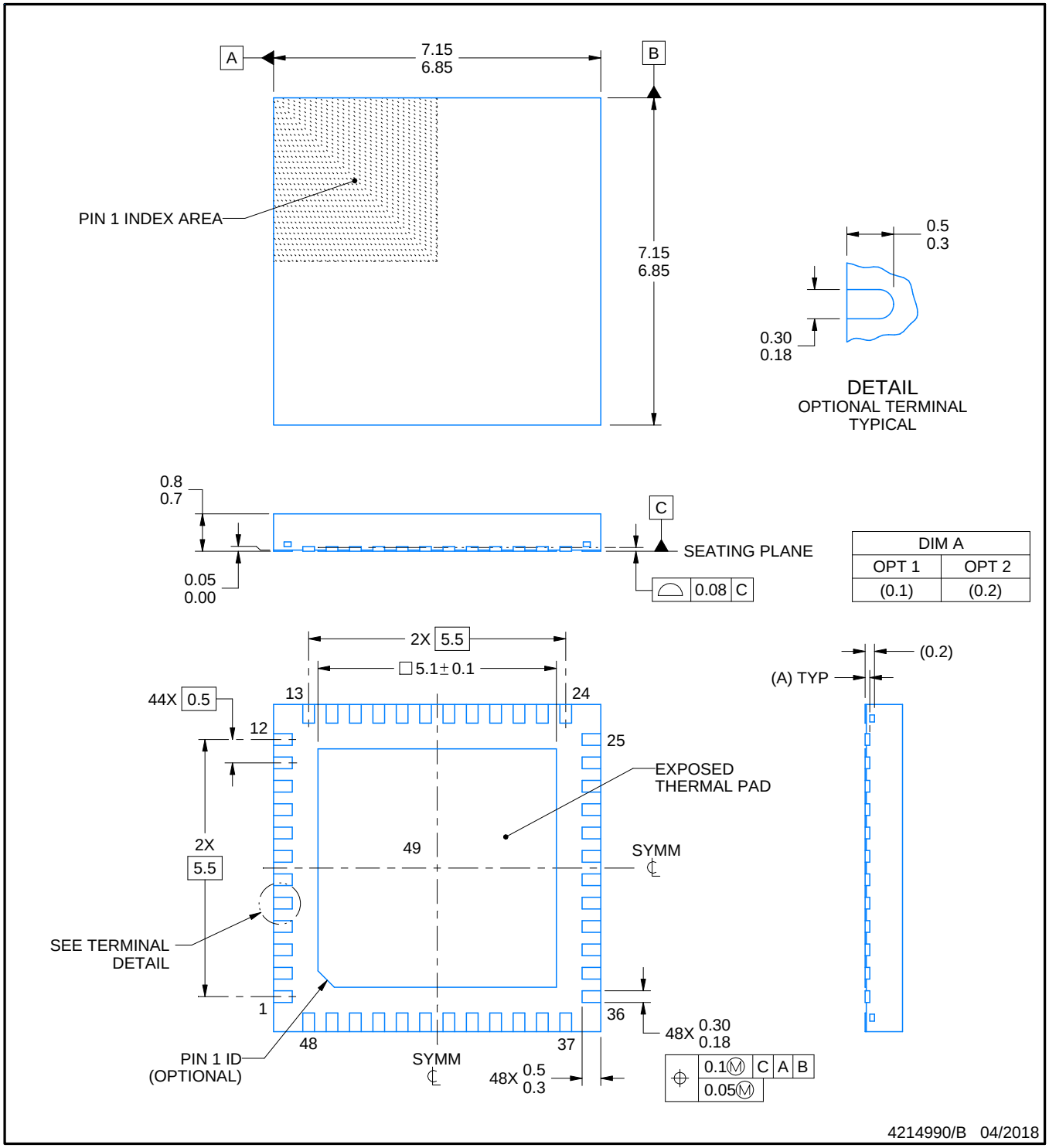
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS100BR410SQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	36.0
DS100BR410SQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS100BR410SQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	36.0

PACKAGE OUTLINE

RHS0048A

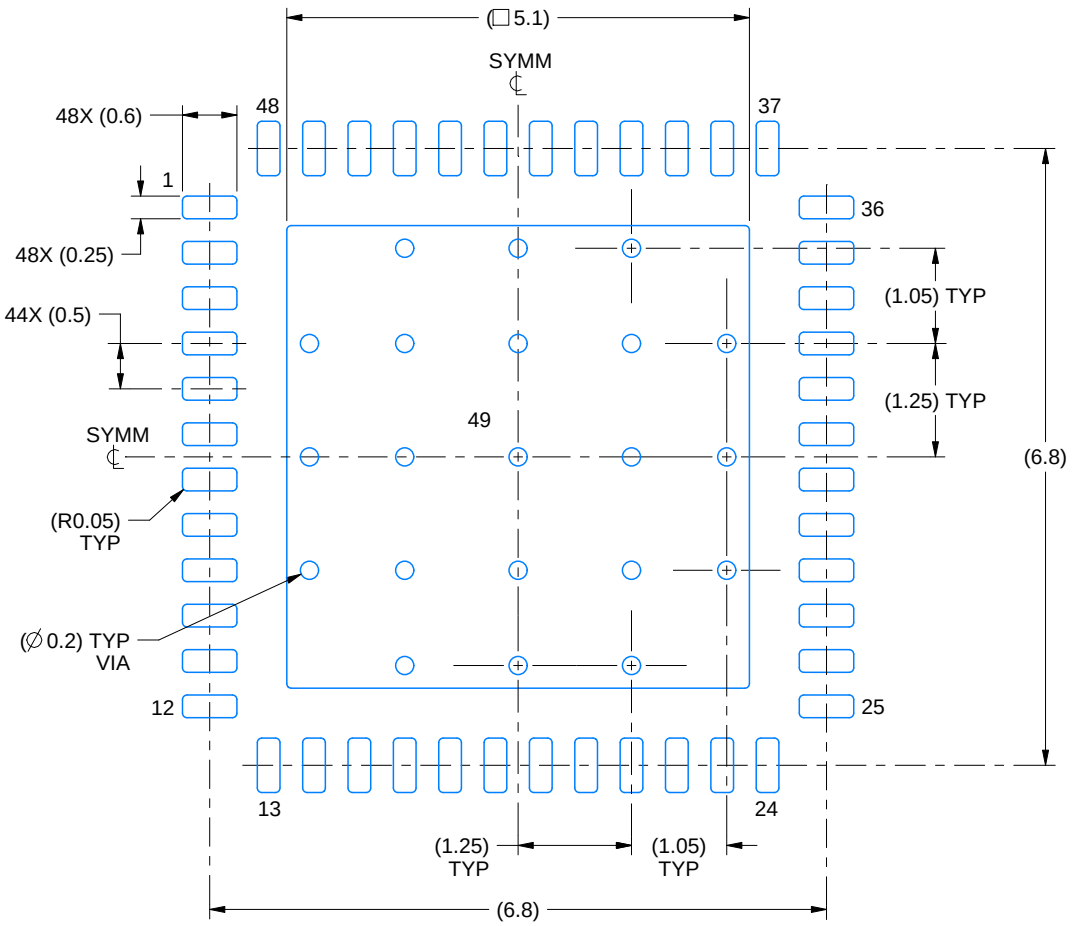
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

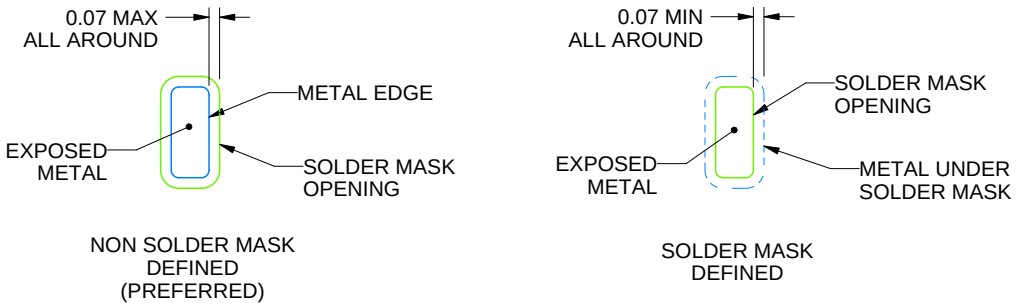


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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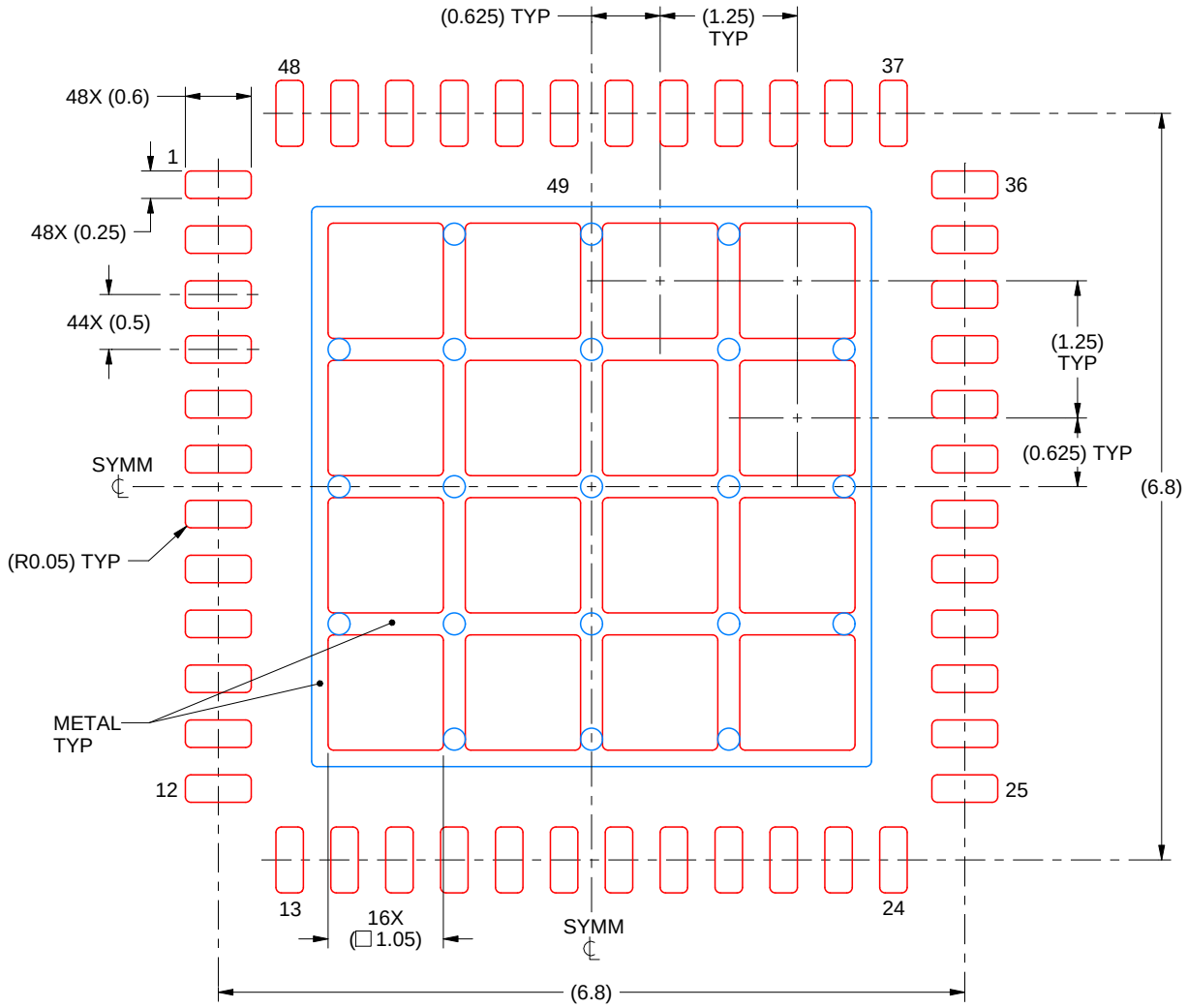
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025