

# DS90LVRA2-Q1 Automotive LVDS Dual Differential Line Receiver

## 1 Features

- AEC-Q100 and AEC-Q006 qualified for automotive applications
  - Temperature grade 2:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- 600Mbps (300MHz) switching rates
- 50ps differential skew (typical)
- 0.1ns channel-to-channel skew (typical)
- Supports 1.8V to 3.3V power supply
- Flow-through pinout
- Power down high impedance on LVDS inputs
- Output slew rate control
- LVDS inputs accept LVDS/CML/LVPECL signals
- Conforms to ANSI/TIA/EIA-644 standard
- Pin compatible with DS90LV028A-Q1

## 2 Applications

- [Automotive infotainment and cluster](#)
- [Automotive head unit](#)

## 3 Description

The DS90LVRA2-Q1 is a dual CMOS differential line receiver designed for applications requiring high input common mode range, high data rates, and CMOS output with slew rate control. The device is designed to support data rates of 600Mbps (300MHz) utilizing low voltage differential signaling (LVDS) technology.

The DS90LVRA2-Q1 accepts low voltage (350mV typical) differential input signals and translates them from 1.8V to 3.3V CMOS output levels depending on power supply voltage. The DS90LVRA2-Q1 has a flow-through design for easy PCB layout.

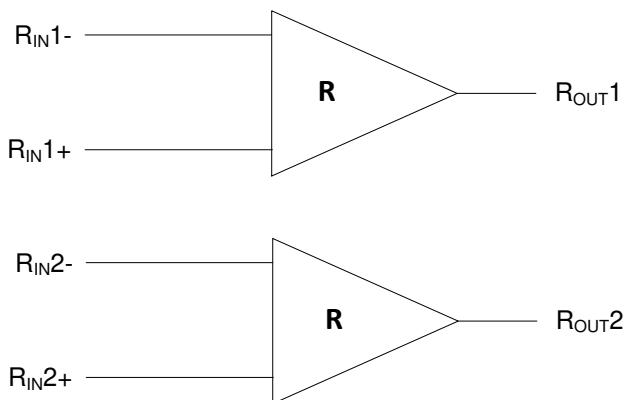
The DS90LVRA2-Q1 and companion LVDS line driver DS90LV027AQ provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
DS90LVRA2-Q1	DEM (WSON, 8)	2mm × 2mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



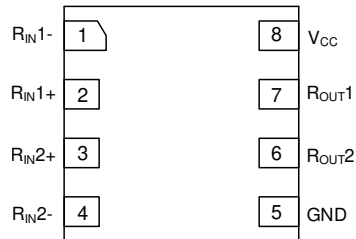
**Functional Diagram**



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## 4 Pin Configuration and Functions



**Figure 4-1. DEM Package, WSON 8 Pin (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
GND	5	G	Ground pin
R <sub>IN1-</sub>	1	I	Inverting receiver input pin
R <sub>IN2-</sub>	4	I	
R <sub>IN1+</sub>	2	I	Non-inverting receiver input pin
R <sub>IN2+</sub>	3	I	
R <sub>OUT2</sub>	6	O	Receiver output pin
R <sub>OUT1</sub>	7	O	
V <sub>CC</sub>	8	P	Power supply pin

(1) I = input, O = output, G = ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage ( $V_{CC}$ )		-0.3	4	V
Input Voltage ( $R_{IN+}$ , $R_{IN-}$ )		-5	6	V
Differential Voltage ( $R_{IN+}$ - $R_{IN-}$ ) for LVDS		0	3	V
Output Voltage ( $R_{OUT}$ )		-0.3	3.6	V
Lead Temperature Range Soldering	(4 sec.)		260	°C
Maximum Junction Temperature			135	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per AEC Q100-011 <sup>(2)</sup>	±1000	

- (1) AEC Q100-002 HBM ESD Classification Level 2  
(2) AEC Q100-011 CDM ESD Classification Level C4A

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage (3.3V mode)	3.0	3.3	3.6	V
$V_{CC}$	Supply voltage (2.5V mode)	2.25	2.5	2.75	V
$V_{CC}$	Supply voltage (1.8V mode)	1.62	1.80	1.98	V
$V_R$	Receiver input voltage (LVDS)	0		3.0	V
$T_A$	Operating free-air temperature	-40		105	°C
$T_{PCB}$	PCB temperature (1mm away from device)			112	°C
$T_J$	Junction temperature			125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DEM	UNIT
		(WSN)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	5.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	69.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ITH}$	Differential input high threshold	$V_{IB} = -4\text{ V or }5\text{ V}, V_{CC} = 1.62\text{ V to }3.6\text{ V}$	100			mV
$V_{ITL}$	Differential input low threshold		-100			
$V_{HYS}$	Differential input voltage hysteresis, $V_{IT1} - V_{IT2}$	$V_{CC} = 1.62\text{ V to }3.6\text{ V}$	20	40	120	mV
$V_{CM\_RANGE}$	Input common mode voltage range	$V_{CC} = 1.62 - 1.98\text{ V}$	-1	1.2	2	V
		$V_{CC} = 2.3 - 2.7\text{ V}$	-2.5	1.2	3	V
		$V_{CC} = 3.0 - 3.6\text{ V}$	-4	1.2	5	V
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}, V_{CC} = 1.8\text{ V} \pm 10\%$	1.3			V
		$I_{OH} = -4\text{ mA}, V_{CC} = 2.5\text{ V} \pm 10\%$	1.8			V
		$I_{OH} = -4\text{ mA}, V_{CC} = 3.3\text{ V} \pm 10\%$	2.6			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}, V_{CC} = 1.8\text{ V} \pm 10\%$			0.2	V
		$I_{OL} = 4\text{ mA}, V_{CC} = 2.5\text{ V} \pm 10\%$			0.3	V
		$I_{OL} = 4\text{ mA}, V_{CC} = 3.3\text{ V} \pm 10\%$			0.4	V
$I_{CC\_ACTIVE}$	Supply current	$V_{CC} = 3.6\text{ V}, \text{ No load, Steady-state, } V_{ID}=200\text{ mV/-}200\text{ mV}$			25	mA
		$V_{CC} = 2.7\text{ V}, \text{ No load, Steady-state, } V_{ID}=200\text{ mV/-}200\text{ mV}$			25	mA
		$V_{CC} = 1.98\text{ V}, \text{ No load, Steady-state, } V_{ID}=200\text{ mV/-}200\text{ mV}$			25	mA
$I_I$	Input current (A or B inputs)	$V_I = -1.0\text{ V}, \text{ Other input open}$			$\pm 35$	$\mu\text{A}$
		$V_I = 2.4\text{ V}, \text{ Other input open}$			$\pm 20$	$\mu\text{A}$
		$V_I = -4\text{ V}, \text{ Other input open (split between } 85^\circ\text{C) } (\pm 80\text{ }\mu\text{A})$			$\pm 120$	$\mu\text{A}$
		$V_I = 5\text{ V}, \text{ Other input open}$			$\pm 40$	$\mu\text{A}$
$I_{I(OFF)}$	Power-off output current (Y or Z outputs)	$V_Y \text{ or } V_Z = 1.98\text{ V}, V_{CC} = 0\text{ V}$			$\pm 20$	$\mu\text{A}$
$I_{I(OFF)}$	Power-off input current (A or B inputs)	$V_A \text{ or } V_B = -1\text{ V or }2.0\text{ V}, V_{CC} = 0\text{ V}$			$\pm 30$	$\mu\text{A}$
		$V_A \text{ or } V_B = -4\text{ or }5\text{ V}, V_{CC} = 0\text{ V}$			$\pm 70$	$\mu\text{A}$
		$V_A \text{ or } V_B = 0\text{ V or }2.4\text{ V}, V_{CC} = 0\text{ V}$			$\pm 30$	$\mu\text{A}$

## 5.6 Switching Characteristics

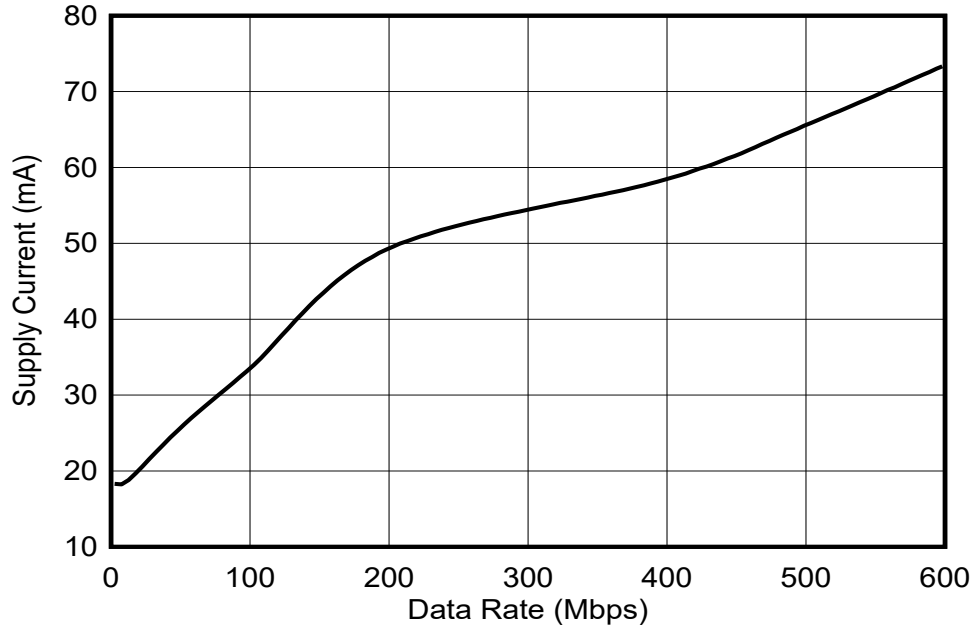
$V_{ID} = 200\text{mV}$ ,  $C_L = 10\text{pF}$  and over operating temperature ranges, unless otherwise specified. <sup>(1)</sup> <sup>(2)</sup>

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{PHLD}$	Differential Propagation Delay High to Low	$V_{CC} = 1.8\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	2.5	4.4	7.7	ns
		$V_{CC} = 2.5\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	2.2	3.3	5.1	ns
		$V_{CC} = 3.3\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	1.9	2.9	4.1	ns
$t_{PLHD}$	Differential Propagation Delay Low to High	$V_{CC} = 1.8\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	2.7	4.4	7.7	ns
		$V_{CC} = 2.5\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	2.4	3.4	5.1	ns
		$V_{CC} = 3.3\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	2.2	3.1	4.1	ns
$t_{SKD1\_S}$	Differential Pulse Skew ( $t_{PHLD} - t_{PLHD}$ ) <sup>(3)</sup>	$V_{CC} = 1.8\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	-680		680	ps
		$V_{CC} = 2.5\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	-500		500	ps
		$V_{CC} = 3.3\text{V} \pm 10\%$ , $\text{trf} = 1\text{ns}$	-610		610	ps
$t_{SKD1\_400M}$	Differential Pulse Skew ( $t_{PHLD} - t_{PLHD}$ ) <sup>(3)</sup>	$V_{CC} = 1.8\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$ , 400Mbps	-1990		1990	ps
		$V_{CC} = 2.5\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$ , 400Mbps	-1400		1400	ps
		$V_{CC} = 3.3\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$ , 400Mbps	-1800		1800	ps
$t_{SKD2}$	Differential Channel-to-Channel Skew <sup>(4)</sup>	$V_{CC} = 1.8\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$			0.6	ns
		$V_{CC} = 2.5\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$			0.3	ns
		$V_{CC} = 3.3\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$			0.3	ns
$t_{SKD3}$	Differential Part to Part Skew <sup>(5)</sup>	$V_{CC} = 1.8\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$			3.0	ns
		$V_{CC} = 2.5\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$			1.7	ns
		$V_{CC} = 3.3\text{V} \pm 10\%$ , $\text{trf} = 0.25\text{ns}$			1.2	ns
$t_R$	Rise Time	$V_{CC} = 1.8\text{V}$	250	500	740	ps
		$V_{CC} = 2.5\text{V}$	250	390	740	ps
		$V_{CC} = 3.3\text{V}$	250	450	740	ps
$t_F$	Fall Time	$V_{CC} = 1.8\text{V}$	250	560	740	ps
		$V_{CC} = 2.5\text{V}$	250	360	740	ps
		$V_{CC} = 3.3\text{V}$	250	400	740	ps
$f_{MAX}$	Maximum Operating Frequency <sup>(11)</sup>		300			MHz

- (1)  $C_L$  includes probe and jig capacitance.
- (2) Generator waveform for all tests unless otherwise specified:  $f = 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r$  and  $t_f$  (0% to 100%)  $\leq 3\text{ns}$  for  $R_{IN}$ .
- (3)  $t_{SKD1}$  is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
- (4)  $t_{SKD2}$  is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
- (5)  $t_{SKD3}$ , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.
- (6)  $f_{MAX}$  generator input conditions:  $t_r = t_f < 1\text{ns}$  (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle,  $V_{OL}$  (max),  $V_{OH}$  (min), load =  $15\text{pF}$  (stray plus probes).

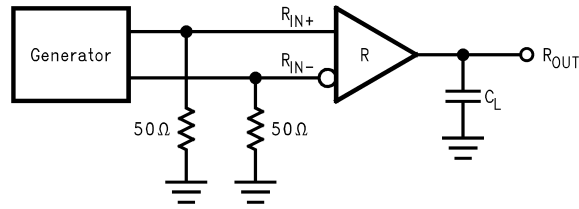
### 5.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ , Load = 5pF (unless otherwise notes)

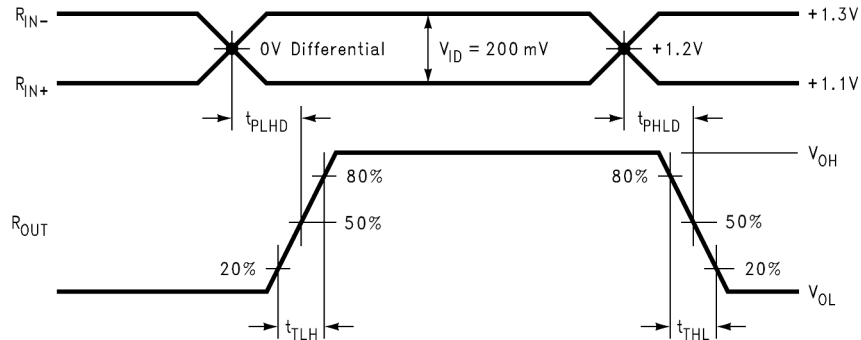


**Figure 5-1. Power Supply Current vs Data Rate ( $V_{CC} = 1.8\text{V}$ , 2 Channels)**

## 6 Parameter Measurement Information



**Figure 6-1. Receiver Propagation Delay and Transition Time Test Circuit**



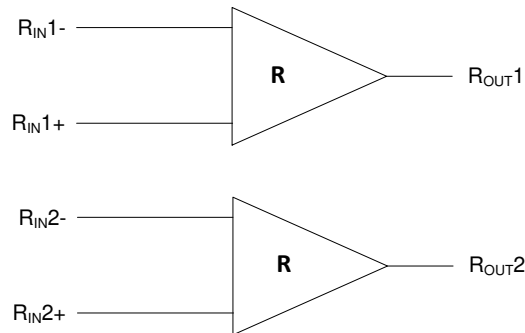
**Figure 6-2. Receiver Propagation Delay and Transition Time Waveforms**

## 7 Detailed Description

### 7.1 Overview

Figure 8-1 shows how LVDS drivers and receivers are intended to be used primarily in a simple point-to-point configuration. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the source through a impedance controlled 100Ω differential PCB traces. Use a termination resistor of 100Ω and place it as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The DS90LVRA2-Q1 differential line receiver is capable of detecting signals as low as 100mV over a common-mode range of -4V to 5V ( $V_{CC}$  at 3.3V). The common voltage range is related to the LVDS driver offset voltage, which is typically +1.2V. The differential signal from the LVDS driver is centered around the +1.2V offset voltage and may shift around this center point. The shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of +0V to +3V (measured from each pin to ground).

### 7.4 Device Functional Modes

**Table 7-1. Truth Table**

INPUTS <sup>(1)</sup>	OUTPUT
$V_{ID} \geq 100\text{mV}$	H
$V_{ID} \leq -100\text{mV}$	L
$-100\text{mV} \leq V_{ID} \leq 100\text{mV}$	Undetermined

(1)  $V_{ID} = [R_{IN+}] - [R_{IN-}]$

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

For general application guidelines and hints about LVDS drivers and receivers, refer to the [LVDS application notes and design guides](#).

### 8.2 Typical Application

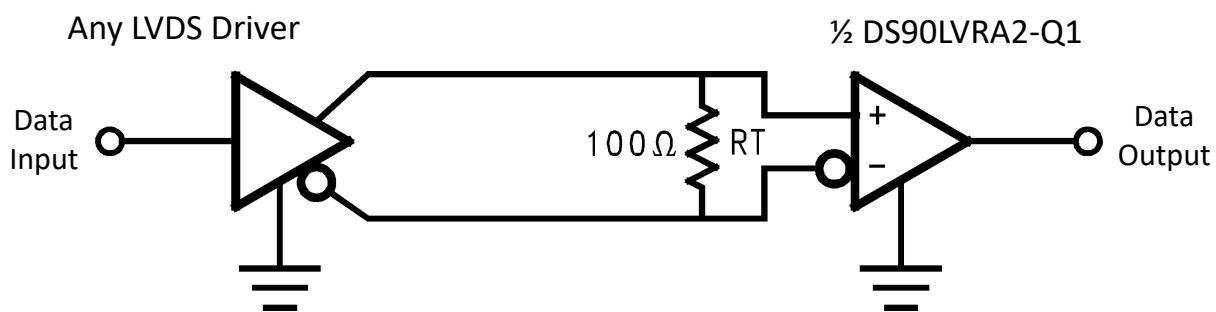


Figure 8-1. Balanced System Point-to-Point Application

#### 8.2.1 Design Requirements

When using LVDS devices, it is important to specify controlled impedance PCB traces. All components of the transmission media must have a matched differential impedance of  $100\Omega$  and must not introduce major impedance discontinuities.

#### 8.2.2 Detailed Design Procedure

##### 8.2.2.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. It is recommended to use surface mount high frequency ceramic  $0.1\mu\text{F}$  and  $0.01\mu\text{F}$  capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A  $10\mu\text{F}$  (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

##### 8.2.2.2 Termination

Use a termination resistor that best matches the differential impedance or the transmission line. The resistor should be between  $90\Omega$  and  $110\Omega$ . Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice. Surface mount 1% resistors are the best

PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be  $< 10\text{mm}$  (12mm maximum).

### 8.2.2.3 Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to  $V_{DD}$  through a pull up resistor and ties the negative LVDS input pin to GND by a pull down resistor. The pull up and pull down resistors should be in the 5k $\Omega$  to 15k $\Omega$  range to minimize loading and waveform distortion to the driver. Set the common-mode bias point to approximately 1.2V so that it is compatible with the internal circuitry. For more information, refer to application note AN-1194 [Failsafe Biasing of LVDS Interfaces](#).

### 8.2.2.4 Probing LVDS Transmission Lines

Always use high impedance (> 100k $\Omega$ ), low capacitance (< 2pF) scope probes with a wide bandwidth (1GHz) scope. Improper probing will give deceiving results.

### 8.2.3 Application Curves

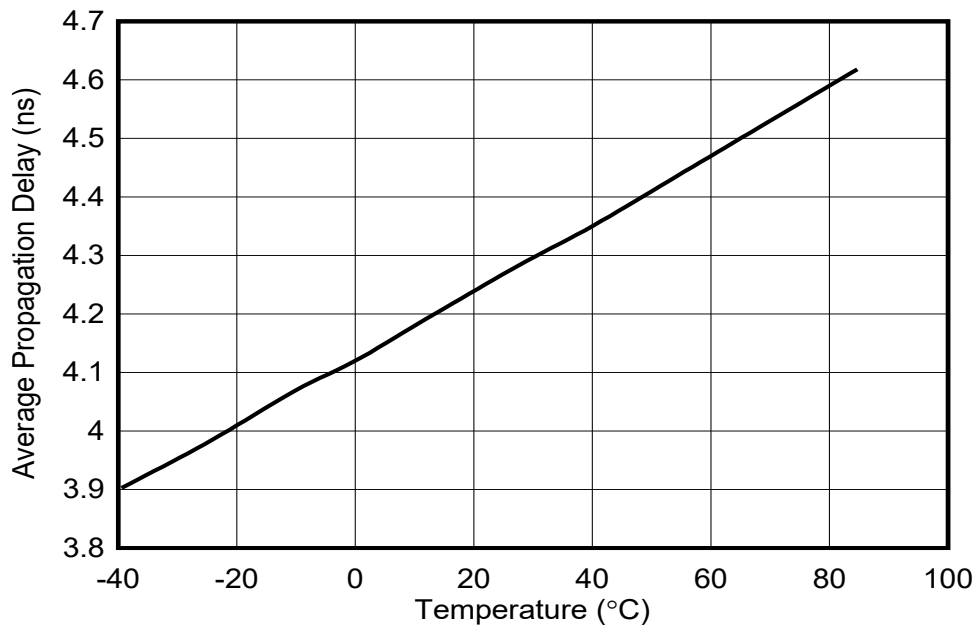


Figure 8-2. Propagation Delay vs Temperature ( $V_{CC} = 1.8V$ , Load = 10pF, Average of 2 Channels)

## 8.3 Power Supply Recommendations

Bypass capacitors must be used on power pins. TI recommends using high-frequency, ceramic, 0.1 $\mu$ F and 0.01 $\mu$ F capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10 $\mu$ F bulk capacitor, 35V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

## 8.4 Layout

### 8.4.1 Layout Guidelines

#### 8.4.1.1 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission trace and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and make sure noise is coupled as common-mode. In fact, differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode, which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. It is important to note: skew between the signals of a pair means a phase difference between signals, which destroys the magnetic field cancellation benefits of differential signals and EMI, will result. (Note that the velocity of propagation,  $v = c/E_r$ , where  $c$  (the speed of light) = 0.2997mm/ps or 0.0118in/ps). Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowed.

#### 8.4.1.2 PC Board Considerations

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, and TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers, which are isolated by one or more power or ground planes.

#### 8.4.2 Layout Examples

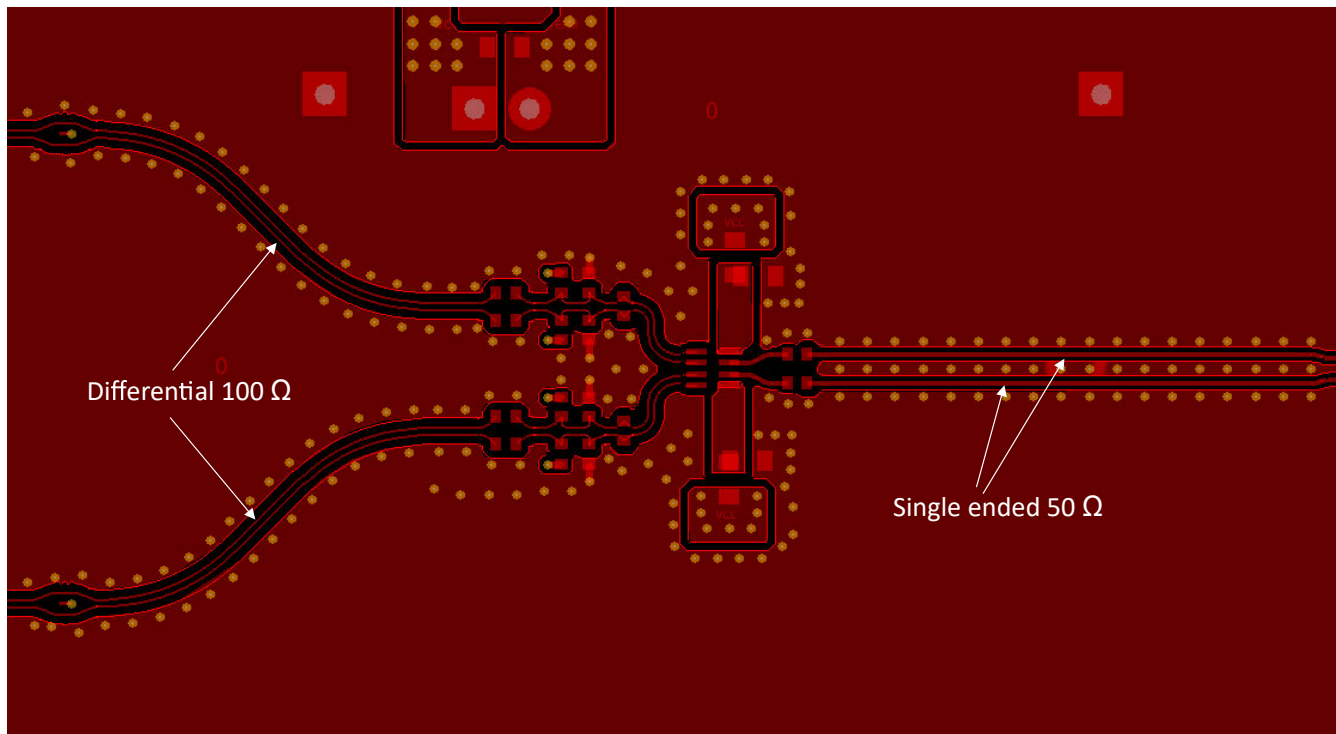


Figure 8-3. EVM Layout

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Failsafe Biasing of LVDS Interfaces application note](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial Release

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">D9LVRA2DEMRQ1</a>	Active	Production	WSON (DEM)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LR2Q
D9LVRA2DEMRQ1.A	Active	Production	WSON (DEM)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LR2Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF DS90LVRA2-Q1 :**

- Catalog : [DS90LVRA2](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
D9LVRA2DEMRQ1	WS0N	DEM	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
D9LVRA2DEMRQ1	WSON	DEM	8	3000	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

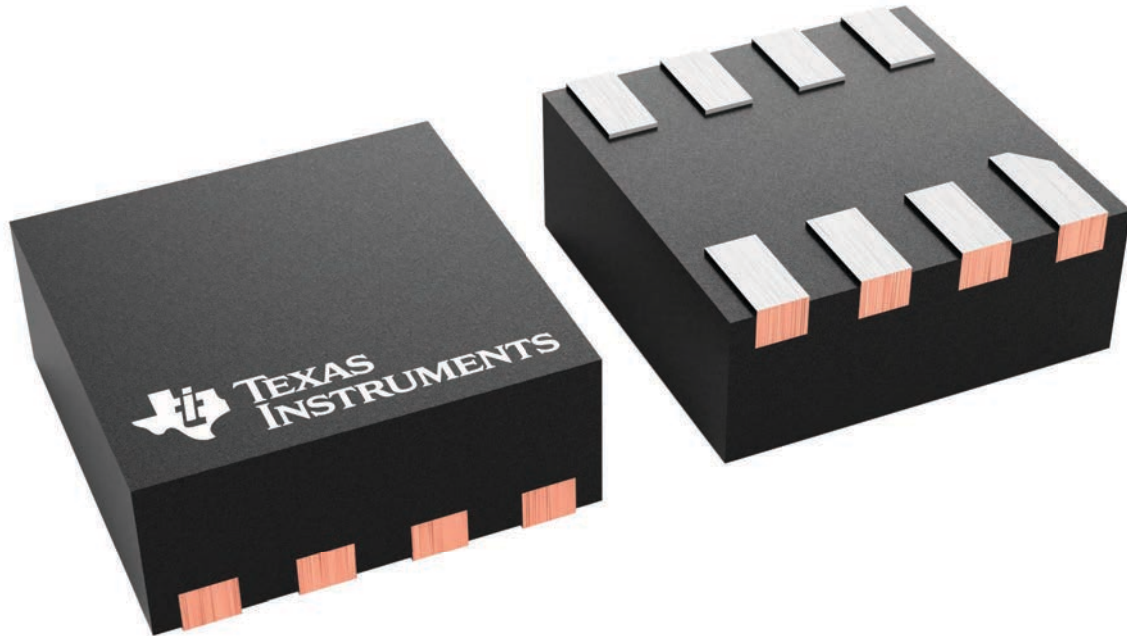
**DQF 8**

**WSON - 0.8 mm max height**

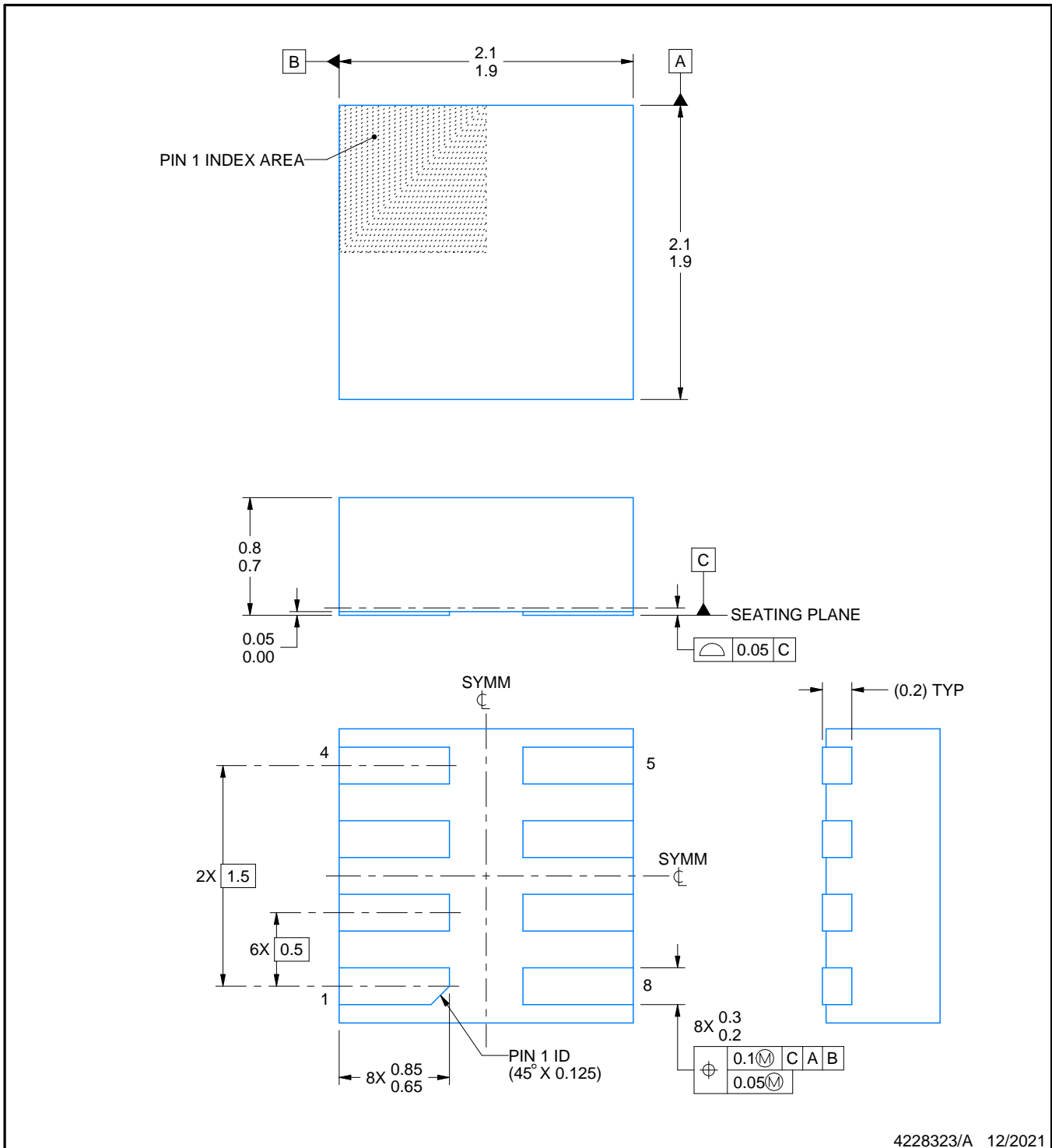
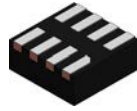
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4232898/A



NOTES:

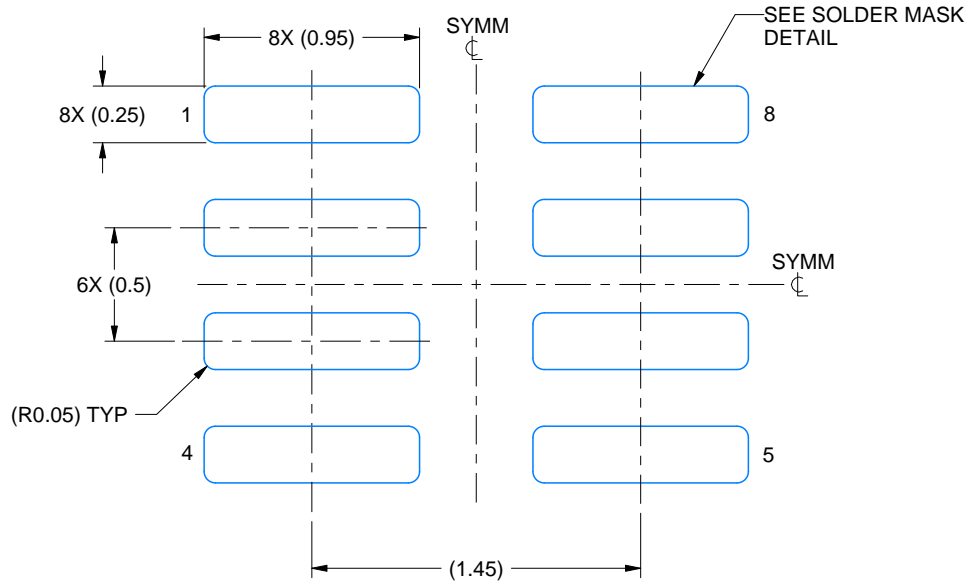
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

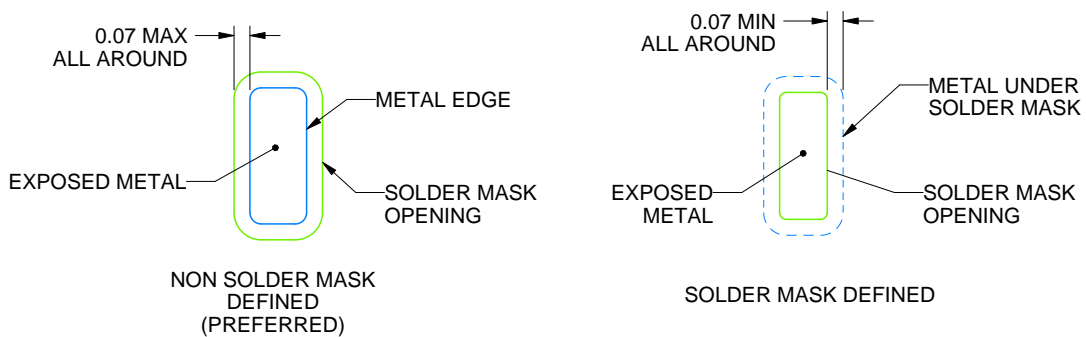
DEM0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 30X



SOLDER MASK DETAILS

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NOTES: (continued)

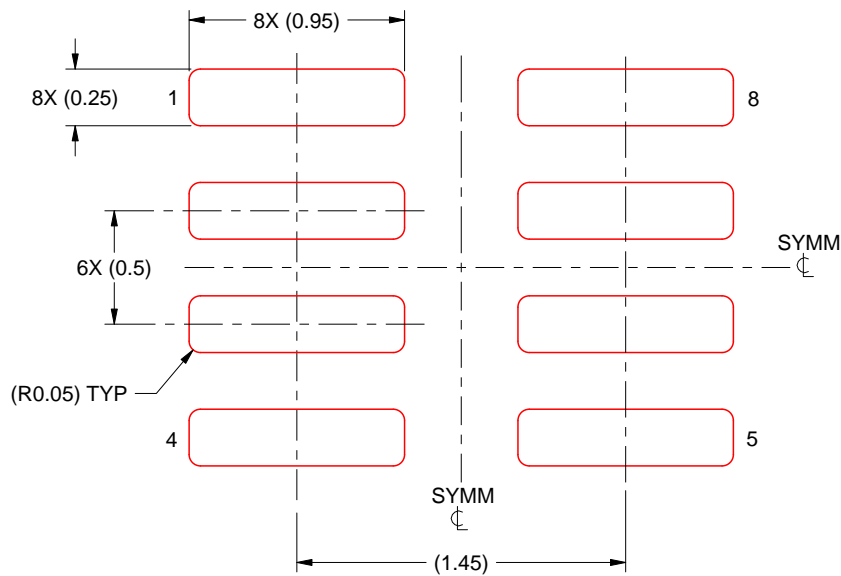
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DEM0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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