DS90UB633A-Q1 FPD-Link III Serializer for 1-MP/60-fps Cameras 10/12 Bits,100 MHz

1 Features

- AEC-Q100 qualified for automotive applications with the following results:
  - Device temperature grade 2: –40°C to +105°C ambient operating temperature
- 56.25-MHz to 100-MHz input pixel clock support
- Robust Power-Over-Coaxial (PoC) operation
- Programmable data payload:
  - 8/10-Bit payload 75-MHz to 100-MHz
  - 12-Bit payload 56.25-MHz to 100-MHz
- Continuous low latency bidirectional control interface channel with I2C support at 400-kHz
- Embedded clock with DC-balanced coding to support AC-coupled interconnects
- Capable of driving up to 15-m coaxial or Shielded Twisted-Pair (STP) cables
- 4 Dedicated General-Purpose Input/Output (GPIO)
- 1.8-V, 2.8-V or 3.3-V compatible parallel inputs on serializer
- Single power supply at 1.8-V
- ISO 10605 and IEC 61000-4-2 ESD compliant
- Compatible with DS90UB66x-Q1 and DS90UB63x-Q1 deserializers

2 Applications

- Automotive
  - Surround View Systems (SVS)
  - Front Cameras (FC)
  - Rear View Cameras (RVC)
  - Sensor fusion
  - Driver Monitor Cameras (DMS)
  - Remote satellite RADAR, ToF, and LIDAR sensors
- Security and surveillance
- Machine vision applications

3 Description

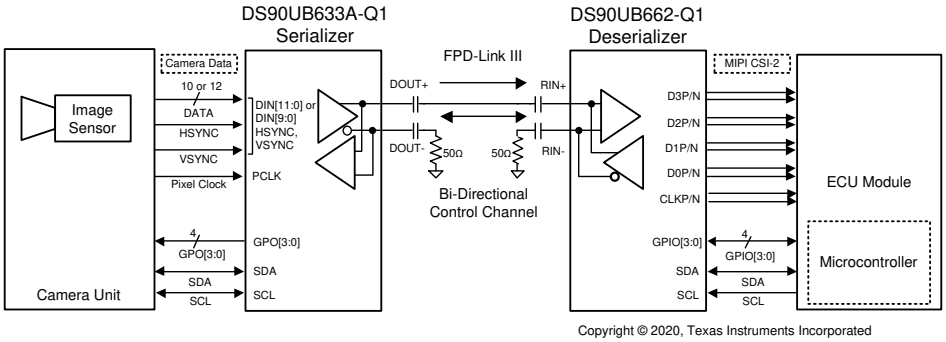
The DS90UB633A-Q1 device offers an FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. The DS90UB633A-Q1 device incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer/deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU). This device is ideally suited for driving video data requiring up to 12-bit pixel depth plus two synchronization signals along with bidirectional control channel bus.

Using TI's embedded clock technology allows transparent full-duplex communication over a single differential pair, carrying asymmetrical-bidirectional control channel information. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. This significantly saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins. Internal DC-balanced encoding/decoding is used to support AC-coupled interconnects.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB633A-Q1	WQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2020) to Revision A (November 2020)	Page
• Updated marketing status from Advance Information to production data.	1

5 Pin Configuration and Functions

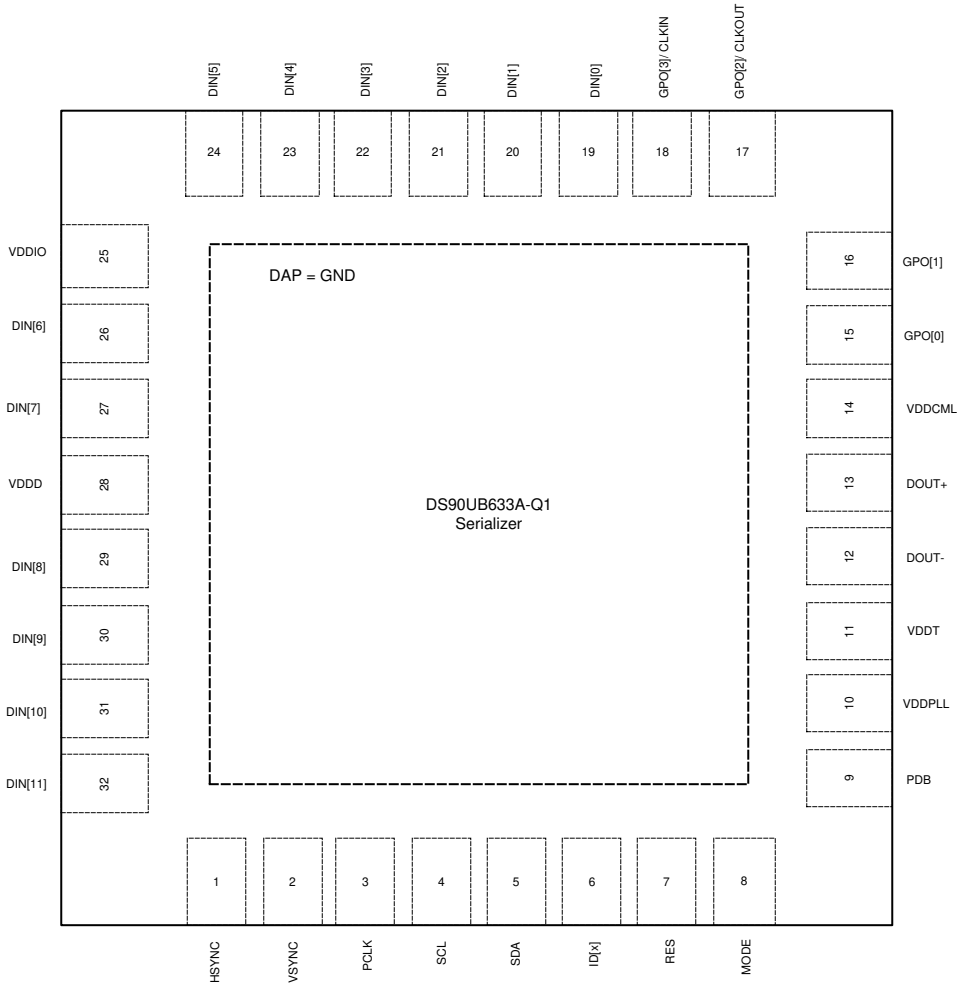


Figure 5-1. RTV Package 32-Pin WQFN Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
DIN[0:11]	19,20,21,22, 23,24,26,27, 29,30,31,32	Inputs, LVCMOS w/ pulldown	Parallel data Inputs. For 10-bit MODE, parallel inputs DIN[0:9] are active. DIN[10:11] are inactive and should not be used. Any unused inputs (including DIN[10:11]) must be No Connect. For 12-bit MODE, parallel inputs DIN[0:11] are active. Any unused inputs must be No Connect.
HSYNC	1	Input, LVCMOS w/ pulldown	Horizontal SYNC input. Note: HS transition restrictions: 1. 12-bit mode: No HS restrictions (raw) 2. 10-bit mode: HS restricted to no more than one transition per 10 PCLK cycles. Leave open if unused.
VSYNC	2	Input, LVCMOS w/ pulldown	Vertical SYNC input. Note: VS transition restrictions: 1. 12-bit mode: No VS restrictions (raw) 2. 10-bit mode: VS restricted to no more than one transition per 10 PCLK cycles. Leave open if unused.
PCLK	3	Input, LVCMOS w/ pulldown	Pixel clock input pin. Strobe edge set by TRFB control register 0x03[0].
GENERAL PURPOSE OUTPUT (GPO)			

PIN		I/O	DESCRIPTION
NAME	NO.		
GPO[1:0]	16,15	Output, LVCMOS	General-purpose output pins can be configured as outputs, used to control and respond to various commands. GPO[1:0] can be configured to be the outputs for input signals coming from GPIO[1:0] pins on the deserializer or can be configured to be outputs of the local register on the serializer. Leave open if unused.
GPO[2]/ CLKOUT	17	Output, LVCMOS	GPO[2] pin can be configured to be the output for input signal coming from the GPIO[2] pin on the deserializer or can be configured to be the output of the local register on the Serializer. It can also be configured to be the output clock pin when the DS90UB633A-Q1 device is used in the external oscillator mode. See *Section 7.4* for a detailed description of External Oscillator mode. It is recommended to pull GPO2 to GND with a minimum 40-kΩ resistor to ensure GPO2=LOW when PDB transitions from LOW to HIGH.
GPO[3]/ CLKIN	18	Input/Output, LVCMOS	GPO[3] can be configured to be the output for input signals coming from the GPIO[3] pin on the deserializer or can be configured to be the output of the local register setting on the serializer. It can also be configured to be the input clock pin when the DS90UB633A-Q1 serializer is working with an external oscillator. See *Section 7.4* for a detailed description of external oscillator mode. Leave open if unused.
BIDIRECTIONAL CONTROL BUS - I2C-COMPATIBLE			
SCL	4	Input/Output, Open Drain	Clock line for the bidirectional control bus communication SCL requires an external pullup resistor to $V_{(VDDIO)}$.
SDA	5	Input/Output, Open Drain	Data line for the bidirectional control bus communication SDA requires an external pullup resistor to $V_{(VDDIO)}$.
MODE	8	Input, analog	Device mode select Resistor (Rmode) to ground and 10-kΩ pullup to 1.8 V rail. MODE pin on the serializer can be used to select whether the system is running off the PCLK from the imager or an external oscillator. See details in Table 7-2.
IDX	6	Input, analog	Device ID Address Select The IDX pin on the serializer is used to assign the I2C device address. Resistor (RID) to Ground and 10-kΩ pullup to 1.8 V rail. See Table 7-6.
CONTROL AND CONFIGURATION			
PDB	9	Input, LVCMOS w/ pulldown	Power-down mode input pin PDB = H, Serializer is enabled and is ON. PDB = L, Serializer is in power down mode. When the serializer is in power down, the PLL is shut down, and IDD is minimized. Programmed control register data is NOT retained and reset to default values.
RES	7	Input, LVCMOS w/ pulldown	Reserved *This pin MUST be tied LOW.*
FPD–Link III INTERFACE			
DOUT+	13	Input/Output, CML	Non-inverting differential output, bidirectional control channel input. The interconnect must be AC coupled with a 0.1-µF capacitor.
DOUT-	12	Input/Output, CML	Inverting differential output, bidirectional control channel input. The interconnect must be AC coupled with a 0.1-µF capacitor. For applications using single-ended coaxial interconnect, place a 0.047-µF AC-coupling capacitor in series with a 50-Ω resistor before terminating to GND.
POWER AND GROUND(1)			
VDDPLL	10	Power, Analog	PLL power, 1.8 V ±5%.
VDDT	11	Power, Analog	Tx analog power, 1.8 V ±5%.
VDDCML	14	Power, Analog	CML and bidirectional channel driver power, 1.8 V ±5%.
VDDD	28	Power, Digital	Digital Power, 1.8 V ±5%.
VDDIO	25	Power, Digital	Power for I/O stage. The single-ended inputs and SDA, SCL are powered from $V_{(VDDIO)}$. VDDIO can be connected to a 1.8 V ±5% or 2.8 V ±10% or 3.3 V ±10%.
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 9 vias.

(1) See *Power-Up Requirements and PDB Pin*.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage – $V_{(VDD\_n)}$ ($V_{(VDDPLL)}$, $V_{(VDDT)}$, $V_{(VDDCML)}$, $V_{(VDDD)}$)	–0.3	2.5	V
Supply voltage – $V_{(VDDIO)}$	−0.3	4	V
LVCMOS input voltage	−0.3	$V_{(VDDIO)}$ + 0.3	V
FPD-Link III I/O voltage – $V_{(VDD\_n)}$	–0.3	$V_{(VDD\_n)}$ + 0.3	V
Junction temperature		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3B		±8000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	Corner pins (1, 8, 9, 16, 17, 24, 25, 32)	±1000	
			Other pins		
		(IEC 61000-4-2) R_D = 330 Ω, C_s = 150 pF	Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	±25000	
			Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	±7000	
		(ISO10605) R_D = 330 Ω, C_s = 150/330 pF R_D = 2 KΩ, C_s = 150/330 pF	Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	±15000	
			Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{(VDD\_n)}$		1.71	1.8	1.89	V
LVCMOS supply voltage	$V_{(VDDIO)}$= 1.8 V	1.71	1.8	1.89	V
	$V_{(VDDIO)}$= 3.3 V	3	3.3	3.6	
	$V_{(VDDIO)}$= 2.8 V	2.52	2.8	3.08	
Supply noise(1)	$V_{(VDD\_n)}$ = 1.8 V			25	mVp-p
	$V_{(VDDIO)}$ = 1.8 V			25	
	$V_{(VDDIO)}$ = 3.3 V			50	
Power-Over-Coax Supply Noise	f = 30 Hz - 1 KHz, t_{rise} > 100 µs Measured differentially between DOUT+ and DOUT– (coax mode only)			35	mVp-p
	f = 1 KHz - 50 MHz Measured differentially between DOUT+ and DOUT- (coax mode only)			35	mVp-p
Operating free air temperature, T_A		–40	25	105	°C
PCLK clock frequency - 10-bit mode		75		100	MHz
PCLK clock frequency - 12-bit mode		56.25		100	MHz
External clock input frequency to GPO3 - 10-bit mode		37.5		50	MHz

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
External clock input frequency to GPO3 - 12-bit mode	37.5		66.67	MHz

(1) Supply noise testing was done with minimum capacitors (as shown on Figure 8-9, Figure 8-5 on the PCB. A sinusoidal signal is AC coupled to the $V_{(VDD\_n)}$ (1.8 V) supply with amplitude = 25 mVp-p measured at the device $V_{(VDD\_n)}$ pins. Bit error rate testing of input to the serializer and output of the deserializer with 10-meter cable shows no error when the noise frequency on the serializer is less than 1 MHz. The deserializer, on the other hand, shows no error when the noise frequency is less than 750 kHz.

6.4 Thermal Information

THERMAL METRIC(1)		DS90UB633A-Q1 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS 3.3 V I/O (SER INPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High level input voltage	V_{IN} = 3 V to 3.6 V		2		V_{IN}	V
V_{IL}	Low level input voltage	V_{IN} = 3 V to 3.6 V		GND		0.8	V
I_{IN}	Input current	V_{IN} = 0 V or 3.6 V, V_{IN} = 3 V to 3.6 V		–20	±1	20	µA
V_{OH}	High level output voltage	$V_{(VDDIO)}$ = 3 V to 3.6 V, I_{OH} = −4 mA		2.4		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	$V_{(VDDIO)}$ = 3 V to 3.6 V, I_{OL} = 4 mA		GND		0.4	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V	Serializer GPO outputs		–15		mA
I_{OZ}	Tri-state output current	PDB = 0 V, V_{OUT} = 0 V or $V_{(VDDIO)}$	Serializer GPO outputs	–20		20	µA
C_{GPO}	Pin capacitance	GPO [3:0]			1.5		pF
LVCMOS DC SPECIFICATIONS 1.8 V I/O (SER INPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High level input voltage	V_{IN} = 1.71 V to 1.89 V		0.65 V_{IN}		V_{IN}	V
V_{IL}	Low level input voltage	V_{IN} = 1.71 V to 1.89 V		GND		0.35 V_{IN}	
I_{IN}	Input current	V_{IN} = 0 V or 1.89 V, V_{IN} = 1.71 V to 1.89 V		–20	±1	20	µA
V_{OH}	High level output voltage	$V_{(VDDIO)}$ = 1.71 V to 1.89 V, I_{OH} = −4 mA		$V_{(VDDIO)}$ – 0.45		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	$V_{(VDDIO)}$ = 1.71 V to 1.89 V I_{OL} = 4 mA		GND		0.45	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V	Serializer GPO outputs		–11		mA
I_{OZ}	Tri-state output current	PDB = 0 V, V_{OUT} = 0 V or $V_{(VDDIO)}$	Serializer GPO outputs	–20		20	µA
C_{GPO}	Pin capacitance	GPO [3:0]			1.5		pF
I_{IN_STRAP}	Strap pin input current	V_{IN} = 0 V to V_{DD_n}	MODE, IDX	–1		1	µA
LVCMOS DC SPECIFICATIONS 2.8 V I/O (SER INPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	V_{IN} = 2.52 V to 3.08 V		0.7 V_{IN}		V_{IN}	V
V_{IL}	Low level input voltage	V_{IN} = 2.52 V to 3.08 V		GND		0.3 V_{IN}	V
I_{IN}	Input current	V_{IN} = 0 V or 3.08 V, V_{IN} = 2.52 V to 3.08 V		–20	±1	20	µA
V_{OH}	High level output voltage	$V_{(VDDIO)}$ = 2.52 V to 3.08 V, I_{OH} = −4 mA		$V_{(VDDIO)}$ - 0.4		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	$V_{(VDDIO)}$ =2.52 V to 3.08V I_{OL} = 4 mA		GND		0.4	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V	Serializer GPO outputs		–11		mA
I_{OZ}	Tri-state output current	PDB = 0 V, V_{OUT} = 0 V or $V_{(VDDIO)}$	Serializer GPO outputs	–20		20	µA
C_{GPO}	Pin capacitance	GPO [3:0]			1.5		pF
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT–)							
V_{OD}	Differential output voltage	R_L = 100 Ω (Figure 6-6)		640		824	mV
V_{OUT}	Single-ended output voltage	R_L = 50 Ω (Figure 6-6)		320		412	mV
ΔV_{OD}	Differential output voltage unbalance	R_L = 100 Ω			1	50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω (Figure 6-6)			$V_{(VDD\_n)} – (V_{OD}/2)$		V
ΔV_{OS}	Offset voltage unbalance	R_L = 100 Ω			1	50	mV
I_{OS}	Output short-circuit current	DOUT+ = 0 V or DOUT– = 0 V			–26		mA
R_T	Differential internal termination resistance	Differential across DOUT+ and DOUT–		80	100	120	Ω
	Single-ended termination resistance	DOUT+ or DOUT–		40	50	60	Ω
SERIALIZER SUPPLY CURRENT							
I_{DDT}	Serializer (Tx) $V_{(VDD\_n)}$ supply current (includes load current)	R_L = 100 Ω WORST CASE pattern (Figure 6-2)	$V_{(VDD\_n)}$ = 1.89 V $V_{(VDDIO)}$ = 3.6 V f = 100 MHz, 12-bit mode Default registers		76	95	mA
			$V_{(VDD\_n)}$ = 1.89 V $V_{(VDDIO)}$ = 3.6 V f = 75 MHz, 12-bit mode Default registers		61	80	mA
I_{DDT}	Serializer (Tx) $V_{(VDD\_n)}$ supply current (includes load current)	R_L = 100 Ω RANDOM PRBS-7 pattern	$V_{(VDD\_n)}$ = 1.89 V $V_{(VDDIO)}$ = 3.6 V f = 100 MHz, 12-bit mode Default Registers		80		mA
			$V_{(VDD\_n)}$ = 1.89 V $V_{(VDDIO)}$ = 3.6 V f = 75 MHz, 12-bit mode Default Registers		64		mA
$I_{(VDDIO)T}$	Serializer (Tx) $V_{(VDDIO)}$ supply current (includes load current)	R_L = 100 Ω WORST CASE pattern (Figure 6-2)	$V_{(VDDIO)}$ = 1.89 V f = 75 MHz, 12-bit mode Default Registers		1.5	3	mA
			$V_{(VDDIO)}$ = 3.6 V f = 75 MHz, 12-bit mode Default registers		5	8	mA

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDTZ}	Serializer (Tx) supply current power down	PDB = 0 V; All other LVCMOS inputs = 0 V	$V_{(VDDIO)}$=1.89 V Default registers		300	1000	µA
			$V_{(VDDIO)}$ = 3.6 V Default registers		300	1000	µA
$I_{(VDDIO)TZ}$	Serializer (Tx) $V_{(VDDIO)}$ supply current power down	PDB = 0 V; All other LVCMOS inputs = 0 V	$V_{(VDDIO)}$ = 1.89 V Default registers		15	100	µA
			$V_{(VDDIO)}$ = 3.6 V Default registers		15	100	µA

(1) The Electrical Characteristics tables list verified specifications under the listed *Section 6.3* except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.

(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD} which are differential voltages.

(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at the *Section 6.3* at the time of product characterization and are not verified.

6.6 Recommended Serializer Timing For PCLK

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2)

PARAMETER		TEST CONDITIONS	PIN / FREQ	MIN	NOM	MAX	UNIT
t_{TCP}	Transmit clock period	10-bit mode 75 MHz – 100 MHz		10	T	13.33	ns
		12-bit mode 56.25 MHz - 100 MHz		10	T	17.78	ns
t_{TCIH}	Transmit clock input high time			0.4T	0.5T	0.6T	
t_{TCIL}	Transmit clock input low time			0.4T	0.5T	0.6T	
t_{CLKT}	PCLK input transition time (Figure 6-7)	10-bit mode 75 MHz – 100 MHz		0.05T	0.25T	0.3T	
		12-bit mode 56.25 MHz – 100 MHz		0.05T	0.25T	0.3T	
t_{JIT0}	PCLK input jitter (3) (PCLK from imager mode)	LPF = f/20, CDR PLL Loop BW = f/15, BER = 1E-10	f_{PCLK} = 56.25 – 100 MHz(5)			0.45	UI
t_{JIT1}	PCLK input jitter(3) (External oscillator mode)	LPF = f/20, CDR PLL Loop BW = f/15, BER = 1E-10	f_{PCLK} = 56.25 – 100 MHz(5)		1T		
t_{JIT2}	External oscillator jitter(3) (4)	LPF = f/20, CDR PLL Loop BW = f/15, BER = 1E-10, paired with DS90UB662-Q1 deserializer	f_{OSC} = 37.5 – 66.67 MHz(6)			0.45	UI
Δ_{OSC}	External Oscillator Frequency Stability		f_{OSC} = 37.5 – 66.67 MHz(6)		±50		ppm
t_{DC}	CLKOUT duty cycle (external oscillator mode)		f_{OSC} = 37.5 – 66.67 MHz(6)	45%	50%	55%	

(1) Recommended input timing requirements are input specifications and not tested in production.
(2) T is the period of the PCLK.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at *Section 6.3* at the time of product characterization and are not verified.
(4) 0.45UI maximum when used with DS90UB662-Q1 deserializer.
(5) f_{PCLK} denotes input PCLK frequency to the device.
(6) f_{OSC} denotes input external oscillator frequency to the device (GPO3/CLKIN).

6.7 AC Timing Specifications (SCL, SDA) - I2C-Compatible

Over recommended supply and temperature ranges unless otherwise specified. (Figure 6-1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
f_{SCL}	SCL Clock Frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{LOW}	SCL Low Period	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HIGH}	SCL high period	Standard mode	4.0			µs
		Fast mode	0.6			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard mode	4.0			µs
		Fast mode	0.6			µs
$t_{SU:STA}$	Setup time for a start or a repeated start condition	Standard mode	4.7			µs
		Fast mode	0.6			µs
$t_{HD:DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		900	ns
$t_{SU:DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
$t_{SU:STO}$	Setup time for stop condition	Standard mode	4.0			µs
		Fast mode	0.6			µs
t_{BUF}	Bus free time between stop and start	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_r	SCL and SDA rise time	Standard mode			1000	ns
		Fast mode			300	ns
t_f	SCL and SDA fall time	Standard mode			300	ns
		Fast mode			300	ns

6.8 Bidirectional Control Bus DC Timing Specifications (SCL, SDA) - I2C-Compatible

Over recommended supply and temperature ranges unless otherwise specified(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
V_{IH}	Input high level	SDA and SCL	0.7 × $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
V_{IL}	Input low level	SDA and SCL	GND		0.3 × $V_{(VDDIO)}$	V
V_{HY}	Input hysteresis			> 50		mV
V_{OL}	Output low level(2)	SDA, $V_{(VDDIO)}$ = 1.8 V, I_{OL}= 0.9 mA	0		0.36	V
		SDA, $V_{(VDDIO)}$ = 3.3 V, I_{OL}= 1.6 mA	0		0.4	
I_{IN}	Input current	SDA or SCL, V_{IN}= $V_{(VDDIO)}$ OR GND	−10		10	µA
t_R	SDA rise time-READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF (Figure 6-1)		430		ns
t_F	SDA fall time-READ			20		ns
C_{IN}		SDA or SCL		<5		pF

(1) Specification is verified by design.

(2) FPD-Link device was designed primarily for point-to-point operation and a small number of attached slave devices. As such the minimum I_{OL} pullup current is targeted to lower value than the minimum I_{OL} in the I2C specification.

6.9 Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{LHT}	CML low-to-high transition time	RL = 100 Ω Figure 6-1			150	330	ps
t_{HLT}	CML high-to-low transition time	RL = 100 Ω Figure 6-1			150	330	ps
t_{DIS}	Data input Setup to PCLK	Serializer data inputs Figure 6-8		2			ns
t_{DIH}	Data input Hold from PCLK			2			ns
t_{PLD}	Serializer PLL lock time.(1) (2)	RL = 100 Ω Figure 6-9			1	2	
t_{SD}	Serializer delay(2)	RT = 100 Ω, 10–bit mode Register 0x03h b[0] (TRFB = 1) Figure 6-10		32.5T	38T	44T	
		RT = 100 Ω, 12–bit mode Register 0x03h b[0] (TRFB = 1) Figure 6-10		11.75T	13T	15T	
t_{JIND}	Serializer output deterministic jitter(3) (4) (5)	PRBS-7 test pattern, CDR PLL Loop BW = f/15, BER = 1E-10	DOUT±		0.17		UI
t_{JINR}	Serializer output random jitter(3) (4) (5)	PRBS-7 test pattern, CDR PLL Loop BW = f/15, BER = 1E-10	DOUT±		0.016		UI
t_{JINT}	Peak-to-peak serializer output total jitter(3) (5) (6)	PRBS-7 test pattern, CDR PLL Loop BW = f/15, BER = 1E-10	DOUT±		0.4		UI
λ_{STXBW}	Serializer jitter transfer function –3 dB bandwidth	10–bit mode PCLK = 100 MHz, Default registers			2.2		MHz
		12–bit mode PCLK = 100 MHz, Default registers			2.2		
δ_{STX}	Serializer jitter Transfer Function (peaking)	10–bit mode PCLK = 100 MHz, Default registers			1.06		dB
		12–bit mode PCLK = 100 MHz, Default registers			1.09		
δ_{STXf}	Serializer jitter transfer function (peaking frequency)	10–bit mode PCLK = 100 MHz, Default registers			400		kHz
		12–bit mode PCLK = 100 MHz, Default registers			500		

(1) t_{PLD} is the time required by the serializer to obtain lock when exiting power-down state with an active PCLK.
(2) Specification is verified by design.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at *Section 6.3* at the time of product characterization and are not verified.
(4) Specification is verified by characterization and is not tested in production.
(5) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.
10-bit mode: 1 UI = 1 / (PCLK_Freq. /2 × 28)
12-bit mode: 1 UI = 1 / (PCLK_Freq. × 2/3 × 28)
(6) Serializer output peak-to-peak total jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input.

6.10 Timing Diagrams

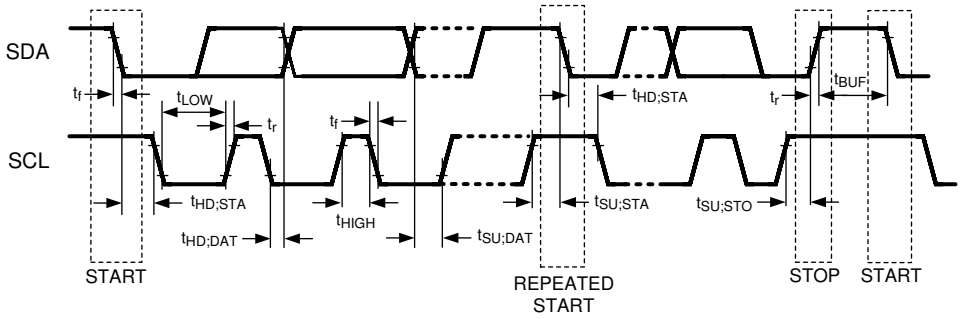


Figure 6-1. Bidirectional Control Bus Timing

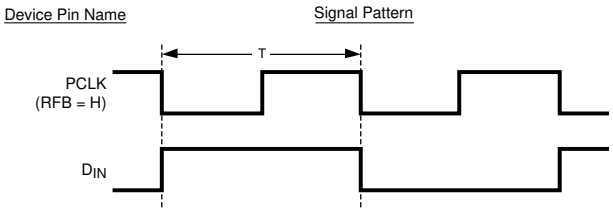


Figure 6-2. "Worst Case" Test Pattern for Power Consumption

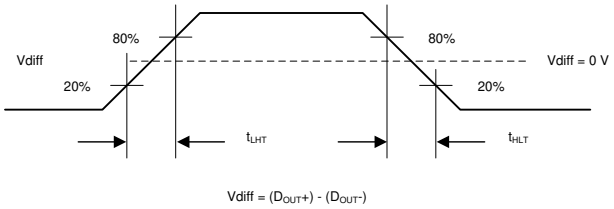


Figure 6-3. Serializer CML Output Load and Transition Times

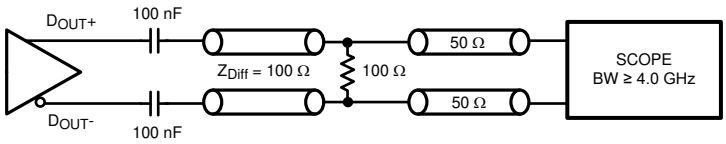


Figure 6-4. Measurement Setup Serializer CML Output Load and Transition Times

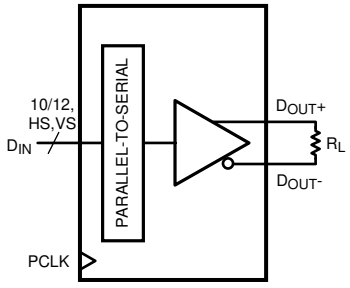


Figure 6-5. Serializer VOD Setup

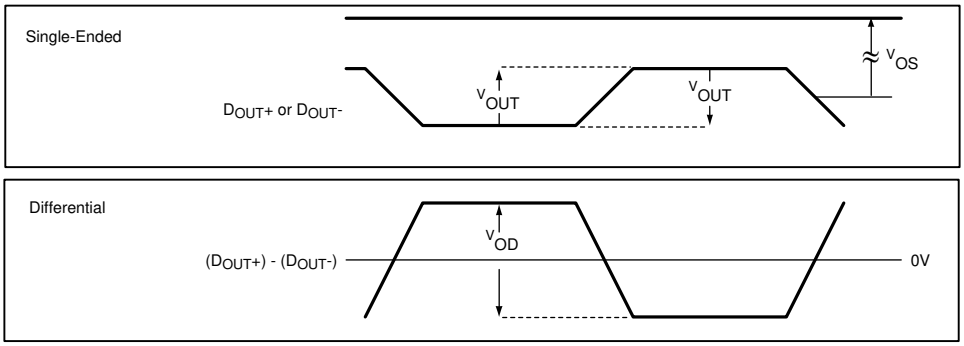


Figure 6-6. Serializer VOD Diagram

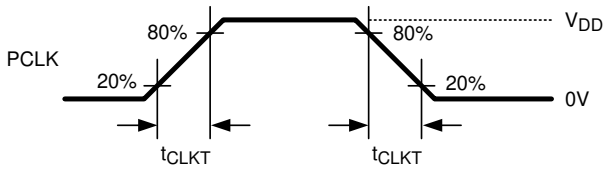


Figure 6-7. Serializer Input Clock Transition Times

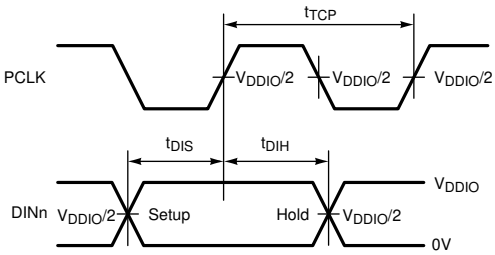


Figure 6-8. Serializer Setup/Hold Times

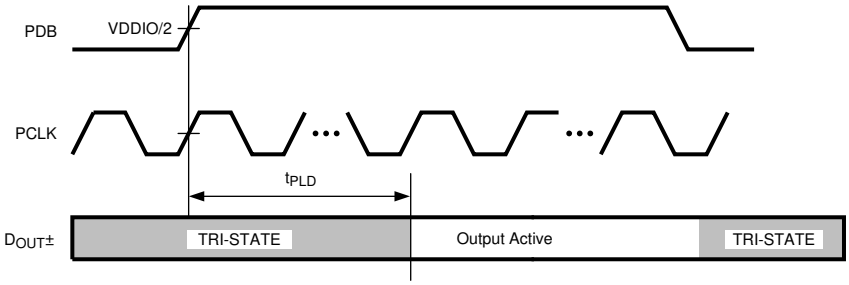


Figure 6-9. Serializer PLL Lock Time

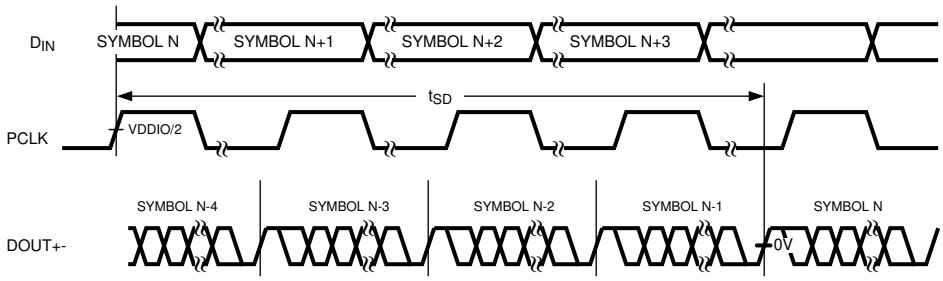


Figure 6-10. Serializer Delay

6.11 Typical Characteristics

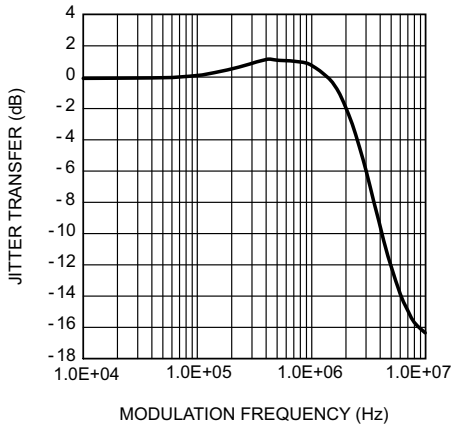


Figure 6-11. Typical Serializer Jitter Transfer Function

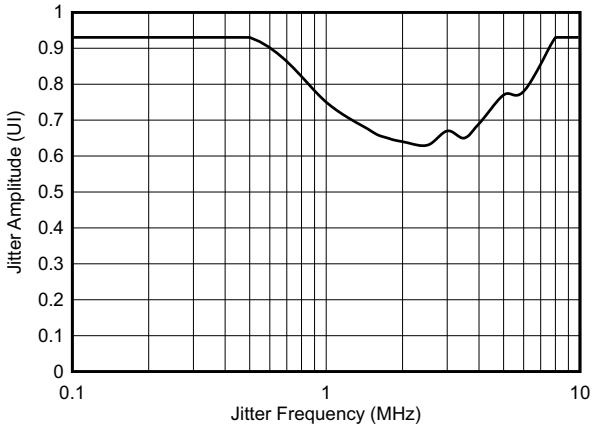


Figure 6-12. Typical System Input Jitter Tolerance Curve - DS90UB633A Linked to DS90UB662

7 Detailed Description

7.1 Overview

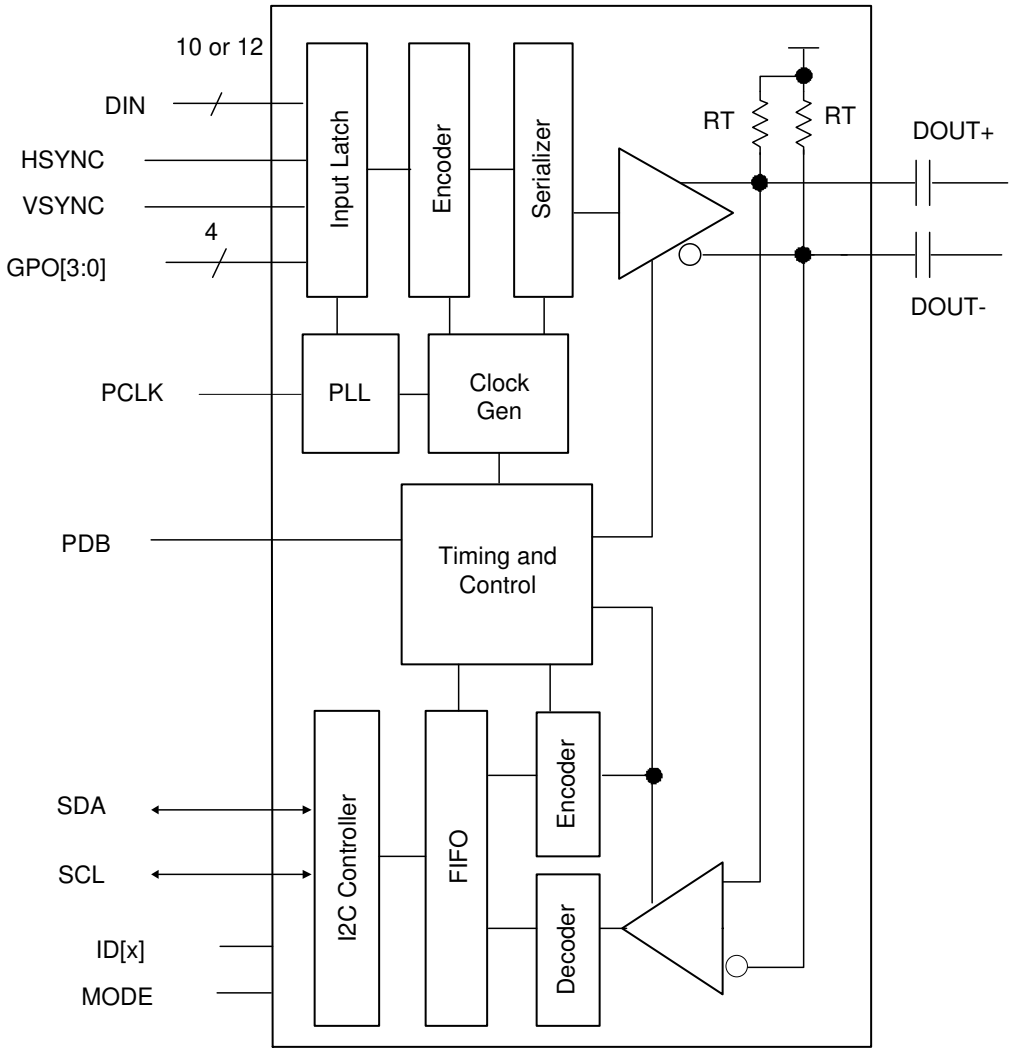
The DS90UB633A-Q1 is optimized to interface with the DS90UB662-Q1 using a 50-Ω coax interface. The DS90UB633A-Q1 also works with the DS90UB662-Q1 using an STP interface.

The DS90UB633A/662 FPD-Link III chipsets are intended to link mega-pixel camera imagers and video processors in ECUs. The Serializer/Deserializer chipset can operate from 56.25 MHz to 100 MHz pixel clock frequency. The DS90UB633A-Q1 device transforms a 10/12-bit wide parallel LVCMOS data bus along with a bidirectional control channel control bus into a single high-speed differential pair. The high-speed serial bit stream contains an embedded clock and DC-balanced information which enhances signal quality to support AC coupling. The DS90UB662-Q1 device receives the single serial data stream and converts it back into a 10/12-bit wide parallel data bus together with the control channel data bus. The DS90UB633A/662 chipsets can accept up to:

- 12-bits of DATA + 2 SYNC bits for an input PCLK range of 56.25 MHz to 100 MHz in the 12-bit mode. Note: No HS/VS restrictions (raw).
- 10/8-bits of DATA + 2 SYNC bits for an input PCLK range of 75 MHz to 100 MHz in the 10/8-bit mode. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles.

The DS90UB633A/662 chipset offer customers the choice to work with different clocking schemes. The DS90UB633A/662 chipsets can use an external oscillator as the reference clock source for the PLL (see *Section 7.4.1*) or PCLK from the imager as primary reference clock to the PLL (see *Section 7.4.2*).

7.2 Functional Block Diagram



DS90UB633A-Q1 - SERIALIZER

7.3 Feature Description

7.3.1 Serial Frame Format

The high-speed forward channel is composed of 28 bits of data containing video data, sync signals, I2C, and parity bits. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. The 28-bit frame structure changes in the 12-bit mode and 10-bit mode internally and is seamless to the customer. The bidirectional control channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full-duplex low-speed forward and backward path across the serial link together with a high-speed forward channel without the dependence on the video blanking phase.

7.3.2 Line Rate Calculations for the DS90UB633A/662

The DS90UB633A-Q1 device divides the clock internally by divide-by-2 in the 10-bit mode and by divide-by-1.5 in the 12-bit mode. Conversely, the DS90UB662-Q1 multiplies the recovered serial clock to generate the proper pixel clock output frequency. The following are the formulae used to calculate the maximum line rate in the different modes:

- For the 12-bit mode, Line rate = f_{PCLK} × (2/3) × 28; for example, f_{PCLK} = 100 MHz, line rate = (100 MHz) × (2/3) × 28 = 1.87 Gbps
- For the 10-bit mode, Line rate = f_{PCLK}/2 × 28; for example, f_{PCLK} = 100 MHz, line rate = (100 MHz/2) × 28 = 1.40 Gbps

7.3.3 Error Detection

The chipset provides error detection operations for validating data integrity in long distance transmission and reception. The data error detection function offers users flexibility and usability of performing bit-by-bit data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bidirectional control channel data across the serial link
- Parallel video/sync data across the serial link

The chipset provides 1 parity bit on the forward channel and 4 cyclic redundancy check (CRC) bits on the back channel for error detection purposes. The DS90UB633A/662 chipset checks the forward and back channel serial links for errors and stores the number of detected errors in two 8-bit registers in the serializer and the deserializer, respectively.

To check parity errors on the forward channel, monitor registers 0x55 and 0x56 on the DS90UB662. The parity error counter registers return the number of data parity errors that have been detected on the FPD3 receiver data since the last detection of valid lock or last read of these registers (0x55 and 0x56). These registers are cleared on read.

To check CRC errors on the back channel, monitor registers 0x0A and 0x0B on the serializer.

7.3.4 Synchronizing Multiple Cameras

For applications requiring multiple cameras for frame-synchronization, TI recommends using the general purpose input/output (GPIO) pins to transmit control signals to synchronize multiple cameras together. To synchronize the cameras properly, the system controller must provide a field sync output (such as a vertical or frame sync signal), and the cameras must be set to accept an auxiliary sync input. The vertical synchronize signal corresponds to the start and end of a frame and the start and end of a field. Note this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the bidirectional control channel, there is a time variation of the GPIO signals arriving at the different target devices (between the parallel links). The maximum latency (t1) of the GPIO data transmitted across the link is 32 µs.

Note

The user must verify that the timing variations between the different links are within their system and timing specifications.

See Figure 7-1 for an example of this function.

The maximum time (t2) between the time the GPIO signal arrives at Camera A and Camera B is 23 µs.

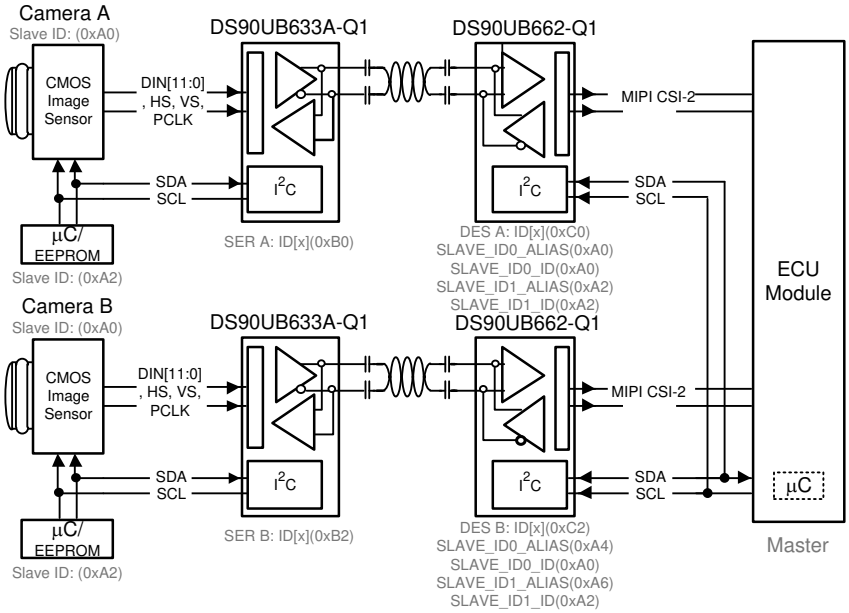


Figure 7-1. Synchronizing Multiple Cameras

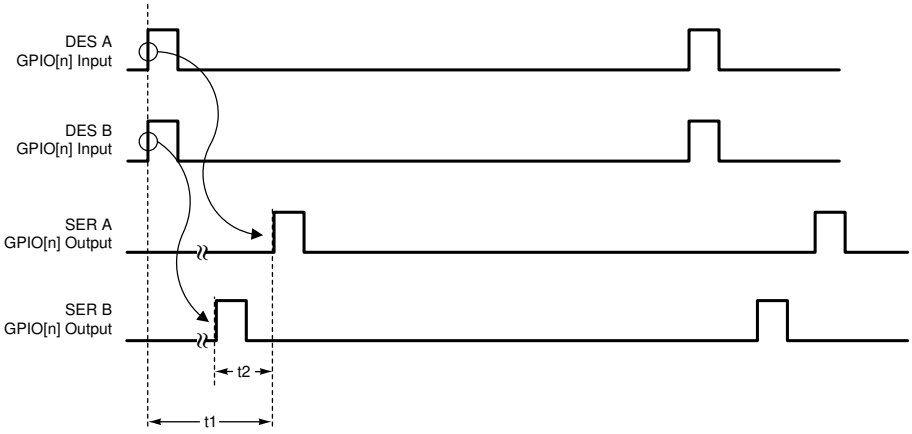


Figure 7-2. GPIO Delta Latency

7.3.5 General Purpose I/O (GPIO) Descriptions

There are 4 GPOs on the serializer and 4 GPIOs on the deserializer when the DS90UB633A/662 chipsets are run off the pixel clock from the imager as the reference clock source. The GPOs on the serializer can be configured as outputs for the input signals that are fed into the deserializer GPIOs. In addition, the GPOs on the serializer can behave as outputs of the local register on the serializer. The GPIOs on the deserializer can be configured to be the input signals feeding the GPOs (configured as outputs) on the serializer. In addition the GPIOs on the deserializer can be configured to behave as outputs of the local register on the deserializer. The DS90UB633A-Q1 serializer GPOs cannot be configured as inputs for remote communication with deserializer. If the DS90UB633A/662 chipsets are run off the external oscillator source as the reference clock, then GPO3 on the serializer is automatically configured to be the input for the external clock and GPO2 is configured to be the output of the divide-by-2 clock which is fed into the imager as its reference clock. In this case, the GPIO2 and GPIO3 on the deserializer can only behave as outputs of the local register on the deserializer. The GPIO maximum switching rate is up to 66 kHz when configured for communication between deserializer GPIO to serializer GPO.

7.3.6 LVCMOS $V_{(VDDIO)}$ Option

1.8 V/2.8 V/3.3 V Serializer inputs are user configurable to provide compatibility with 1.8 V, 2.8 V, and 3.3 V system interfaces.

7.3.7 Pixel Clock Edge Select (TRFB / RRFB)

The TRFB/RRFB selects which edge of the pixel clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the rising edge of the PCLK. If TRFB register is 0, data is latched on the falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the rising edge of the PCLK. If RRFB register is 0, data is strobed on the falling edge of the PCLK.

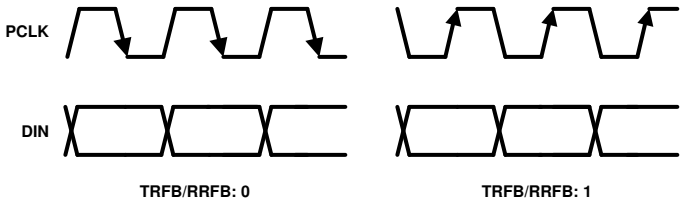


Figure 7-3. Programmable PCLK Strobe Select

7.3.8 Power Down

The SER has a PDB input pin to ENABLE or power down the device. Enabling PDB on the SER disables the link to save power. If PDB = HIGH, the SER operates at its internal default oscillator frequency when the input PCLK stops. When the PCLK starts again, the SER locks to the valid input PCLK and transmit the data to the DES. When PDB = LOW, the high-speed driver outputs are static HIGH. See *Power-Up Requirements and PDB Pin* for power-up requirements.

7.4 Device Functional Modes

7.4.1 DS90UB633A/662 Operation With External Oscillator as Reference Clock

In some applications, the pixel clock that comes from the imager can have jitter which exceeds the tolerance of the DS90UB633A/662 chipsets. In this case, operate the DS90UB633A-Q1 device by using an external clock source as the reference clock for the DS90UB633A/662 chipsets. *This is the recommended operating mode.* The external oscillator clock output goes through a divide-by-2 circuit in the DS90UB633A-Q1 serializer, and this divided clock output is used as the reference clock for the imager. The output data and pixel clock from the imager are then fed into the DS90UB633A-Q1 device. Figure 7-4 shows the operation of the DS90UB633A/662 chipsets while using an external automotive grade oscillator.

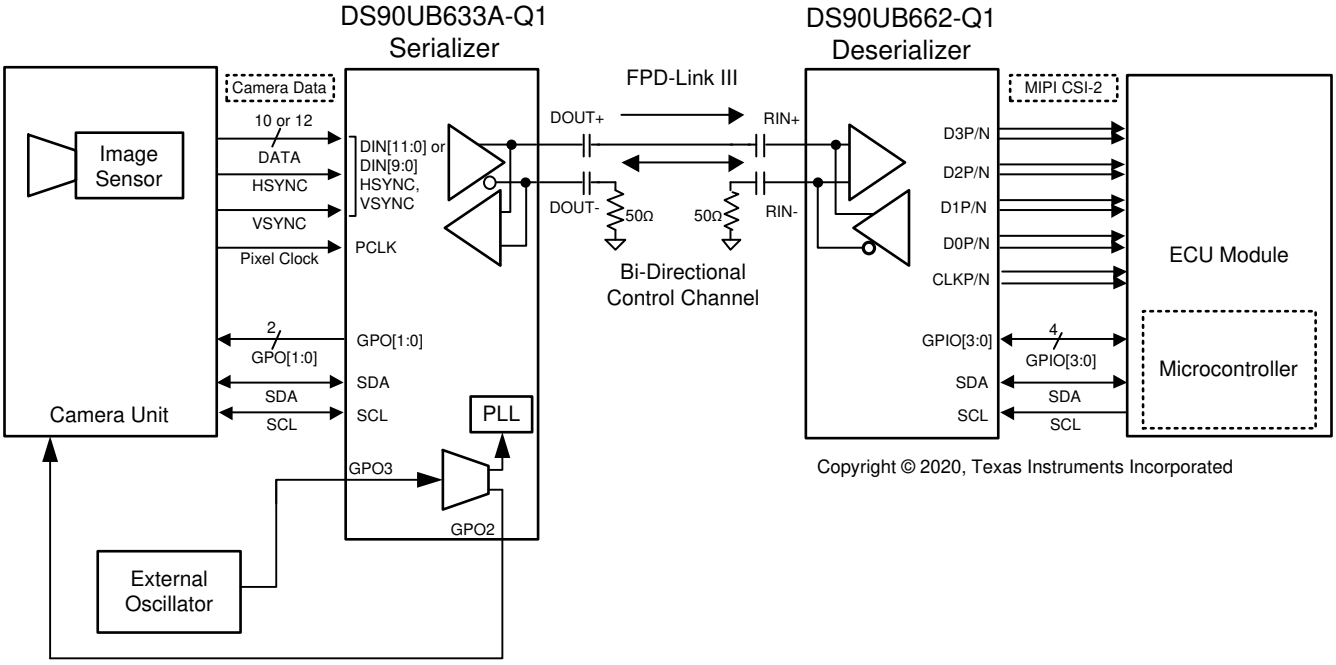


Figure 7-4. DS90UB633A-Q1/662-Q1 Operation in the External Oscillator Mode

When the DS90UB633A-Q1 device is operated using an external oscillator, the GPO3 pin on the DS90UB633A-Q1 is the input pin for the external oscillator. In applications where the DS90UB633A-Q1 device is operated from an external oscillator, the divide-by-2 circuit in the DS90UB633A-Q1 device feeds back the divided clock output to the imager device through GPO2 pin. The pixel clock to external oscillator ratios must be fixed for the 12–bit mode and the 10–bit mode. *In the 10-bit mode, the pixel clock frequency divided by the external oscillator frequency must be 2. In the 12-bit mode, the pixel clock frequency divided by the external oscillator frequency must be 1.5.* For example, if the external oscillator frequency is 48 MHz in the 10-bit mode, the pixel clock frequency of the imager must be twice of the external oscillator frequency, that is, 96 MHz. If the external oscillator frequency is 48 MHz in the 12-bit mode, the pixel clock frequency of the imager must be 1.5 times of the external oscillator frequency, that is, 72 MHz. For the range of PCLK frequency and the external clock input frequency to GPO3 in 10-bit and 12-bit modes, see *Section 6.3*.

When PCLK signal edge is detected, and 0x03[1] = 0, the DS90UB633A-Q1 switches from internal oscillator mode to an external PCLK. Upon removal of PCLK input, the device switches back into internal oscillator mode. In external oscillator mode, GPO2 and GPO3 on the serializer cannot act as the output of the input signal coming from GPIO2 or GPIO3 on the deserializer.

Table 7-1. Device Functional Mode With Example XCLKIN = 48 MHz

MODE	GPIO3 XCLKIN	GPIO2 XCLKOUT = XCLKIN / 2	RATIO	INPUT PCLK FREQUENCY = XLCKIN * RATIO
10-bit	48 MHz	24 MHz	2	96 MHz

Table 7-1. Device Functional Mode With Example XCLKIN = 48 MHz (continued)

MODE	GPIO3 XCLKIN	GPIO2 XCLKOUT = XCLKIN / 2	RATIO	INPUT PCLK FREQUENCY = XLCKIN * RATIO
12-bit	48 MHz	24 MHz	1.5	72 MHz

7.4.2 DS90UB633A/662 Operation With Pixel Clock From Imager as Reference Clock

The DS90UB633A/662 chipsets can be operated by using the pixel clock from the imager as the reference clock. Figure 7-5 shows the operation of the DS90UB633A/662 chipsets using the pixel clock from the imager. If the DS90UB633A-Q1 device is operated using the pixel clock from the imager as the reference clock, then the imager uses an external oscillator as its reference clock. There are 4 GPIOs available in this mode (PCLK from imager mode).

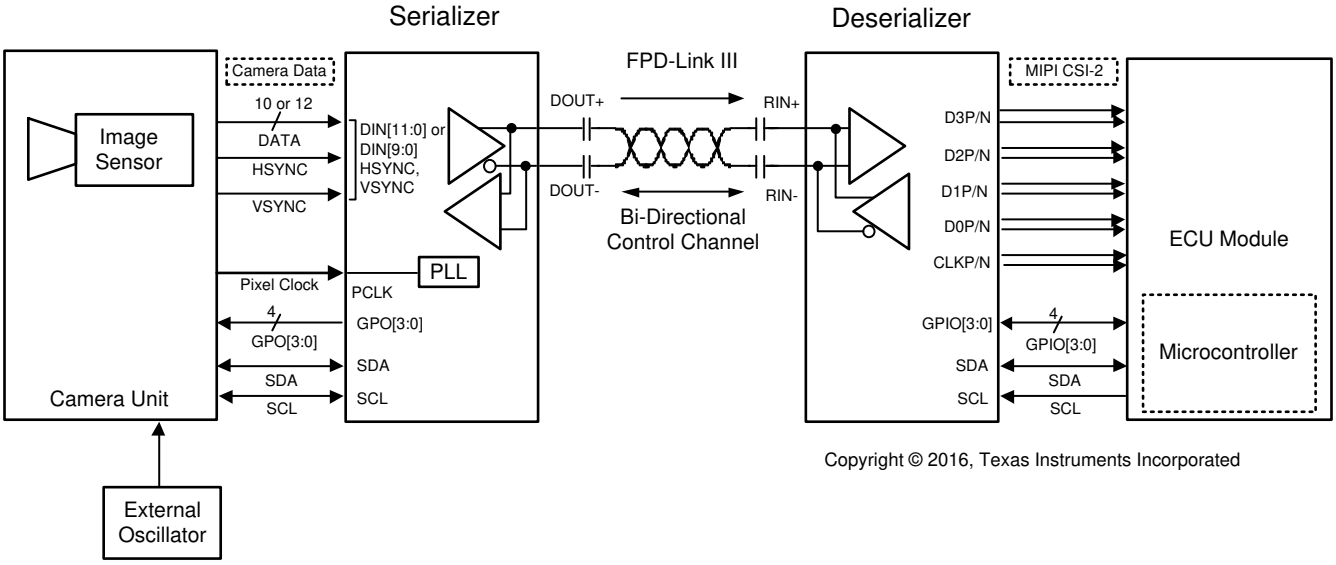


Figure 7-5. DS90UB633A-Q1/662-Q1 Operation in PCLK mode

7.4.3 MODE Pin on Serializer

The MODE pin on the serializer can be configured to select if the DS90UB633A-Q1 device is to be operated from the external oscillator or the PCLK from the imager. The pin must be pulled to V_{DD_n}(1.8 V, not V_{DDIO}) with a resistor R_1 and a pulldown resistor R_2 for external oscillator mode to create the ratio shown in Figure 7-6. If the device is to be operated from PCLK from imager mode, MODE pin can be pulled up to V_{DD_n} (1.8V) with a 10-kΩ resistor directly or use the ratio shown in Figure 7-6 and Table 7-2. Suggested resistor values are given in Table 7-2. The recommended maximum resistor tolerance is 1%. Other resistor values can be used as long as the ratio is met under all conditions.

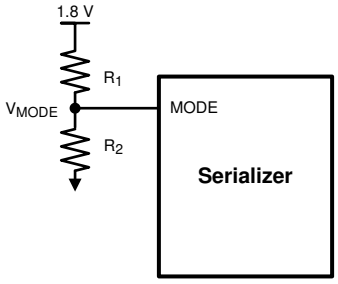


Figure 7-6. MODE Pin Configuration on DS90UB633A-Q1

Table 7-2. DS90UB633A-Q1 Serializer MODE Setting

DS90UB633A-Q1 SERIALIZER MODE SETTING				
MODE SELECT	MINIMUM RATIO ($V_{MODE}/V_{(VDD\_n)}$)	MAXIMUM RATIO ($V_{MODE}/V_{(VDD\_n)}$)	SUGGESTED R_1 RESISTOR VALUE (kΩ)	SUGGESTED R_2 RESISTOR VALUE (kΩ)
PCLK from imager mode	0.750	1.000	10	50
External oscillator mode	0.292	0.339	10	4.7

7.4.4 Internal Oscillator

When a PCLK is not applied to the DS90UB633A-Q1, the serializer establishes the FPD-III link using an internal oscillator. During normal operation (not BIST) the frequency of the internal oscillator can be adjusted from DS90UB633A-Q1 register 0x14[2:1] according to Table 7-3. In BIST mode, the internal oscillator frequency should only be adjusted from the DS90UB662-Q1. The BIST frequency can be set by either pin strapping (Table 7-4) or register (Table 7-5). In BIST DS90UB633A-Q1 register 0x14[2:1] is automatically loaded from the DS90UB662-Q1 through the bi-directional control channel.

Table 7-3. Clock Sources for Forward Channel Frame on the Serializer During Normal Operation

DS90UB633A-Q1 Reg 0x14 [2:1]	10-BIT MODE	12-BIT MODE
00	Reserved	Reserved
01	100 MHz	75 MHz
10	Reserved	Reserved
11	Reserved	Reserved

7.4.5 Built-In Self Test

An optional at-speed built-in self test (BIST) feature supports the testing of the high-speed serial link and low-speed back channel. This is useful in the prototype stage, equipment production, and in-system test and also for system diagnostics.

7.4.6 BIST Configuration and Status

The chipset can be programmed into BIST mode using either pins or registers on the DES only. By default, BIST configuration is controlled through pins. BIST can be configured via registers using BIST Control register (0xB3). Pin-based configuration is defined as follows:

- BISTEN = HIGH: Enable the BIST mode, BISTEN = LOW: Disable the BIST mode.
- Deserializer GPIO0 and GPIO1: Defines the BIST clock source (PCLK vs various frequencies of internal OSC)

Table 7-4. BIST Pin Configuration

DESERIALIZER GPIO[0:1]	OSCILLATOR SOURCE	BIST FREQUENCY
00	External PCLK	PCLK or external oscillator
01	Reserved	Reserved
10	Reserved	Reserved

Table 7-5. BIST Register Configuration

DS90UB662-Q1 Reg 0xB3 [2:1]	10-BIT MODE	12-BIT MODE
00	PCLK	PCLK
01	100 MHz	75 MHz
10	Reserved	Reserved
11	Reserved	Reserved

BIST mode provides various options for the PCLK source. Either external pins (GPIO0 and GPIO1) or registers can be used to program the BIST to use external PCLK or various OSC frequencies. Refer to Table 7-4 for pin settings. The BIST status can be monitored real-time on the PASS pin. For every frame with error(s), the PASS pin toggles low for one-half PCLK period. If two consecutive frames have errors, PASS toggles twice to allow counting of frames with errors. Once the BIST is done, the PASS pin reflects the pass/fail status of the last BIST run only for one PCLK cycle. The status can also be read through I2C for the number of frames in errors. BIST status register retains results until it is reset by a new BIST session or a device reset. To evaluate BIST in external oscillator mode, both the external oscillator and PCLK must be present. For all practical purposes, the BIST status can be monitored from the BIST Error Count register 0x57 on the DS90UB662 deserializer.

7.4.7 Sample BIST Sequence

- **Step 1:** For the DS90UB633A/662 FPD-Link III chipset, BIST mode is enabled via the BISTEN pin of DS90UB662-Q1 FPD-Link III deserializer. The desired clock source is selected through the deserializer GPIO0 and GPIO1 pins as shown in Table 7-4.
- **Step 2:** DS90UB633A-Q1 serializer BIST pattern is enabled through the back channel. The BIST pattern is sent through the FPD-Link III to the deserializer. Once the serializer and deserializer are in the BIST mode and the deserializer acquires lock, the PASS pin of the deserializer goes high, and BIST starts checking the FPD-Link III serial stream. If an error in the payload is detected, the PASS pin switches low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.
- **Step 3:** To stop the BIST mode, the deserializer BISTEN pin is set LOW. The deserializer stops checking the data. The final test result is not maintained on the PASS pin. To monitor the BIST status, check the BIST Error Count register, 0x57 on the deserializer.
- **Step 4:** The link returns to normal operation after the deserializer BISTEN pin is low. Figure 7-8 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission, etc.); thus, they may be introduced by greatly extending the cable length, faulting the interconnect, or by reducing signal condition enhancements (Rx equalization).

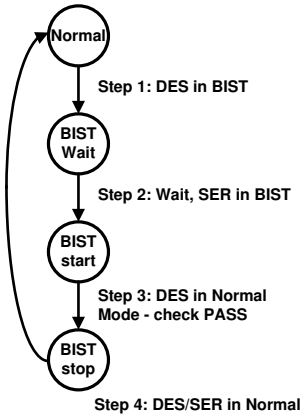


Figure 7-7. At-Speed BIST System Flow Diagram

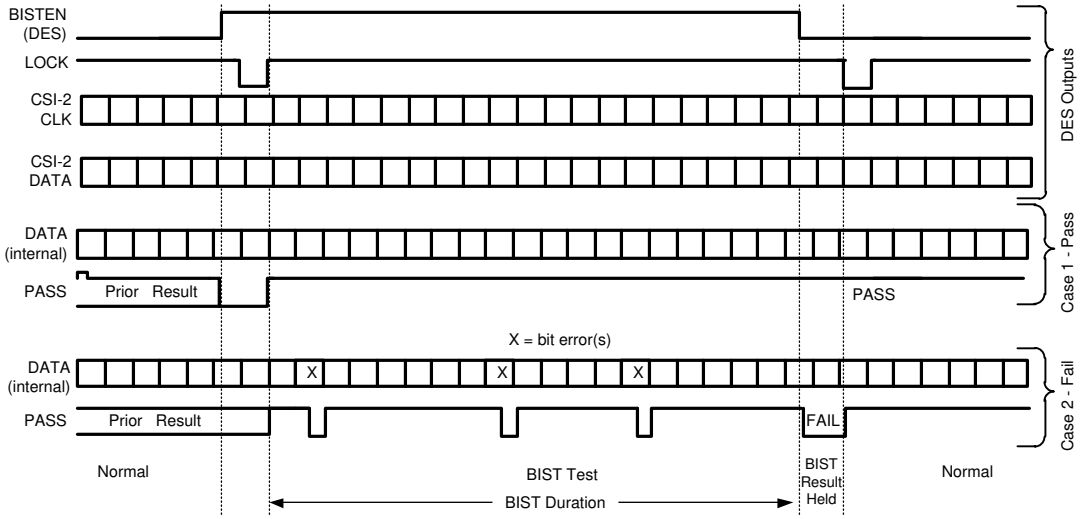


Figure 7-8. BIST Timing Diagram

7.5 Programming

7.5.1 Programmable Controller

An integrated I2C slave controller is embedded in the DS90UB633A-Q1 serializer. It must be used to configure the extra features embedded within the programmable registers or it can be used to control the set of programmable GPIOs.

7.5.2 Description of Bidirectional Control Bus and I2C Modes

The I2C-compatible interface allows programming of the DS90UB633A-Q1, DS90UB662-Q1, or an external remote device (such as image sensor) through the bidirectional control channel. Register programming transactions to/from the DS90UB633A/662 chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os, and both lines must be pulled up to $V_{(VDDIO)}$ by an external resistor. Pullup resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic LOW is transmitted by driving the output low. Logic HIGH is transmitted by releasing the output and allowing it to be pulled up externally. The appropriate pullup resistor values depend upon the total bus capacitance and operating speed. The DS90UB633A-Q1 I2C bus data rate supports up to 400 kbps according to I2C fast mode specifications.

For further description of general I2C communication, refer to the *Understanding the I2C Bus* application note . For more information on choosing appropriate pullup resistor values, see the *I2C Bus Pullup Resistor Calculation* application note .

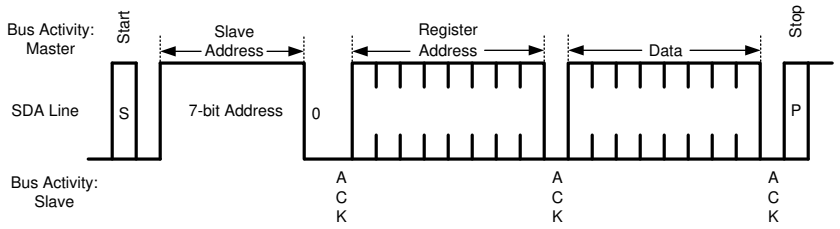


Figure 7-9. Write Byte

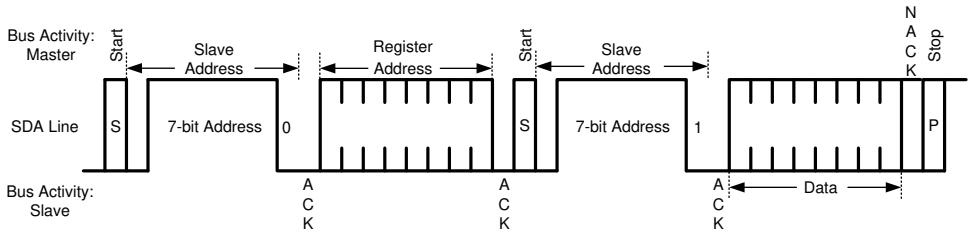


Figure 7-10. Read Byte

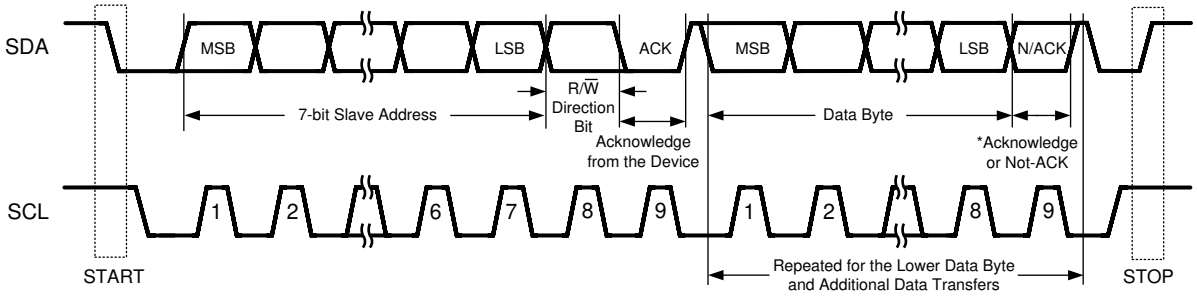


Figure 7-11. Basic Operation

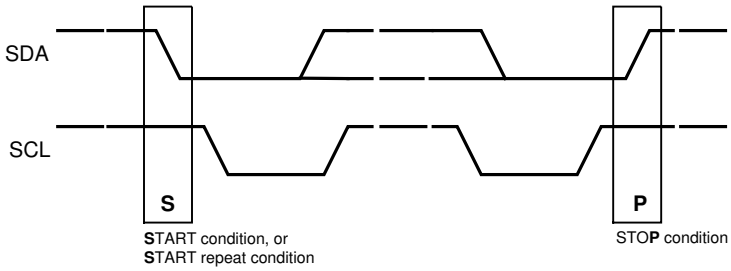


Figure 7-12. Start and Stop Conditions

7.5.3 I2C Pass-Through

I2C pass-through provides a way to access remote devices at the other end of the FPD-Link III interface. This option is used to determine if an I2C instruction is transferred over to the remote I2C bus. For example, when the I2C master is connected to the deserializer and I2C pass-through is enabled on the deserializer, any I2C traffic targeted for the remote serializer or remote slave is allowed to pass through the deserializer to reach those respective devices.

If the master controller transmits an I2C transaction for address 0xA0, the DES A with I2C pass-through enabled transfers I2C commands to remote Camera A. The DES B (with I2C pass-through disabled) will NOT pass I2C commands on the I2C bus to Camera B.

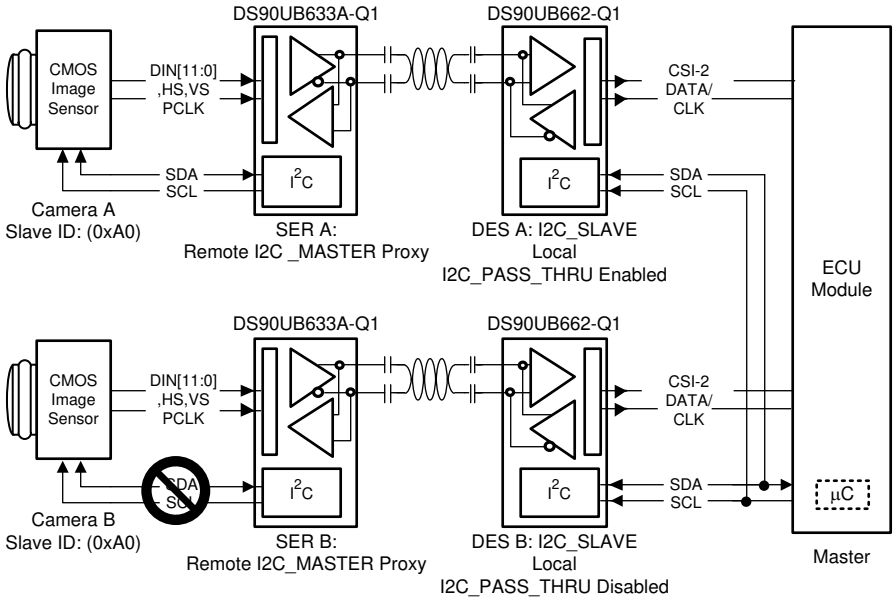


Figure 7-13. I2C Pass-Through

7.5.4 Slave Clock Stretching

The I2C-compatible interface allows programming of the DS90UB633A-Q1, DS90UB662-Q1, or an external remote device (such as image sensor) through the bidirectional control. To communicate and synchronize with remote devices on the I2C bus through the bidirectional control channel/MCU, *the chipset utilizes bus clock stretching (holding the SCL line low) during data transmission*; where the I2C slave pulls the SCL line low on the 9th clock of every I2C transfer (before the ACK signal). The slave device does not control the clock and only stretches it until the remote peripheral has responded. The I2C master must support clock stretching to operate with the DS90UB633A/662 chipset.

7.5.5 IDX Address Decoder on the Serializer

The IDX pin on the serializer is used to decode and set the physical slave address of the serializer (I2C only) to allow up to five devices on the bus connected to the serializer using only a single pin. The pin sets one of the 4

possible addresses for each serializer device. The pin must be pulled to $V_{(VDD\_n)}$ (1.8 V, not $V_{(VDDIO)}$) with a resistor, R_3, and a pulldown resistor R_4. Suggested resistor values are given in Table 7-6. The recommended maximum resistor tolerance is 1%. Other resistor values can be used as long as the ratio is met under all conditions.

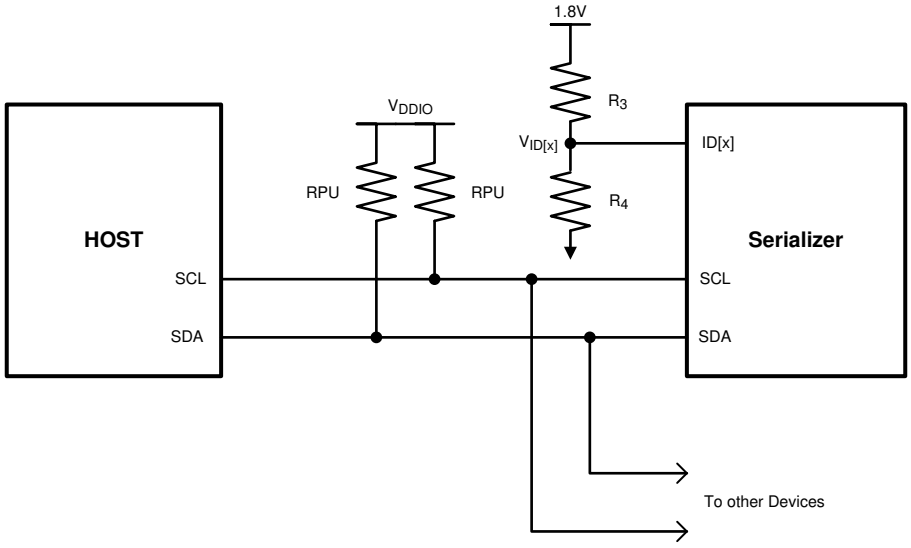


Figure 7-14. IDX Address Decoder on the Serializer

Table 7-6. IDX Setting for DS90UB633A-Q1 Serializer

IDX SETTING — DS90UB633A-Q1 SERIALIZER					
MINIMUM RATIO (V_{IDX}/$V_{(VDD\_n)}$)	MAXIMUM RATIO (V_{IDX}/$V_{(VDD\_n)}$)	SUGGESTED R_3 RESISTOR VALUE (kΩ)	SUGGESTED R_4 RESISTOR VALUE (kΩ)	Address 7-bit	Address 8-bit 0 appended (WRITE)
0	0	Open	0	0x58	0xB0
0.114	0.186	10	2	0x59	0xB2
0.297	0.347	10	4.7	0x5A	0xB4
0.742	1.0	10	100	0x5D	0xBA

7.5.6 Multiple Device Addressing

Some applications require multiple camera devices with the same fixed address to be accessed on the same I2C bus. The DS90UB633A-Q1 provides slave ID matching/aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming of the slave alias register on deserializer. This remaps the slave alias address to the target SLAVE_ID address; up to 8 ID aliases are supported in sensor mode when slaves are attached to the DS90UB633A-Q1 serializer. In display mode, when the external slaves are at the deserializer the DS90UB633A-Q1 supports one ID alias. The ECU controller must keep track of the list of I2C peripherals in order to properly address the target device.

See Figure 7-15 for an example of this function.

- ECU is the I2C master and has an I2C master interface.
- The I2C interfaces in DES A and DES B are both slave interfaces.
- The I2C protocol is bridged from DES A to SER A and from DES B to SER B.
- The I2C interfaces in SER A and SER B are both master interfaces.

If master controller transmits I2C slave 0xA0, DES A (address 0xC0), with pass-through enabled, forwards the transaction to remote Camera A. If the controller transmits slave address 0xA4, the DES B 0xC2 recognizes that 0xA4 is mapped to 0xA0 and is transmitted to the remote Camera B. If controller sends command to address 0xA6, the DES B (address 0xC2), with pass-through enabled, forwards the transaction to slave device 0xA2.

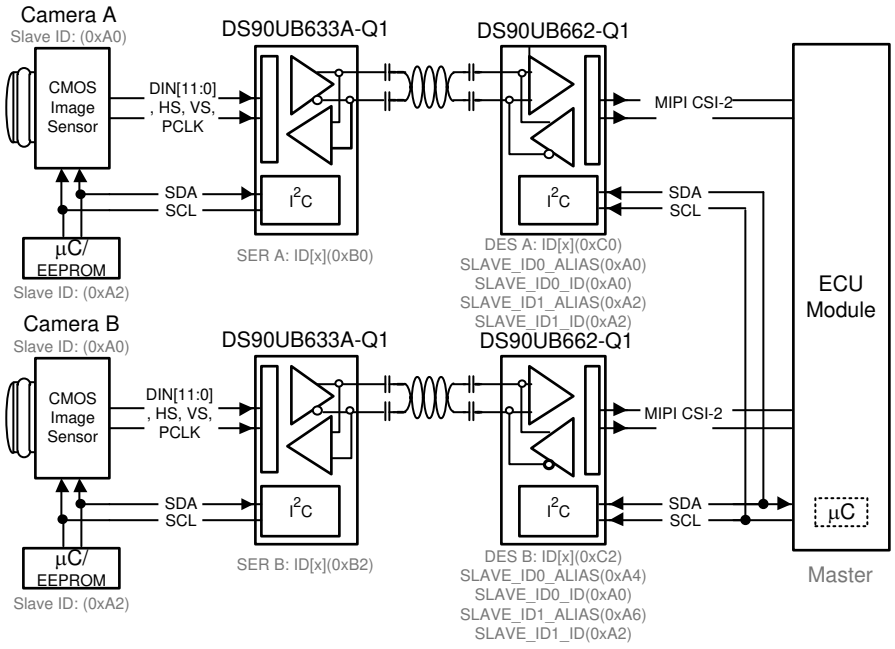


Figure 7-15. Multiple Device Addressing

7.6 Register Maps

See note(1)

In the register definitions under the *TYPE* and *DEFAULT* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access
- R/RC = Read only access, Read to Clear
- (R/W)/SC = Read / Write access, Self-Clearing bit
- (R/W)/S = Read / Write access, Set based on strap pin configuration at startup
- LL = Latched Low and held until read
- LH = Latched High and held until read
- S = Set based on strap pin configuration at startup

Table 7-7. DS90UB633A-Q1 Control Registers

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x00	I2C Device ID	7:1	DEVICE ID	R/W	0xB0	7-bit address of serializer (0x58'h default). This field does not auto update IDX strapped address.
		0	Serializer ID SEL			0: Device ID is from IDX 1: Register I2C Device ID overrides IDX
0x01	Power and Reset	7	RSVD	R/W	0	Reserved
		6	RDS	R/W	0	Digital output drive strength 1: High drive strength 0: Low drive strength
		5	$V_{(VDDIO)}$ Control	R/W	1	Auto voltage control 1: Enable 0: Disable
		4	$V_{(VDDIO)}$ MODE	R/W	1	$V_{(VDDIO)}$ voltage set 1: $V_{(VDDIO)}$ = 3.3 V 0: $V_{(VDDIO)}$ = 1.8 V
		3	ANAPWDN	R/W	0	This register can be set only through local I2C access. 1: Analog power down. Powers down the analog block in the serializer. 0: No effect
		2	RSVD	R/W	0	Reserved
		1	DIGITAL RESET1	R/W	0	1: Resets the digital block except for register values. Does not affect device I2C bus or Device ID. This bit is self-clearing. 0: Normal operation
		0	DIGITAL RESET0	R/W	0	1: Digital reset, resets the entire digital block including all register values. This bit is self-clearing. 0: Normal operation.
0x02	**Reserved**					

Table 7-7. DS90UB633A-Q1 Control Registers (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x03	General Configuration	7	RX CRC Checker Enable	R/W	1	Back-channel CRC checker enable 1: Enable 0: Disable
		6	TX Parity Generator Enable	R/W	1	Forward channel parity generator enable. 1: Enable 0: Disable
		5	CRC Error Reset	R/W	0	Clear CRC error counters This bit is NOT self-clearing. 1: Clear counters 0: Normal operation
		4	I2C Remote Write Auto Acknowledge	R/W	0	Automatically acknowledge I2C remote write The mode works when the system is LOCKed. 1: Enable: When enabled, I2C writes to the deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the deserializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. 0: Disable
		3	I2C Pass-Through All	R/W	0	1: Enable Forward Control Channel pass-through of all I2C accesses to I2C IDs that *do not match* the serializer I2C ID. *The I2C accesses are then remapped to address specified in register 0x06.* 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C IDs *matching* either the remote deserializer ID or the remote I2C IDs.
		2	I2C Pass-Through	R/W	1	I2C Pass-through mode 1: Pass-through enabled. DES alias 0x07 and slave alias 0x09 0: Pass-through disabled
		1	OV_CLK2PLL	R/W	0	1:Enabled : When enabled this register overrides the clock to PLL mode (External Oscillator mode or Direct PCLK mode) defined through MODE pin and allows selection through register 0x35 in the serializer. 0: Disabled : When disabled, Clock to PLL mode (External Oscillator mode or Direct PCLK mode) is defined through MODE pin on the Serializer.
		0	TRFB	R/W	1	Pixel clock edge select 1: Parallel interface data is strobed on the rising clock edge 0: Parallel interface data is strobed on the falling clock edge
0x04	**Reserved**					

Table 7-7. DS90UB633A-Q1 Control Registers (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x05	Mode Select	7	RSVD	R/W	0	Reserved
		6	RSVD	R/W	0	Reserved
		5	MODE_ OVERRIDE	R/W	0	Allows overriding mode select bits coming from back-channel. 1: Overrides MODE select bits 0: Does not override MODE select bits
		4	MODE_UP_ TO_DATE	R	0	1: Status of mode select from deserializer is up-to-date. 0: Status is NOT up-to-date.
		3	Pin_MODE_ 12–bit mode	R	0	1: 12-bit mode is selected. 0: 12-bit mode is not selected.
		2	Pin_MODE_ 10–bit mode	R	0	1: 10-bit mode is selected. 0: 10-bit mode is not selected.
		1	TX_MODE_12b	R/W	0	Selects 12 bit data-bus. This bit changes the Tx mode settings if MODE_OVERRIDE is SET 0x05[5] = 1. 1: Enables 12 bit HF mode 0: Disables 12 bit HF mode Note: This bit changes mode settings on TX. When TX_MODE_12b is set TX_MODE_10b must be cleared; 0x05[1:0] = 10.
		0	TX_MODE_10b	R/W	0	Selects 10 bit data-bus. This bit changes the Tx mode settings if MODE_OVERRIDE is SET 0x05[5] = 1. 1: Enables 10b mode 0: Disables 10b mode Note: This bit changes mode settings on TX. When TX_MODE_10b is set TX_MODE_12b must be cleared; 0x05[1:0] = 01.
0x06	DES ID	7:1	Deserializer Device ID	R/W	0x00	7-bit *deserializer* Device ID Configures the I2C Slave ID of the remote *deserializer*. A value of 0 in this field disables I2C access to the remote *deserializer*. This field is automatically configured by the bidirectional control channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the bidirectional control channel.
		0	Freeze Device ID	R/W	0	1: Prevents auto-loading of the *deserializer* Device ID by the bidirectional control channel. The ID is frozen at the value written. 0: Update
0x07	DES Alias	7:1	Deserializer ALIAS ID	R/W	0x00	7-bit remote *deserializer* device alias ID Configures the decoder for detecting transactions designated for an I2C *deserializer* device. The transaction is remapped to the address specified in the DES ID register. A value of 0 in this field disables access to the remote *deserializer*.
		0	RSVD	R/W	0	Reserved
0x08	SlaveID	7:1	SLAVE ID	R/W	0x00	7-bit remote slave device ID Configures the physical I2C address of the remote I2C slave device attached to the remote *deserializer*. If an I2C transaction is addressed to the slave alias ID, the transaction is remapped to this address before passing the transaction across the bidirectional control channel to the *deserializer* and then to remote slave. A value of 0 in this field disables access to the remote I2C slave.
		0	RSVD	R/W	0	Reserved

Table 7-7. DS90UB633A-Q1 Control Registers (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x09	Slave Alias	7:1	SLAVE ALIAS ID	R/W	0x00	7-bit remote slave device alias ID Configures the decoder for detecting transactions designated for an I2C slave device attached to the remote *deserializer*. The transaction is remapped to the address specified in the slave ID register. A value of 0 in this field disables access to the remote I2C slave.
		0	RSVD	R/W	0	Reserved
0x0A	CRC Errors	7:0	CRC Error Byte 0	R	0x00	Number of back-channel CRC errors during normal operation. Least significant byte.
0x0B	CRC Errors	7:0	CRC Error Byte 1	R	0x00	Number of back-channel CRC errors during normal operation. Most significant byte
0x0C	General Status	7:5	Rev-ID	R	0x0	Revision ID 0x0: Production Revision ID
		4	RX Lock Detect	R	0	1: RX LOCKED 0: RX not LOCKED
		3	BIST CRC Error Status	R	0	1: CRC errors in BIST mode 0: No CRC errors in BIST mode
		2	PCLK Detect	R	0	1: Valid PCLK detected 0: Valid PCLK not detected
		1	DES Error	R	0	1: CRC error is detected during communication with deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x03[5]. 0: No effect
		0	LINK Detect	R	0	1: Cable link detected 0: Cable link not detected This includes any of the following faults: — Cable open — '+' and '-' shorted — Short to GND — Short to battery
0x0D	GPO[0] and GPO[1] Configuration	7	GPO1 Output Value	R/W	0	Local GPIO output value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is output, and remote GPIO control is disabled.
		6	GPO1 Remote Enable	R/W	1	Remote GPIO Control 1: Enable GPIO control from remote deserializer. The GPIO pin must be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote deserializer
		5	RSVD	R/W	0	Reserved
		4	GPO1 Enable	R/W	1	1: GPIO enable 0: Tri-state
		3	GPO0 Output Value	R/W	0	Local GPIO output value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is output, and remote GPIO control is disabled.
		2	GPO0 Remote Enable	R/W	1	Remote GPIO Control 1: Enable GPIO control from remote deserializer. The GPIO pin must be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote deserializer.
		1	RSVD	R/W	0	Reserved
		0	GPO0 Enable	R/W	1	1: GPIO enable 0: Tri-state

Table 7-7. DS90UB633A-Q1 Control Registers (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x0E	GPO[2] and GPO[3] Configuration	7	GPO3 Output Value	R/W	0	Local GPIO output value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is output, and remote GPIO control is disabled.
		6	GPO3 Remote Enable	R/W	0	Remote GPIO vontrol 1: Enable GPIO control from remote Deserializer. The GPIO pin must be an output, and the value is received from the remote deserializer. 0: Disable GPIO control from remote Deserializer.
		5	GPO3 Direction	R/W	1	1: Input 0: Output
		4	GPO3 Enable	R/W	1	1: GPIO enable 0: Tri-state
		3	GPO2 Output Value	R/W	0	Local GPIO output value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is output, and remote GPIO control is disabled.
		2	GPO2 Remote Enable	R/W	1	Remote GPIO Control 1: Enable GPIO control from remote deserializer. The GPIO pin must be an output, and the value is received from the remote deserializer. 0: Disable GPIO control from remote deserializer.
		1	RSVD	R/W	0	Reserved
		0	GPO2 Enable	R/W	1	1: GPIO enable 0: Tri-state
0x0F	I2C Master Config	7:5	RSVD	R	0x0	Reserved
		4:3	SDA Output Delay	R/W	00	SDA output delay This field configures output delay on the SDA output. Setting this value increases output delay in units of 50 ns. Nominal output delay values for SCL to SDA are: 00: ~350 ns 01: ~400 ns 10: ~450 ns 11: ~500 ns
		2	Local Write Disable	R/W	0	Disable remote writes to local registers setting this bit to a 1 prevents remote writes to local device registers from across the control channel. This prevents writes to the serializer registers from an I2C master attached to the deserializer. setting this bit does not affect remote access to I2C slaves at the serializer.
		1	I2C Bus Timer Speed up	R/W	0	Speed up I2C bus watchdog timer 1: Watchdog timer expires after approximately 50 microseconds. 0: Watchdog timer expires after approximately 1 second.
		0	I2C Bus Timer Disable	R/W	0	1. Disable I2C bus watchdog timer when the I2C watchdog timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus is assumed to be free. If SDA is low and no signaling occurs, the device attempts to clear the bus by driving 9 clocks on SCL. 0: No effect

Table 7-7. DS90UB633A-Q1 Control Registers (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x10	I2C Control	7	RSVD	R/W	0	Reserved
		6:4	SDA Hold Time	R/W	0x1	Internal SDA hold time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 ns.
		3:0	I2C Filter Depth	R/W	0x7	I2C glitch filter depth. This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10 ns.
0x11	SCL High Time	7:0	SCL High Time	R/W	0x82	I2C master SCL high time This field configures the high pulse width of the SCL output when the serializer is the master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4 µs + 1 µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x12	SCL LOW Time	7:0	SCL Low Time	R/W	0x82	I2C SCL low time This field configures the low pulse width of the SCL output when the serializer is the master on the local I2C bus. This value is also used as the SDA setup time by the I2C slave for providing data prior to releasing SCL during accesses over the bidirectional control channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7 µs + 0.3 µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x13	General Purpose Control	7:0	GPCR[7:0]	R/W	0x00	1: High 0: Low
0x14	BIST Control	7:5	RSVD	R	0x0	Reserved
		4:3	RSVD	R/W	0x0	Reserved
		2:1	Clock Source	R/W	0x0	Allows choosing different OSC clock frequencies for forward channel frame. OSC clock frequency in functional mode when OSC mode is selected or when the selected clock source is not present, for example, missing PCLK/ external oscillator. See Table 7-3 for oscillator clock frequencies when PCLK/ external clock is missing.
		0	RSVD	R/W	0	Reserved
0x15 - 0x1D	**Reserved**					
0x1E	BCC Watchdog Control	7:1	BCC Watchdog Timer	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the bidirectional control channel watchdog timeout value in units of 2 ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	R/W	0	1: Disables BCC watchdog timer operation 0: Enables BCC watchdog timer operation
0x1F - 0x26	**Reserved**					
0x27	Analog Power Down Control	7:6	Reserved	R	0	Reserved
		5	Power Down PLL	RW	0	1: Power down forward channel PLL 0: Normal operation
		4	Reserved	RW	0	Reserved
		3	Power Down NCLK	RW	0	1: Power Down NCLK 0: Normal Operation
		2:0	Reserved	RW	0	Reserved

Table 7-7. DS90UB633A-Q1 Control Registers (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x28	**Reserved**					
0x29	OSC Divider	7:6	RSVD	R/W	0x0	Reserved
		5	OSC Divider	R/W	0	Selects the OSC frequency to drive out on GPO2 in external oscillator mode. 0: Divide by 2 (default) 1: Divide by 4
		4:0	RSVD	R/W	0x06	Reserved
0x2A	CRC Errors	7:0	BIST Mode CRC Errors Count	R	0x00	Number of CRC errors in the back channel when in BIST mode
0x2B - 0x2C	**Reserved**					
0x2D	Inject Forward Channel Error	7	Force Forward Channel Error	R/W	0	1: Forces 1 (one) error over forward channel frame in normal operating mode. Self-clearing bit. 0: No error
		6:0	Force BIST Error	R/W	0x00	N: Forces N number of errors in BIST mode. This register MUST be set BEFORE BIST mode is enabled. BIST error count register on the deserializer must be read AFTER BIST mode is disabled for the correct number of errors incurred while in BIST mode. 0: No error
0x2E - 0x34	**Reserved**					
0x35	PLL Clock Overwrite	7:4	RSVD	R/W	0x0	Reserved
		3	PIN_LOCK to External Oscillator	R	0	Status of mode select pin 1: Indicates external oscillator mode is selected by mode-resistor 0: External oscillator mode is not selected by mode-resistor
		2	RSVD	R	0	Reserved
		1	LOCK to External Oscillator	R/W	0	Affects only when 0x03[1] =1 (OV_CLK2PLL) and 0x35[0] = 0 1: Routes GPO3 directly to PLL 0: Allows PLL to lock to PCLK
		0	LOCK2OSC	R/W	1	Affects only when 0x03[1] = 1 (OV_CLK2PLL) 1: Allows internal OSC clock to feed into PLL 0: Allows PLL to lock to either PCLK or external clock from GPO3

(1) To ensure optimum device functionality, TI recommends to *NOT* write to any RESERVED registers.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UB633A-Q1 was designed as a serializer to support automotive camera designs. Automotive cameras are often located in remote positions such as bumpers or trunk lids, and a major component of the system cost is the wiring. For this reason it is desirable to minimize the wiring to the camera. This chipset allows the video data, along with a bidirectional control channel, and power to all be sent over a single coaxial cable. The chipset is also able to transmit over STP.

8.1.1 Power Over Coax

See application report *Sending Power Over Coax in DS90UB933 Designs* for more details.

8.1.2 Power-Up Requirements and PDB Pin

Transition of the PDB pin from LOW to HIGH must occur after the V_{VDDIO} and V_{VDD_n} supplies have reached their required operating voltage levels. Direct control of the PDB timing by processor GPIO is recommended if possible. When direct control of PDB is not available, the PDB pin can be tied to the power supply rail with an RC filter network to help ensure proper power up timing. GPO2 should be low when PDB goes high. Timing constraints are noted in Figure 8-1 and Table 8-1. Please refer to Section 7.3.8 for device operation when powered down.

If GPO2 state is not determined when PDB goes high, DS90UB633A-Q1 registers must be programmed to configure the transmission mode. Mode Select register 0x05[5] must be set to 1 and register 0x05 bit 1 and 0 are to be selected based on desired 12-bit or 10-bit transmit data format.

Common applications tie the $V_{(VDDIO)}$ and $V_{(VDD\_n)}$ supplies to the same power source of 1.8 V typically. This is an acceptable method for ramping the $V_{(VDDIO)}$ and $V_{(VDD\_n)}$ supplies. The main constraint here is that the $V_{(VDD\_n)}$ supply does not lead in ramping before the $V_{(VDDIO)}$ system supply. This is noted in Figure 8-1 with the requirement of $t_1 \geq 0$. $V_{(VDDIO)}$ must reach the expected operating voltage earlier than $V_{(VDD\_n)}$ or at the same time.

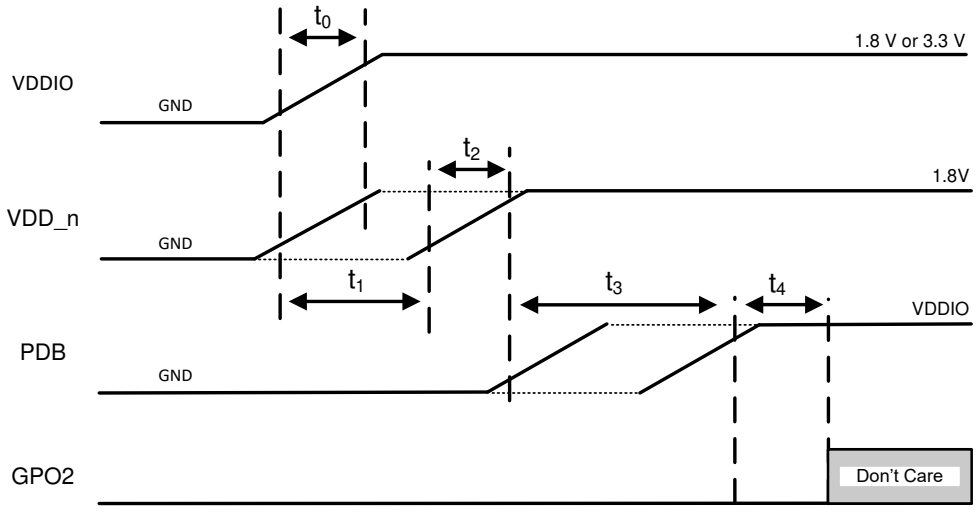


Figure 8-1. Suggested Power-Up Sequencing

Table 8-1. Power-Up Sequencing Constraints

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	Units
t_0	$V_{(VDDIO)}$ rise time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required	0.05		5	ms
t_1	$V_{(VDDIO)}$ to $V_{(VDD\_n)}$ delay	10% of rising edge ($V_{(VDDIO)}$) to 10% of rising edge ($V_{(VDD\_n)}$)	0			ms
t_2	$V_{(VDD\_n)}$ rise time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required. V_{PDB} < 10% of $V_{(VDDIO)}$	0.05		5	ms
t_3*	$V_{(VDD\_n)}$ to PDB V_{IH} delay	90% rising edge ($V_{(VDD\_n)}$) to PDB V_{IH}	0		10	ms
t_4	PDB to GPO2 delay	PDB V_{IH} to 10% of rising edge (GPO2)	1.3			ms

* If timing constraint t_3 cannot be assured, the following programming steps should be issued to the DS90UB633A-Q1 via local I2C control (not via remote back channel). These programming steps should be completed > 10ms after the power sequence is complete (V_{PDB} > PDB V_{IH}) with no delay between write commands. This step will cause a brief restart of the forward channel output:

- Write Register 0x27 = 0x28
- Write Register 0x27 = 0x20
- Write Register 0x27 = 0x00

8.1.3 AC Coupling

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in Figure 8-2. For applications utilizing single-ended 50-Ω coaxial cable, the unused data pin (DOUT–, RIN–) must utilize a 0.047-µF capacitor and must be terminated with a 50-Ω resistor. For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC-coupling capacitor. This helps minimize degradation of signal quality due to package parasitics.

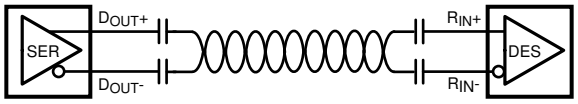


Figure 8-2. AC-Coupled Connection (STP)

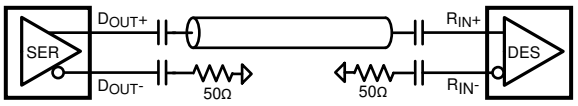


Figure 8-3. AC-Coupled Connection (Coaxial)

8.1.4 Transmission Media

The DS90UB633A/662 chipset is intended to be used in a point-to-point configuration through a shielded coaxial cable. The serializer and deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connectors) must have a differential impedance of 100 Ω, or a single-ended impedance of 50 Ω. The maximum length of cable that can be used is dependent on the quality of the cable (gauge, impedance), connector, board(discontinuities, power plane), the electrical environment (for example, power stability, ground noise, input clock jitter, PCLK frequency, etc.). The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. A differential probe should be used to measure across the termination resistor at the CMLOUTP/N pins.

Contact TI for a channel specification regarding cable loss parameters and further details on adaptive equalizer loss compensation.

8.2 Typical Applications

8.2.1 Coax Application

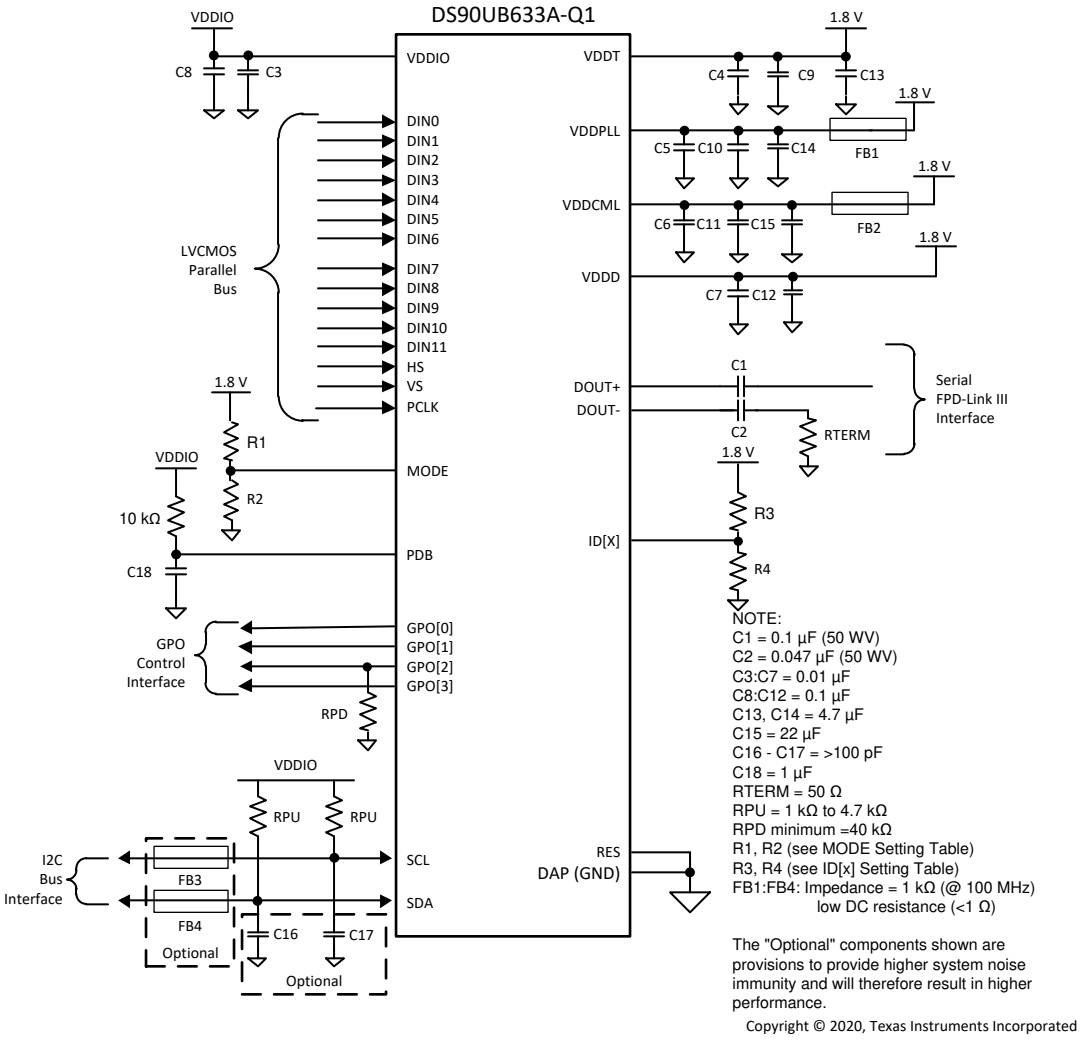


Figure 8-4. Coax Application Connection Diagram

8.2.1.1 Design Requirements

For the typical coax design applications, use the following as input parameters:

Table 8-2. Coax Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{(VDDIO)}$	1.8 V, 2.8 V, or 3.3 V
$V_{(VDD\_n)}$	1.8 V
AC-coupling capacitors for DOUT±	0.1 µF, 0.047 µF (For the unused data pin, DOUT–)
PCLK frequency	100 MHz (12-bit), 100 MHz (10-bit)

8.2.1.2 Detailed Design Procedure

Figure 8-5 shows the typical connection of a DS90UB633A-Q1 serializer using a *coax* interface.

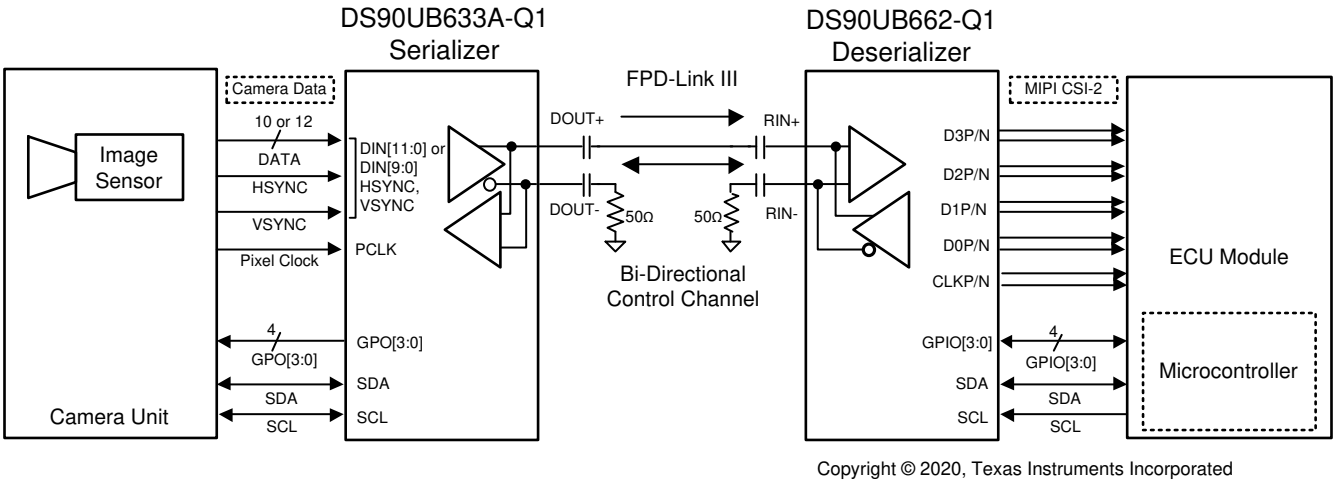


Figure 8-5. Coax Application Block Diagram

8.2.1.3 Application Curves

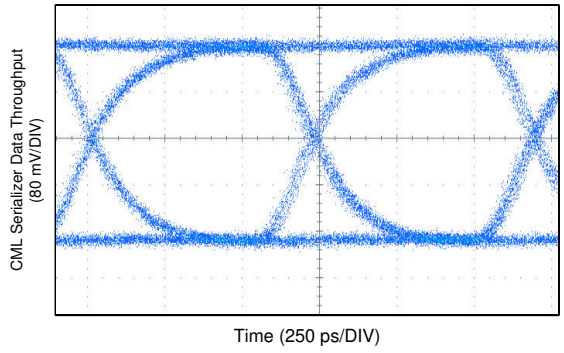


Figure 8-6. Coax Eye Diagram at 1.4-Gbps Line Rate (100-MHz Pixel Clock, 10-bit Mode) from Serializer Output (DOUT+)

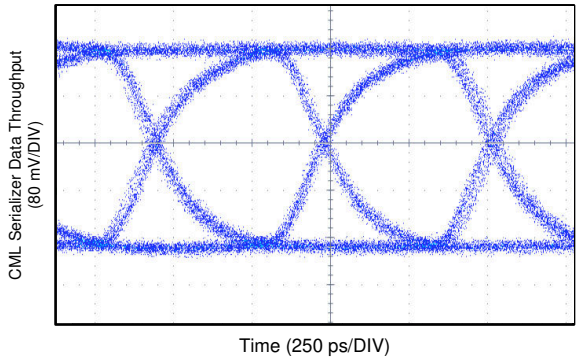


Figure 8-7. Coax Eye Diagram at 1.87-Gbps Line Rate (100-MHz Pixel Clock, 12-bit Mode) from Serializer Output (DOUT+)

8.2.2 STP Application

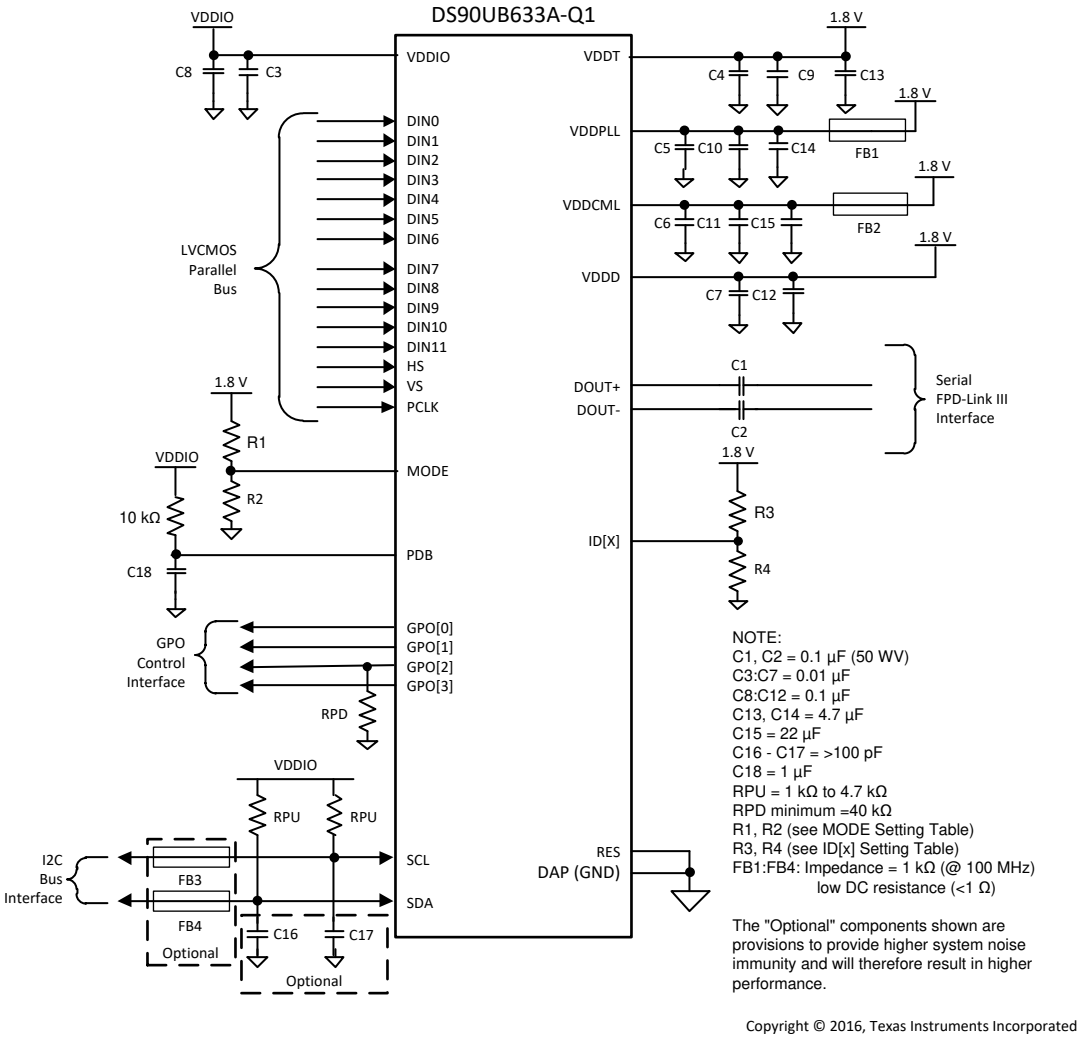


Figure 8-8. STP Application Connection Diagram

8.2.2.1 Design Requirements

For the typical STP design applications, use the following as input parameters:

Table 8-3. STP Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{(VDDIO)}$	1.8 V, 2.8 V, or 3.3 V
$V_{(VDD\_n)}$	1.8 V
AC-coupling capacitors for DOUT±	0.1 µF
PCLK frequency	100 MHz (12-bit), 100 MHz (10-bit)

8.2.2.2 Detailed Design Procedure

Figure 8-9 shows a typical connection of a DS90UB633A-Q1 Serializer using an **STP** interface.

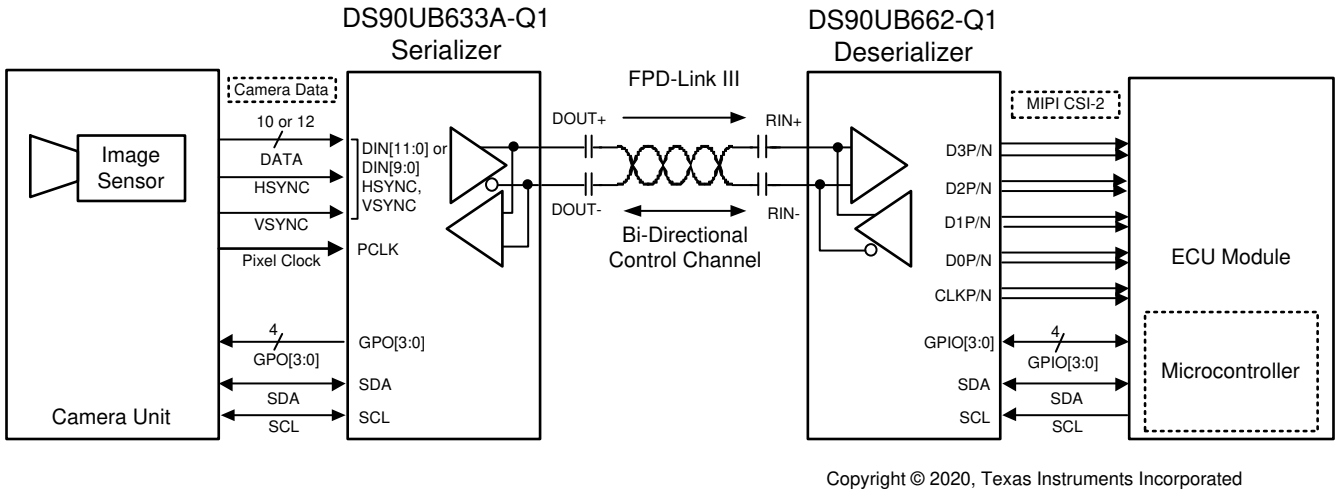


Figure 8-9. STP Application Block Diagram

Eye diagrams in STP applications have roughly double the swing as with coax (Figure 8-6 and Figure 8-7).

9 Power Supply Recommendations

This device is designed to operate from an input core voltage supply of 1.8 V. Some devices provide separate power and ground terminals for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin description tables typically provide guidance on which circuit blocks are connected to which power terminal pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs. The voltage applied on $V_{(VDDIO)}$ (1.8 V, 2.8 V, 3.3 V) or other power supplies making up $V_{(VDD\_n)}$ (1.8 V) must be at the input pin - any board level DC drop must be compensated (that is, ferrite beads in the path of the power supply rails).

10 Layout

10.1 Layout Guidelines

Design circuit board layout and stack-up for the serializer/deserializer devices to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, making the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors should be at least 5× the power supply voltage being used.

TI recommends surface mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range and smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

Information on the WQFN package is provided in *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the DS90UB633A-Q1 to the GND plane with vias.

Routing FPD-Link III Signal Traces and PoC Filter

Routing the FPD-Link III signal traces between the RIN pins and the connector as well as connecting the PoC filter to these traces are the most critical pieces of a successful DS90UB633A-Q1 PCB layout. Figure 10-2 shows an example PCB layout of the DS90UB633A-Q1 configured for interface to remote sensor modules over coaxial cables. The layout example also uses a footprint of an edge-mount FAKRA connector provided by Rosenberger (P/N: 59S20X-40ML5-Z).

The following list provides essential recommendations for routing the FPD-Link III signal traces between the DS90UB633A-Q1 receiver output pins (DOUT) and the FAKRA connector, and connecting the PoC filter.

- The routing of the FPD-Link III traces may be all on the top layer (as shown in the example) or partially embedded in middle layers if EMI is a concern

- The AC-coupling capacitors should be on the top layer and very close to the DS90UB633A-Q1 output pins to minimize the length of coupled differential trace pair between the pins and the capacitors
- Route the DOUT+ trace between the AC-coupling capacitor and the FAKRA connector as a 50-Ω single-ended micro-strip with tight impedance control (±10%). Calculate the proper width of the trace for a 50-Ω impedance based on the PCB stack-up. Ensure that the trace can carry the PoC current for the maximum load presented by the remote sensor module.
- The PoC filter should be connected to the ROUT+ trace through the first ferrite bead (FB1). The FB1 should be touching the high-speed trace to minimize the stub length seen by the transmission line. Create an anti-pad or a moat under the FB1 pad that touches the trace. The anti-pad should be a plane cutout of the ground plane directly underneath the top layer without cutting out the ground reference under the trace. The purpose of the anti-pad is to maintain the impedance as close to 50 Ω as possible.
- Route the DOUT– trace loosely coupled to the DOUT+ trace for the length similar to the DOUT+ trace length when possible. This will help the differential nature of the receiver to cancel out any common-mode noise that may be present in the environment that may couple on to the DOUT+ and DOUT– signal traces. When routing on inner layers, length matching for single-ended traces does not provide as significant benefit.

When configured for STP and routing differential signals to the DS90UB633A-Q1 receiver inputs, the traces should maintain 100-Ω differential impedance routed to the connector. When choosing to implement a common mode choke for common mode noise reduction, take care to minimize the effect of any mismatch. Figure 60 shows an example PCB layout for STP configuration.

10.1.1 Interconnect Guidelines

See *Application Note 1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instrument web site at: www.ti.com/lvds.

10.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in the following:

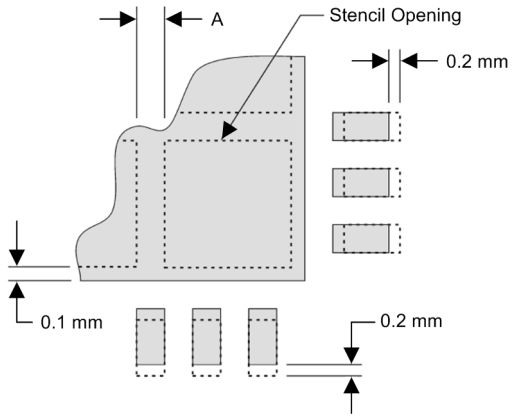


Figure 10-1. No Pullback WQFN, Single Row Reference Diagram

Table 10-1. No Pullback WQFN Stencil Aperture Summary for DS90UB633A-Q1

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE(mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS90UB633A-Q1	32	RTV	0.25 × 0.6	0.5	3.1 × 3.1	0.25 × 0.7	1.4 × 1.4	4	0.2

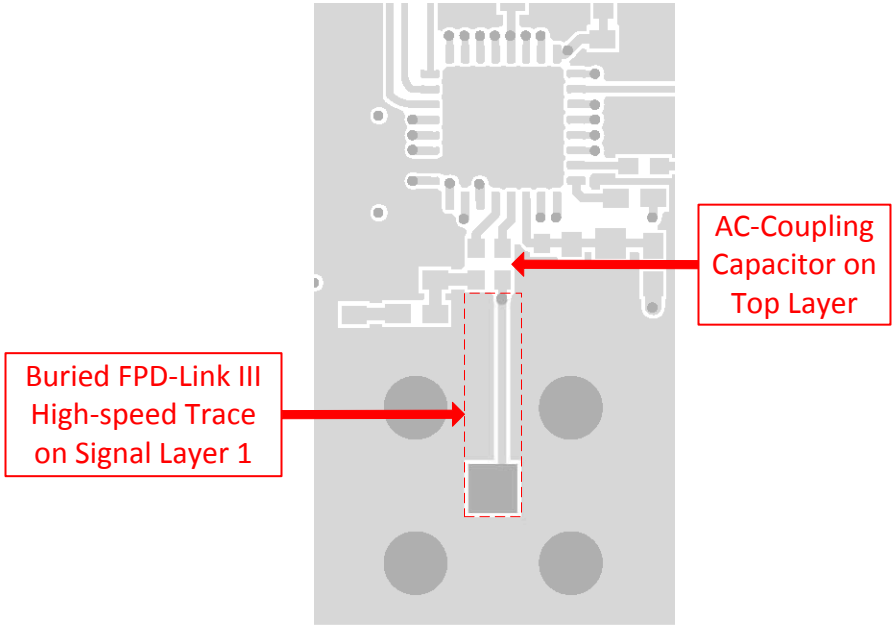


Figure 10-2. DS90UB633A-Q1 Serializer DOUT+ Trace Layout

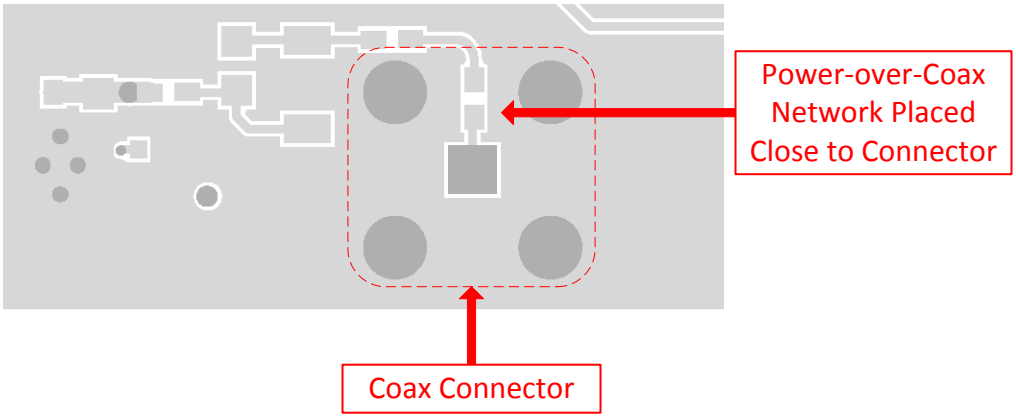


Figure 10-3. DS90UB633A-Q1 Power-over-Coax Layout

Figure 10-2 and Figure 10-3 are derived from the layout design of the DS90UB633A-Q1 evaluation module (EVM). The EVM is designed for coax operation. The trace carrying high-speed serial signal DOUT+ is critical and must be kept as short as possible. Burying this trace in an internal PCB layer may help reduce emissions. If Power-over-Coax is used, the stub must be minimized by placing the filter network as close as possible to the coax connector. These graphics and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in this serializer.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel* (SNLA222)
- *Sending Power Over Coax in DS90UB913A Designs* (SNOA549)
- *FPD-Link Learning Center*
- *Understanding the I2C Bus*
- *I2C Bus Pullup Resistor Calculation*
- *Soldering Specifications Application Report,*
- *IC Package Thermal Metrics Application Report,*
- *AN-1187 Leadless Leadframe Package (LLP) Application Report*
- *LVDS Owner's Manual*
- *An EMC/EMI System-Design and Testing Methodology for FPD-Link III SerDes*
- *Ten Tips for Successfully Designing with Automotive EMC/EMI Requirements*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

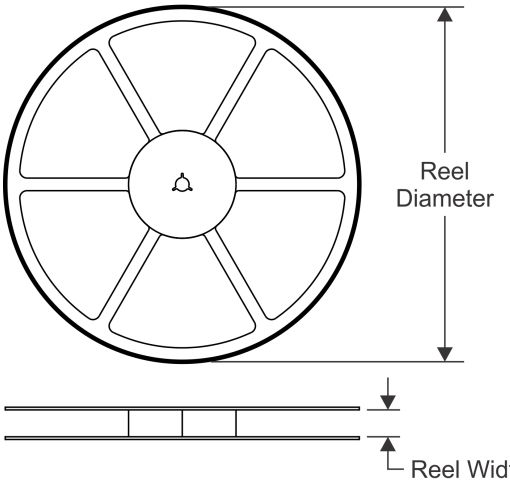
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Packaging Information

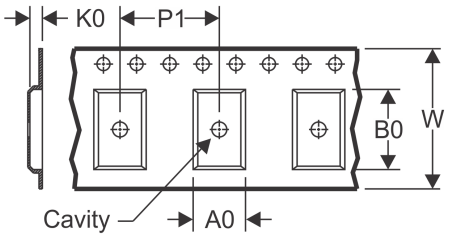
Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
DS90UB633ATRTVRQ1	PREVIEW	WQFN	RTV	32	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260 C-168 HR	-40 to 105	UB633AQ
DS90UB633ATRTVTQ1	PREVIEW	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	SN	Level-3-260 C-168 HR	-40 to 105	UB633AQ

12.2 Tape and Reel Information

REEL DIMENSIONS

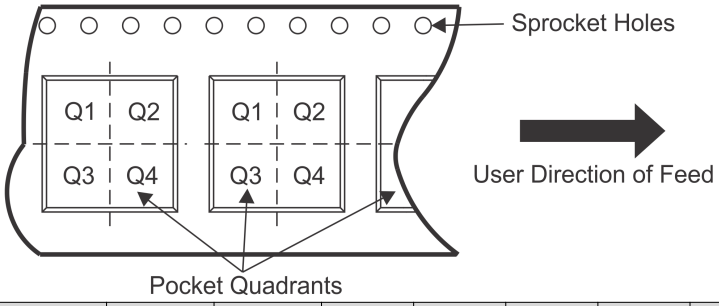


TAPE DIMENSIONS



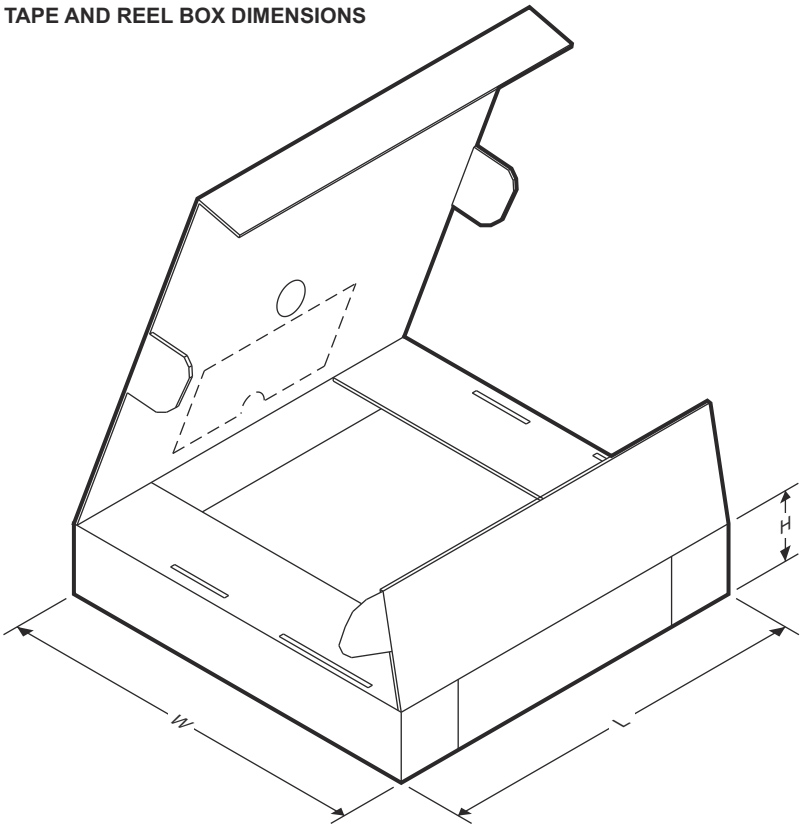
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB633ATRTVQ1	WQFN	RTV	32	2500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q2
DS90UB633ATRTVQ1	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q2

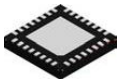
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB633ATRTVRQ1	WQFN	RTV	32	2500	367.0	367.0	35.0
DS90UB633ATRTVTQ1	WQFN	RTV	32	250	210.0	185.0	35.0

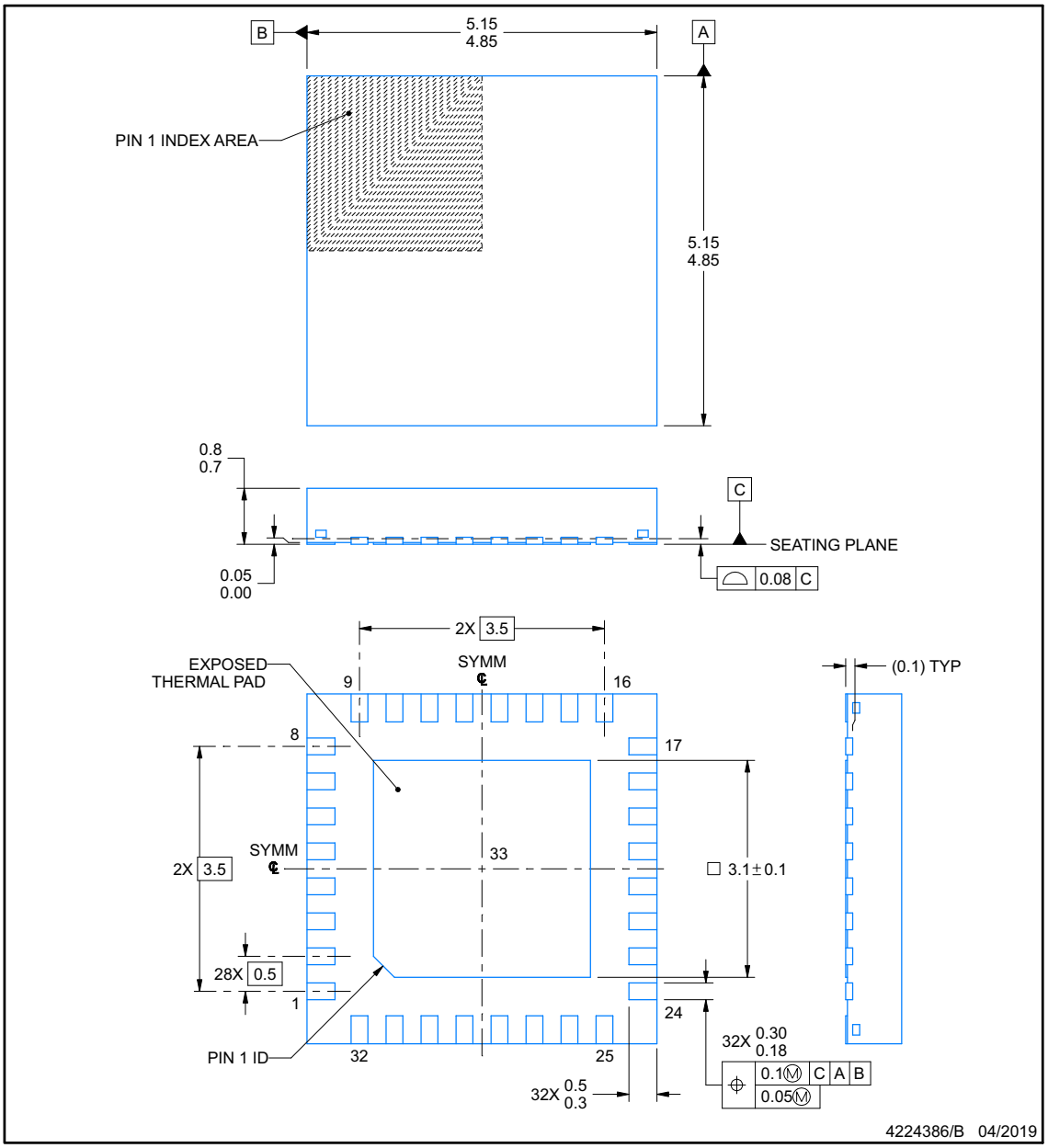
PACKAGE OUTLINE

RTV0032A



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



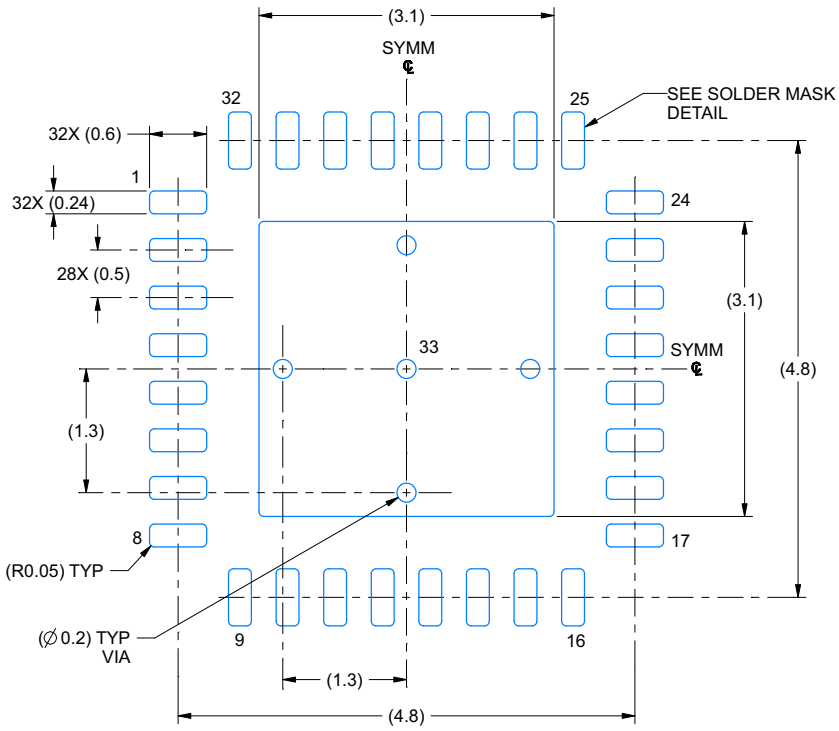
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

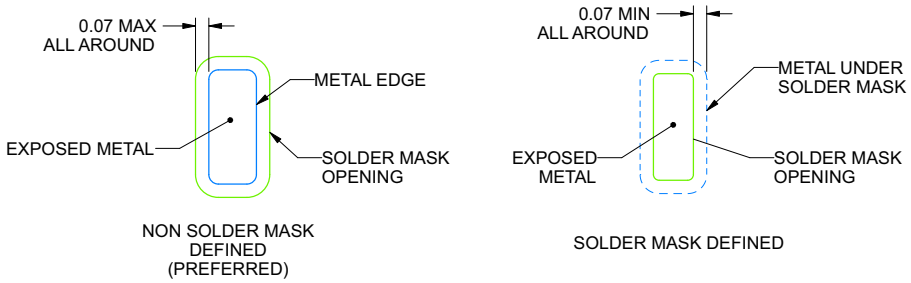
EXAMPLE BOARD LAYOUT

RTV0032A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4224386/B 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UB633ARTVRQ1	Active	Production	WQFN (RTV) | 32	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UB633AQ
DS90UB633ARTVRQ1.A	Active	Production	WQFN (RTV) | 32	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UB633AQ
DS90UB633ARTVTQ1	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UB633AQ
DS90UB633ARTVTQ1.A	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UB633AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

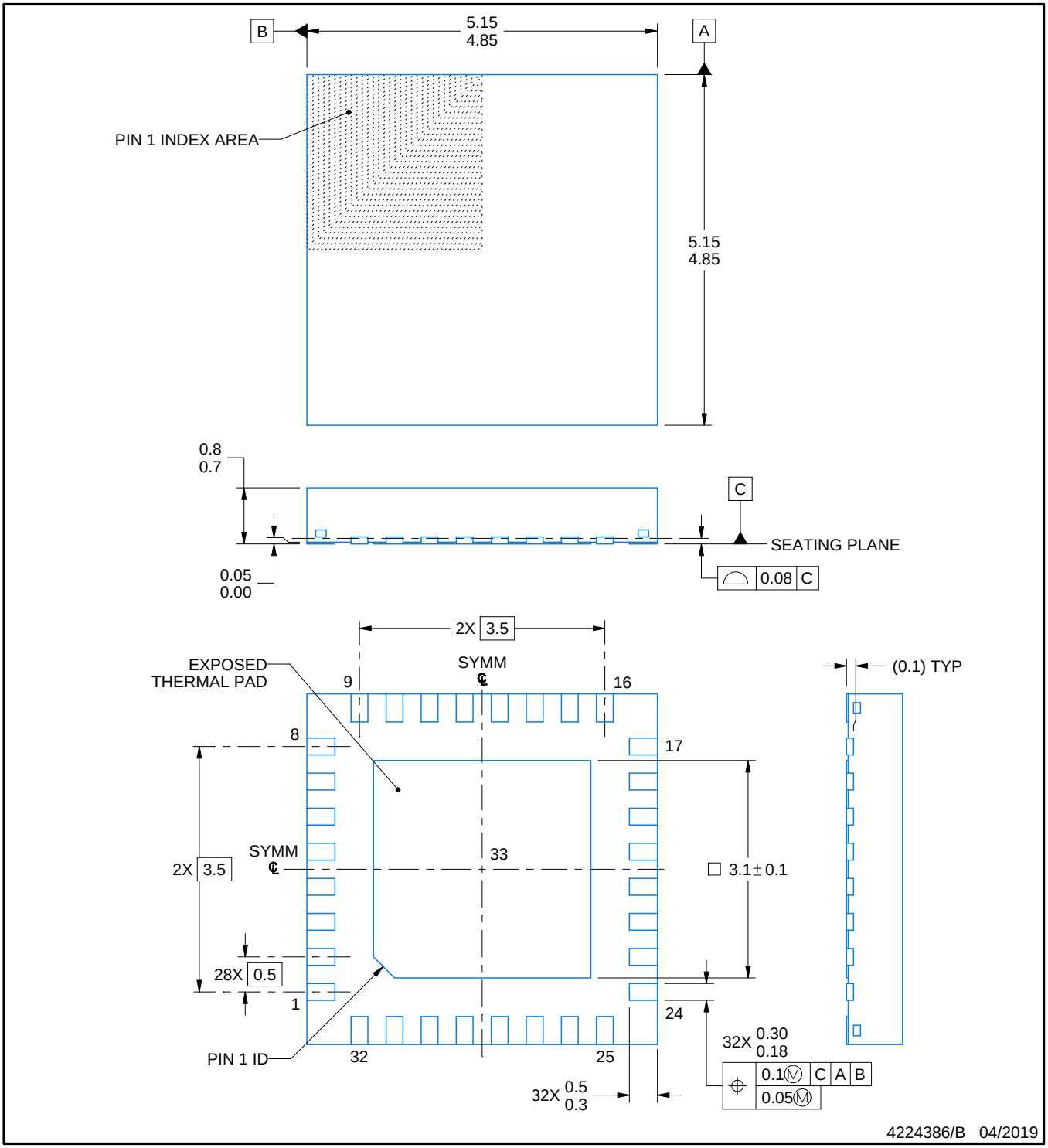
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RTV0032A

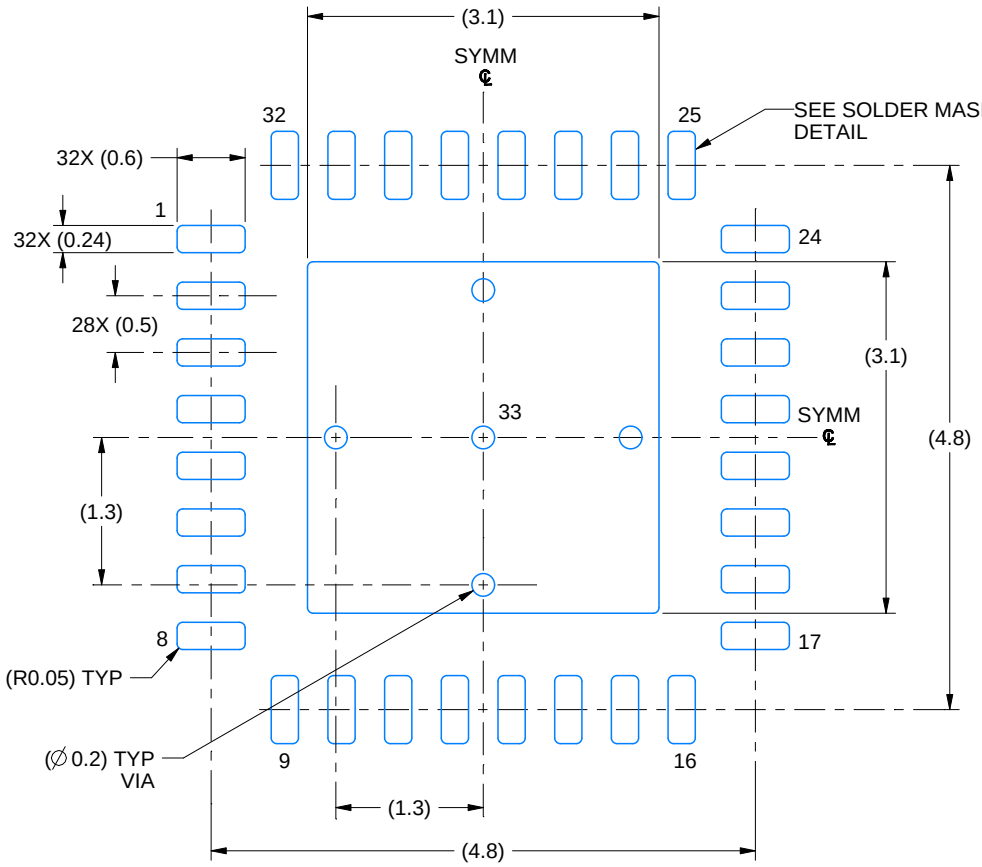
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

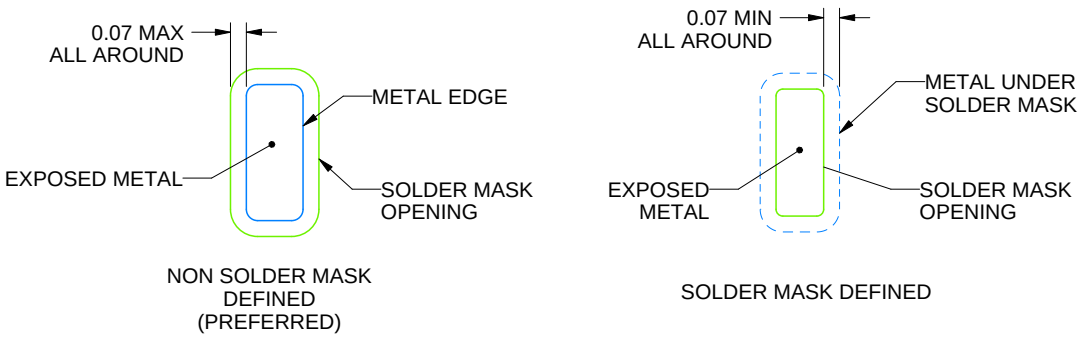


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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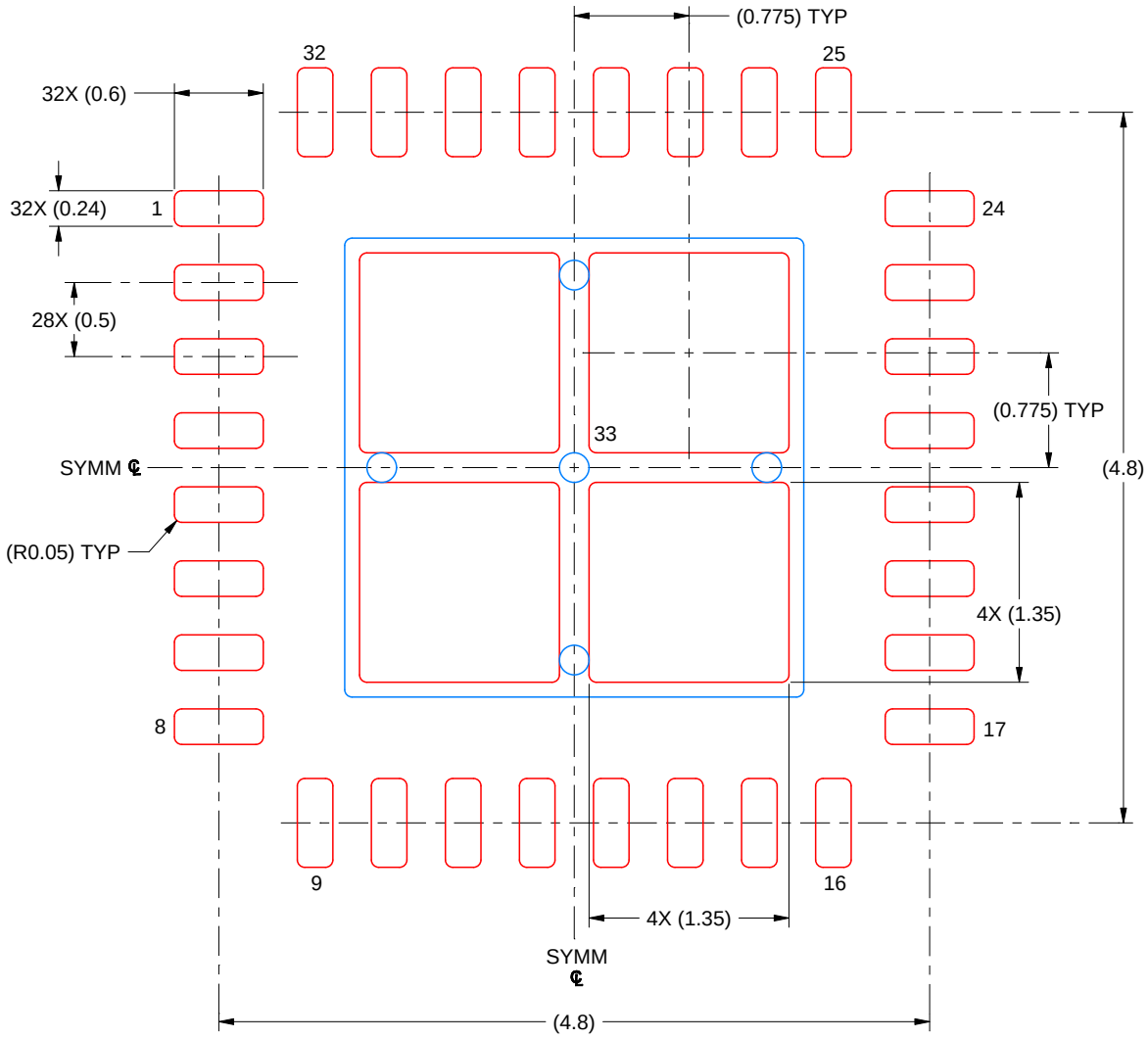
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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