ESD401 1-Channel ESD Protection Diode With Robust IEC ESD Performance

1 Features

- Robust IEC 61000-4-2 level 4 ESD protection:
  - ±24kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-5 surge protection:
  - 4.5A (8/20µs)
  - Low V_{clamp} of 12V at 1.8A I_{PP} (8/20µs)
- IEC 61000-4-4 EFT protection:
  - 80A (5/50ns)
- Bi-directional ESD diode to protect interfaces up to ± 5.5V
- IO capacitance: 0.77pF (typical)
- High DC breakdown voltage: 8.3V (typical)
- Ultra low leakage current: 30pA (typical)
- Low dynamic resistance 0.7Ω (typical)
- Industrial temperature range: –40°C to +125°C
- Industry standard 0402 package

2 Applications

- End equipment:
  - Wearables
  - Laptops and desktops
  - Mobile and tablets
  - Set-top boxes
  - DVR and NVR
  - TV and monitors
  - EPOS (electronic point of sale)
- Interfaces:
  - 1 Gbps ethernet
  - USB 2.0/1.1 with 5.5 V tolerance
  - GPIO
  - Pushbuttons/keypad
  - Audio

3 Description

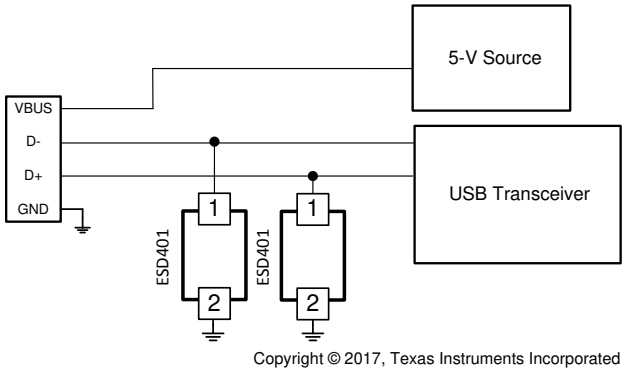
The ESD401 is a bidirectional TVS ESD protection diode featuring low R_{DYN} and low clamping voltage. The ESD401 is rated to dissipate ESD strikes exceeding the maximum level specified in the IEC 61000-4-2 international standard (Level 4). The low dynamic resistance (0.7Ω) to ensure system level protection against transient events. This device features a 0.77pF IO capacitance making it ideal for protecting interfaces such as USB 2.0. The device can operate with ultra-low leakage up to ±5.5V and survive DC faults up to 8.3V.

The ESD401 is offered in the industry standard 0402 (DPY) package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD401	DPY (X1SON, 2)	1mm × 0.6mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical USB 2.0 Application Schematic

Table of Contents

4 Pin Configuration and Functions

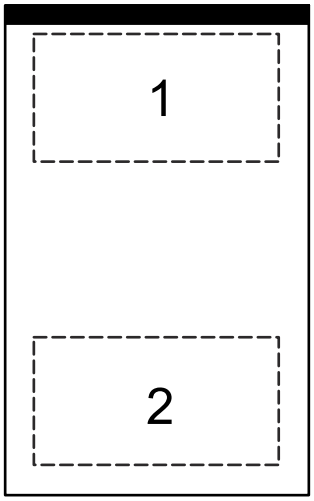


Figure 4-1. DPY Package, 2-Pin X1SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
IO	2	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		67	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		4.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings — JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±24000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

5.5 Thermal Information

THERMAL METRIC(1)		ESD401 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	420	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	169.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	276.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	122.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	157.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–5.5		5.5	V
V_{BRF}	Breakdown voltage, Pin 1 to Pin 2 (1)	I_{IO} =1 mA, at T_A = 25°C	7.5		9.1	V
V_{BRR}	Breakdown voltage, Pin 2 to Pin 1 (1)	I_{IO} =1 mA, at T_A = 25°C	7.5		9.1	V
V_{HOLD}	Holding voltage (2)	I_{IO} =1 mA		8.3		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		11		V
		I_{PP} = 5 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		16		
		I_{PP} = 16 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		24		
		I_{PP} = 1.8 A, IEC-61000-4-5 (t_p - 8/20 µs) from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		12		
		I_{PP} = 4.5 A, IEC-61000-4-5 (t_p - 8/20 µs) from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		15		
I_{LEAK}	Leakage current, Pin 1 to Pin2 and PIn2 to Pin 1	V_{IO} = ±2.5 V		0.03	10	nA
R_{DYN}	Dynamic resistance	Measured between TLP I_{PP} of 10 A and 20 A, Pin 2 to Pin 1 and Pin 1 to Pin2, T_A = 25°C		0.7		Ω
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, Pin 1 to Pin 2 and Pin2 to Pin1, T_A = 25°C		0.77	0.95	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state.
(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

5.7 Typical Characteristics

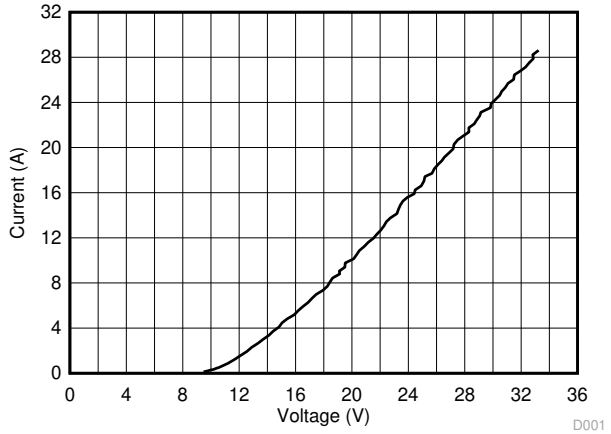


Figure 5-1. Positive TLP Curve, Pin 1 to Pin 2

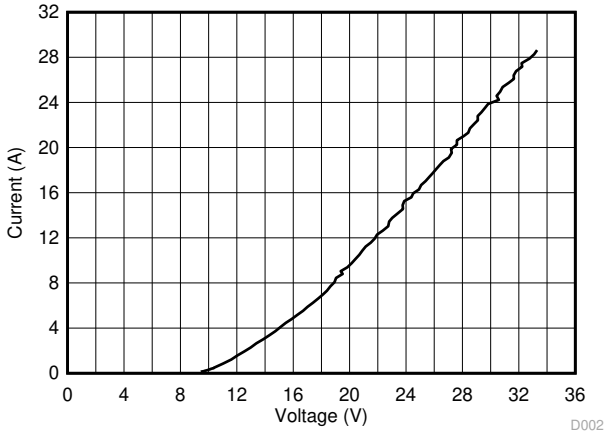


Figure 5-2. Negative TLP Curve, Pin 1 to Pin 2 (Plotted as Positive TLP Curve Pin 2 to Pin 1

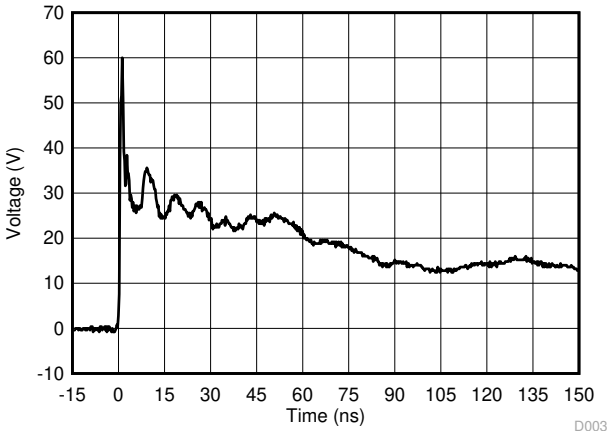


Figure 5-3. 8-kV IEC 61000-4-2 Waveform, Pin1 to Pin 2

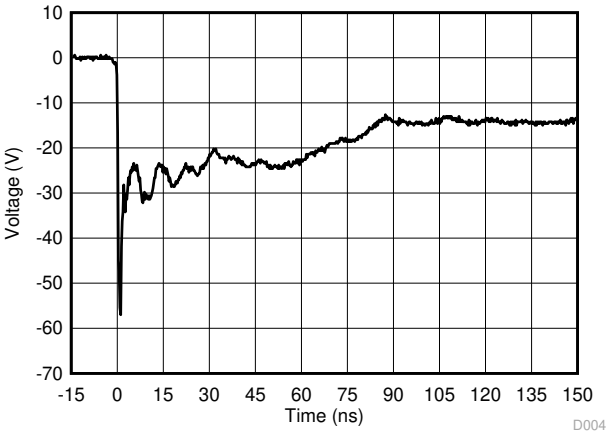


Figure 5-4. –8-kV IEC 61000-4-2 Waveform, Pin 1 to Pin 2

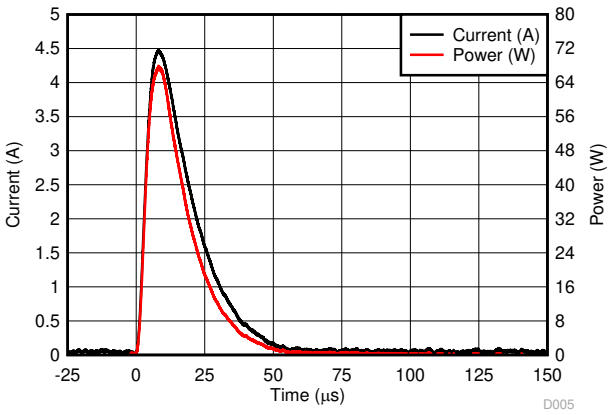


Figure 5-5. Surge (IEC 61000-4-5) Curve (tp = 8/20 µs), Pin 1 to Pin 2

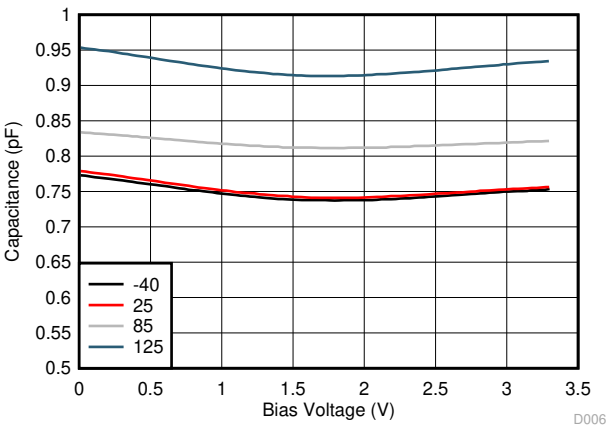


Figure 5-6. Capacitance vs Bias Voltage, Pin 1 to Pin 2

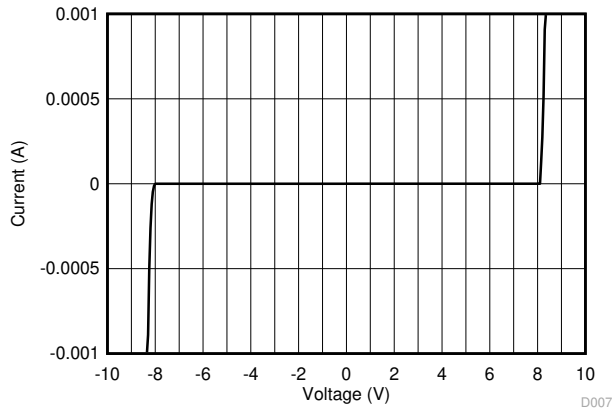


Figure 5-7. DC Voltage Sweep I-V Curve, Pin 1 to Pin 2

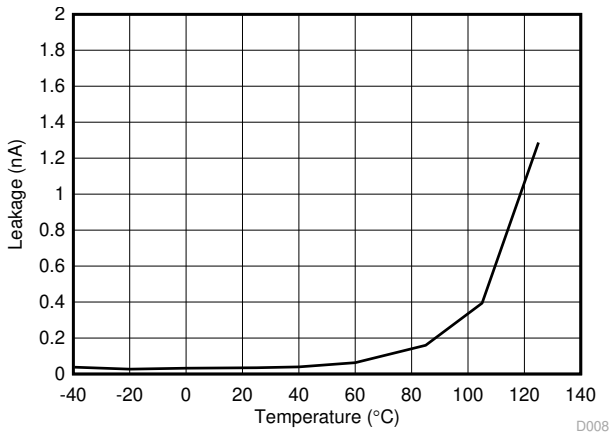


Figure 5-8. Leakage Current vs. Temperature, Pin 1 to Pin 2

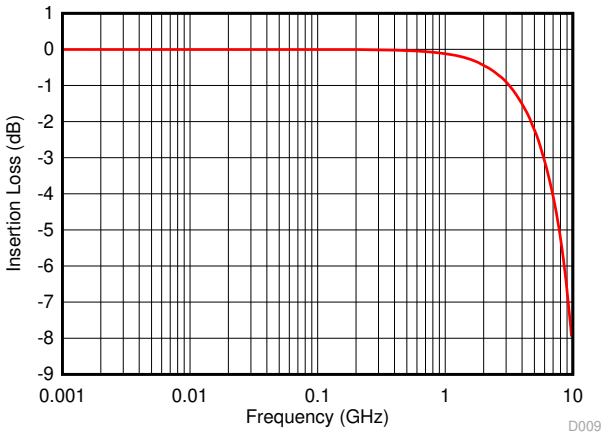


Figure 5-9. Insertion Loss

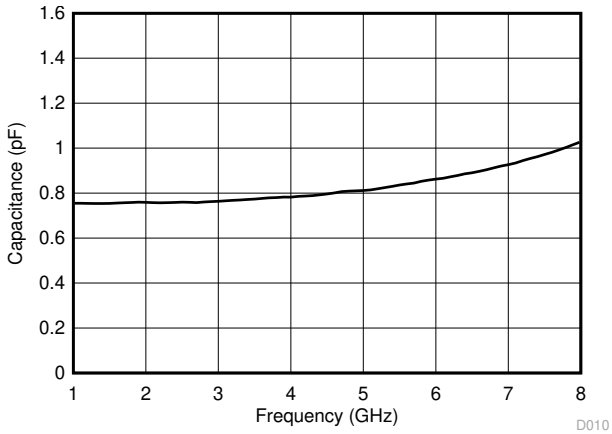


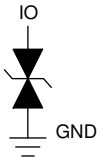
Figure 5-10. Capacitance vs. Frequency, Pin 1 to Pin 2

6 Detailed Description

6.1 Overview

The ESD401 is a bidirectional ESD Protection Diode with ultra-low clamping voltage. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low clamping makes this device ideal for protecting any sensitive signal pins.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±24-kV contact and ±30-kV air gap. An ESD-surge clamp diverts the current to ground.

6.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

6.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 4.5 A and 67W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

6.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.77 pF (typical) and 0.95 pF (maximum).

6.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±8.3 V typical. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±5.5 V.

6.3.6 Low Leakage Current

The I/O pins feature an low leakage current of 10 nA (maximum) with a bias of ±2.5 V.

6.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 24 V (TLP I_{PP} = 16 A).

6.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

6.3.9 Industry Standard Footprint

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

6.4 Device Functional Modes

The ESD401 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±24 kV (contact) or ±30 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD401 (usually within 10s of nano-seconds) the device reverts to passive.

Figure 6-1 shows typical TLP behavior of bi-directional ESD device that does not exhibit snapback.

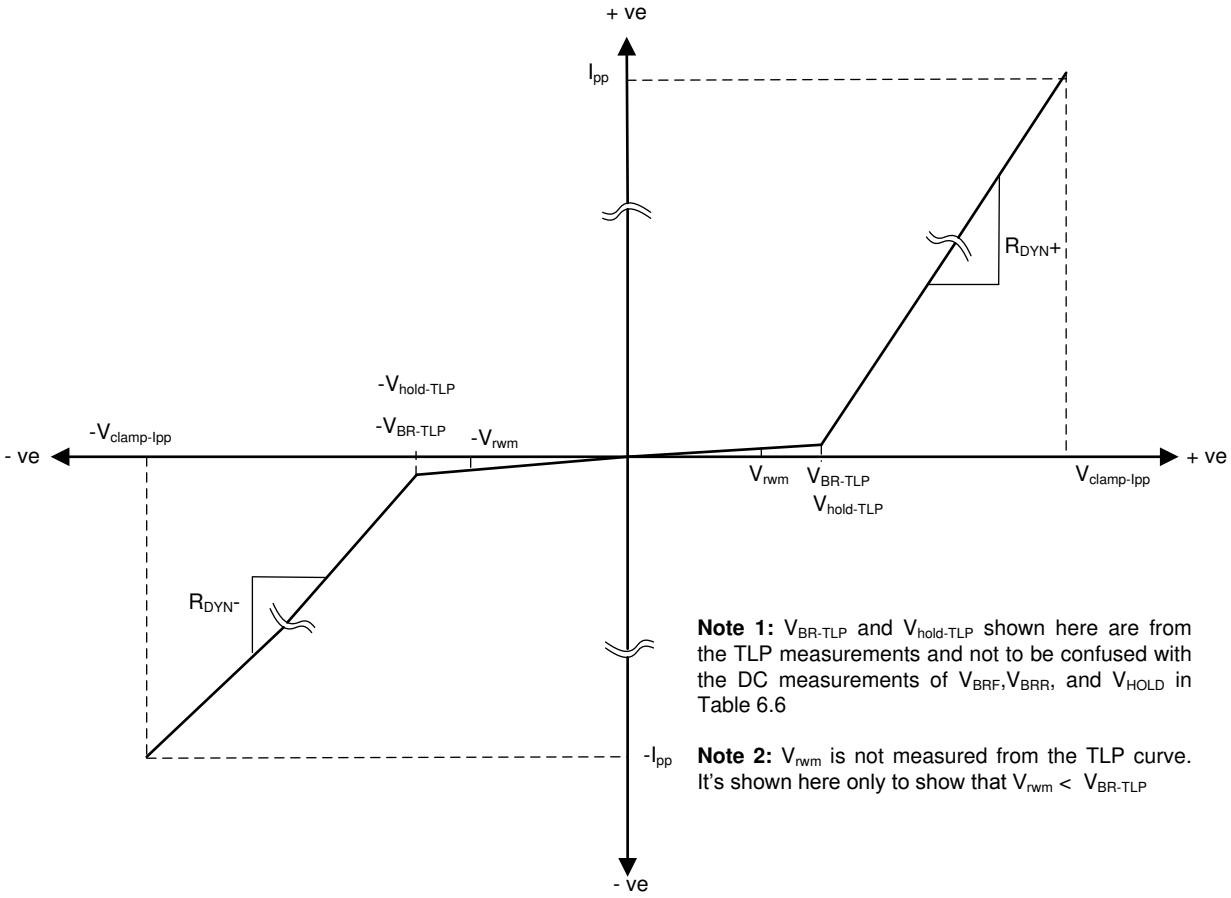


Figure 6-1. Typical TlpLP Behavior Of Bi-directional ESD Device that Does Not Exhibit Snapback

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESD401 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

7.2 Typical Application

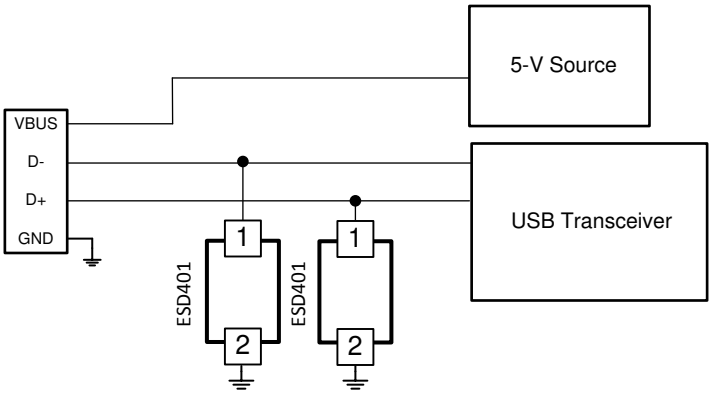


Figure 7-1. USB 2.0 ESD Schematic

7.2.1 Design Requirements

For this design example, two ESD401 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in Table 7-1 are known.

Table 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz or 480 Mbps

7.2.2 Detailed Design Procedure

7.2.2.1 Signal Range

The ESD401 supports signal ranges between –5.5 V and 5.5 V, which supports the USB 2.0 signal range of 0 to 3.6 V on the DM/DP lines..

7.2.2.2 Operating Frequency

The ESD401 has a 0.85 pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

7.2.3 Application Curves

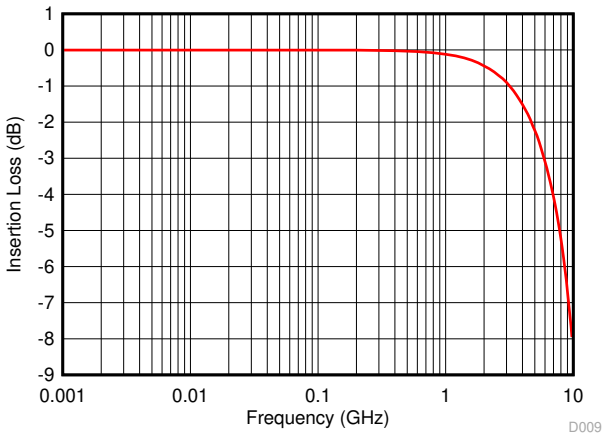


Figure 7-2. Insertion Loss

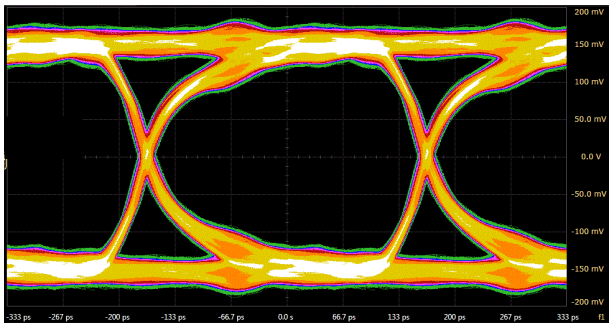


Figure 7-3. Eye Diagram - 3-Gbps Signal No Device

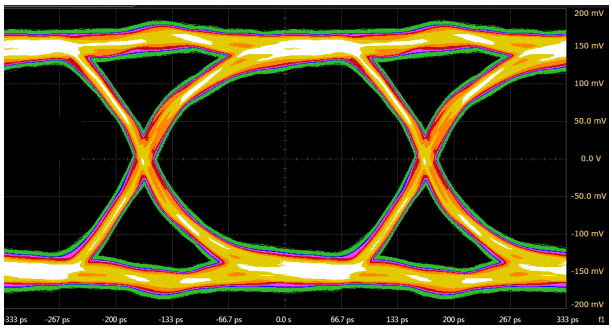


Figure 7-4. Eye Diagram - 3-Gbps Signal With ESD401

7.3 Power Supply Recommendations

The ESD401 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–5.5 V to 5.5 V) to ensure the device functions properly.

7.4 Layout

7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

7.4.2 Layout Example

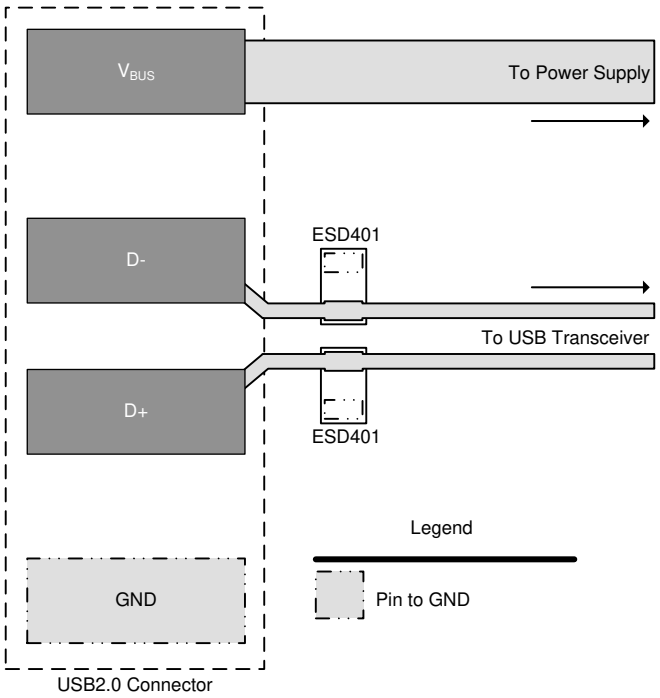


Figure 7-5. USB 2.0 ESD Layout

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2017) to Revision B (August 2024)	Page
• Updated Tape and Reel Information	14

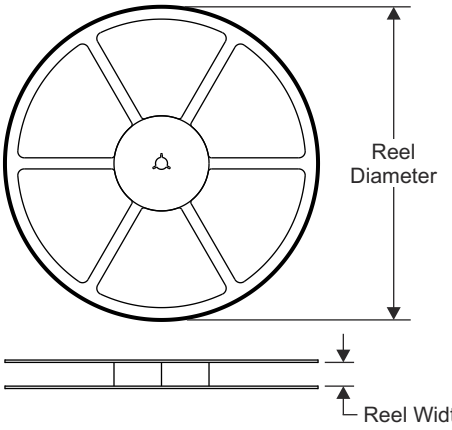
Changes from Revision * (July 2017) to Revision A (July 2017)	Page
• Updated Figure 5-9 andFigure 7-2	6

10 Mechanical, Packaging, and Orderable Information

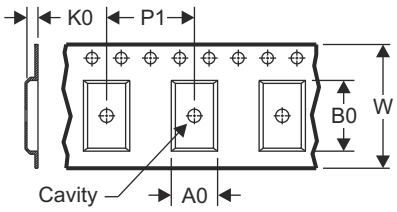
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

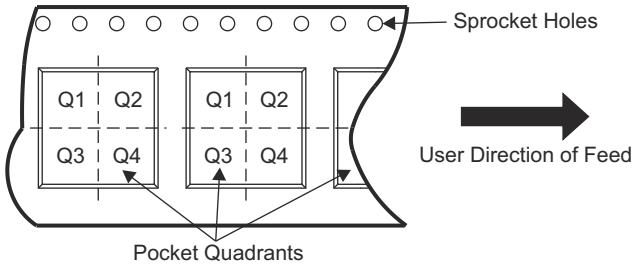


TAPE DIMENSIONS



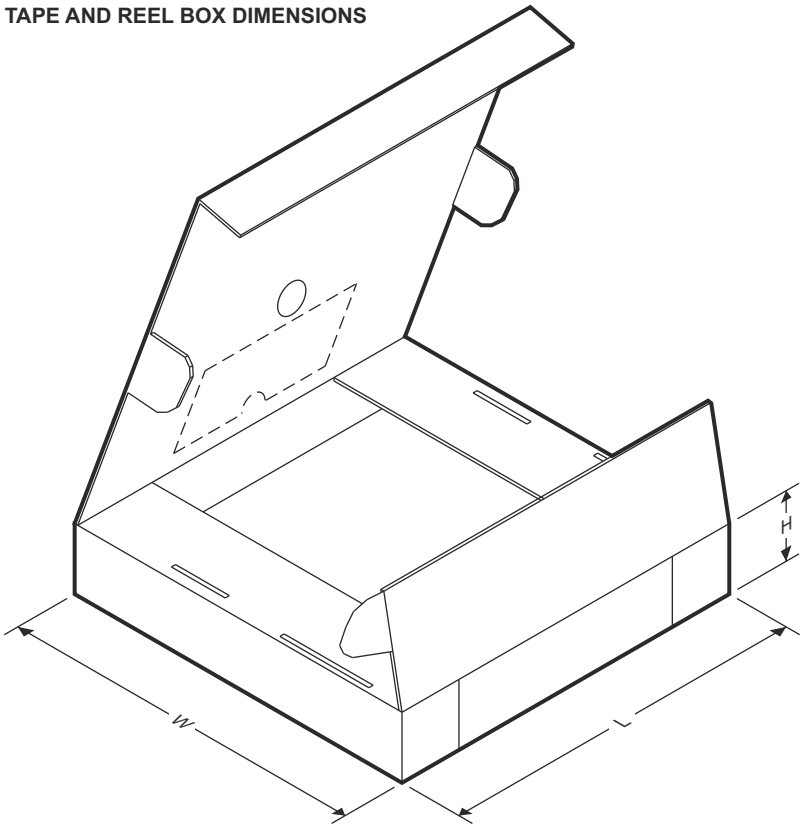
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD401DPYR	X1SON	DPY	2	10,000	180.00	8.400	0.67	1.15	0.46	2.0	8.000	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD401DPYR	X1SON	DPY	2	10,000	185.000	210.000	35.000

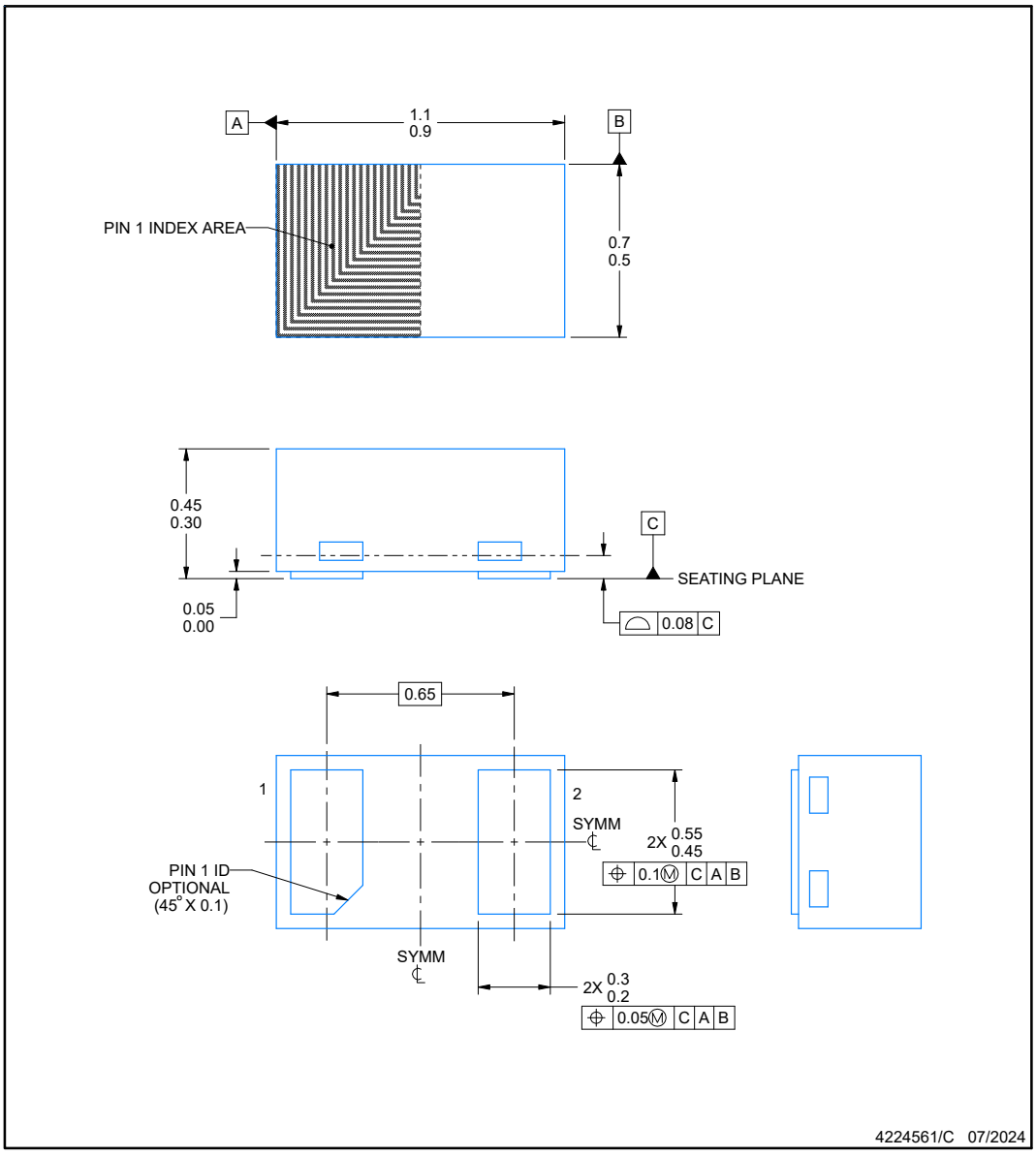
11 Mechanical Data

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



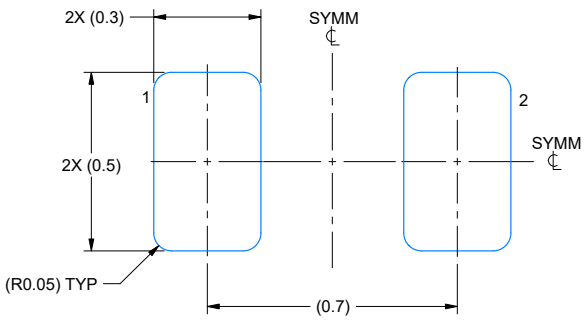
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

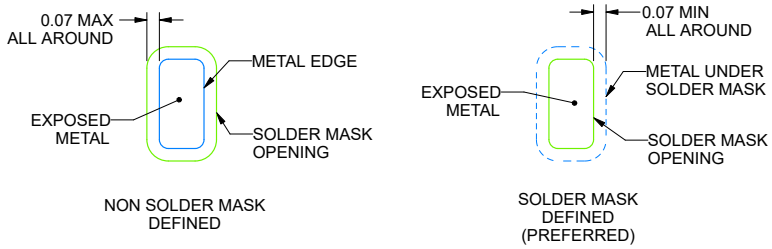
EXAMPLE BOARD LAYOUT

DPY0002A — **X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

4224561/C 07/2024

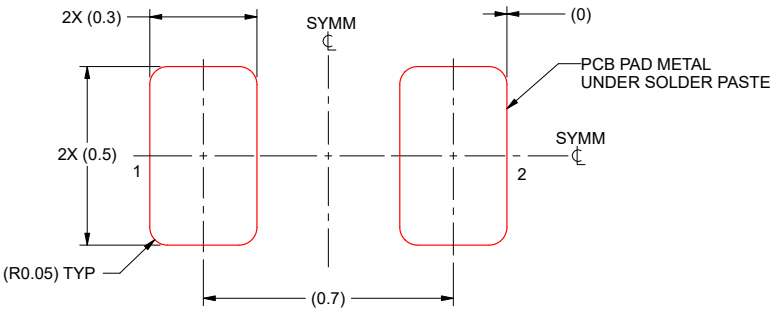
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A — **X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD401DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

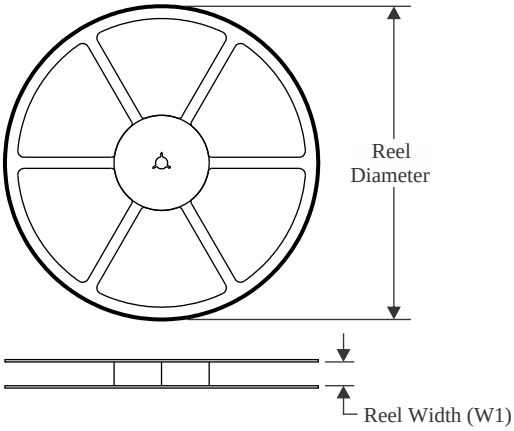
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

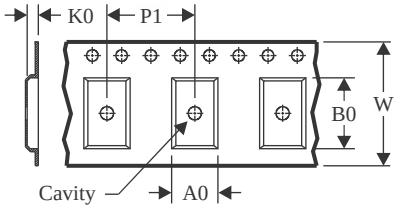
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

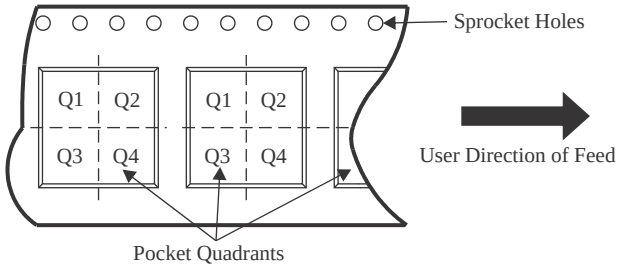


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

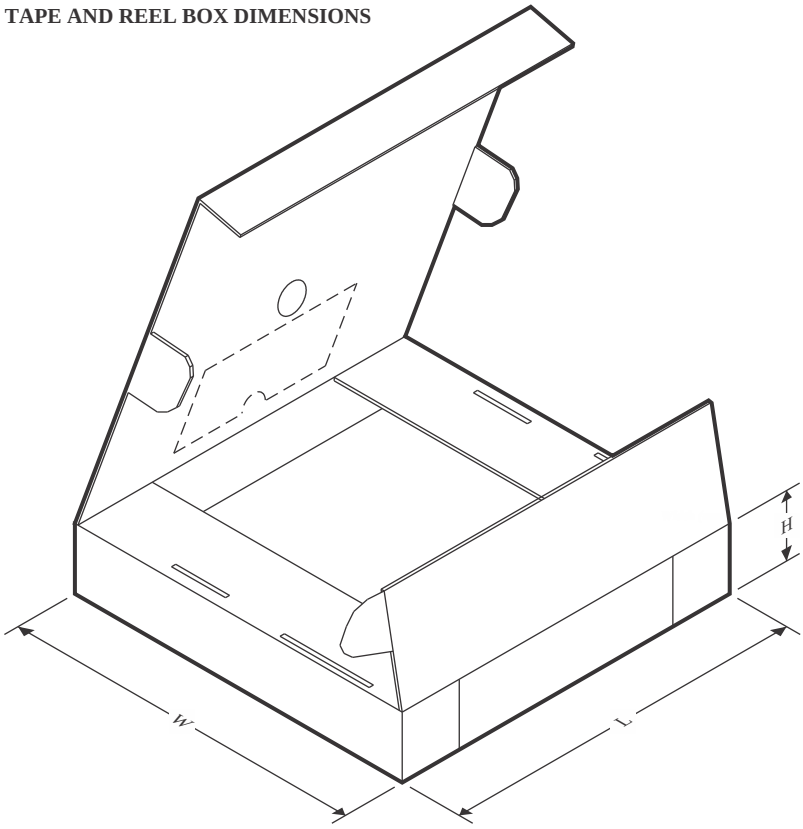
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD401DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD401DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

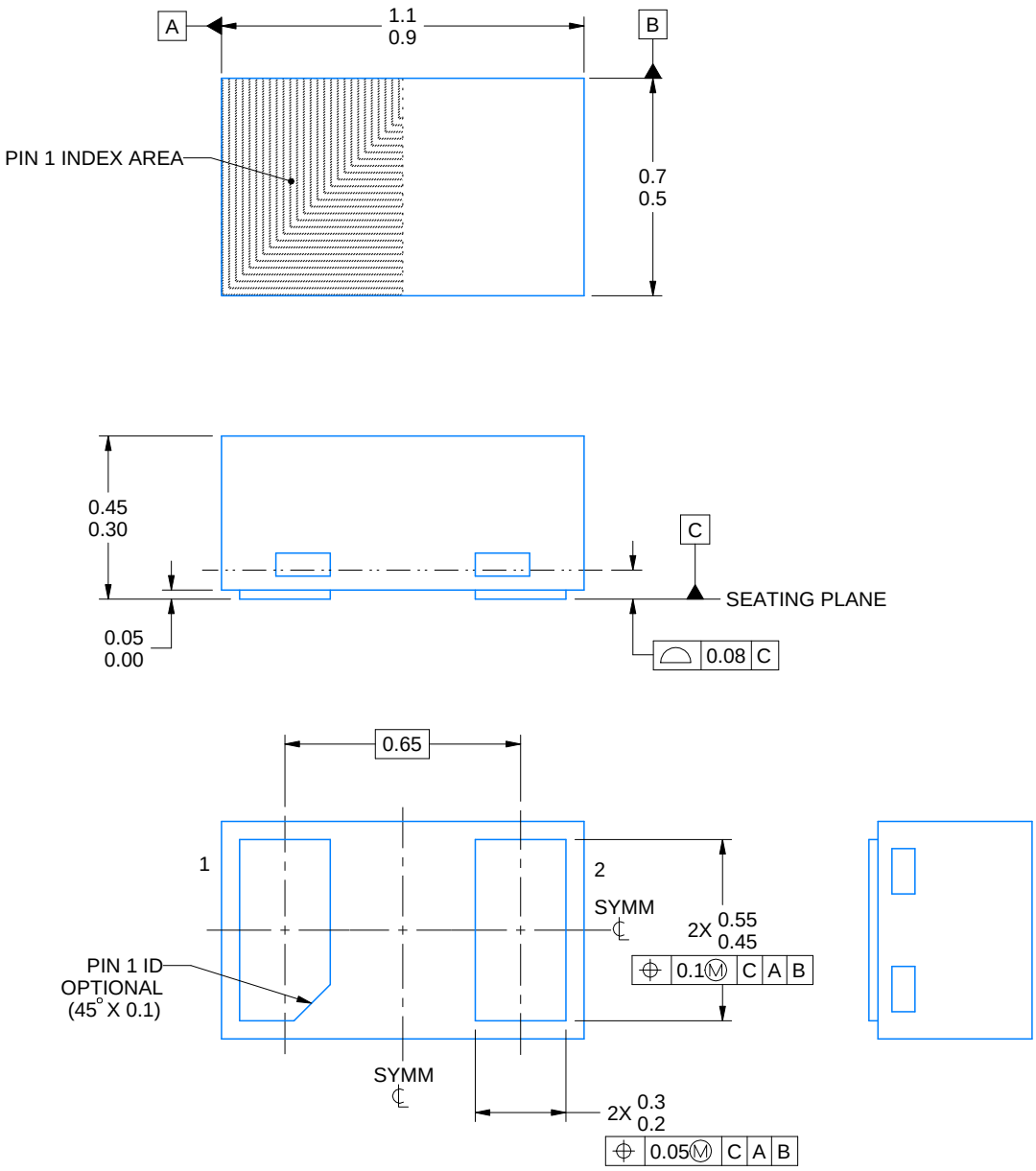
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

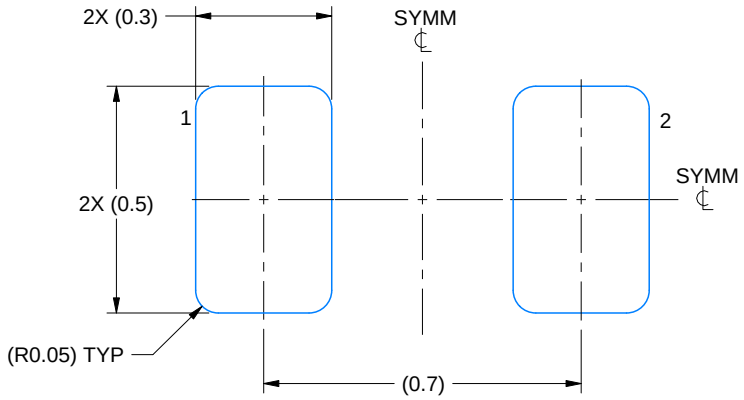
PLASTIC SMALL OUTLINE - NO LEAD



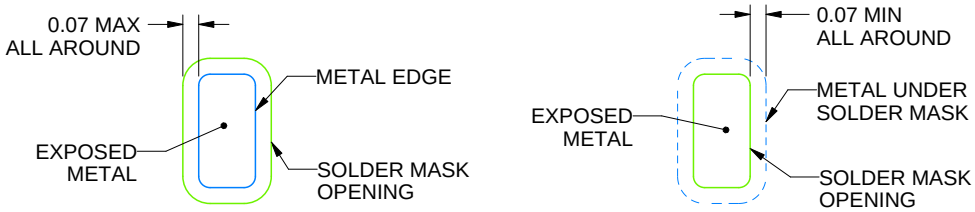
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

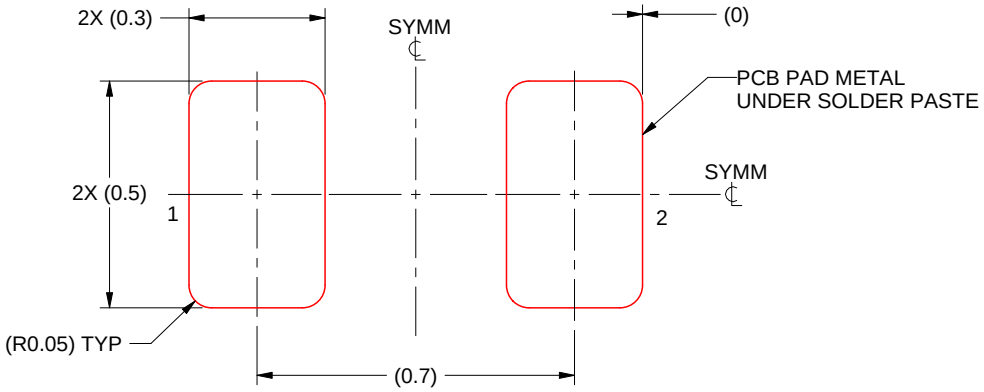


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265