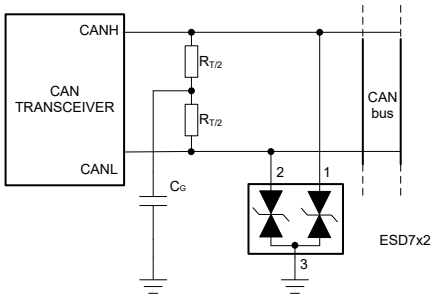
ESD772 24V, 2-Channel ESD Protection Diode in DFN1110 Industry Standard Package for In-Vehicle Networks

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±23kV contact discharge
  - ±23kV air-gap discharge
- Tested in compliance to IEC 61000-4-5
- 24V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 2pF (typical)
- DFN1110 (DXA) small, standard, common footprint

2 Applications

- Automotive in-vehicle networks:
  - Controller area network (CAN)
  - Controlled area network flexible data-rate (CAN-FD)
  - Low, fault tolerant CAN
  - High-speed CAN
- Industrial control networks:
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4



ESD7x2 Typical Application

3 Description

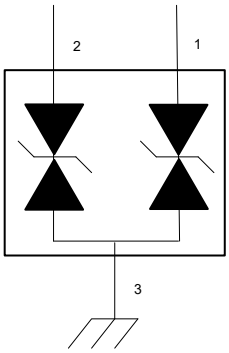
ESD772 is a bidirectional ESD protection diode for Controller Area Network (CAN) interface protection. ESD772 is rated to dissipate contact ESD strikes specified in the IEC 61000-4-2 standard. The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key as automotive systems require a high level of robustness and reliability for safety applications.

This device features a low IO capacitance per channel and a pin-out to suit two automotive CAN bus lines (CANH and CANL) from the damage caused by ElectroStatic Discharge (ESD) and other transients. Additionally, the 2pF (typical) line capacitance of ESD772 is suitable for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10Mbps.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
ESD772	DXA (DFN1110, 3)	1.1mm × 1.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

4 Pin Configuration and Functions

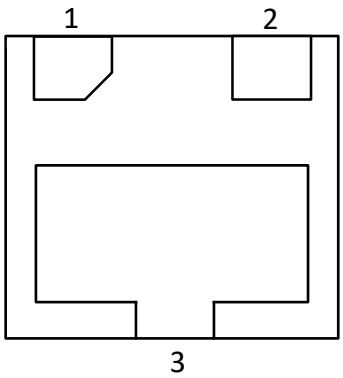


Figure 4-1. DXA Package, 3-Pin DFN1110 (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20µs) at 25°C		133	W
	IEC 61000-4-5 current (t_p - 8/20µs) at 25°C		3	A
T_A	Operating free-air temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002	± 1000	

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±23000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±23000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

5.5 Thermal Information

THERMAL METRIC(1)		ESD772 DXA (DFN1110-3) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	318.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	164.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	163.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		–24		24	V
V_{BR}	Breakdown voltage	I_{IO} = 10mA, both Positive and Negative	25.5		35.5	V
I_{LEAK}	Leakage current, any IO pin to GND	V_{IO} = ±24V	-20	1	20	nA
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 3A, t_p = 8/20µs, from IO to GND		37		V
	Clamping voltage(3)	I_{PP} = 16A, TLP, from IO to GND		42		
R_{DYN}	Dynamic resistance(3)	IO to GND		0.61		Ω
		GND to IO		0.61		
C_L	Line capacitance, any IO to GND	V_{IO} = 0V, f = 1MHz, V_{p-p} = 30mV		2		pF

(1) Measurements made on both IO channels
(2) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

5.7 Typical Characteristics

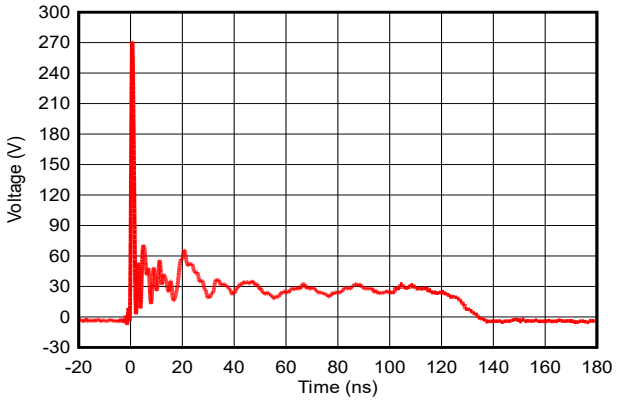


Figure 5-1. +8kV Clamped IEC Waveform

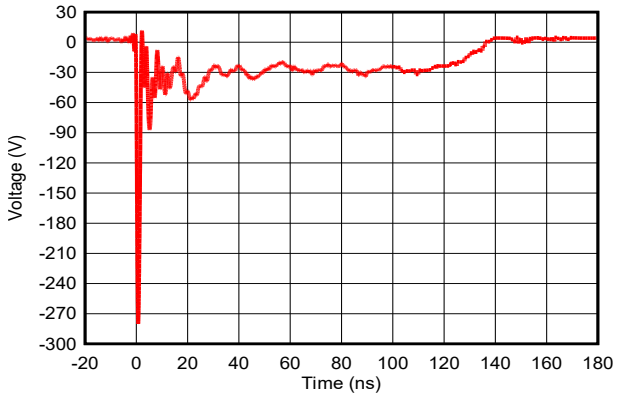


Figure 5-2. -8kV Clamped IEC Waveform

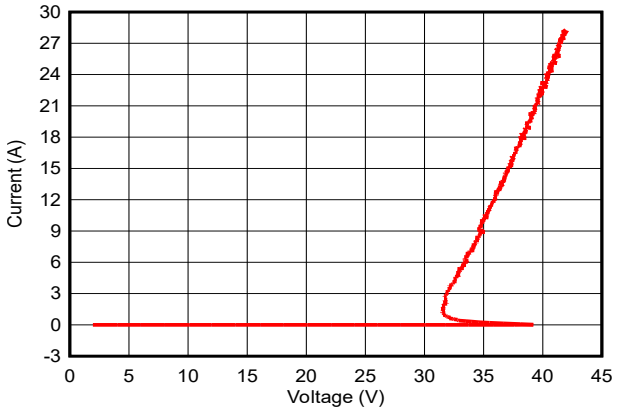


Figure 5-3. Positive TLP Curve

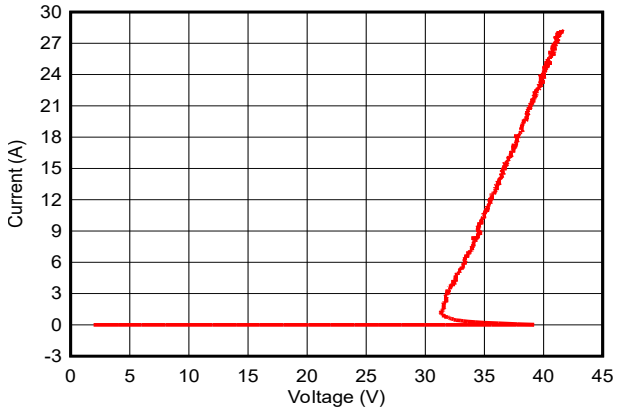


Figure 5-4. Negative TLP Curve

5.7 Typical Characteristics (continued)

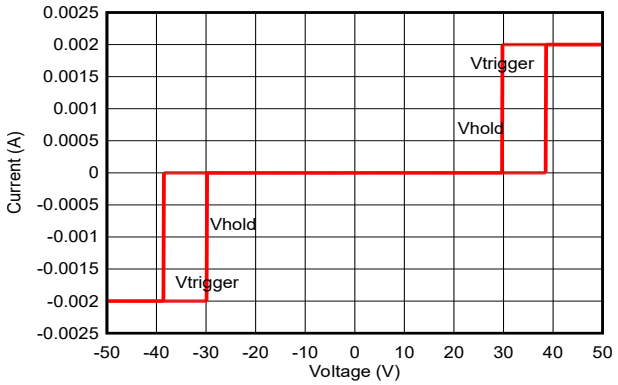


Figure 5-5. DC I-V Curve

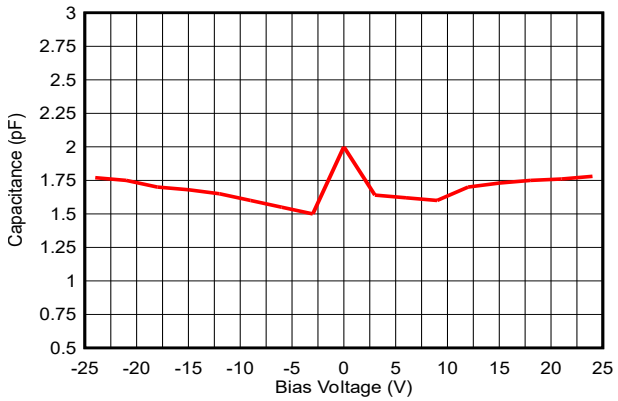


Figure 5-6. Bias Voltage vs. Capacitance

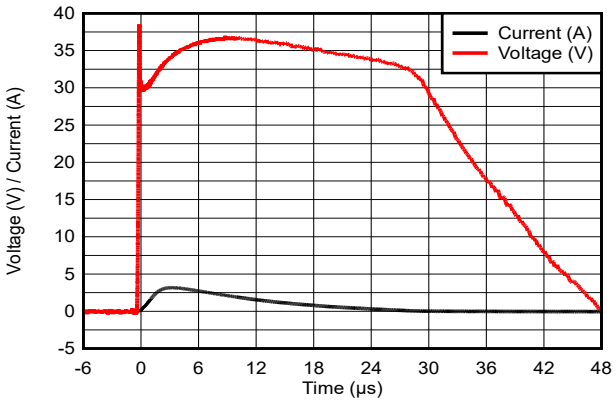


Figure 5-7. 8/20µs Surge Response

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD772 is a dual channel TVS diode which is used to provide a path to ground for dissipating ESD events on differential CAN signal lines. The CAN signal lines are typically routed throughout the automobile to connect between the different ECUs. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

6.1.1 Typical Application

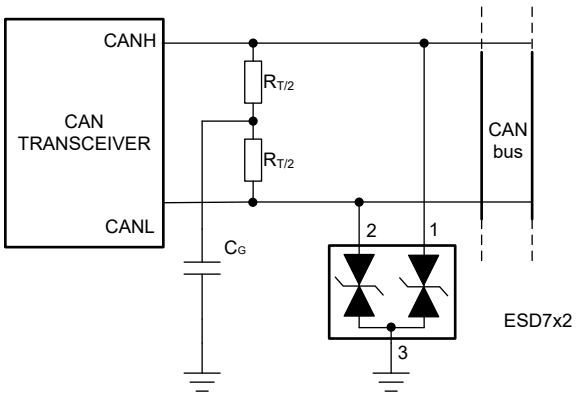


Figure 6-1. ESD7x2 Typical Application

7 Layout

7.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

7.2 Layout Example

This example is typical of a dual channel differential data pair application, such as CAN.

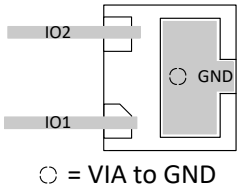


Figure 7-1. Routing with DXA Package

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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