INA114 Precision Instrumentation Amplifier

1 Features

- Low offset voltage: 50µV maximum for high gains
- Low drift: 0.3µV/°C maximum for high gains
- Low input bias current: 2nA maximum
- High common-mode rejection: 115dB minimum
- Input over-voltage protection: ±40V
- Wide supply range: ±2.25V to ±18V
- Packages: PDIP-8 and SOIC-16

2 Applications

- Surgical equipment
- Actuator
- Multifunction relay
- Train control and management
- Trackside signaling and control

3 Description

The INA114 is a low-cost, general-purpose instrumentation amplifier offering excellent accuracy. The versatile three-op-amp design and small size make this device an excellent choice for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection withstands up to ±40V without damage.

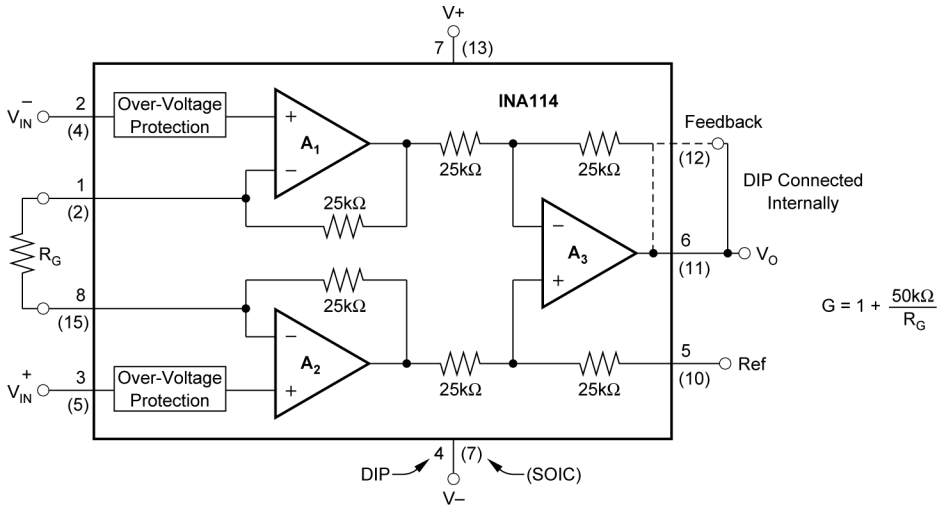
The INA114 is laser trimmed for very low offset voltage (50µV), low drift (0.3µV/°C), and high common-mode rejection (115dB at G = 1000). The device operates with power supplies as low as ±2.25V, allowing use in battery-operated and single 5V supply systems.

The INA114 is available in 8-pin PDIP and 16-pin SOIC surface-mount packages. Both are specified for a temperature range of −40°C to +85°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA114	P (PDIP, 8)	9.81mm × 9.43mm
	DW (SOIC, 16)	10.3mm × 10.3mm

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Schematic

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4 Pin Configuration and Functions

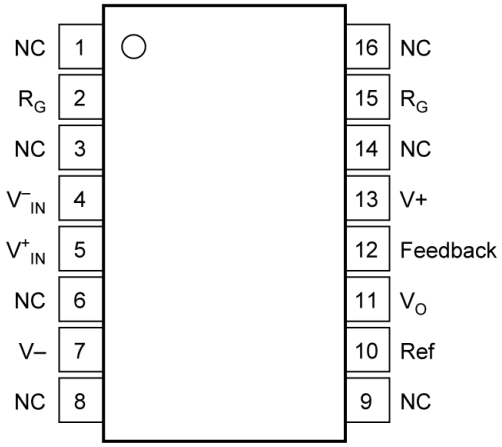


Figure 4-1. DW Package, 16-Pin SOIC (Top View)

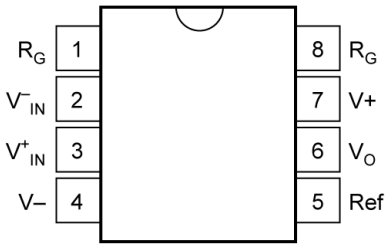


Figure 4-2. P Package, 8-Pin PDIP (Top View)

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 7.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$		36	V
		Dual supply, $V_S = (+V_S) – (–V_S)$	–18	18	
	Signal input pins		–40	40	V
V_O	Signal output voltage		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
I_S	Output short-circuit (to $V_S/2$)		Continuous		
T_A	Operating temperature		–40	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–40	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$	4.5	36	V
		Dual supply, $V_S = (+V_S) – (–V_S)$	±2.25	±18	
T_A	Specified temperature		–40	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA114		UNIT
		DW (SOIC)	P (PDIP)	
		16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	110.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ, V_{REF} = 0V, G = 1, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage	RTI	INA114BP, BU			±10 + 20/G	±50 + 150/G	µV
			INA114AP, AU			±25 + 30/G	±125 + 500/G	
	Offset voltage drift	T_A = –40°C to +85°C, RTI	INA114BP, BU			±0.1 + 0.5/G	±0.3 + 5/G	µV/°C
			INA114AP, AU			±0.25 + 5/G	±1 + 10/G	
	Long-term stability					±0.2 + 0.5/G		µV/mo
	Differential impedance					100 || 6		GΩ || pF
	Common-mode impedance					100 || 6		GΩ || pF
	Operating input voltage				(V–) + 4		(V+) – 4	V
PSRR	Power-supply rejection ratio	RTI, ±2.25V to ±18V				0.5 + 2/G	3 + 10/G	µV/V
CMRR	Common-mode rejection ratio	At dc to 60Hz, RTI, V_{CM} = ±10V, ΔR_S = 1kΩ	G = 1	INA114BP, BU	80	96		dB
				INA114AP, AU	75	90		
			G = 10	INA114BP, BU	96	115		
				INA114AP, AU	90	106		
			G = 100	INA114BP, BU	110	120		
				INA114AP, AU	106	110		
			G = 1000	INA114BP, BU	115	120		
				INA114AP, AU	106	110		
BIAS CURRENT								
I_B	Input bias current	V_{CM} = V_S / 2	INA114BP, BU			±0.5	±2	nA
			INA114AP, AU			±0.5	±5	
	Input bias current drift	T_A = –40°C to +85°C	INA114BP, BU			±8		pA/°C
			INA114AP, AU			±8		
I_{OS}	Input offset current	V_{CM} = V_S / 2	INA114BP, BU			±0.5	±2	nA
			INA114AP, AU			±0.5	±5	
	Input offset current drift	T_A = –40°C to +85°C	INA114BP, BU			±8		pA/°C
			INA114AP, AU			±8		
NOISE VOLTAGE								
	Voltage noise	G = 1000, R_S = 0Ω	CSO: SHE	f = 10Hz		15		nV/√Hz
				f = 100Hz		11		
				f = 1kHz		11		
			CSO: TID	f = 10Hz to 1kHz		7		
			CSO: SHE	f_B = 0.1Hz to 10Hz		0.4		$µV_{PP}$
			CSO: TID	f_B = 0.1Hz to 10Hz		0.45		
	Noise current	f = 10Hz				0.4		pA/√Hz
		f = 1kHz				0.2		
		f_B = 0.1Hz to 10Hz				18		pA_{PP}

5.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ, V_{REF} = 0V, G = 1, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
GAIN								
G	Gain equation					1 + (50kΩ / R_G)		V/V
	Range of gain				1		10000	V/V
GE	Gain error	V_O = ±10V, G = 1				±0.01	±0.05	%
		V_O = ±10V	G = 10	INA114BP, BU		±0.02	±0.4	
				INA114AP, AU		±0.02	±0.5	
			G = 100	INA114BP, BU		±0.05	±0.5	
				INA114AP, AU		±0.05	±0.7	
			G = 1000	INA114BP, BU		±0.5	±1	
				INA114AP, AU		±0.5	±2	
	Gain drift					±2	±10	ppm/°C
		R_S = 50kΩ(1)				±25	±100	
	Gain nonlinearity	V_O = –10V to +10V	G = 1	INA114BP, BU		±0.0001	±0.001	% of FSR
				INA114AP, AU		±0.0001	±0.002	
			G = 10, 100	INA114BP, BU		±0.0005	±0.002	
				INA114AP, AU		±0.0005	±0.004	
			G = 1000	INA114BP, BU		±0.002	±0.01	
				INA114AP, AU		±0.002	±0.02	
OUTPUT								
	Output voltage	I_O = 5mA, T_A = –40°C to 85°C			(V–) +1.5		(V+) –1.5	V
			V_S = ±11.4V		(V–) + 1.4		(V+) – 1.4	
			V_S = ±2.25V		(V–) +1		(V+) – 1	
	Load capacitance stability					1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2				+20 / –15		mA
FREQUENCY RESPONSE								
BW	Bandwidth, –3 dB	G = 1		CSO: SHE		1		MHz
				CSO: TID		1.5		
		G = 10		CSO: SHE		100		kHz
				CSO: TID		600		
		G = 100		CSO: SHE		10		
				CSO: TID		200		
		G = 1000		CSO: SHE		1		
				CSO: TID		30		
SR	Slew rate	G = 10, V_O = ±10V		CSO: SHE	0.3	0.6		V/µs
				CSO: TID		1.2		
t_S	Settling time	0.01%, V_{STEP} = 10V	G = 1			18		µs
			G = 10			20		
			G = 100			120		
			G = 1000			1100		
	Overload recovery	50% overdrive		CSO: TID		2		µs
				CSO: SHE		20		
POWER SUPPLY								
I_Q	Quiescent current	V_S = ±2.25V to ±18V, V_{IN} = 0V				±2.2	±3	mA

(1) Temperature coefficient of the "50kΩ" term in the gain equation.

5.6 Typical Characteristics

at T_A = +25 °C, V_S = ±15 V, G = 1 V/V, and all chip site origins (CSO), unless otherwise noted.

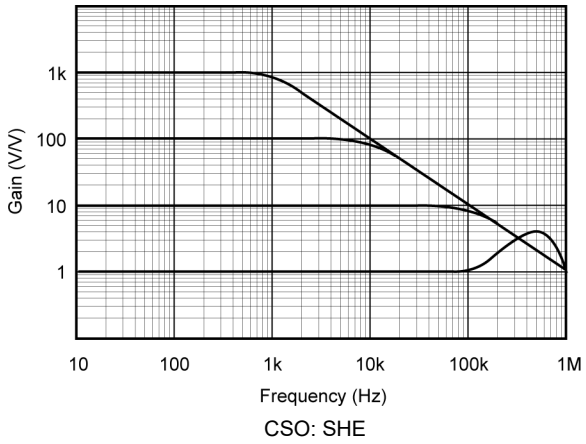


Figure 5-1. Gain vs Frequency

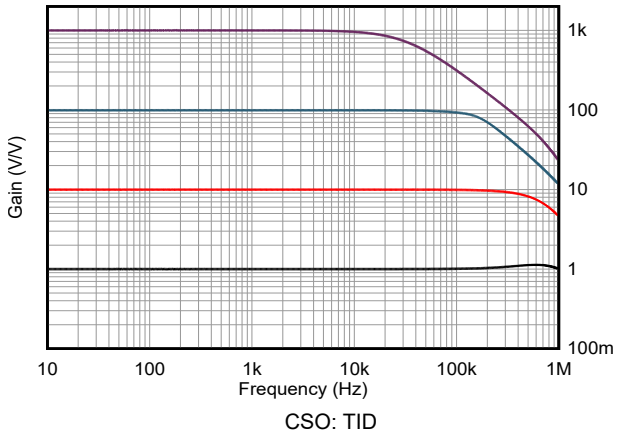


Figure 5-2. Gain vs Frequency

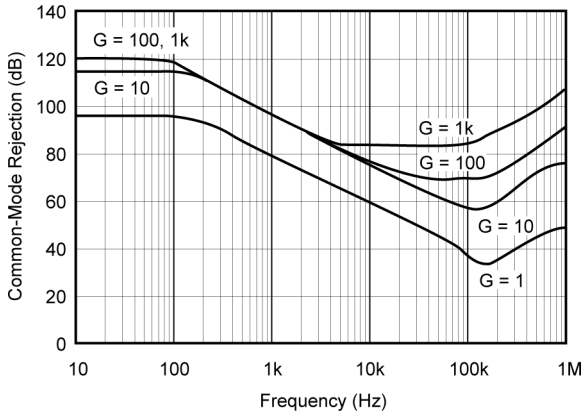


Figure 5-3. Common-mode Rejection vs Frequency

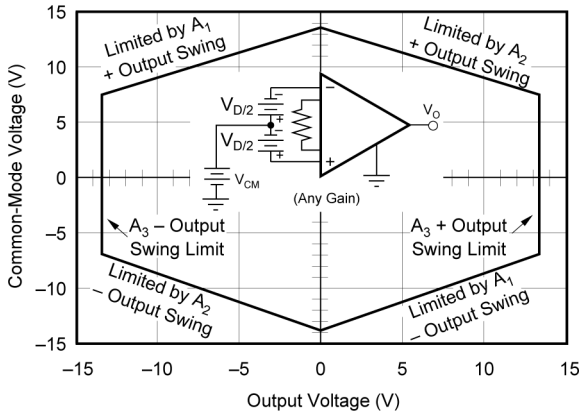


Figure 5-4. Input Common-mode Voltage Range vs Output Voltage

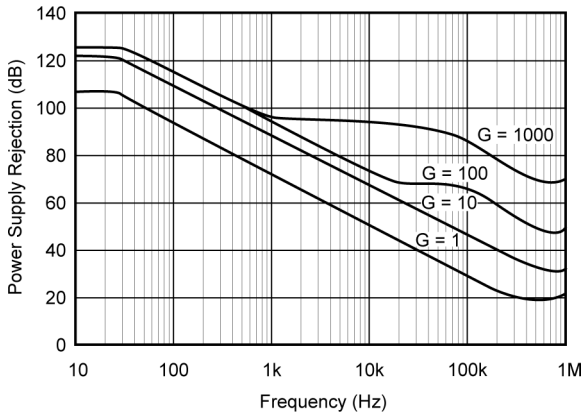


Figure 5-5. Positive Power Supply Rejection vs Frequency

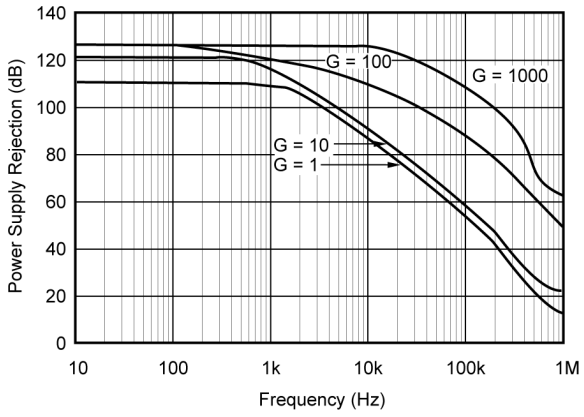
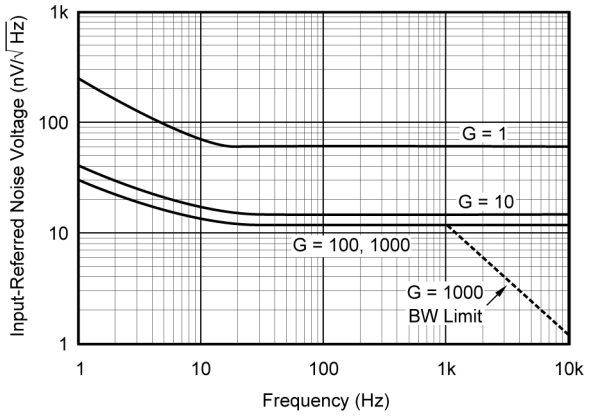


Figure 5-6. Negative Power Supply Rejection vs Frequency

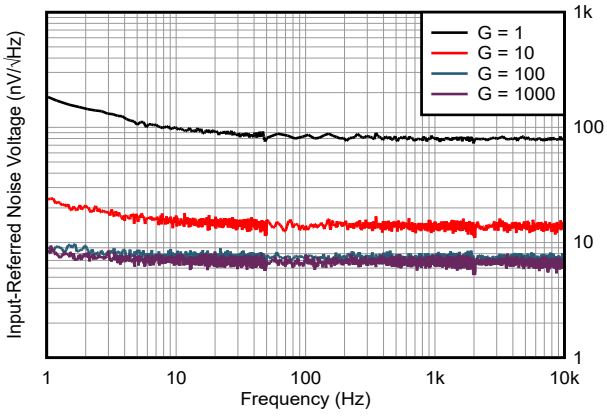
5.6 Typical Characteristics (continued)

at T_A = +25 °C, V_S = ±15 V, G = 1 V/V, and all chip site origins (CSO), unless otherwise noted.



CSO: SHE

Figure 5-7. Input-Referred Noise Voltage vs Frequency



CSO: TID

Figure 5-8. Input-Referred Noise Voltage vs Frequency

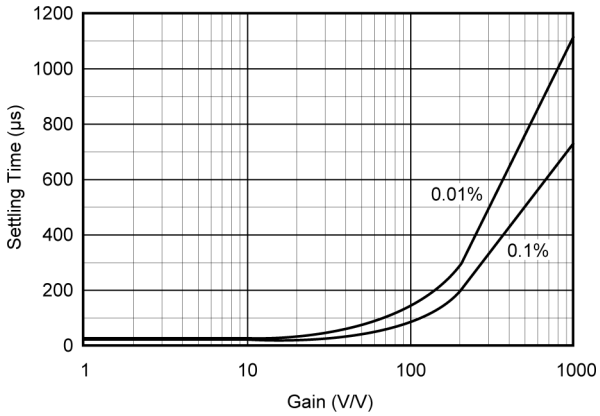


Figure 5-9. Settling Time vs Gain

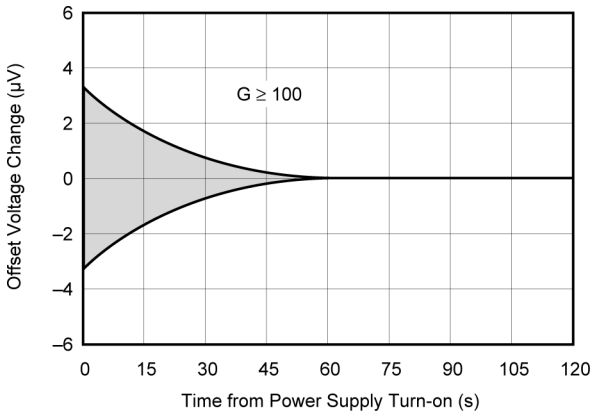


Figure 5-10. Offset Voltage Warm-up vs Time

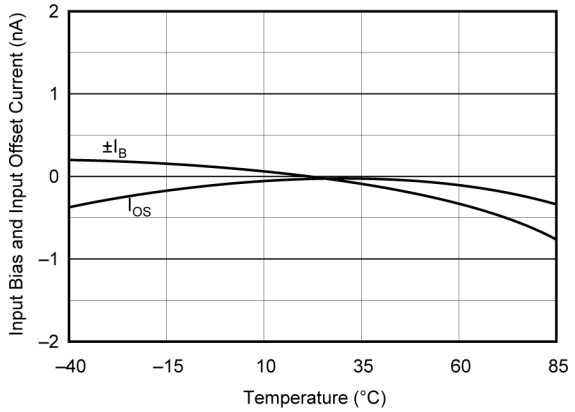
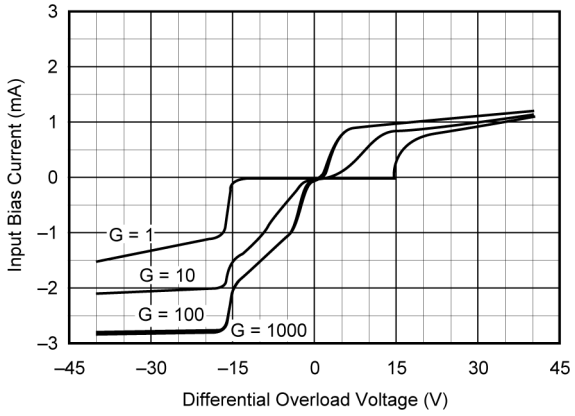


Figure 5-11. Input Bias and Input Offset Current vs Temperature

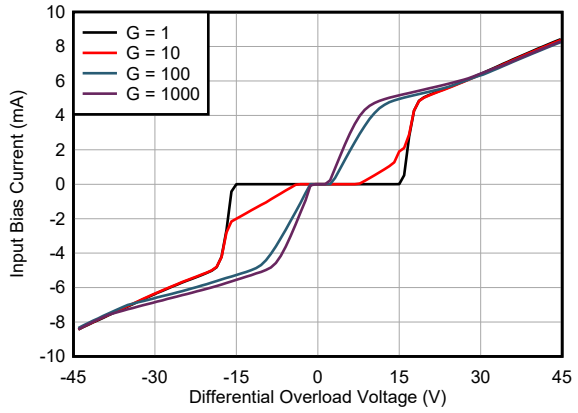


CSO: SHE

Figure 5-12. Input Bias Current vs Differential Input Voltage

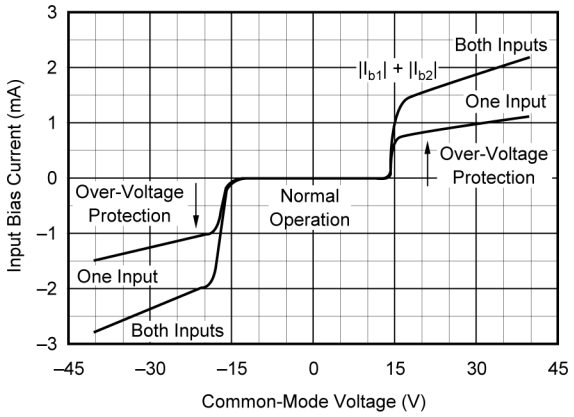
5.6 Typical Characteristics (continued)

at T_A = +25 °C, V_S = ±15 V, G = 1 V/V, and all chip site origins (CSO), unless otherwise noted.



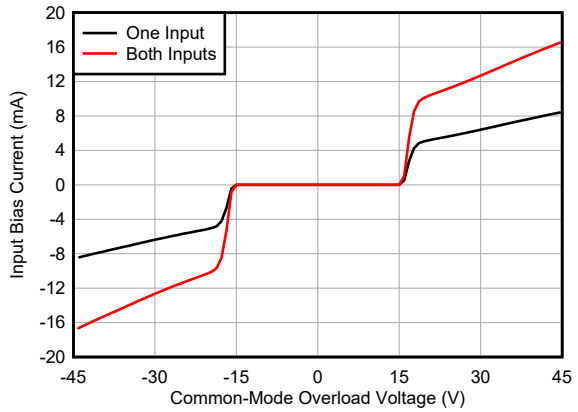
CSO: TID

Figure 5-13. Input Bias Current vs Differential Input Voltage



CSO: SHE

Figure 5-14. Input Bias Current vs Common-Mode Input Voltage



CSO: TID

Figure 5-15. Input Bias Current vs Common-Mode Input Voltage

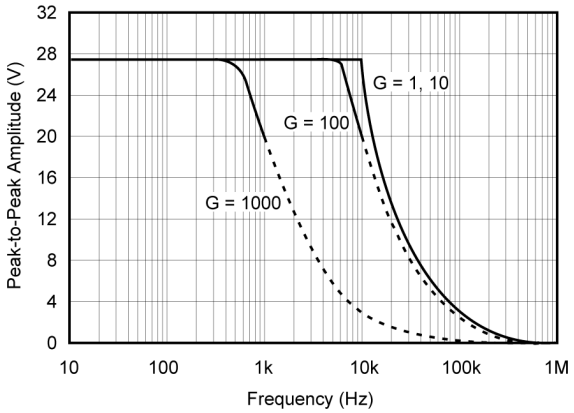


Figure 5-16. Maximum Output Swing vs Frequency

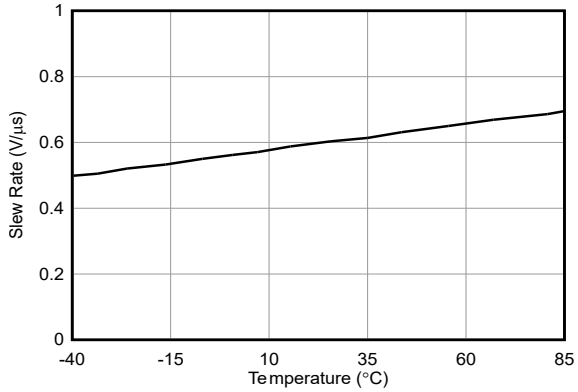


Figure 5-17. Slew Rate vs Temperature

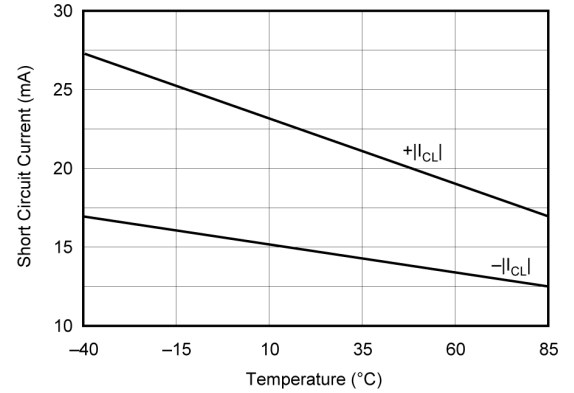


Figure 5-18. Output Current Limit vs Temperature

5.6 Typical Characteristics (continued)

at T_A = +25 °C, V_S = ±15 V, G = 1 V/V, and all chip site origins (CSO), unless otherwise noted.

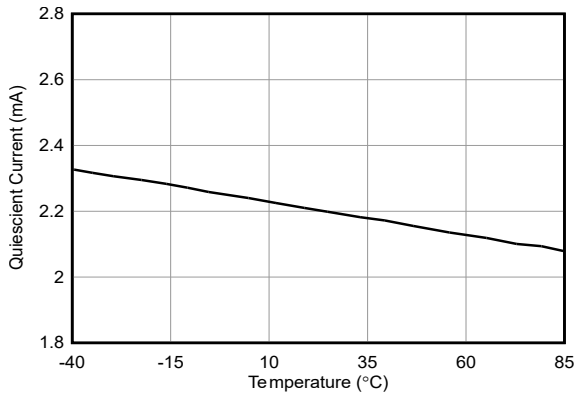


Figure 5-19. Quiescent Current vs Temperature

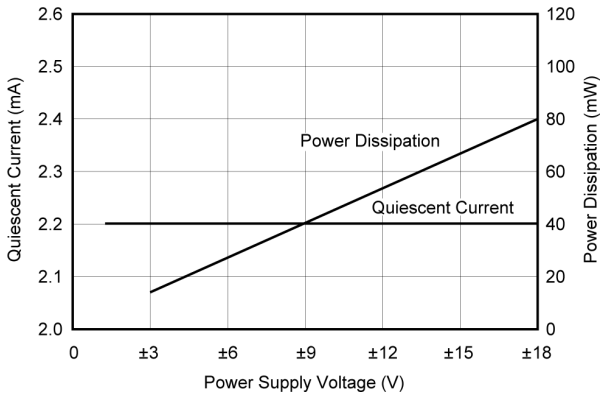
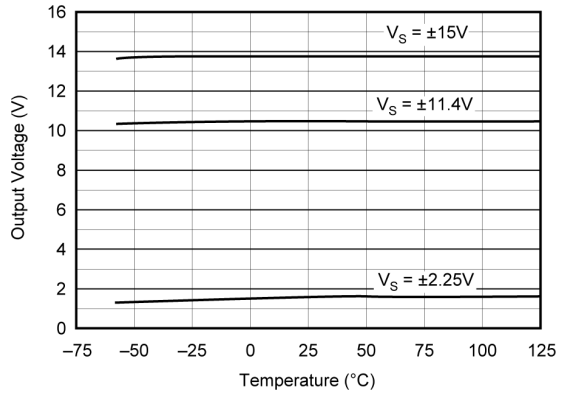
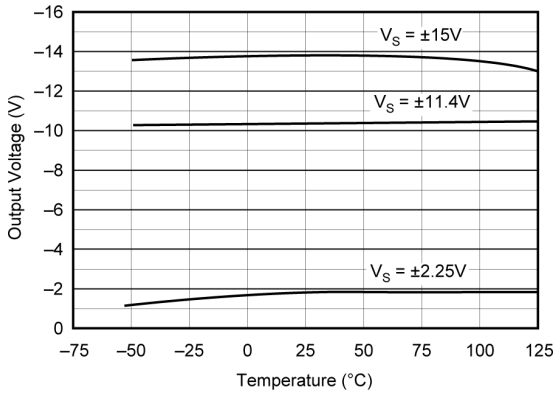


Figure 5-20. Quiescent Current and Power Dissipation vs Power Supply Voltage



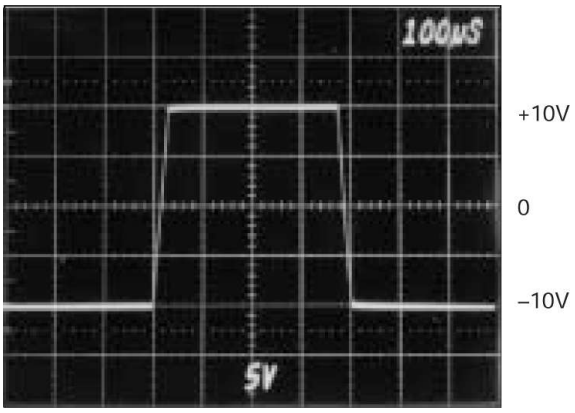
R_L = 2 kΩ

Figure 5-21. Positive Signal Swing vs Temperature



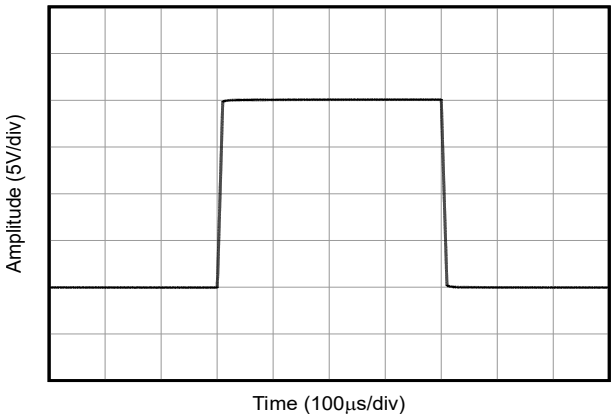
R_L = 2 kΩ

Figure 5-22. Negative Signal Swing vs Temperature



CSO: SHE G=1

Figure 5-23. Large-Signal Response

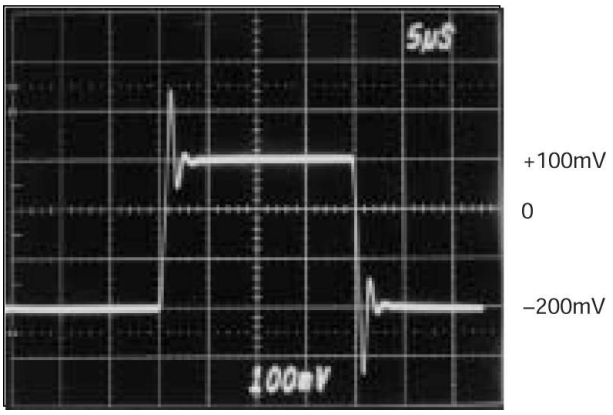


CSO: TID G=1

Figure 5-24. Large-Signal Response

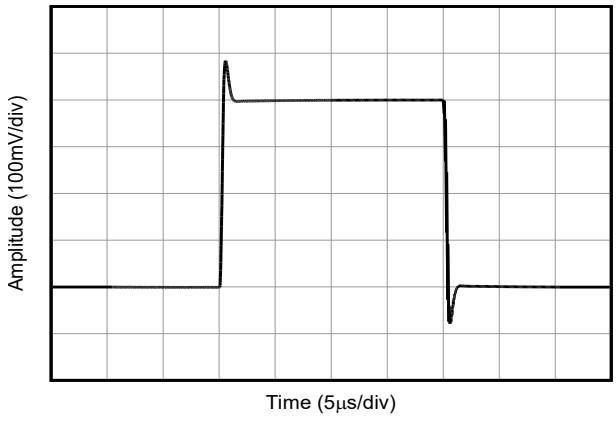
5.6 Typical Characteristics (continued)

at T_A = +25 °C, V_S = ±15 V, G = 1 V/V, and all chip site origins (CSO), unless otherwise noted.



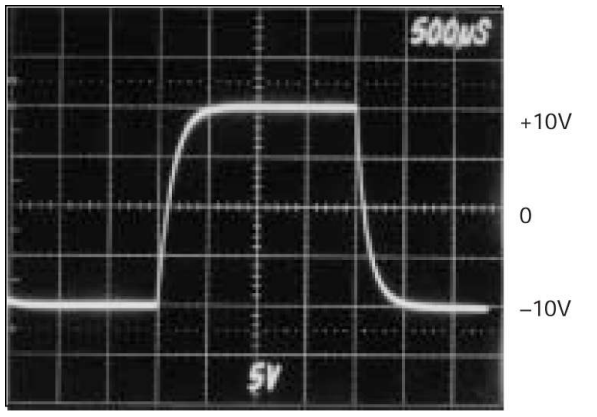
CSO: SHE G = 1

Figure 5-25. Small-Signal Response



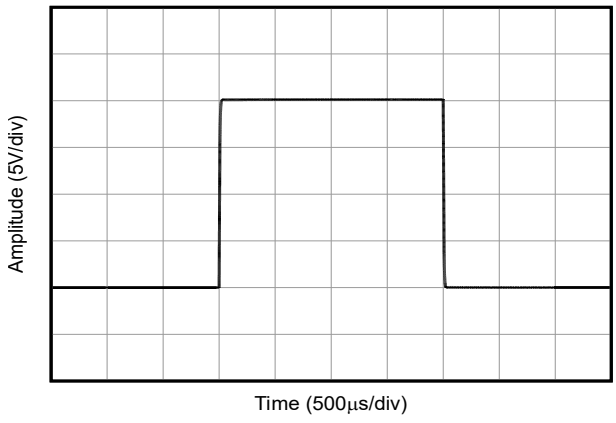
CSO: TID G=1

Figure 5-26. Small-Signal Response



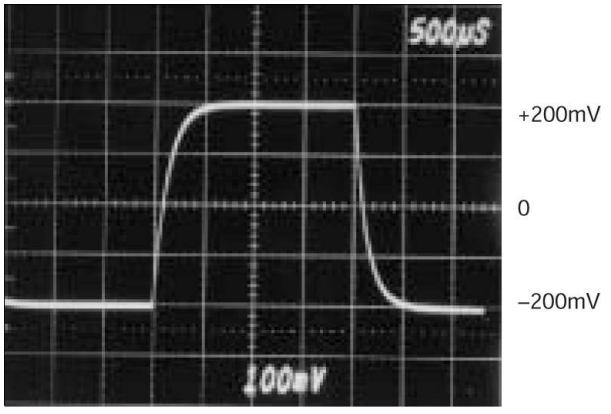
CSO: SHE G = 1000

Figure 5-27. Large-Signal Response



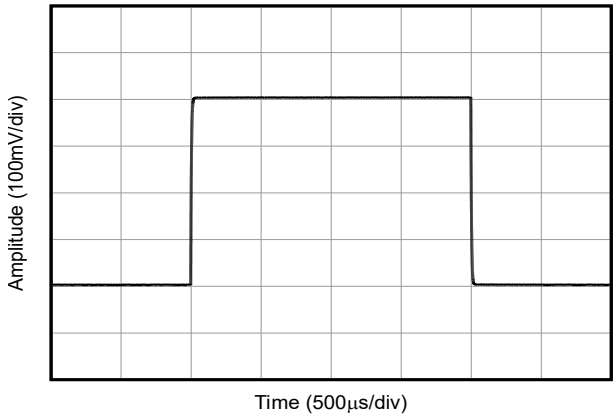
CSO: TID G=1000

Figure 5-28. Large-Signal Response



CSO: SHE G = 1000

Figure 5-29. Small-Signal Response



CSO: TID G=1000

Figure 5-30. Small-Signal Response

5.6 Typical Characteristics (continued)

at T_A = +25 °C, V_S = ±15 V, G = 1 V/V, and all chip site origins (CSO), unless otherwise noted.

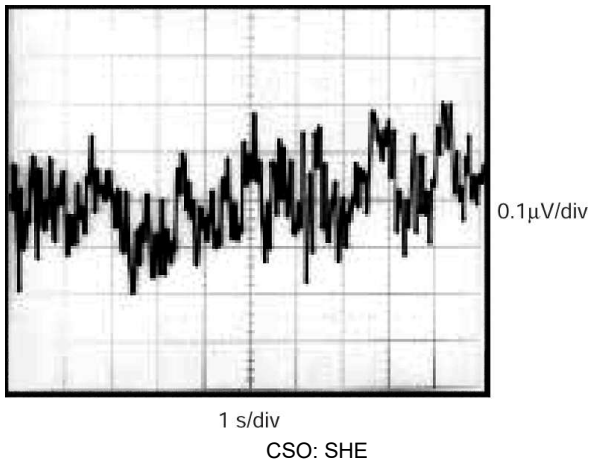


Figure 5-31. Input-Referred Noise, 0.1 Hz to 10 Hz

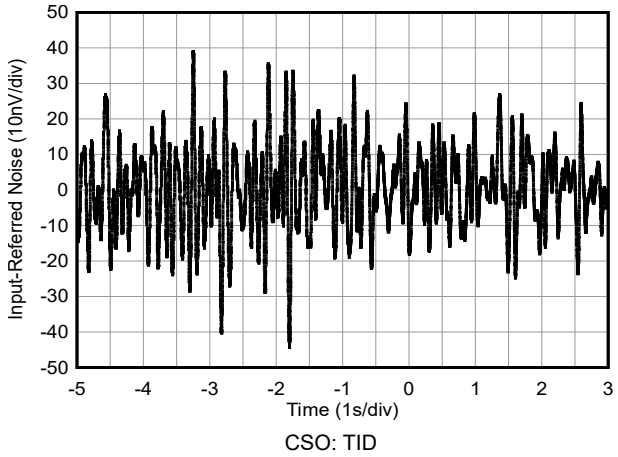


Figure 5-32. Input-Referred Noise, 0.1 Hz to 10 Hz

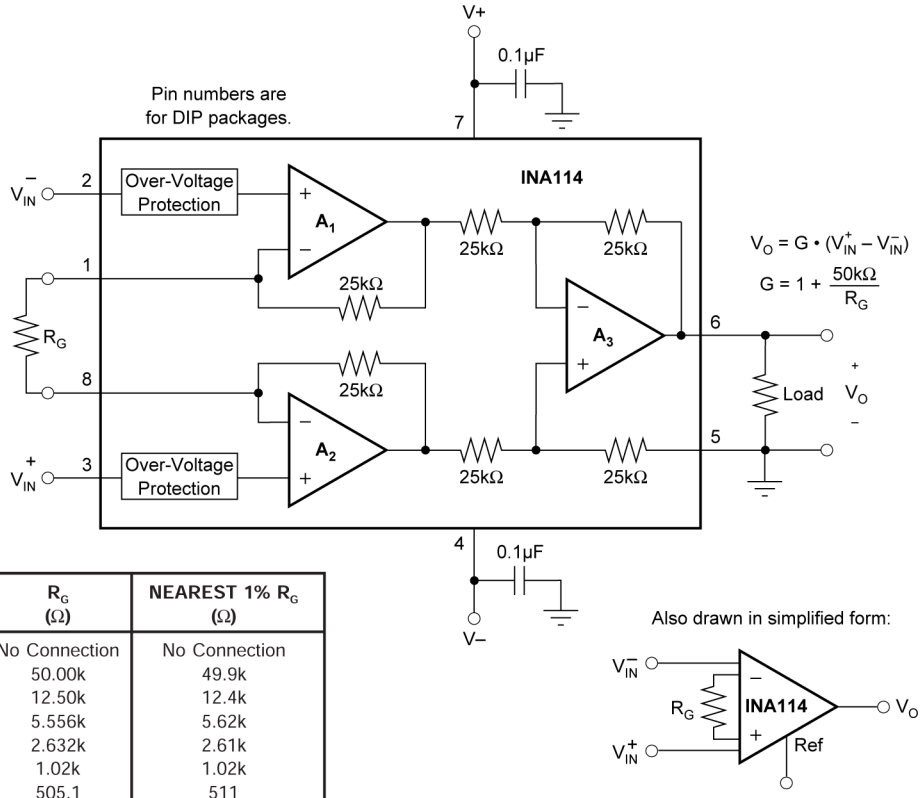
6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

Figure 6-1 shows the basic connections required for operation of the INA114. Applications with noisy or high-impedance power supplies can require decoupling capacitors close to the device pins as shown.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

Figure 6-1. Basic Connections.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to provide good common-mode rejection. A resistance of 5Ω in series with the Ref pin causes a typical device to degrade to approximately 80dB CMR (G = 1).

6.1.1 Setting the Gain

Gain of the INA114 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{50\ k\Omega}{R_G} \quad (1)$$

Figure 6-1 shows commonly used gains and resistor values.

The 50-kΩ term in Equation 1 comes from the sum of the two internal feedback resistors. These resistors are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift is directly inferred from the gain Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

6.1.2 Noise Performance

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 can provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier can provide lower noise.

Low frequency noise of the INA114 is approximately 0.4μV_{PP} measured from 0.1Hz to 10Hz. This noise is approximately one-tenth the noise of *low noise* chopper-stabilized amplifiers.

6.1.3 Offset Trimming

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 6-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref pin is summed at the output. Maintain low impedance at this node to maintain good common-mode rejection by buffering trim voltage with an op amp as shown.

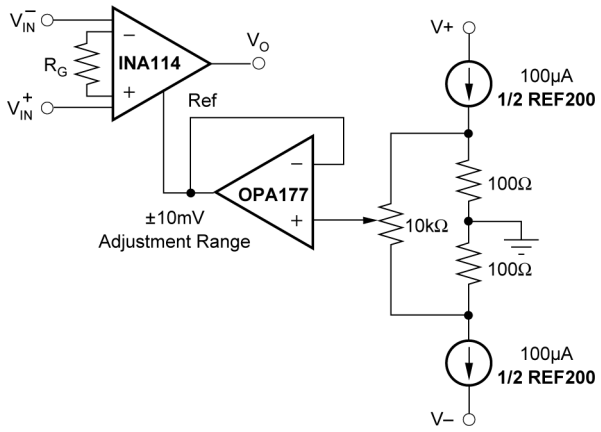


Figure 6-2. Optional Trimming of Output Offset Voltage.

6.1.4 Input Bias Current Return Path

The input impedance of the INA114 is extremely high-approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA, and can be either polarity as a result of cancellation circuitry. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. Figure 6-3 shows various provisions for an input bias current path. Without a bias current return path, the inputs float to a potential that exceeds the common-mode range of the INA114 and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see thermocouple example in Figure 6-3). With higher source impedance, use two resistors to provide a balanced input, with the possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

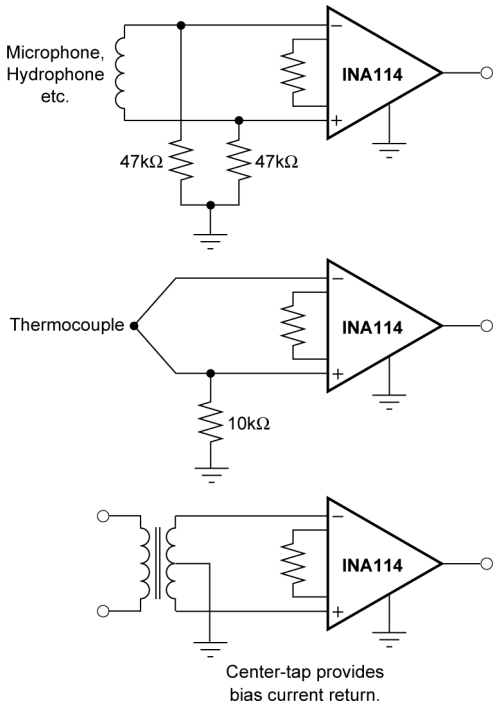


Figure 6-3. Providing an Input Common-Mode Current Path.

6.1.5 Input Common-Mode Range

The linear common-mode range of the input op amps of the INA114 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range is limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see typical characteristic curve *Input Common-Mode Range vs Output Voltage*.

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 6-4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve *Input Common-Mode Voltage Range vs Output Voltage*). If necessary, add gain after the INA114 to increase the voltage swing.

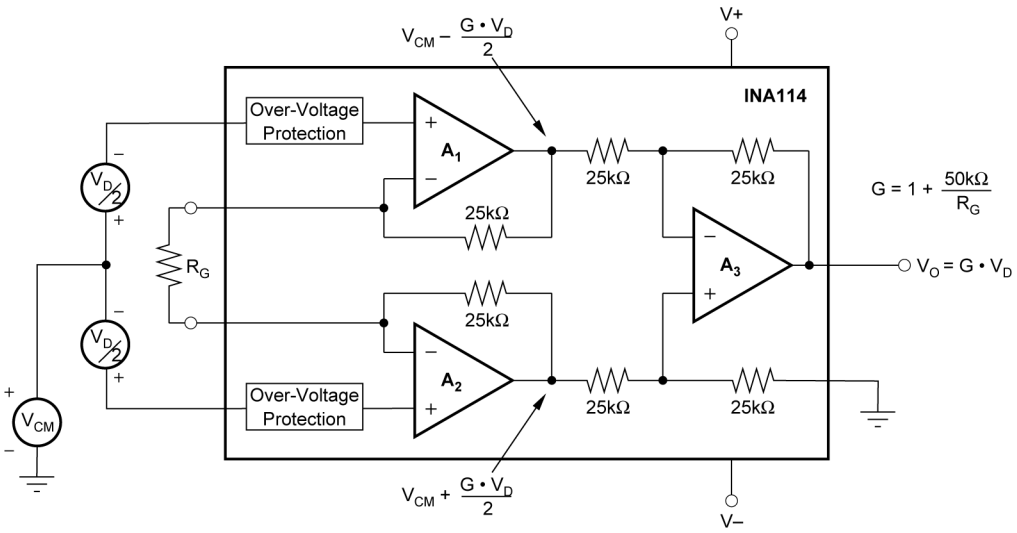


Figure 6-4. Voltage Swing of A_1 and A_2

Input overload often produces an output voltage that appears normal. For example, an input voltage of 20V on one input and 40V on the other input obviously exceeds the linear common-mode range of both input amplifiers. Both input amplifiers are saturated to nearly the same output voltage limit; therefore, the difference voltage measured by the output amplifier is near zero. The output of the INA114 is near 0V even though both inputs are overloaded.

6.1.6 Input Protection

The inputs of the INA114 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). Typical performance curve *Input Bias Current vs Common-Mode Input Voltage* shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

6.1.7 Output Voltage Sense (SOIC-16 Package Only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 6-5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths can cause instability. This instability can be generally be eliminated with a high-frequency feedback path through C_1. Drive heavy loads or long lines by connecting a buffer inside the feedback path (see Figure 6-6).

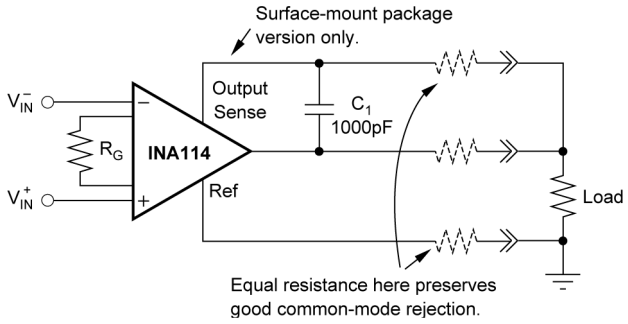


Figure 6-5. Remote Load and Ground Sensing

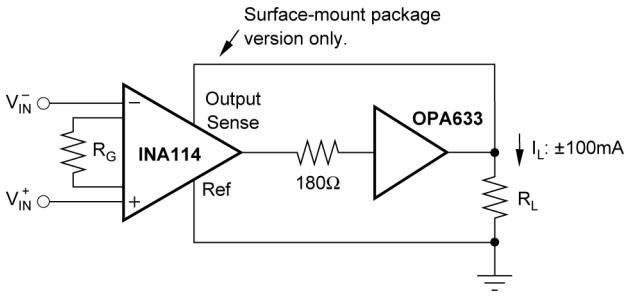


Figure 6-6. Buffered Output for Heavy Loads

6.2 Typical Applications

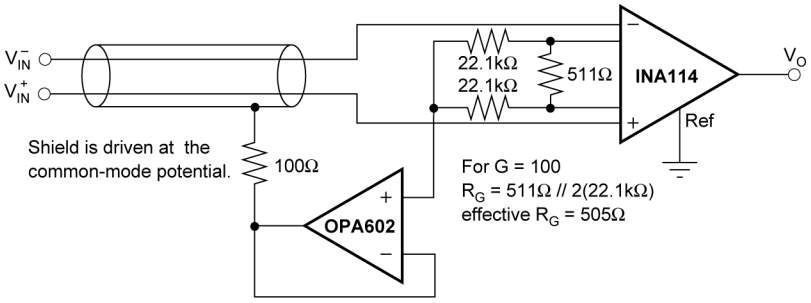


Figure 6-7. Shield Driver Circuit

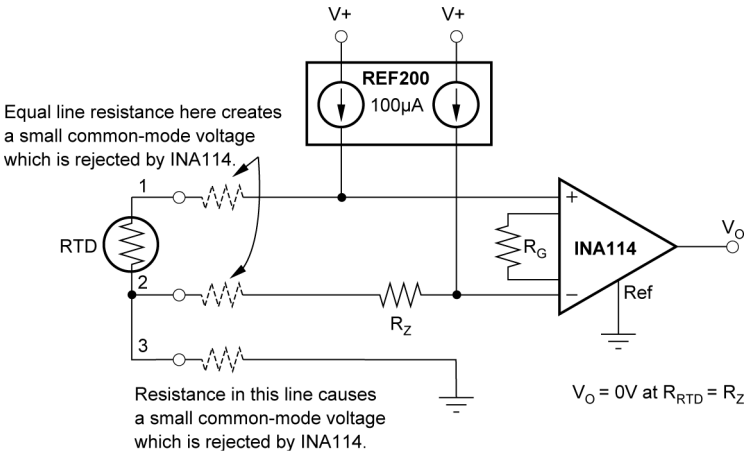
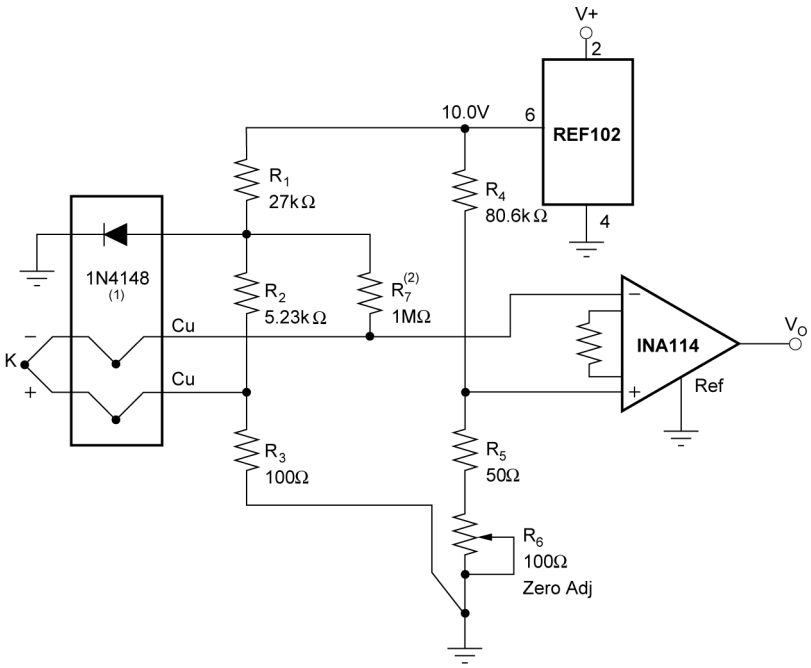


Figure 6-8. RTD Temperature Measurement Circuit



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

NOTES: (1) –2.1mV/°C at 200µA. (2) R_7 provides down-scale burn-out indication.

Figure 6-9. Thermocouple Amplifier with Cold Junction Compensation

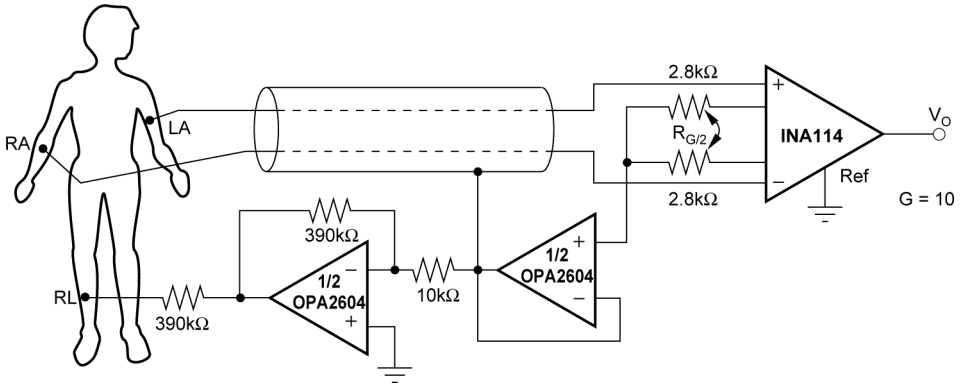


Figure 6-10. ECG Amplifier with Right-Leg Drive

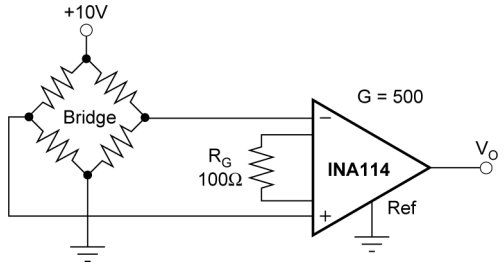


Figure 6-11. Bridge Transducer Amplifier

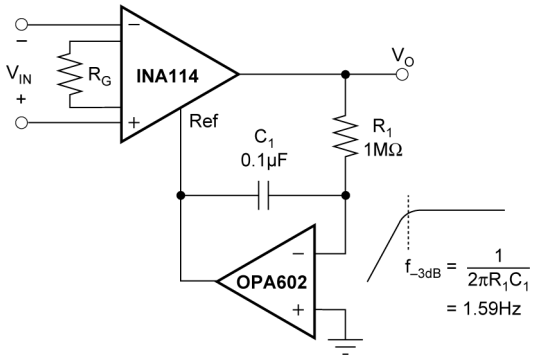
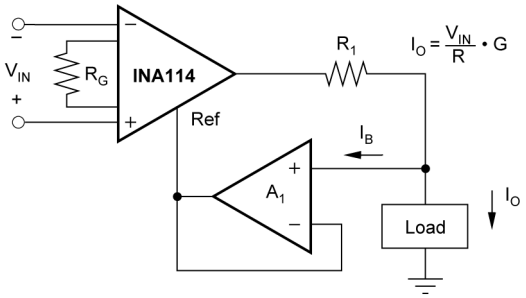


Figure 6-12. AC-Coupled Instrumentation Amplifier



A_1	I_B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

Figure 6-13. Differential Voltage-to-Current Converter

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Device Nomenclature

Table 7-1. Device Nomenclature

PART NUMBER	DEFINITION
INA114AP INA114AU INA114AU/1K INA114BP INA114BU INA114BU/1K	The die is manufactured in CSO: SHE or CSO:TID.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2024) to Revision B (January 2026)	Page
• Added description of device flow information in *Specifications*.	4
• Added all chip site origins (CSO) condition to the typical test conditions in the *Electrical Characteristics*	5
• Added different fabrication process specifications for voltage noise in the *Electrical Characteristics*	5
• Added different fabrication process specifications for bandwidth in the *Electrical Characteristics*	5
• Added different fabrication process specifications for slew rate in the *Electrical Characteristics*	5
• Added different fabrication process specifications for overload recovery in the *Electrical Characteristics*	5
• Added all chip site origins (CSO) condition to the typical test conditions in the *Typical Characteristics*	7

- Added "CSO:SHE" to Gain vs Frequency and Input-Referred Noise, 0.1 Hz to 10 Hz, curves in the *Typical Characteristics* 7
- Added "CSO:TID" to Input Bias Current vs Differential Input Voltage, Input Bias Current vs Common-Mode Input Voltage, Large-Signal Response (G=1 and G=1000), and Small-Signal Response (G=1 and G=1000) curves in the *Typical Characteristics* 7
- Added Gain vs Frequency, Input-Referred Noise Voltage vs Frequency, and Input-Referred Noise, 0.1 Hz to 10 Hz, curves for CSO: TID in the *Typical Characteristics* 7
- Added Input-Referred NoiseVoltage vs Frequency, Input Bias Current vs Differential Input Voltage, Input Bias Current vs Common-Mode Input Voltage, Large-Signal Response (G=1 and G =1000), and Small-Signal Response (G=1 and G=1000) curves for CSO: SHE in the *Typical Characteristics* 7
- Updated Slew Rate vs Temperature and Quiescent Current vs Temperature curves to reflect operating temperature range in the *Typical Characteristics* 7
- Added part number flow information table to the *Device Nomenclature* 20

Changes from Revision * (March 1998) to Revision A (January 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added the *ESD Ratings*, *Recommended Operating Conditions*, *Thermal Information*, *Application and Implementation*, *Typical Applications*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections..... 1
- Changed SOL package name to SOIC throughout data sheet..... 1
- Added "for high gains" to low offset voltage and low drift bullets in *Features* 1
- Changed low drift bullet value from 0.25µV/°C to 0.3µV/°C in *Features* 1
- Updated bullets in *Applications* 1
- Added symbols in *Absolute Maximum Ratings* 4
- Changed supply voltage to show dual supply and single supply in *Absolute Maximum Ratings* 4
- Changed "Input Voltage Range" to "Signal input pins" in *Absolute Maximum Ratings* 4
- Added signal output voltage to *Absolute Maximum Ratings* 4
- Changed output short-circuit from "ground" to "V_S / 2" in Absolute Maximum Ratings..... 4
- Added DW (SOIC) package ambient thermal resistance value..... 4
- Changed ambient thermal resistance value for P (PDIP) package from 80°C/W to 110.2°C/W..... 4
- Added symbols in *Electrical Characteristics* 5
- Changed offset voltage maximum value from ±50 + 100/G to ±50 + 150/G..... 5
- Changed "Offset Voltage vs Temperature" to "Offset voltage drift"..... 5
- Changed offset voltage drift test condition from $T_A = T_{MIN}$ to T_{MAX} to T_A = –40°C to +85°C..... 5
- Changed offset voltage drift maximum value from ±0.25 + 5/G to ±0.3 + 5/G..... 5
- Deleted safe input voltage from *Electrical Characteristics* 5
- Changed "Input Common-Mode Range" to "Operating input voltage"..... 5
- Changed "Offset Voltage vs Power Supply" to "Power-supply rejection ratio"..... 5
- Changed "Bias current vs Temperature" to "Input bias current drift"..... 5
- Added "T_A = –40°C to +85°C" test condition to input bias current drift..... 5
- Changed "Offset Current vs Temperature" to "Input offset current drift"..... 5
- Added "T_A = –40°C to +85°C" test condition to input offset current drift..... 5
- Added "V_O = ±10V" test condition to gain error..... 5
- Changed "Gain vs Temperature" to "Gain drift"..... 5
- Added "V_O = –10V to +10V" test condition to gain nonlinearity..... 5
- Changed output voltage values from ±13.5 (min) and ±13.7 (typ) to (V–) + 1.5 (min) and (V+) – 1.5 (max)..... 5
- Changed output voltage test condition from T_{MIN} to T_{MAX} to T_A = –40°C to +85°C..... 5
- Added output voltage test conditions for V_S = ±11.4V and V_S = ±2.25V..... 5
- Added V_{STEP} = 10V test condition to settling time..... 5
- Deleted power supply voltage range typical value of ±15V..... 5
- Moved voltage range, operating temperature range, and thermal resistance from *Electrical Characteristics* to *Recommended Operating Conditions* and *Thermal Information* 5

- Updated Figure 5-6, *Input-referred Noise Voltage vs Frequency* 7
- Updated Figure 5-10, *Input Bias Current vs Differential Input Voltage* 7
- Updated Figure 5-11, *Input Bias Current vs Common-Mode Input Voltage* 7
- Updated Figure 5-19 to Figure 22, Small- and Large-Signal Response plots..... 7

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA114AP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	INA114AP
INA114AP.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA114AP
INA114AU	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114AU.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114AU/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114AU/1K.B	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	INA114BP
INA114BP.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA114BP
INA114BU	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA114BU
INA114BU.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114BU
INA114BU/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA114BU
INA114BU/1K.B	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114BU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

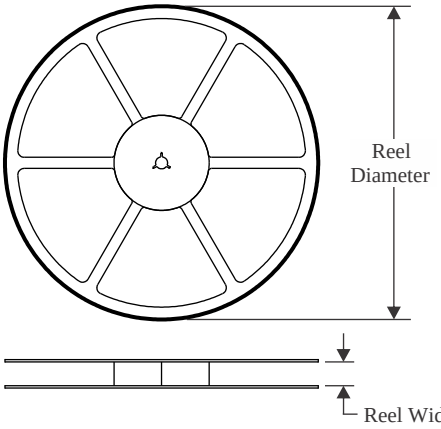
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

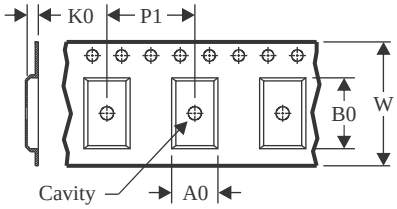
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

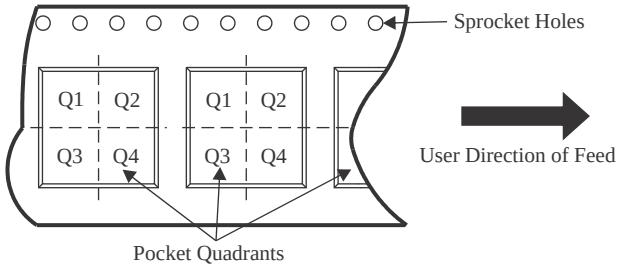


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

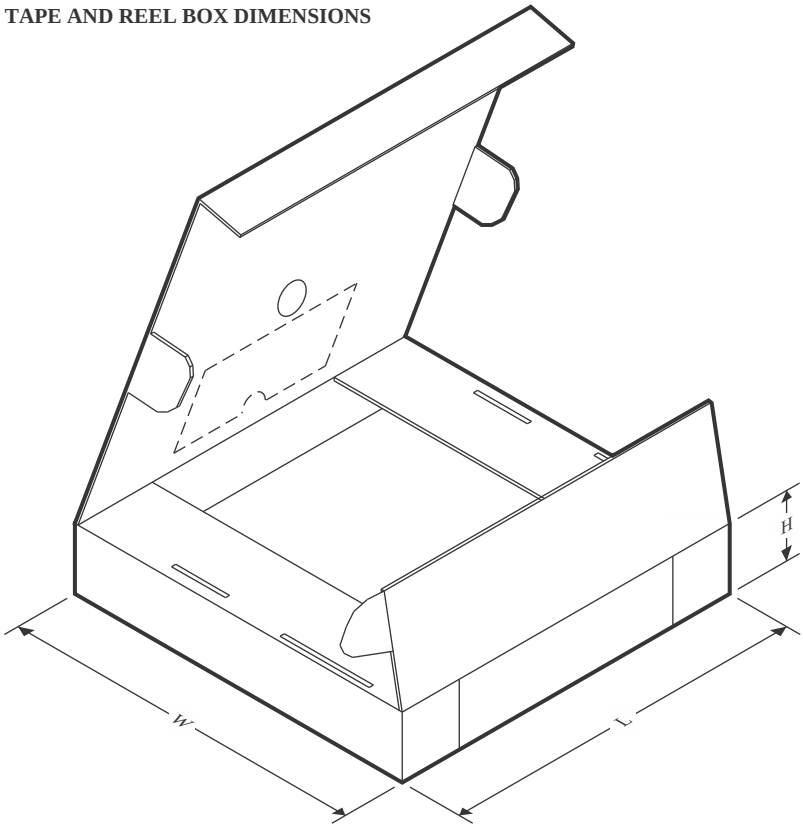
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA114AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA114BU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

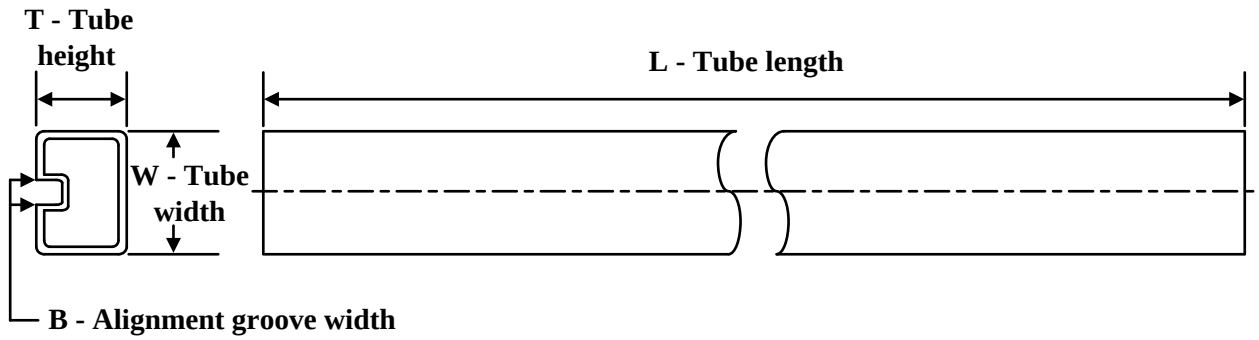
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA114AU/1K	SOIC	DW	16	1000	353.0	353.0	32.0
INA114BU/1K	SOIC	DW	16	1000	353.0	353.0	32.0

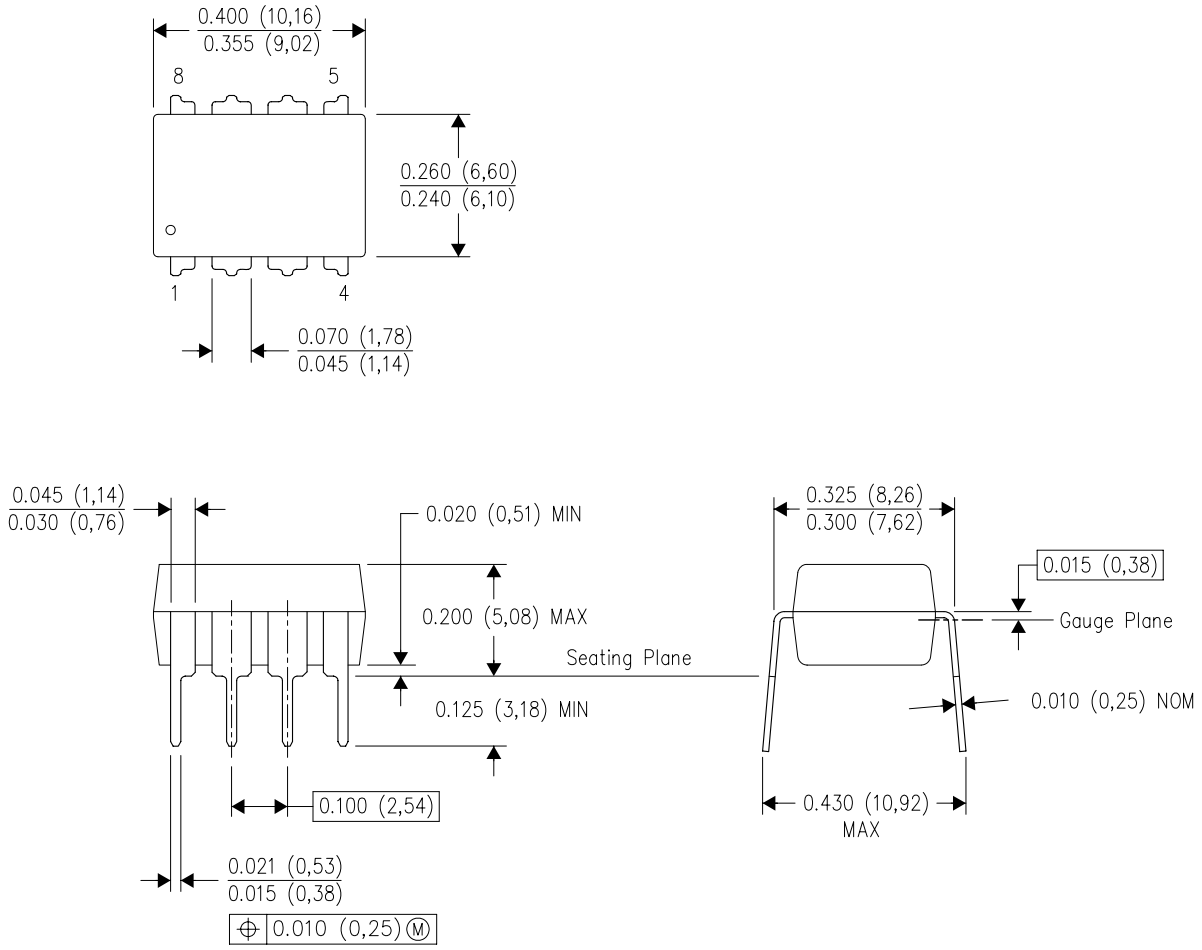
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA114AP	P	PDIP	8	50	506	13.97	11230	4.32
INA114AP.B	P	PDIP	8	50	506	13.97	11230	4.32
INA114AU	DW	SOIC	16	40	507	12.83	5080	6.6
INA114AU.B	DW	SOIC	16	40	507	12.83	5080	6.6
INA114BP	P	PDIP	8	50	506	13.97	11230	4.32
INA114BP.B	P	PDIP	8	50	506	13.97	11230	4.32
INA114BU	DW	SOIC	16	40	507	12.83	5080	6.6
INA114BU.B	DW	SOIC	16	40	507	12.83	5080	6.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

GENERIC PACKAGE VIEW

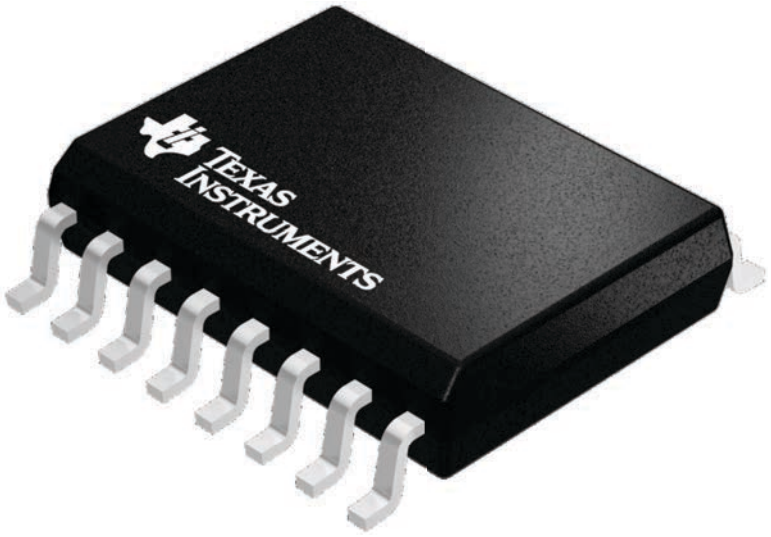
DW 16

SOIC - 2.65 mm max height

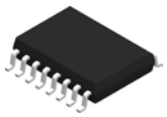
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

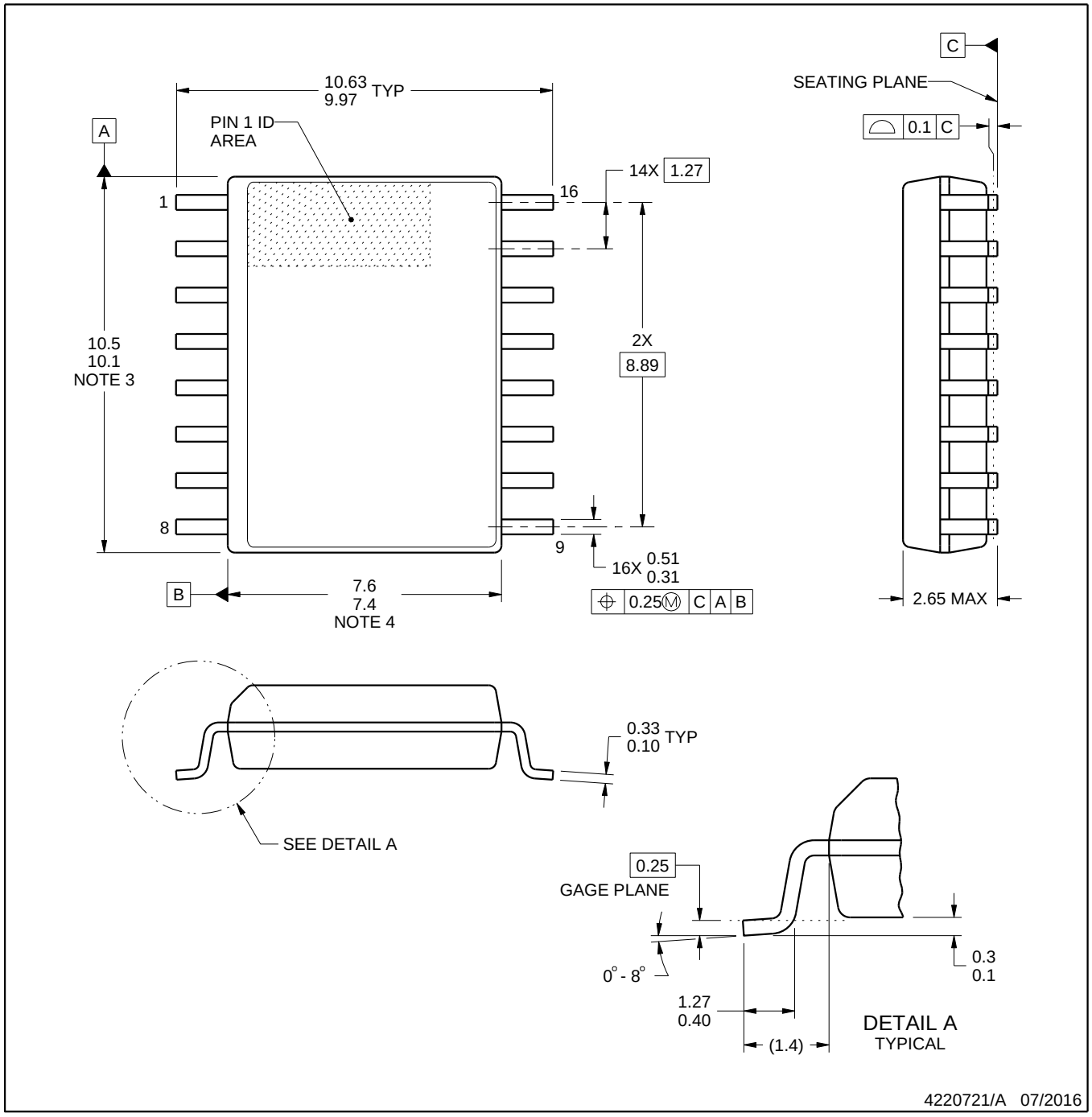


PACKAGE OUTLINE

DW0016A

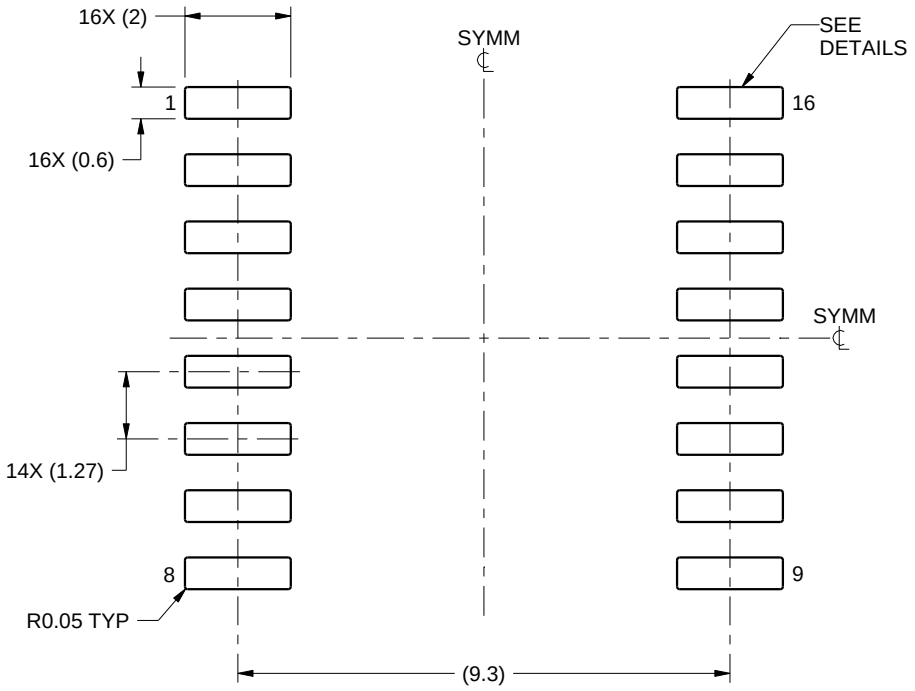
SOIC - 2.65 mm max height

SOIC

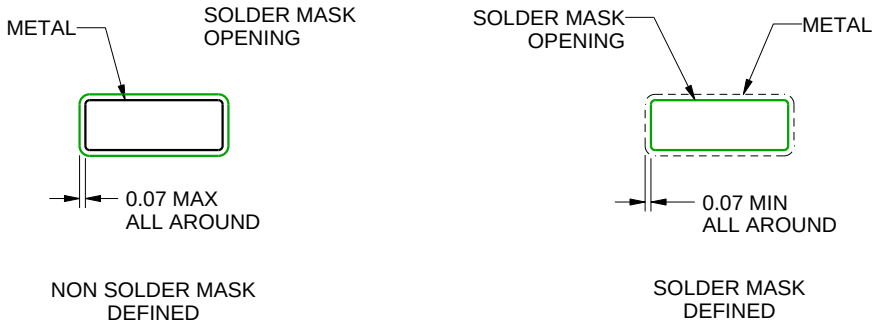


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

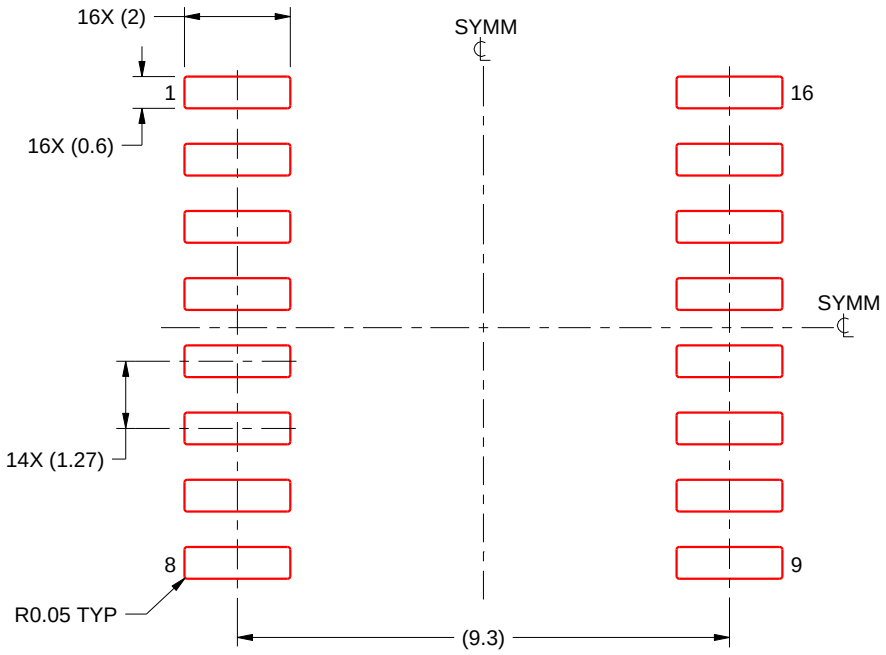


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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