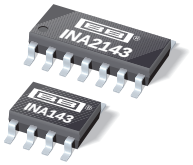
BURR - BROWN®



INA143
INA2143

For most current data sheet and other product information, visit www.burr-brown.com

High-Speed, Precision, G = 10 or G = 0.1 DIFFERENCE AMPLIFIERS

FEATURES

- DESIGNED FOR LOW COST
- G = 10V/V or G = 0.1V/V
- SINGLE, DUAL VERSIONS
- LOW OFFSET VOLTAGE: ±250μV max, ±3μV/°C max
- LOW GAIN ERROR: 0.01%
- HIGH SLEW RATE: 5V/μs
- FAST SETTLING TIME: 9μs to 0.01%
- LOW QUIESCENT CURRENT: 950μA
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- SO-8 and SO-14 PACKAGES

APPLICATIONS

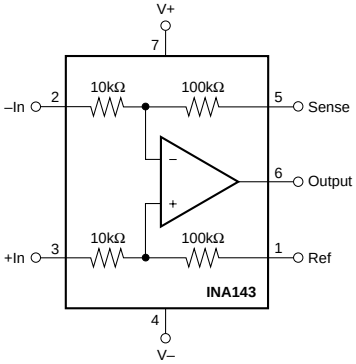
- DIFFERENTIAL INPUT AMPLIFIER BUILDING BLOCK
- DIFF IN/DIFF OUT AMPLIFIER
- GAIN = –10 INVERTING AMPLIFIER
- GAIN = +10 NON-INVERTING AMPLIFIER
- GAIN = +11 NON-INVERTING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT/DIFFERENTIAL LINE RECEIVER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- BATTERY POWERED SYSTEMS
- LOW COST AUTOMOTIVE

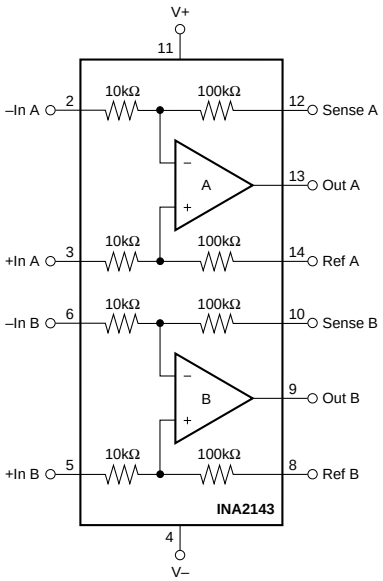
DESCRIPTION

The INA143 and INA2143 are high slew rate, gain of 10V/V or 0.1V/V difference amplifiers consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistor maintains gain accuracy and common-mode rejection over temperature. They operate over a wide supply range, ±2.25V to ±18V (+4.5V to +36V single supply), and input common-mode voltage range extends beyond the positive and negative supply rails.

The differential amplifier is the foundation of many commonly used circuits. The low cost INA143 and INA2143 provide this precision circuit function without using an expensive precision network.

The single version, INA143, package is the SO-8 surface mount. The dual version, INA2143, package is the SO-14 surface mount. Both are specified for operation over the extended industrial temperature range, –40°C to +85°C. Operation is from –55°C to +125°C.





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SBOS116

SPECIFICATIONS: $V_S = \pm 15V$

At T_A = +25°C, V_S = ±15V, G = 10, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA143U INA2143U MIN	INA143U INA2143U TYP	INA143U INA2143U MAX	INA143UA INA2143UA MIN	INA143UA INA2143UA TYP	INA143UA INA2143UA MAX	UNITS
OFFSET VOLTAGE[1]	RTI							
Initial[1]	V_{CM} = 0V		±100	±250		*	±500	µV
vs Temperature			±1	±3		See Typical Curve		µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		±5	±20		*	±30	µV/V
vs Time			0.2			*		$\mu V/\sqrt{mo}$
Channel Separation (dual)	dc		140					dB
INPUT IMPEDANCE[3]								
Differential			20			*		kΩ
Common-Mode			55			*		kΩ
INPUT VOLTAGE RANGE	RTI							
Common-Mode Voltage Range								
Positive	V_O = 0V	1.1[(V+)–1.5]	1.1[(V+)–1]		*	*		V
Negative	V_O = 0V	1.1[(V–)+1.5]	1.1[(V–)+1]		*	*		V
Common-Mode Rejection Ratio	V_{CM} = –14.85V to 14.85V, R_S = 0Ω	86	96		80	*		dB
OUTPUT VOLTAGE NOISE[3]	RTI							
f = 0.1Hz to 10Hz			1			*		µVp-p
f = 10Hz			45			*		$nV/\sqrt{Hz}$
f = 100Hz			30			*		$nV/\sqrt{Hz}$
f = 1kHz			27			*		$nV/\sqrt{Hz}$
GAIN								
Initial			10			*		V/V
Error	V_O = –14V to +13.5V		±0.01	±0.05		*	±0.1	%
vs Temperature			±1	±10		*	*	ppm/°C
Nonlinearity	V_O = –14V to +13.5V		±0.0001	±0.001		*	±0.002	% of FS
OUTPUT								
Voltage Output	Gain Error < 0.1%							
Positive	R_L = 10kΩ to Ground	(V+) –1.5	(V+) –1.3		*	*		V
Negative	R_L = 10kΩ to Ground	(V–) +1	(V–) +0.8		*	*		V
Positive	R_L = 100kΩ to Ground		(V+) –0.8			*		V
Negative	R_L = 100kΩ to Ground		(V–) +0.3			*		V
Current Limit	Continuous-to-Common		–25, +32			*		mA
Capacitive Load (stable operation)			1000			*		pF
FREQUENCY RESPONSE								
Small-Signal Bandwidth	–3dB		0.15			*		MHz
Slew Rate			5			*		V/µs
Settling Time: 0.1%	V_O = 10V Step, C_L = 100pF		6			*		µs
0.01%	V_O = 10V Step, C_L = 100pF		9			*		µs
Overload Recovery Time	50% Overdrive		6			*		µs
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range								
Dual Supplies		±2.25		±18	*		*	V
Single Supply		+4.5		+36	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±0.95	±1.2		*	*	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operation		–55		+125	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Resistance θ_{JA}								
SO-8 Surface Mount			150			*		°C/W
SO-14 Surface Mount			100			*		°C/W

* Specifications the same as INA143U, INA2143U.

NOTES: (1) Includes the effects of amplifier's input bias and offset currents. (2) Internal resistors are ratio matched but have ±20% absolute value. (3) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

SPECIFICATIONS: $V_S = \pm 5V$

At T_A = +25°C, V_S = ±5V, G = 10, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA143U INA2143U MIN	INA143U INA2143U TYP	INA143U INA2143U MAX	INA143UA INA2143UA MIN	INA143UA INA2143UA TYP	INA143UA INA2143UA MAX	UNITS
OFFSET VOLTAGE[1]	RTI							
Initial[1]	V_{CM} = 0V		±200	±500		*	±750	µV
vs Temperature			±1			*		µV/°C
INPUT VOLTAGE RANGE	RTI							
Common-Mode Voltage Range								
Positive	V_O = 0V	1.1[(V+)–1.5]	1.1[(V+)–1]		*	*		V
Negative	V_O = 0V	1.1[(V–)+1.5]	1.1[(V–)+1]		*	*		V
Common-Mode Rejection Ratio	V_{CM} = –3.85V to +3.85V, R_S = 0Ω	86	96		80	*		dB
GAIN								
Initial			10			*		V/V
Gain Error	V_O = –4V to +3.5V		±0.01	±0.05		*	±0.1	%
Nonlinearity	V_O = –4V to +3.5V		±0.0001	±0.001		*	±0.002	% of FS
OUTPUT								
Voltage Output	Gain Error < 0.1%							
Positive	R_L = 10kΩ to Ground	(V+) –1.5	(V+)–1.3		*	*		V
Negative	R_L = 10kΩ to Ground	(V–) +1	(V–)+0.8		*	*		V
Positive	R_L = 100kΩ to Ground		(V+)–0.8			*		V
Negative	R_L = 100kΩ to Ground		(V–)+0.3			*		V
POWER SUPPLY								
Rated Voltage			+5			*		V
Operating Voltage Range								
Dual Supplies		±2.25		±18	*		*	V
Single Supply		+4.5		+36	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±0.92	±1.2		*	*	mA

* Specifications the same as INA143U, INA2143U.

NOTES: (1) Includes the effects of amplifier's input bias and offset currents.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Input Signal (G = 10), Voltage	1.1 • V_S
Current	0.5mA
Input Signal (G = 0.1), Voltage	11 • V_S
Current	0.5mA
Output Short-Circuit (to ground)[2]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) One channel per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

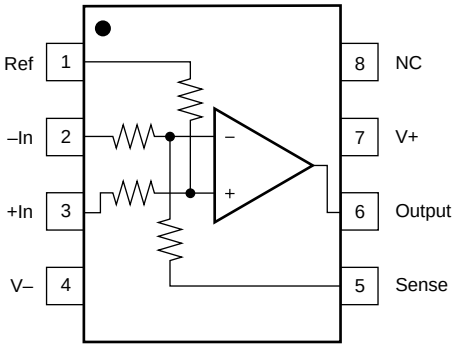
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA
Single						
INA143U	SO-8 Surface Mount	182	–40°C to +85°C	INA143U	INA143U	Rails
"	"	"	"	"	INA143U/2K5	Tape and Reel
INA143UA	SO-8 Surface Mount	182	–40°C to +85°C	INA143UA	INA143UA	Rails
"	"	"	"	"	INA143UA/2K5	Tape and Reel
Dual						
INA2143U	SO-14 Surface Mount	235	–40°C to +85°C	INA2143U	INA2143U	Rails
"	"	"	"	"	INA2143U/2K5	Tape and Reel
INA2143UA	SO-14 Surface Mount	235	–40°C to +85°C	INA2143UA	INA2143UA	Rails
"	"	"	"	"	INA2143UA/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA143UA/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

PIN CONFIGURATIONS

Top View **SO-8**

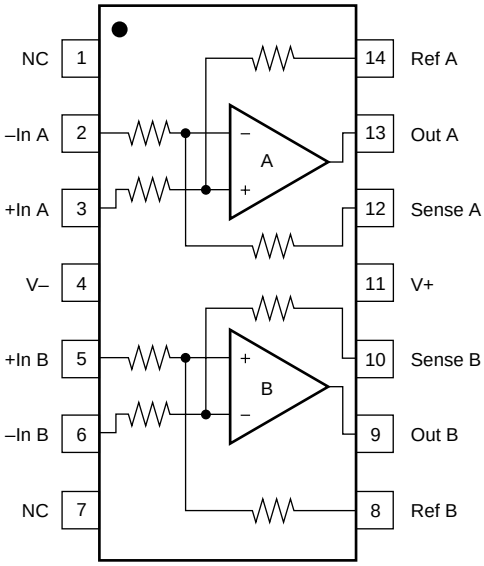
INA143



NC = No Connection

Top View **SO-14**

INA2143

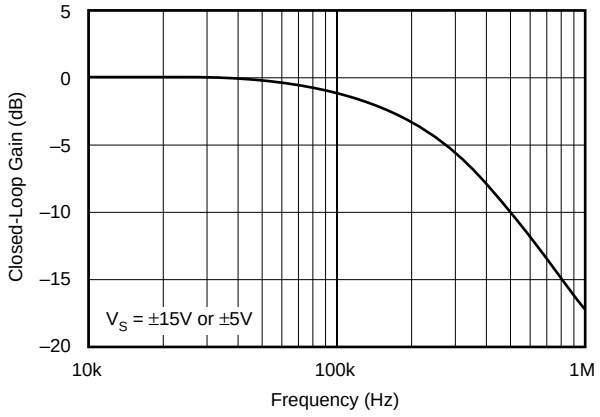


NC = No Connection

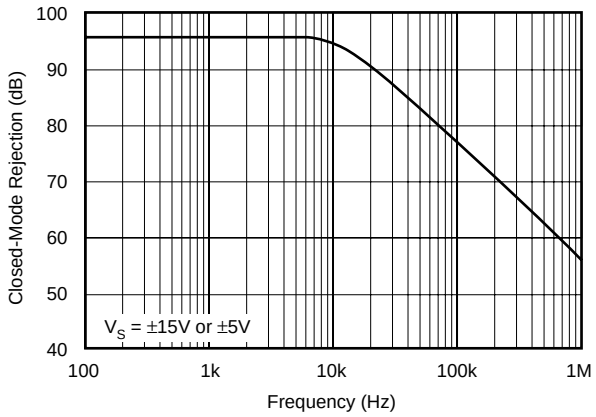
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, G = 10, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

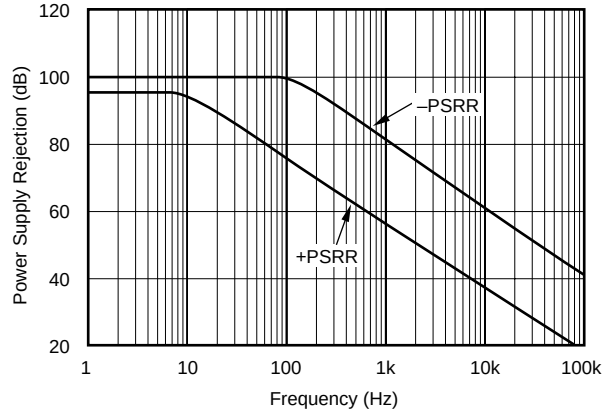
GAIN vs FREQUENCY



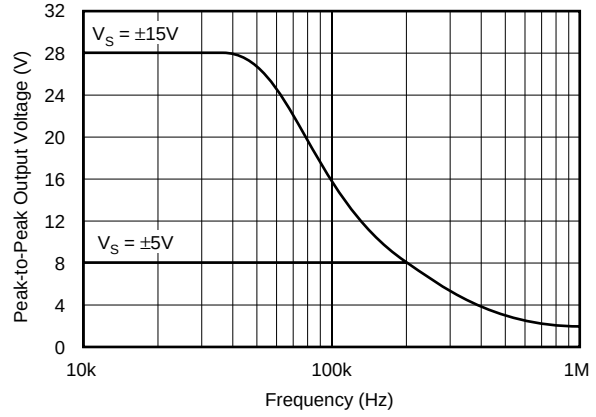
COMMON-MODE REJECTION vs FREQUENCY



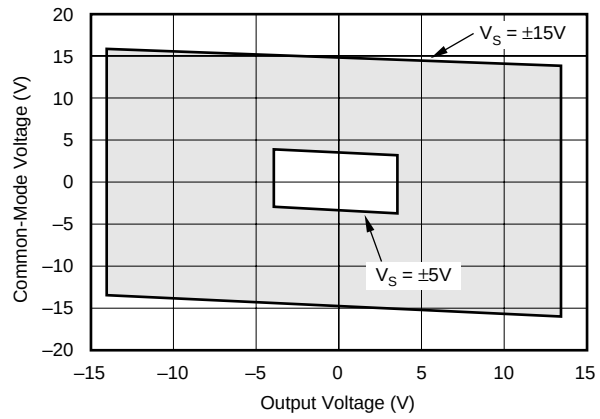
POWER SUPPLY REJECTION vs FREQUENCY



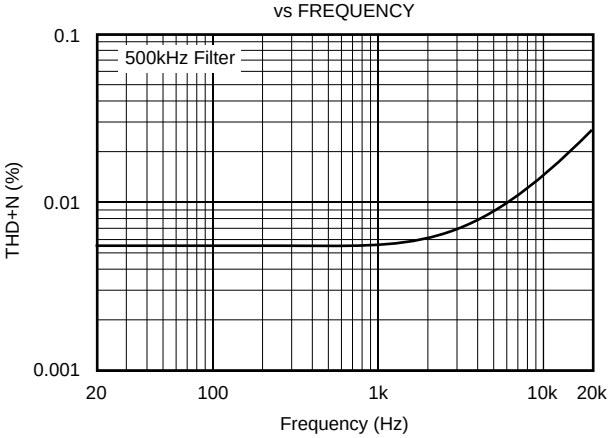
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



INPUT COMMON-MODE VOLTAGE
vs OUTPUT VOLTAGE



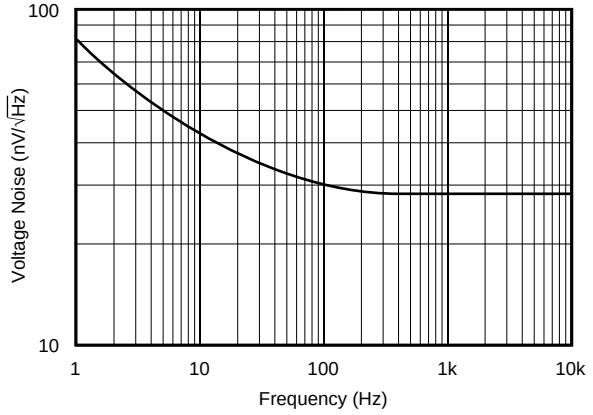
TOTAL HARMONIC DISTORTION+NOISE
vs FREQUENCY



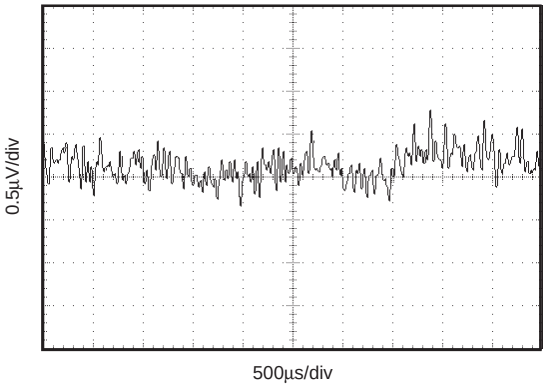
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, G = 10, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

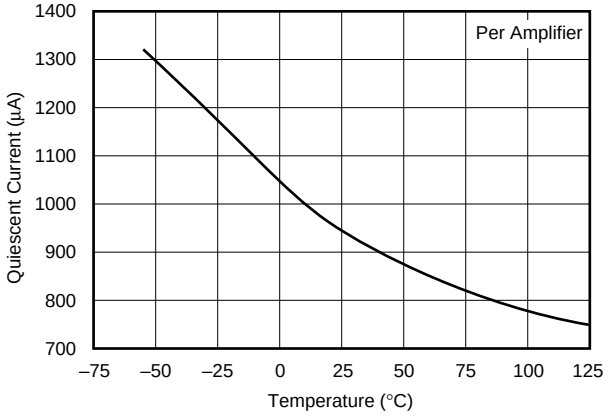
VOLTAGE NOISE DENSITY vs FREQUENCY



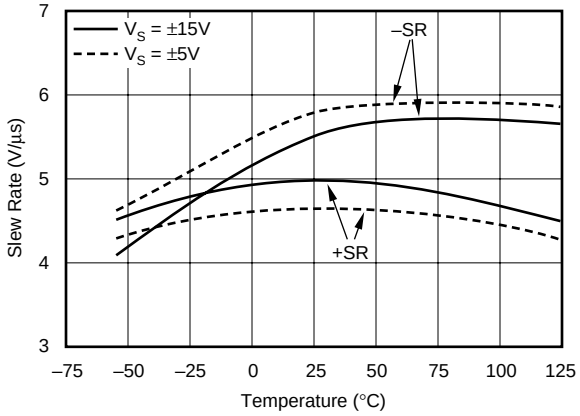
0.1Hz TO 10Hz PEAK-TO-PEAK VOLTAGE NOISE



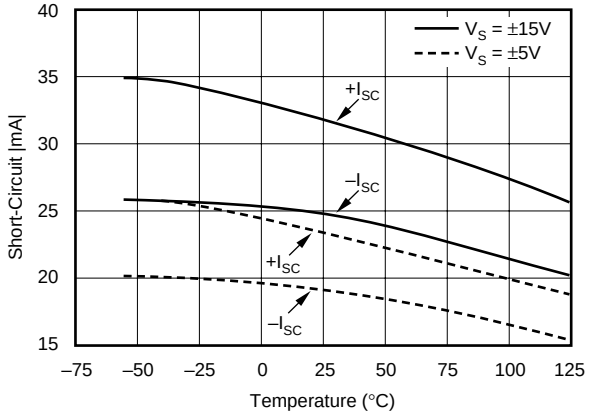
QUIESCENT CURRENT vs TEMPERATURE



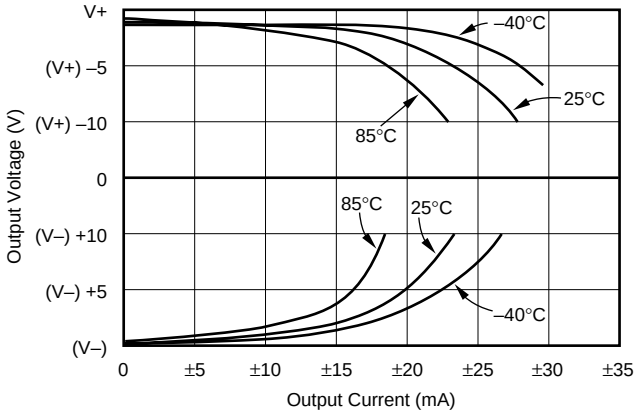
SLEW RATE vs TEMPERATURE



SHORT-CIRCUIT CURRENT vs TEMPERATURE



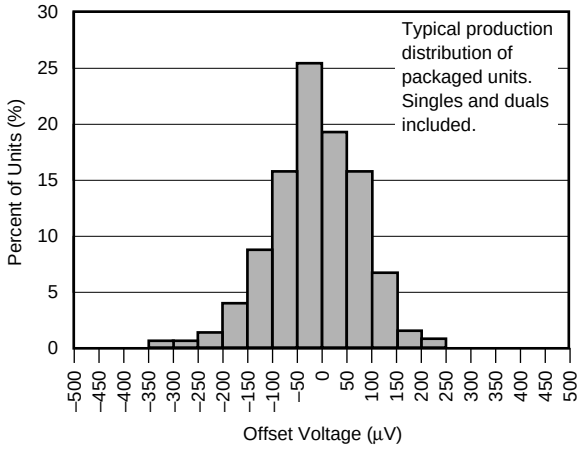
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



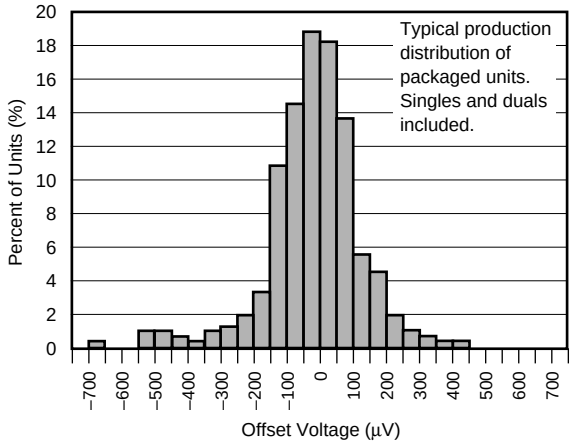
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, G = 10, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

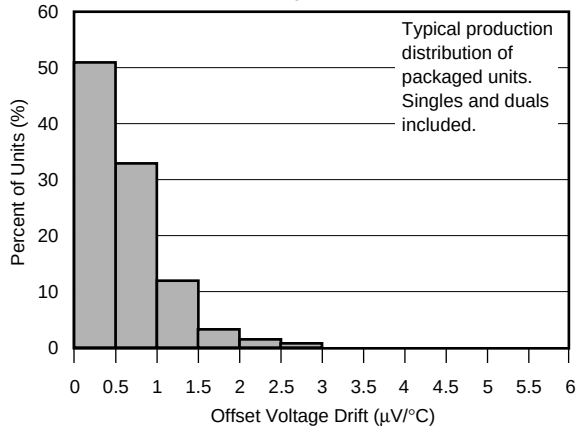
OFFSET VOLTAGE PRODUCTION DISTRIBUTION
V_S = ±15V



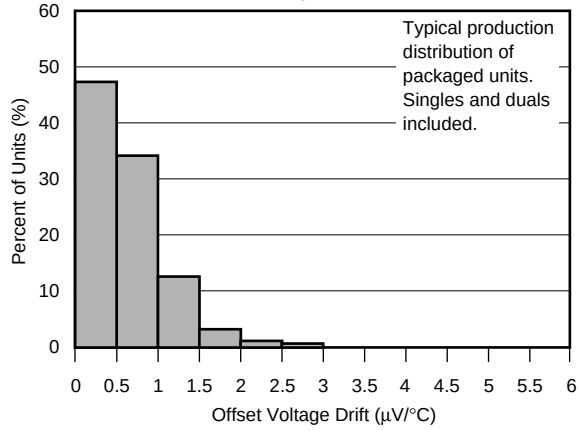
OFFSET VOLTAGE PRODUCTION DISTRIBUTION
V_S = ±5V



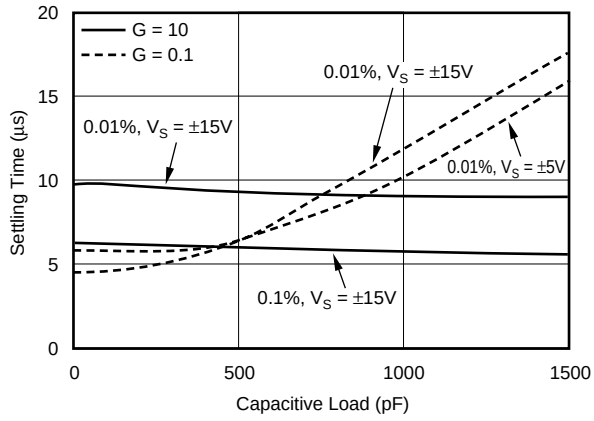
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION
V_S = ±15V



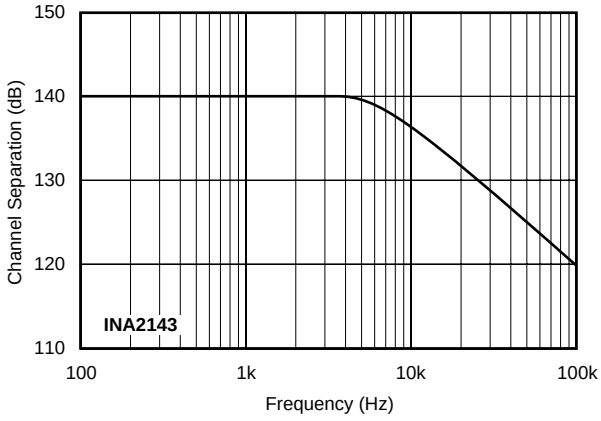
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION
V_S = ±5V



SETTLING TIME vs CAPACITIVE LOAD



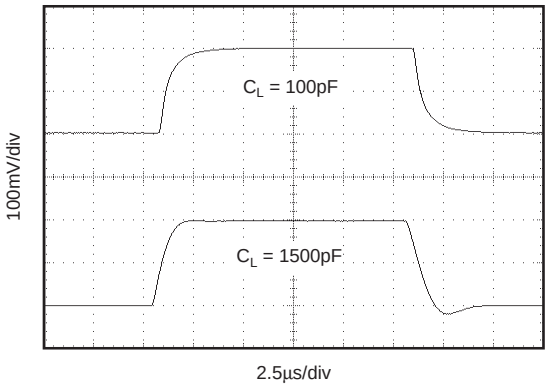
CHANNEL SEPARATION vs FREQUENCY



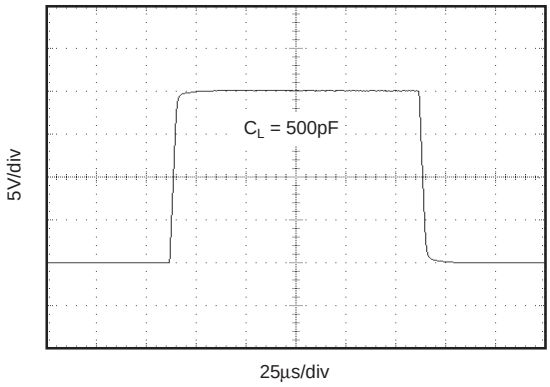
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, G = 10, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE



LARGE-SIGNAL STEP RESPONSE



APPLICATIONS INFORMATION

The INA143 and INA2143 are high-speed difference amplifiers suitable for a wide range of general-purpose applications. Figure 1 shows the basic G = 10 configuration. The input and feedback resistors can be reversed to achieve G = 0.1, as shown in Figure 2. For applications requiring G = 1, the INA133 and INA2133 are recommended.

Decoupling capacitors are strongly recommended for applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 1. All circuitry is completely independent in the dual version assuring lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 1, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 86dB (RTI). If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

The INA143's internal resistors are accurately ratio trimmed to match. That is, R_1/R_2 and R_3/R_4 are trimmed to equal 0.1. However, the absolute values may not be equal ($R_1 + R_2$ may be slightly different than $R_3 + R_4$). Thus, large series resistors on the input (greater than 100Ω), even if well matched, will degrade common-mode rejection.

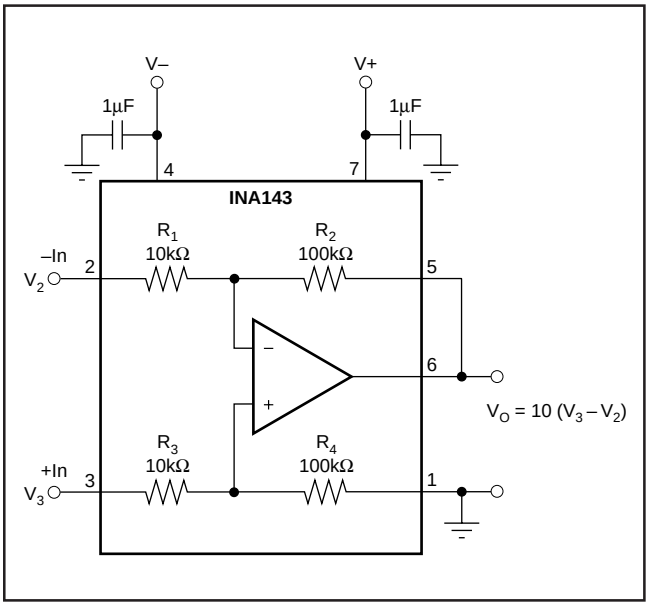


FIGURE 1. G = 10 Basic Power Supply and Signal Connections.

OPERATING VOLTAGE

The INA143 and INA2143 operate from single (+4.5V to +36V) or dual (±2.25V to ±18V) supplies with excellent performance. Specifications are production tested with ±5V and ±15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Performance Curves.

OFFSET VOLTAGE TRIM

The INA143 and INA2143 are laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 3 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 3. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

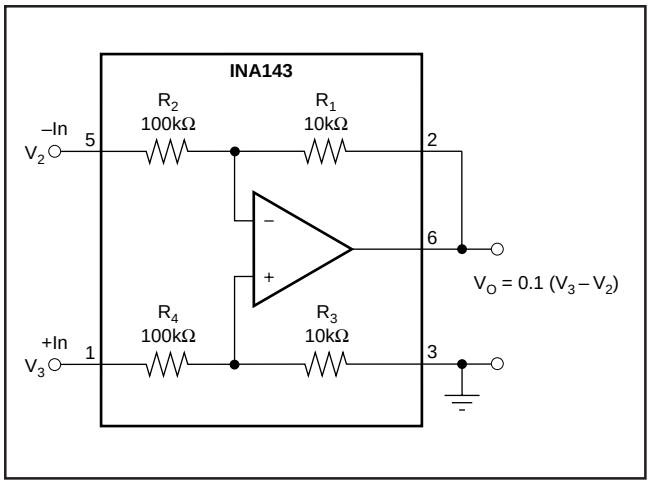


FIGURE 2. G = 0.1 Difference Amplifier.

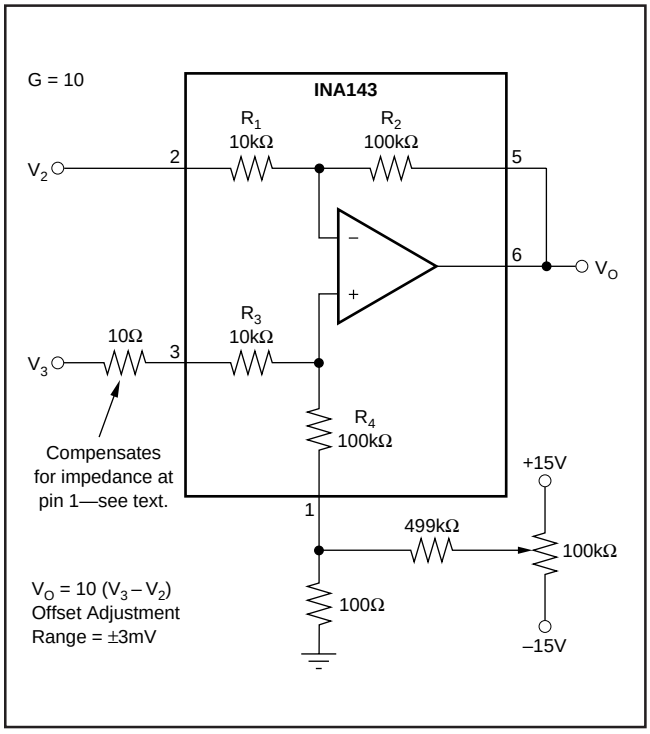


FIGURE 3. Offset Adjustment.

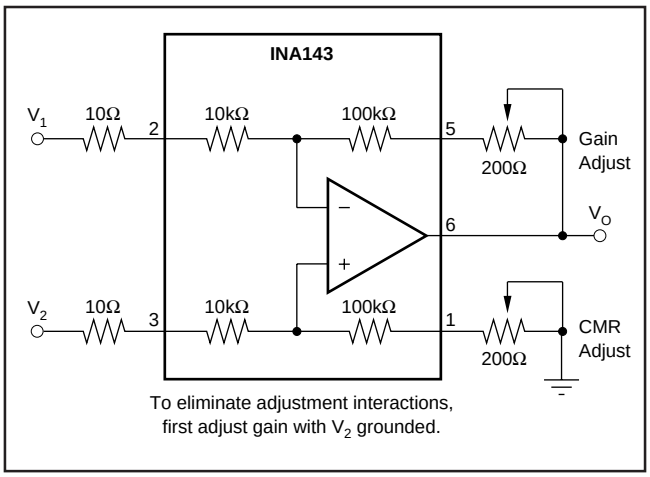


FIGURE 4. Difference Amplifier with Gain and CMR Adjust.

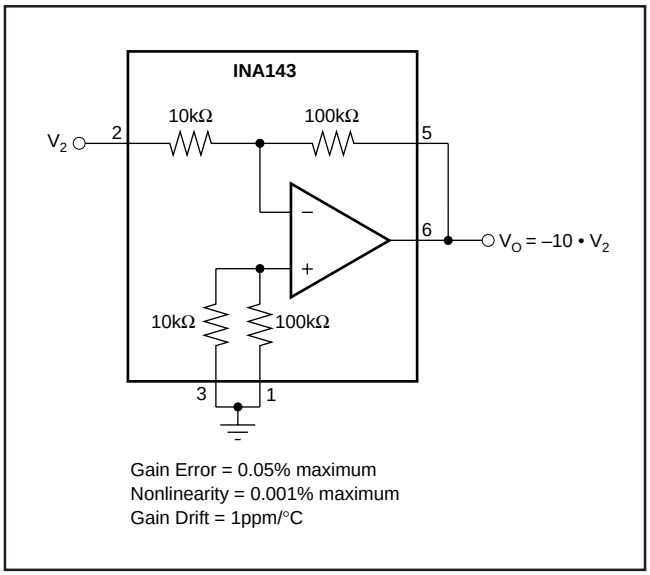


FIGURE 5. Precision G = –10 Inverting Amplifier.

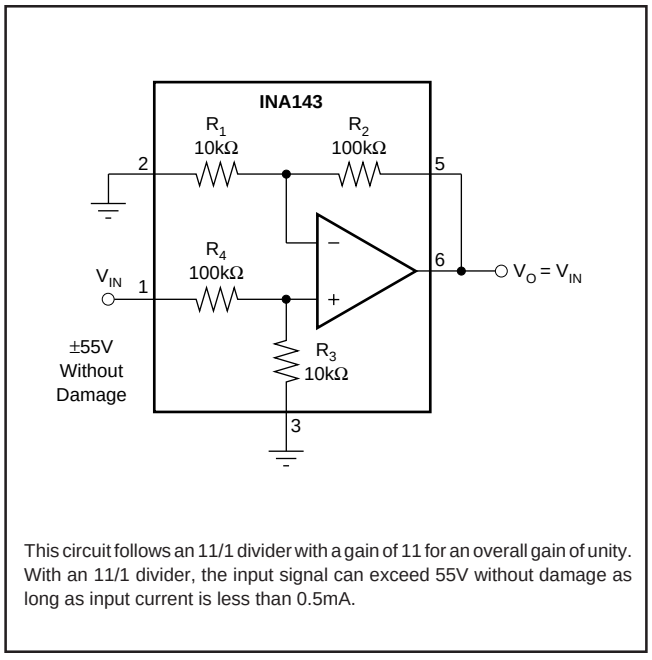
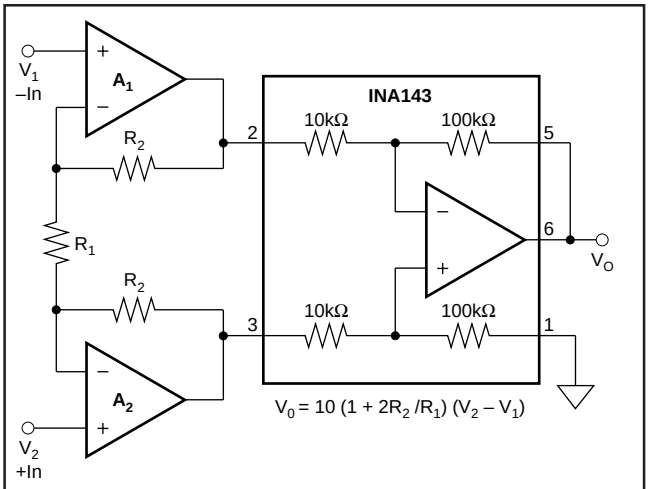


FIGURE 6. Voltage Follower with Input Protection.



The INA143 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics. Burr-Brown offers many complete high performance IAs. Products with related performances are shown at the right in the table below.

A_1, A_2	FEATURE	SIMILAR COMPLETE BURR-BROWN IA
OPA2227	Low Noise	INA103
OPA129	Ultra Low Bias Current (fA)	INA116
OPA2277	Low Offset Drift, Low Noise	INA114, INA128
OPA2130	Low Power, FET-Input (pA)	INA121
OPA2234	Single Supply, Precision, Low Power	INA122, INA118
OPA2237	Single Supply, Low Power, MSOP-8	INA122, INA126

FIGURE 7. Precision Instrumentation Amplifier.

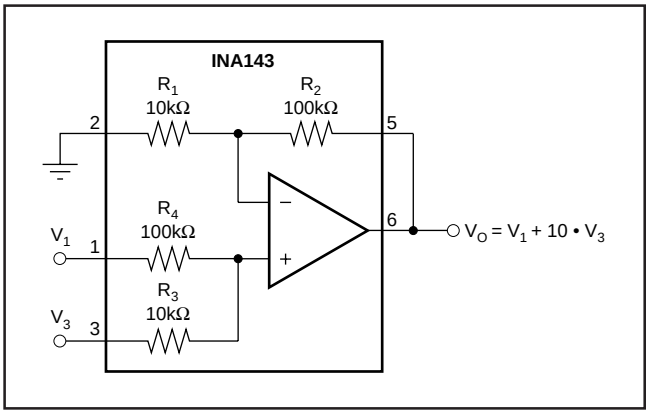


FIGURE 8. Precision Summing Amplifier.

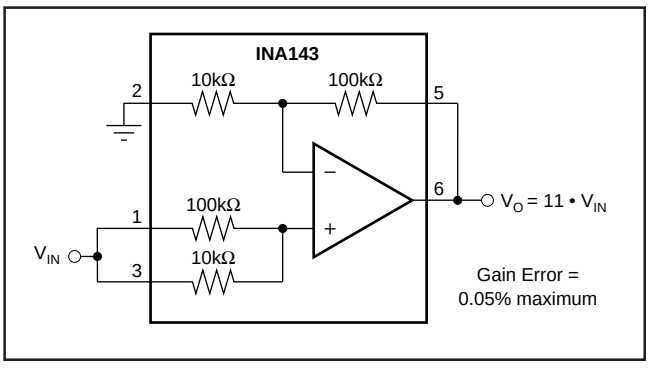


FIGURE 9. Precision G = 11 Buffer.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA143U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	INA 143U	
INA143U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 143U	Samples
INA143UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI		INA 143U A	
INA143UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		INA 143U A	Samples
INA2143U	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2143U A	Samples
INA2143UA	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2143U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

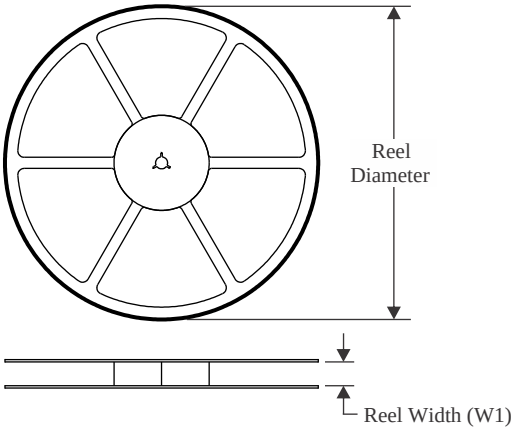
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

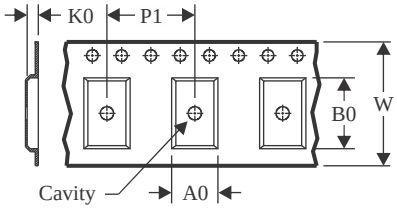
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

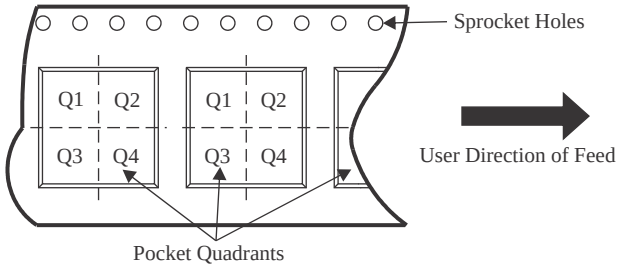


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

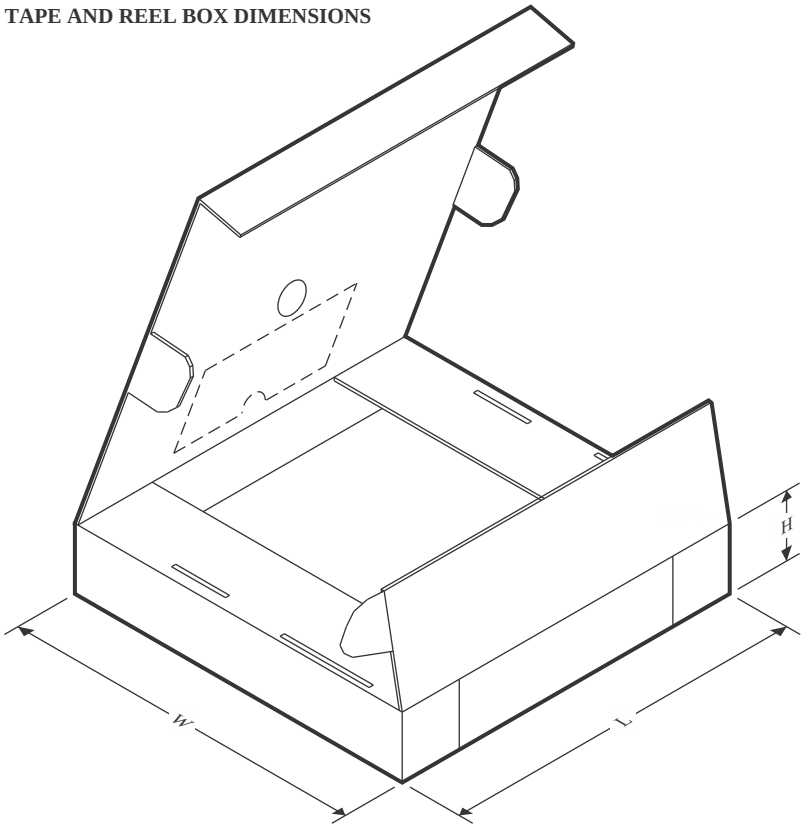
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA143U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA143UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

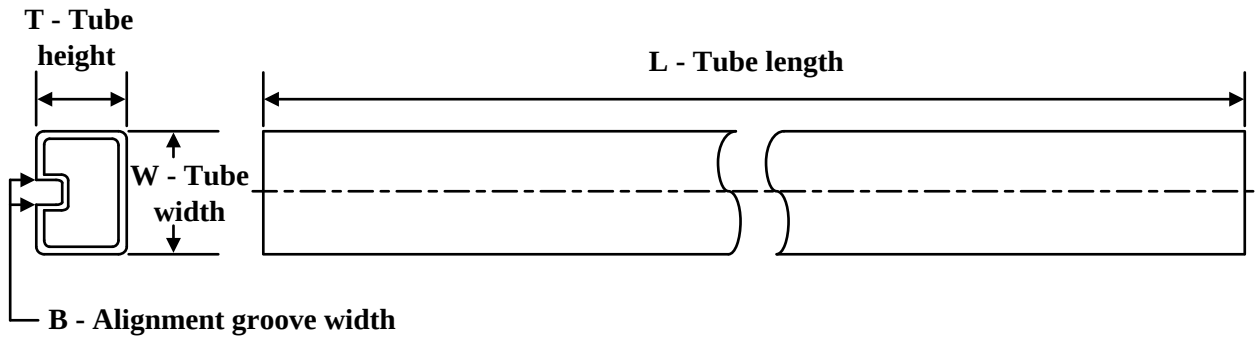
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

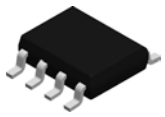
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA143U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA143UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA2143U	D	SOIC	14	50	506.6	8	3940	4.32
INA2143UA	D	SOIC	14	50	506.6	8	3940	4.32

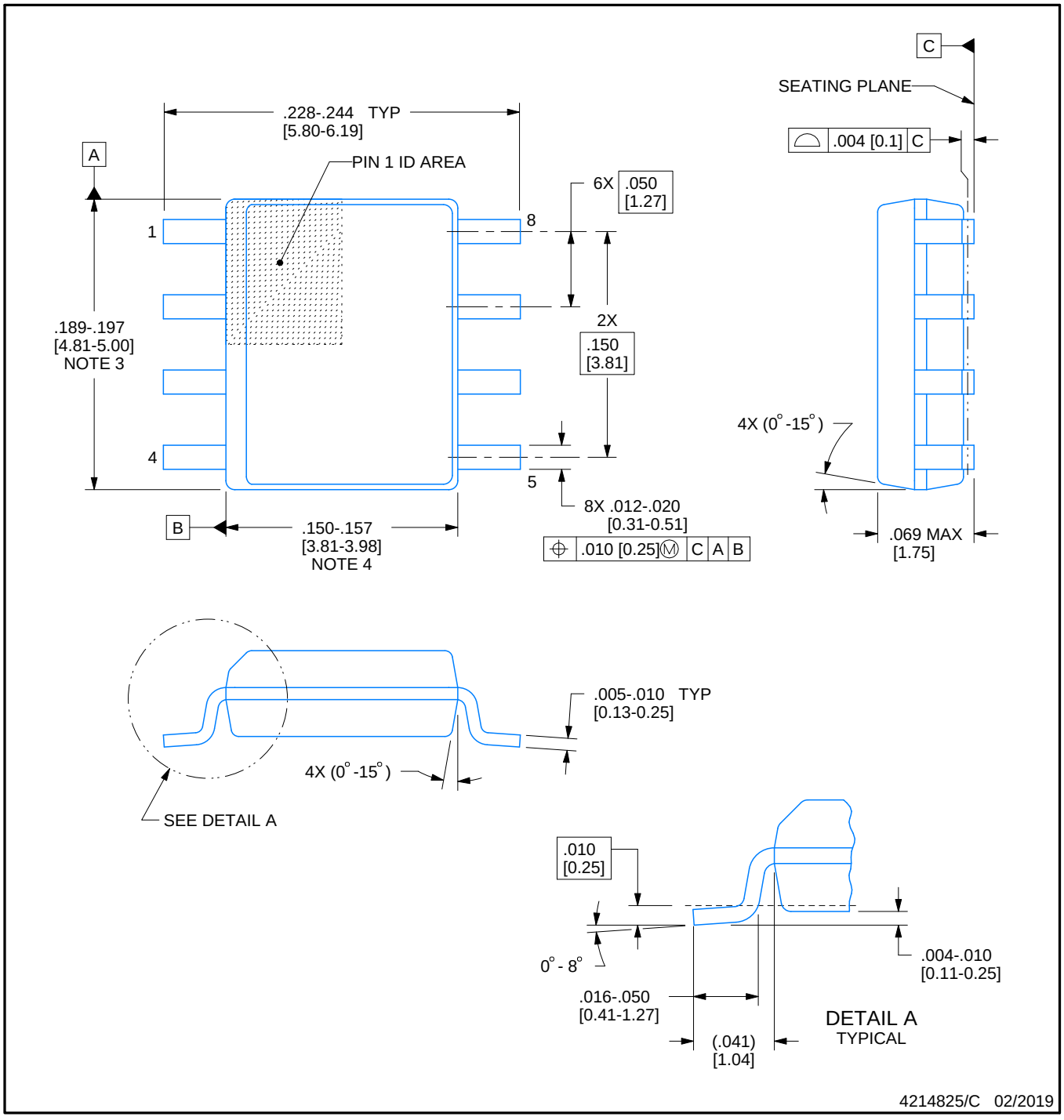


PACKAGE OUTLINE

D0008A

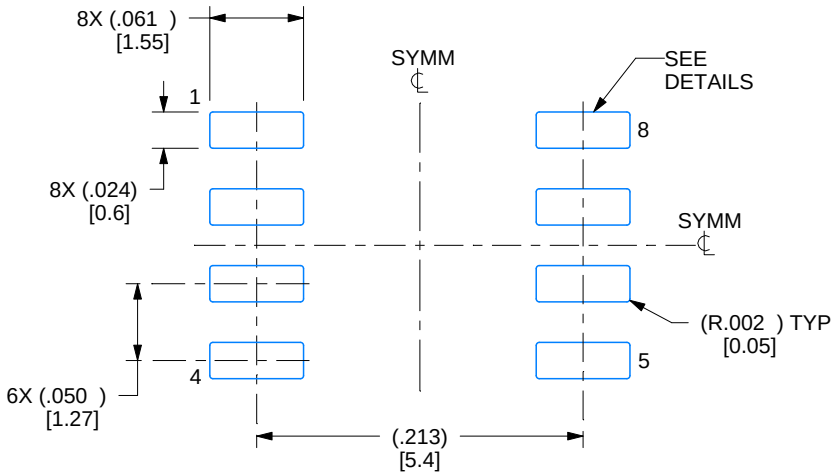
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

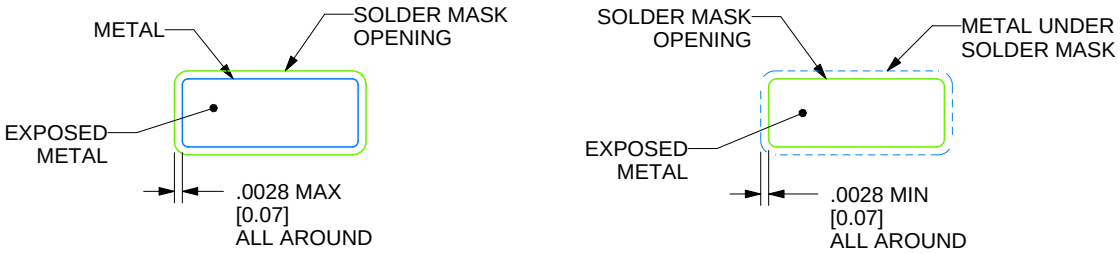


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

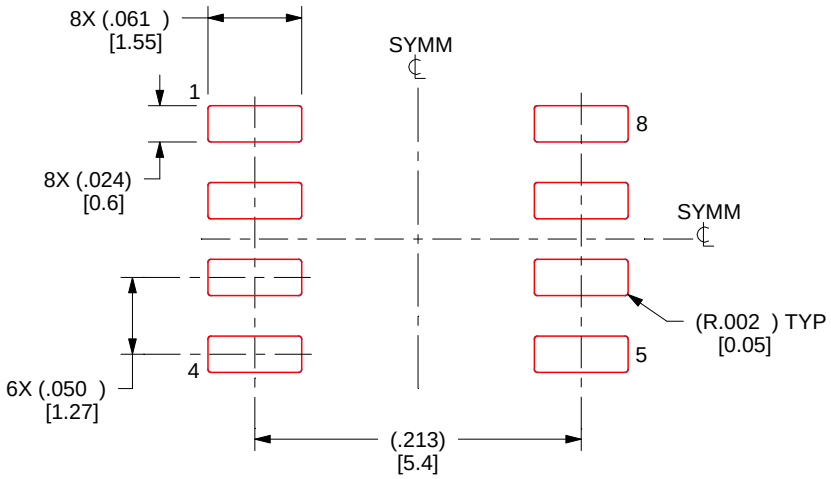
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

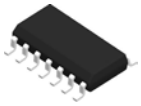


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

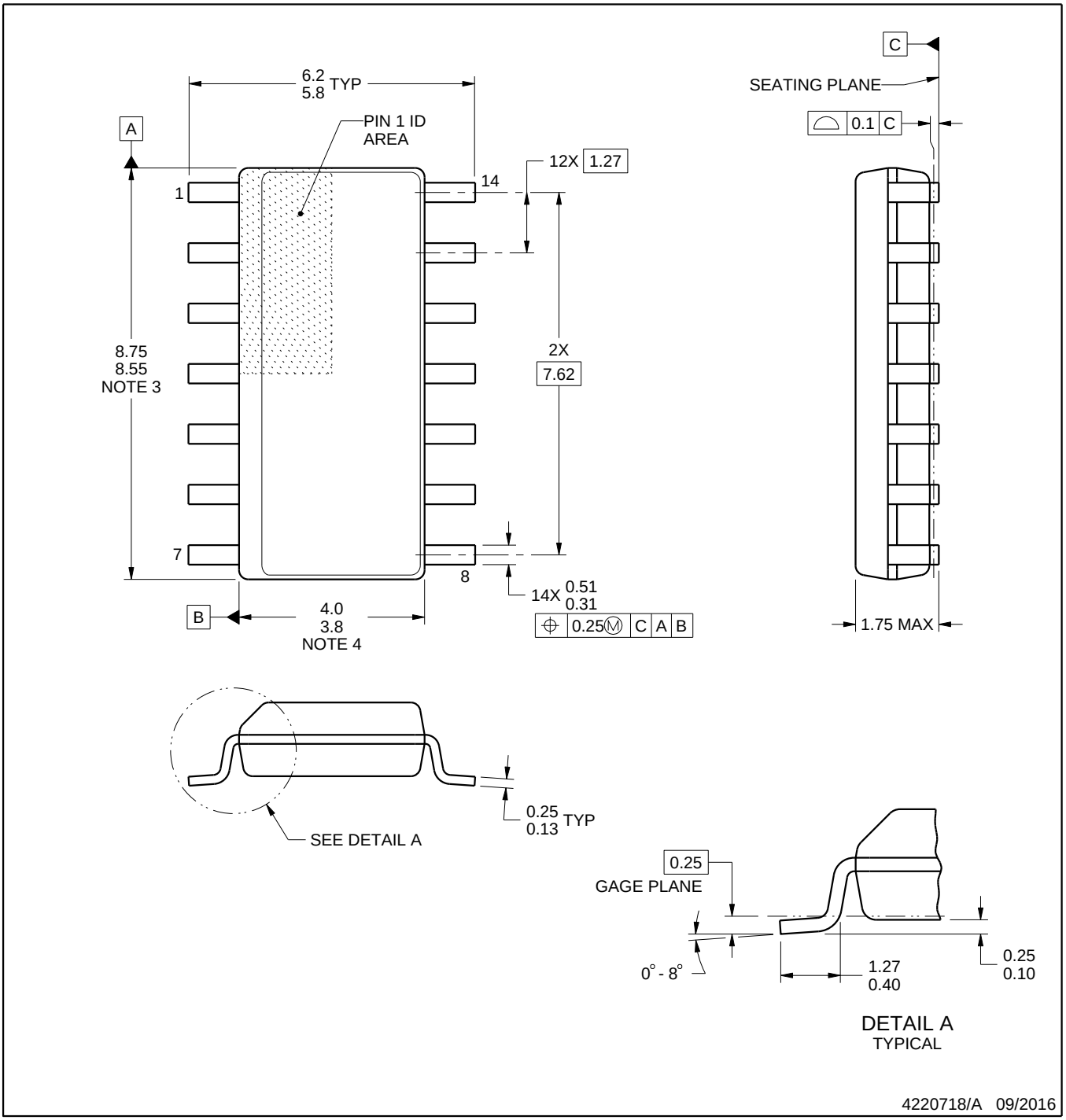


PACKAGE OUTLINE

D0014A

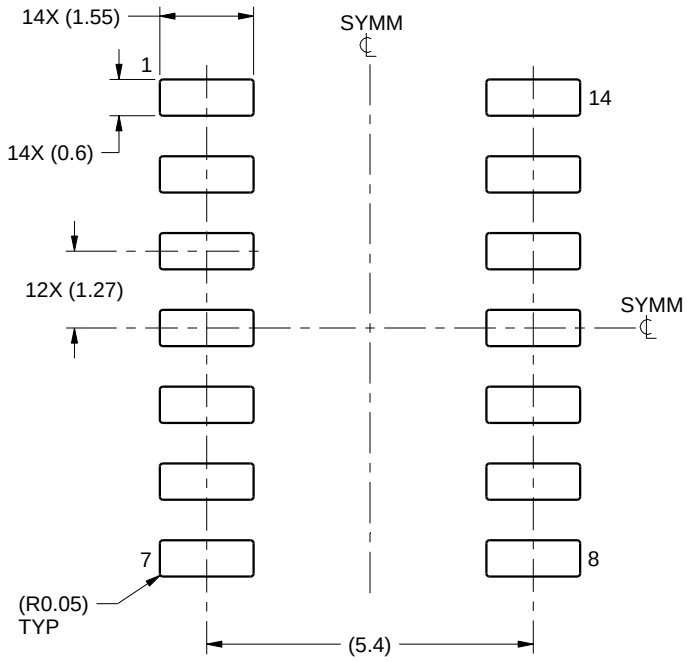
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

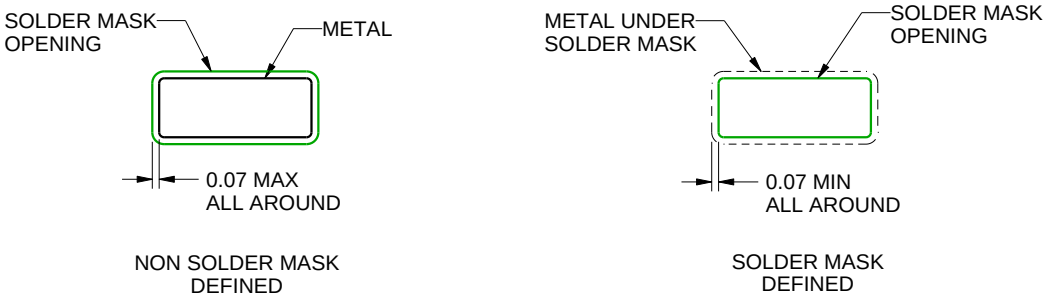


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

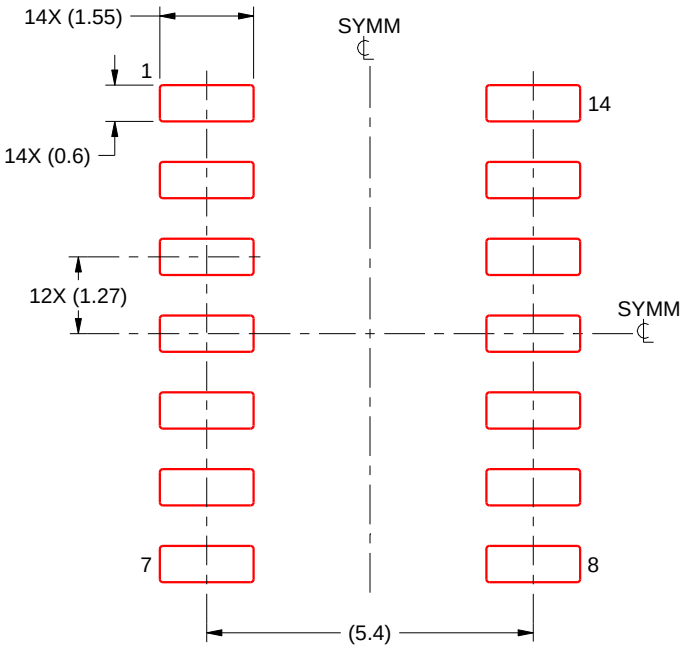
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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