INAx133 High-Speed, Precision Difference Amplifiers

1 Features

- Single, dual versions
- Low offset voltage: ±450µV (maximum)
- Low offset voltage drift: ±5µV/°C (maximum)
- Low gain error: 0.05% (maximum)
- Wide bandwidth: 1.5MHz
- High slew rate:
  - 5V/µs (CSO: SHE)
  - 20V/µs (CSO: RFB)
- Fast settling time: 5.5µs to 0.01%
- Low quiescent current: 950µA
- Wide supply range: ±2.25V to ±18V

2 Applications

- Battery cell formation & test equipment
- Sensor tag & data logger
- Servo drive position feedback
- Level transmitter
- String inverter

3 Description

The INA133 and INA2133 are high slew rate, unity gain difference amplifiers made up of a precision operational amplifier with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent tracking of resistors (TCR) maintains gain accuracy and common-mode rejection over temperature. The INAx133 operates over a wide supply range, ±2.25V to ±18V (+4.5V to +36V single supply), and that input common-mode voltage range extends beyond the positive and negative supply rails.

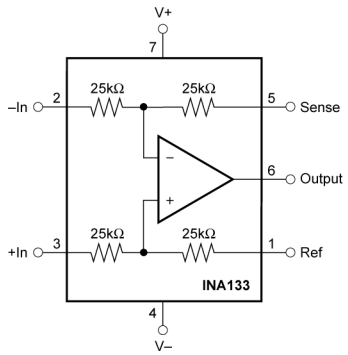
The differential amplifier is the foundation of many commonly used circuits. The INAx133 provides this precision circuit function for cost-optimized designs.

The single INA133 version is available in the SOIC-8 surface mount package. The dual INA2133 version is available in SOIC-14 package. Both are specified for operation over the industrial temperature range −40°C to +85°C.

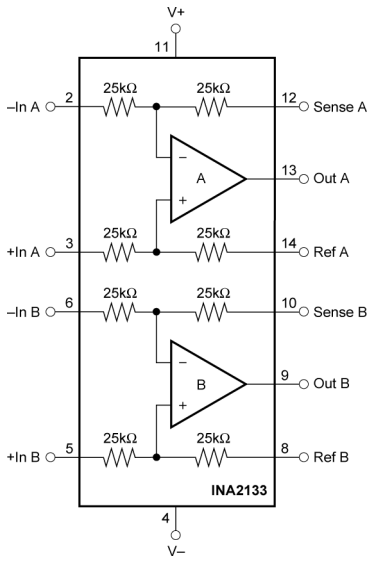
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA133	D (SOIC, 8)	4.90mm × 6.00mm
INA2133	D (SOIC, 14)	8.65mm × 6.00mm

(1) For all available packages, see the orderable addendum in Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



INA133 Simplified Internal Schematic



INA2133 Simplified Internal Schematic

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Table of Contents

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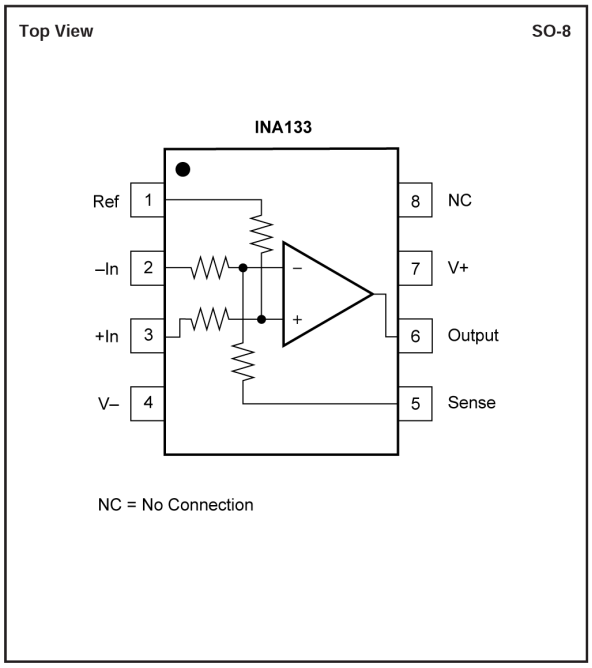
4 Pin Configuration and Functions



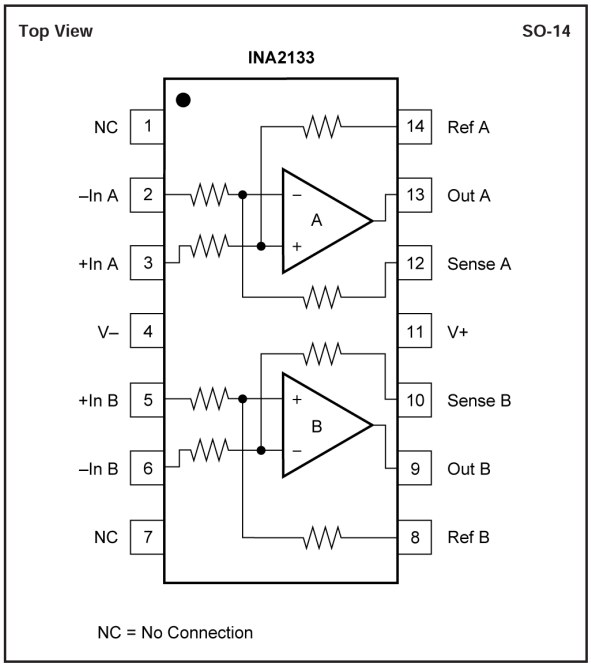


Table 4-1. Pin Functions: INA133

NAME	NO.	TYPE	DESCRIPTION
+In	3	Input	Positive (noninverting) input 25kΩ resistor to noninverting terminal of op amp
-In	2	Input	Negative (inverting) input 25kΩ resistor to inverting terminal of op amp
Output	6	Output	Output
Ref	1	Input	Reference input 25kΩ resistor to noninverting terminal of op amp
V+	7	–	Positive (highest) power supply
V-	4	–	Negative (lowest) power supply
Sense	5	Input	Sense input 25kΩ resistor to inverting terminal of op amp
NC	8	–	No internal connection (can be left floating)

Table 4-2. Pin Functions: INA2133

NAME	NO.	TYPE	DESCRIPTION
+In A	3	Input	Positive (noninverting) input, Channel A 25kΩ resistor to noninverting terminal of op amp
-In A	2	Input	Negative (inverting) input, Channel A 25kΩ resistor to inverting terminal of op amp
+In B	5	Input	Positive (noninverting) input, Channel B 25kΩ resistor to non-inverting terminal of op amp
-In B	6	Input	Negative (inverting) input, Channel B 25kΩ resistor to inverting terminal of op amp
Out A	13	Output	Output, Channel A
Out B	9	Output	Output, Channel B
Ref A	14	Input	Reference input, Channel A 25kΩ resistor to noninverting terminal of op amp
Ref B	8	Input	Reference input, Channel B 25kΩ resistor to noninverting terminal of op amp
Sense A	12	Input	Sense input, Channel A 25kΩ resistor to inverting terminal of op amp
Sense B	10	Input	Sense input, Channel B 25kΩ resistor to inverting terminal of op amp
V+	11	–	Positive (highest) power supply
V-	4	–	Negative (lowest) power supply

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5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 8.1.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	36	V
Signal input pins	Input pins	0	2 x V_S	V
	Sense, and REF pins	0	V_S	
Output short-circuit(2)		Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–55	125	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S/2, one channel per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single supply	4.5	30	36	V
	Dual supply	±2.25	±15	±18	
Specified temperature		–40		85	°C

5.3 Thermal Information

THERMAL METRIC(1)		INA133 8 PINS D (SOIC)	INA2133 14 PINS D (SOIC)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.9	71.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.9	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	31.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.7	30.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.4 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to ground, V_{REF} = 0V, G = 1, applies to all packages and part variants, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage	RTO(1) (2), V_{CM} = 0V		U variant		±150	±450	µV
				UA variant		±150	±900	
		RTO(1) (2), V_{CM} = 0V, V_S = ±5V		U variant		±300	±750	
				UA variant		±300	±1500	
	Offset voltage drift	RTO(1) (2), T_A = –40°C to +85°C				±2	±5	µV/°C
				V_S = ±5V		±2		
PSRR	Power-supply rejection ratio	RTO(1) (2), V_S = ±2.25V to ±18V		U variant		±10	±30	µV/V
				UA variant	850	900	950	
	Long-term stability	RTO(1) (2)				0.3		µV/√mo
Z_{IN-DM}	Differential impedance (3)					50		kΩ
Z_{IN-CM}	Common-mode impedance(3)	V_{CM} = 0V				25		kΩ
V_{CM}	Common-mode voltage range(4)	V_O = 0V, V_S = ±15V and V_S = ±5V		Positive	2 x (V+) – 3	2 x (V+) – 2		V
				Negative	2 x (V–) + 3	2 x (V–) + 2		
CMRR	Common-mode rejection ratio	V_S = ±15V and V_S = ±5V, V_{CM} = 2 x (V–) + 3 to 2 x (V+)–3, R_S = 0Ω		U variant	80	90		dB
				UA variant	74	90		
NOISE VOLTAGE								
e_N	Voltage noise	RTO(2) (5)	f = 0.01Hz to 10Hz	CSO: SHE		2		$µV_{PP}$
			f = 10Hz	CSO: SHE		80		nV/√Hz
				CSO: RFB		40		
			f = 100Hz	CSO: SHE		60		
				CSO: RFB		21		
			f = 1kHz	CSO: SHE		57		
				CSO: RFB		20		
GAIN								
G	Initial gain	V_S = ±15V and V_S = ±5V				1		V/V
GE	Gain error	V_S = ±15V and V_S = ±5V, (V-) + 1V ≤ V_O ≤ (V+) - 1.5V		U variant		±0.02	±0.05	%
				UA variant		±0.02	±0.1	
	Gain drift	T_A = –40°C to +85°C				±1	±10	ppm/°C
	Gain nonlinearity	V_S = ±15V and V_S = ±5V, (V-) + 1V ≤ V_O ≤ (V+) - 1.5V		U variant		±0.0001	±0.001	% of FSR
				UA variant		±0.0001	±0.002	
OUTPUT								
V_O	Output voltage, gain error < 0.1%	Positive, V_S = ±15V and V_S = ±5V			(V+) - 1.5	(V+) - 1.3		V
				R_L = 100kΩ		(V+) - 0.8		
		Negative, V_S = ±15V and V_S = ±5V			(V-) + 1	(V-) - 0.8		
				R_L = 100kΩ		(V-) + 0.3		
	Capacitive load (stable operation)					1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2	Sourcing	CSO: SHE		32		mA
				CSO: RFB		70		
			Sinking	CSO: SHE		25		
				CSO: RFB		70		

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at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to ground, V_{REF} = 0V, G = 1, applies to all packages and part variants, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB				1.5		MHz
SR	Slew rate	CSO: SHE			5		V/µs
		CSO: RFB			20		
t_S	Settling time	V_{STEP} = 10V, C_L = 100pF	0.1%		4		µs
			0.01%		5.5		
	Overload recovery time	50% Overdrive			4		µs
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0A			±0.95	±1.2	mA
			V_S = ±5V		±0.92	±1.2	

(1) Referred to output in unity-gain difference configuration.
(2) Includes effects of input bias and offset currents of the amplifier.
(3) 25kΩ resistors are ratio matched but have ±20% absolute value.
(4) Maximum input voltage without protection is 10V more than either ±15V supply (±25V). Limit I_{IN} to 1mA.
(5) Includes effects of input current noise of the amplifier and thermal noise contribution of resistor network.

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5.5 Typical Characteristics

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ connected to ground, V_{REF} = 0 V, and all chip site origins (CSO), unless otherwise noted.

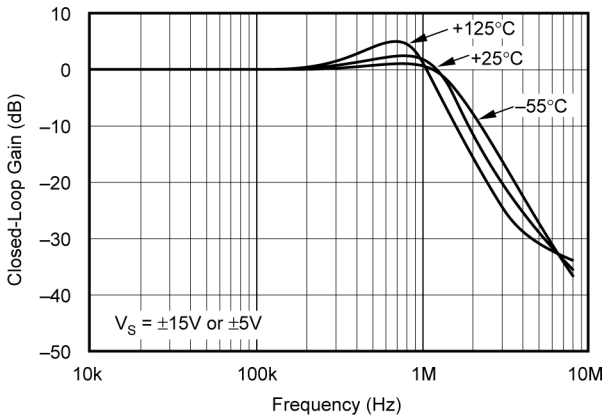


Figure 5-1. Gain vs Frequency

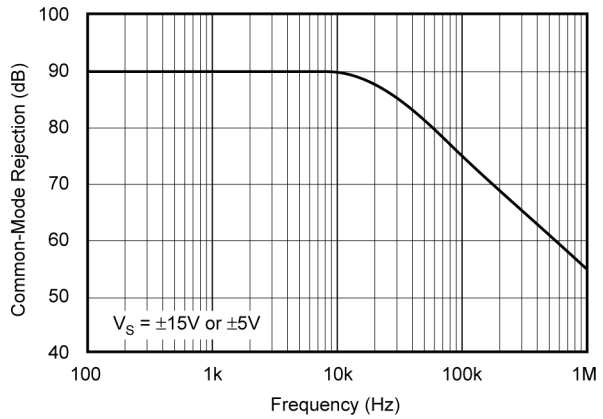


Figure 5-2. Common-Mode Rejection vs Frequency

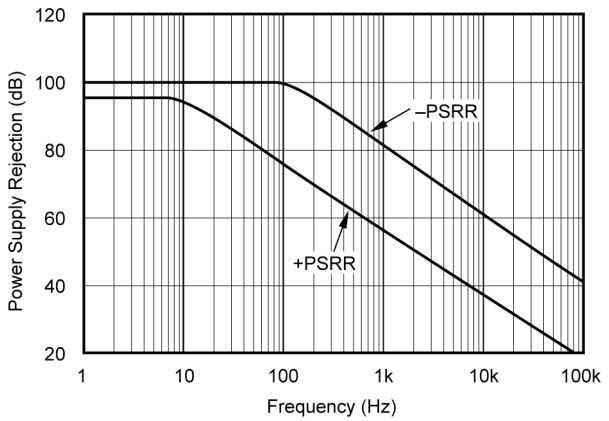


Figure 5-3. Power Supply Rejection vs Frequency

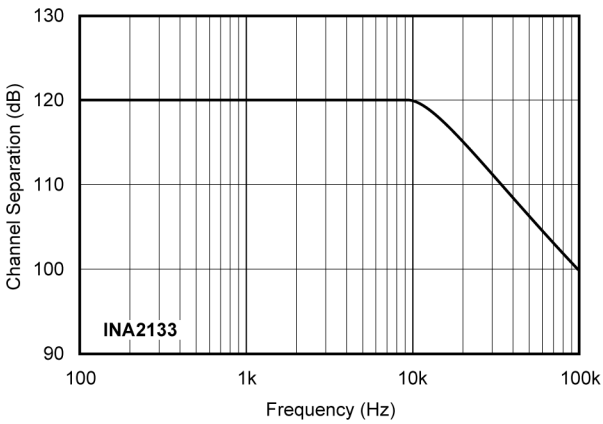


Figure 5-4. Channel Separation vs Frequency

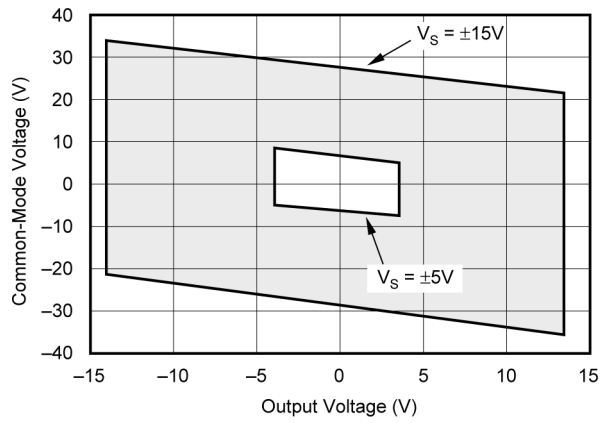
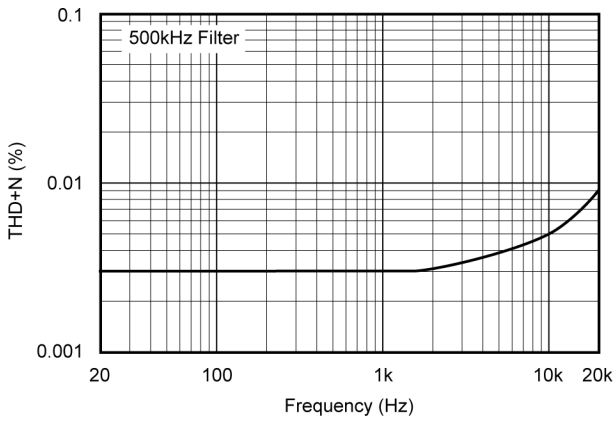


Figure 5-5. Input Common-Mode Voltage vs Output Voltage



CSO: SHE

Figure 5-6. Total Harmonic Distortion + Noise vs Frequency

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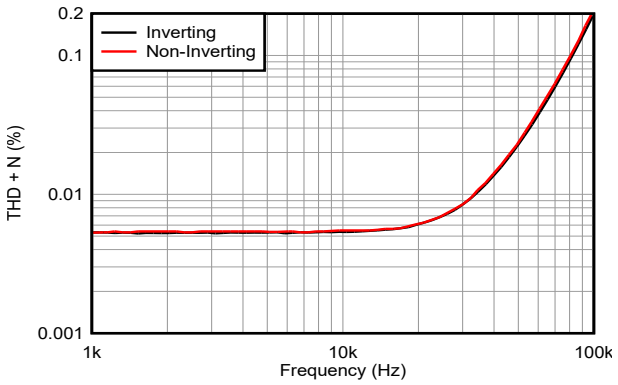
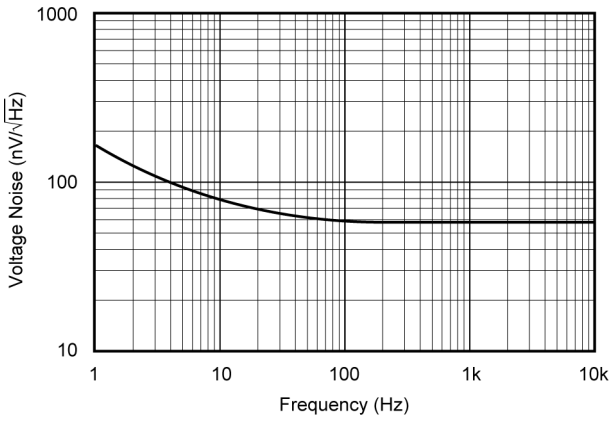
5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ connected to ground, V_{REF} = 0 V, and all chip site origins (CSO), unless otherwise noted.



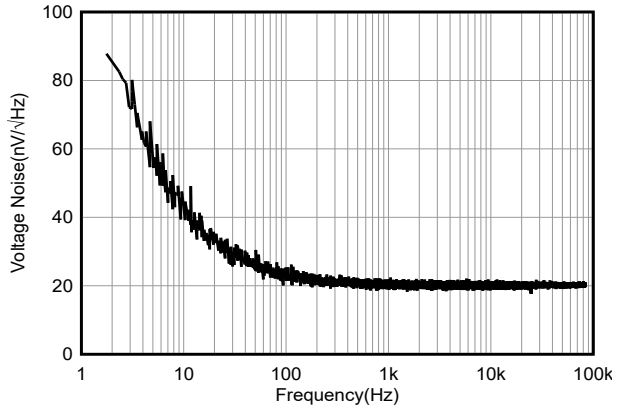
CSO: RFB

Figure 5-7. Total Harmonic Distortion + Noise vs Frequency



CSO: SHE

Figure 5-8. Voltage Noise Density vs Frequency



CSO: RFB

Figure 5-9. Voltage Noise Density vs Frequency

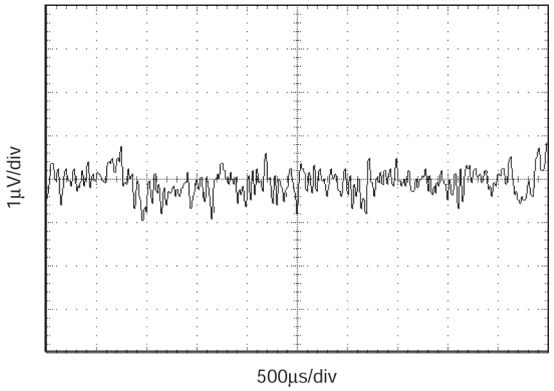


Figure 5-10. 0.1 Hz to 10 Hz Peak-to-Peak Voltage Noise

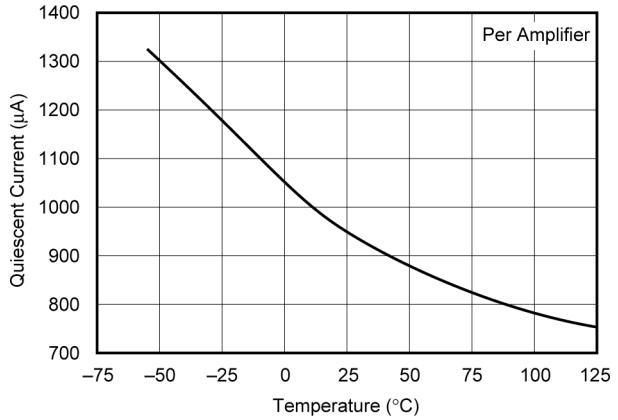
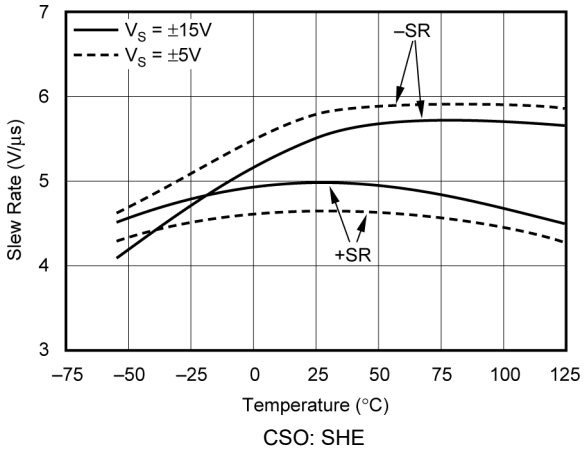


Figure 5-11. Quiescent Current vs Temperature



CSO: SHE

Figure 5-12. Slew Rate vs Temperature

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5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ connected to ground, V_{REF} = 0 V, and all chip site origins (CSO), unless otherwise noted.

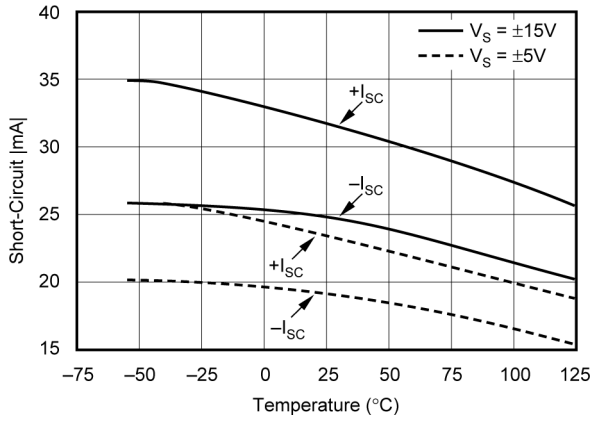

Figure 5-13. Short-Circuit Current vs Temperature

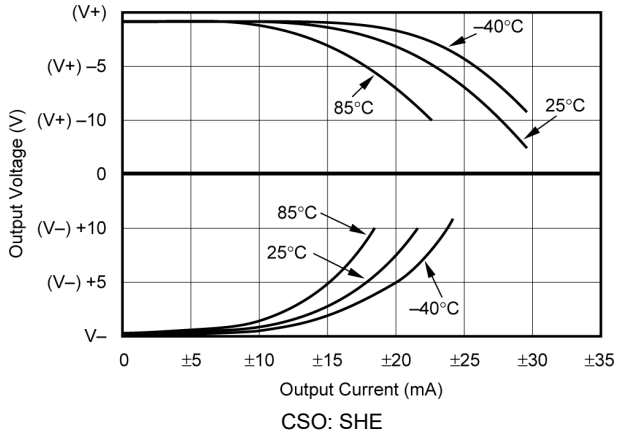

Figure 5-14. Output Voltage Swing vs Output Current

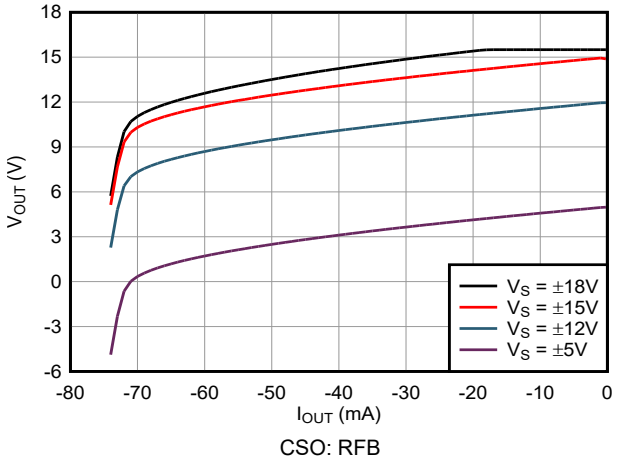

Figure 5-15. Output Voltage Swing vs Output Current (Sinking)

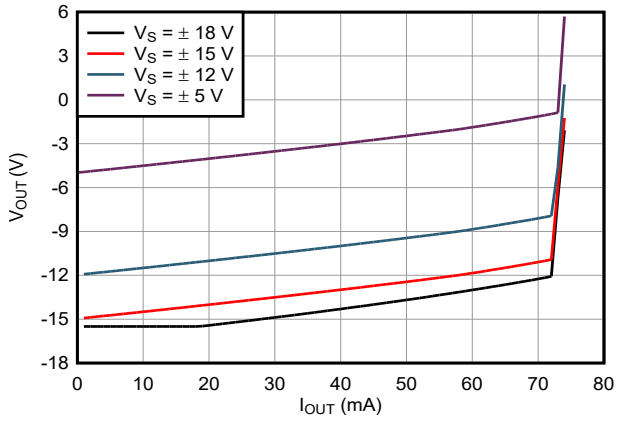

Figure 5-16. Output Voltage Swing vs Output Current (Sourcing)

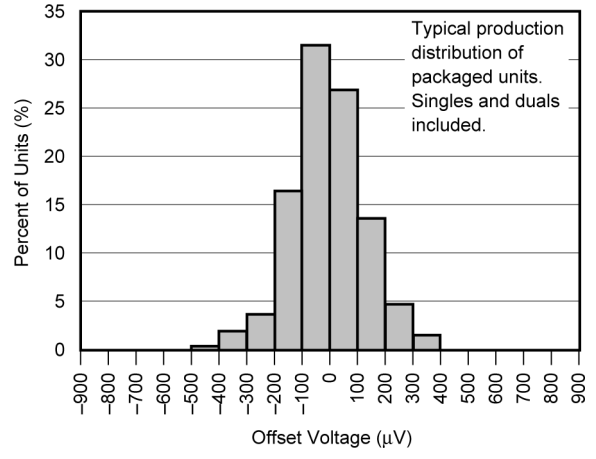

Figure 5-17. Offset Voltage Production Distribution V_S = ±15V

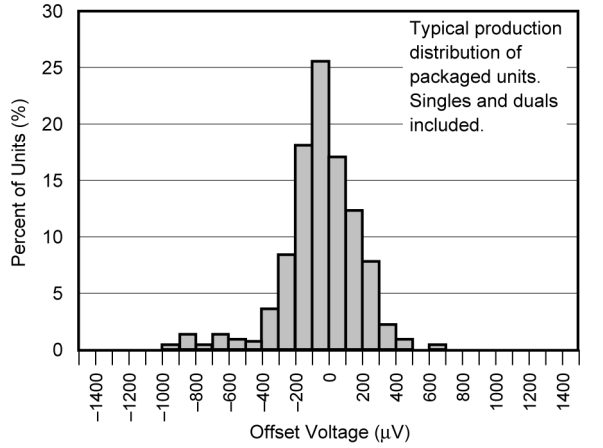

Figure 5-18. Offset Voltage Production Distribution V_S = ±5V

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5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ connected to ground, V_{REF} = 0 V, and all chip site origins (CSO), unless otherwise noted.

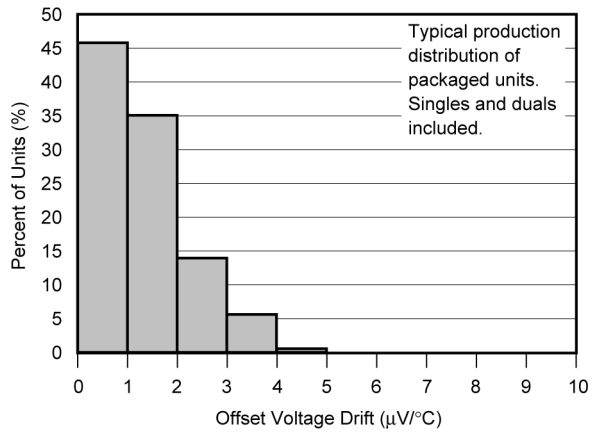


Figure 5-19. Offset Voltage Drift Production Distribution V_S = ±15V

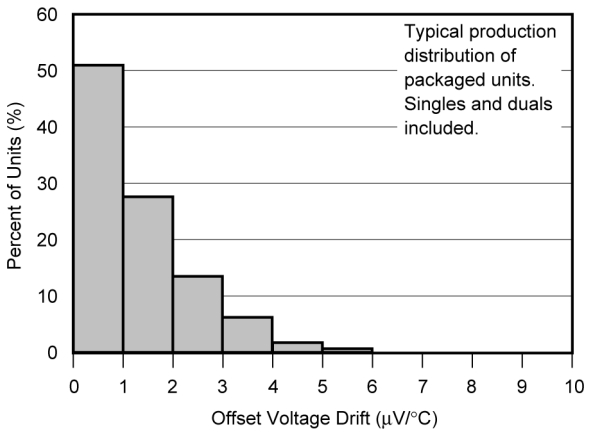


Figure 5-20. Offset Voltage Drift Production Distribution V_S = ±5V

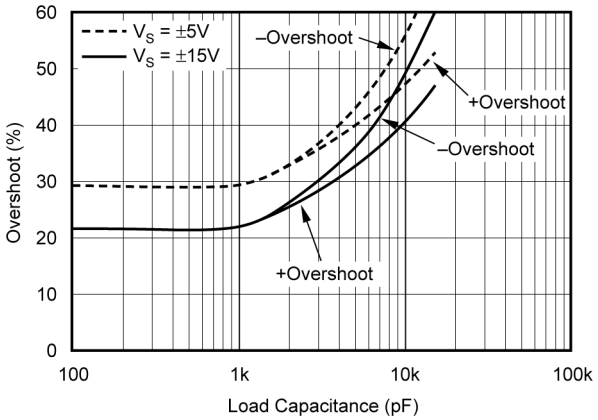


Figure 5-21. Small-Signal Overshoot vs Load Capacitance

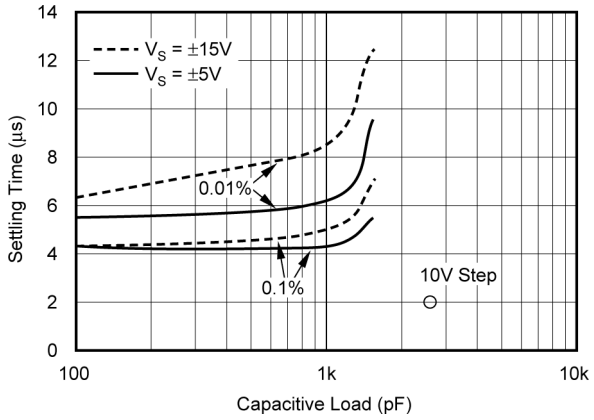


Figure 5-22. Settling Time vs Load Capacitance

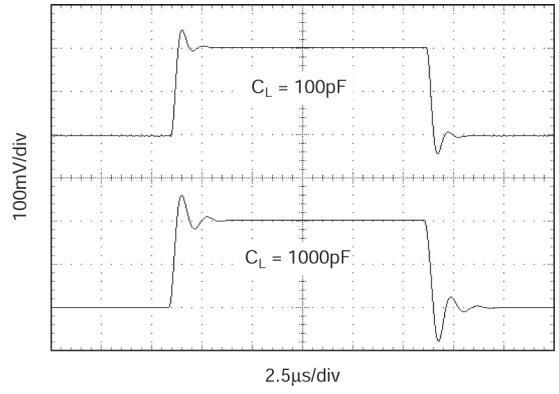
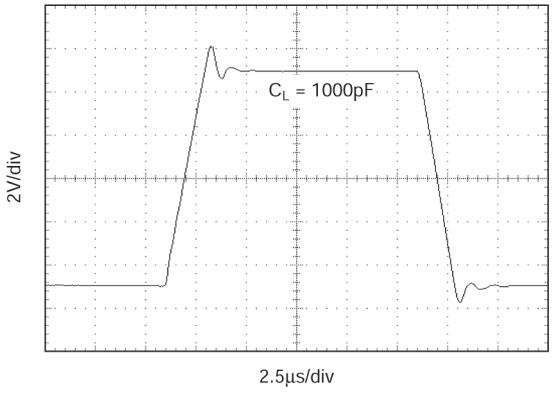


Figure 5-23. Small-Signal Step Response



CSO: SHE

Figure 5-24. Large-Signal Step Response

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5.5 Typical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ connected to ground, V_{REF} = 0 V, and all chip site origins (CSO), unless otherwise noted.

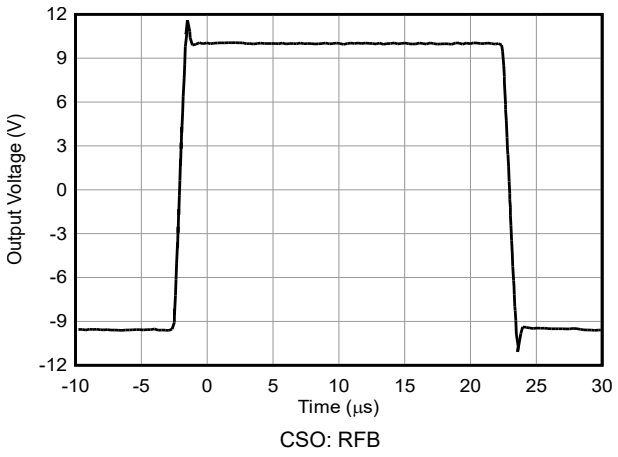

Figure 5-25. Large-Signal Step Response

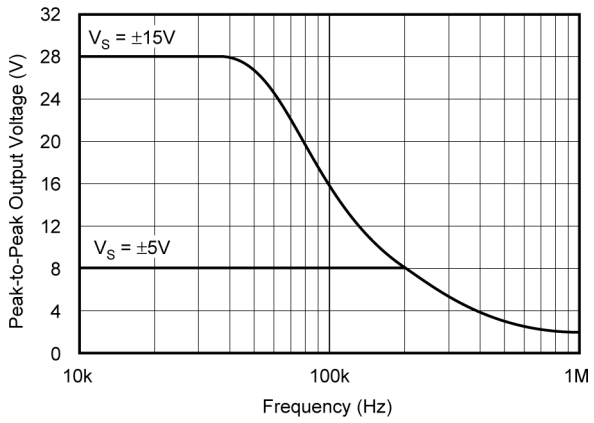

Figure 5-26. Maximum Output Voltage vs Frequency

6 Detailed Description

6.1 Overview

The INAx133 has a high-precision operational amplifier and four trimmed, on-chip resistors. The device can be configured to make a wide variety of amplifier configurations, including difference, noninverting, and inverting configurations. The integrated, matched resistors provide an advantage over discrete implementation.

Much of the DC performance of op amp circuits depends on the accuracy of the surrounding resistors. The resistors on the INAx133 are laid out to be tightly matched. The resistors of each part are matched on-chop and tested for matching accuracy. As a result, the INAx133 provides high accuracy for specifications such as gain drift, common-mode rejection ratio, and gain error.

6.2 Functional Block Diagram

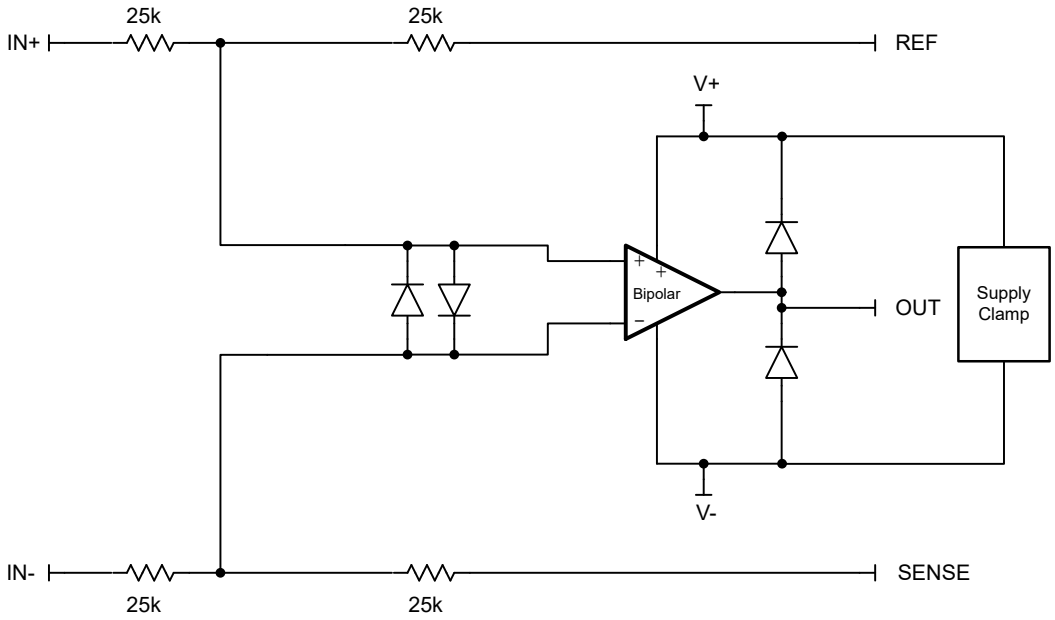

Figure 6-1. INA133 Internal Schematic for CSO:SHE

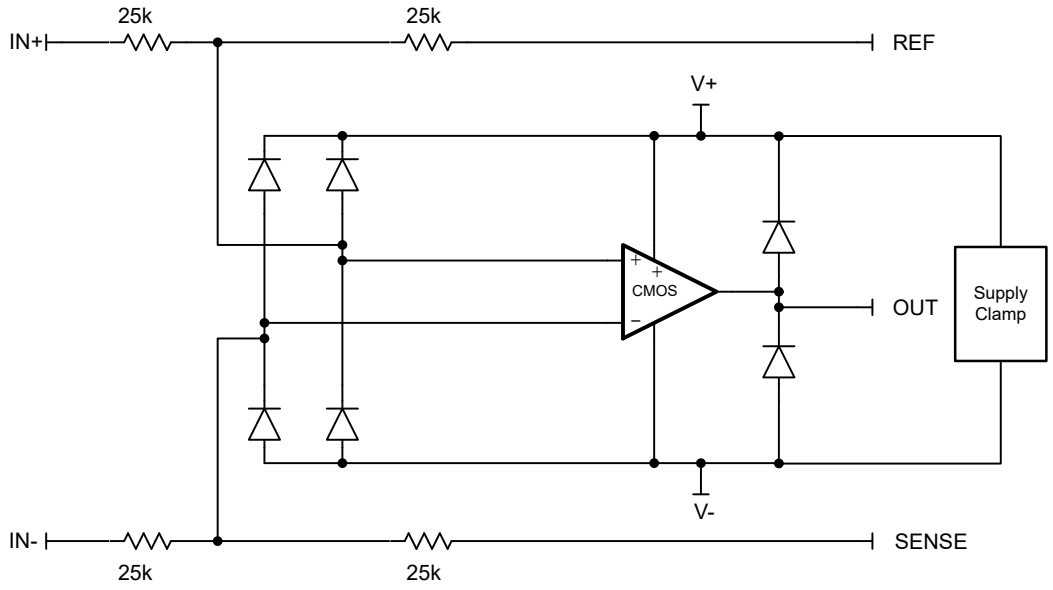

Figure 6-2. INA133 Internal Schematic for CSO: RFB

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6.3 Feature Description

6.3.1 Gain Error and Drift

Gain error in the INAx133 is limited by the mismatch of the integrated precision resistors. Gain drift is limited by the slight mismatch of the temperature coefficient of integrated resistors. The integrated resistors are precision-matched with low temperature coefficient resistors to improve overall gain drift compared to the discrete implementation of differences amplifiers build when using external resistors.

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6.3.2 Input Voltage Range

The INAx133 difference amplifier is able to achieve a wide input common-mode voltage range by dividing down the input signal with a high-precision resistor divider. The internal resistors divide down the voltage before the voltage reaches the internal op amp and provide protection to the op amp inputs. Figure 6-3 shows an example of how the voltage division works in a difference-amplifier configuration.

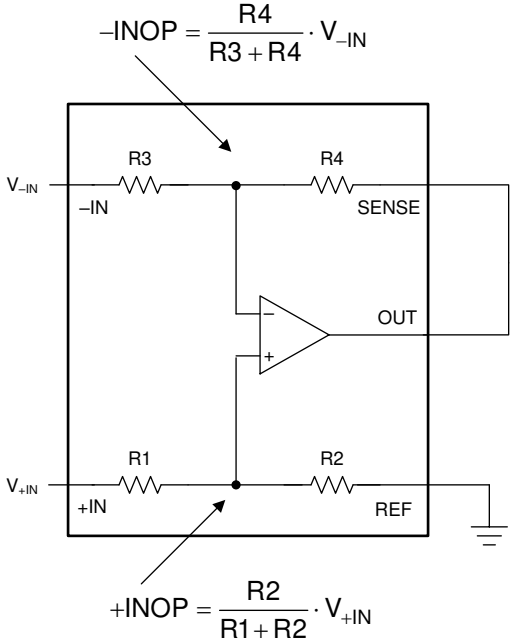

Figure 6-3. Voltage Division in the Difference Amplifier Configuration

6.4 Device Functional Modes

The INAx133 has one functional mode. The device is specified on a power supply of ±15V or ±5V and can operate on a power supply from ±2.25V to ±18V with derated performance. See *Typical Characteristics*.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The INA133 and INA2133 are high-speed difference amplifiers are designed for a wide range of general-purpose applications. Figure 7-2 shows the basic connections required for operation of the INA133. Place decoupling capacitors close to the device pins as shown in Figure 7-2 in applications with noisy or high impedance power supplies. All circuitry is completely independent in the dual version to provide lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 7-2, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to maintain good common-mode rejection. A 5Ω mismatch in source impedance degrades the common-mode rejection of a typical device to approximately 80dB (a 10Ω mismatch degrades CMR to 74dB). If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

The internal resistors of the INA133 are accurately ratio trimmed to match. That is, R_1 is trimmed to match R_2 and R_3 is trimmed to match R_4. However, the absolute values cannot be equal (R_1 + R_2 can be slightly different than R_3 + R_4). Thus, large series resistors on the input (greater than 250Ω), even if well matched, can degrade common-mode rejection.

Circuit board layout constraints can suggest possible variations in connections of the internal resistors, like that pins 1 and 3 can be interchanged. However, because of the ratio trimming technique used, CMRR can degrade. If pins 1 and 3 are interchanged, pins 2 and 5 must also be interchanged to maintain proper ratio matching.

7.1.1 Operating Voltage

The INA133 and INA2133 operate from single (+4.5V to +36V) or dual (±2.25V to ±18V) supplies with excellent performance. Specifications are production tested with ±5V and ±15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the *Typical Characteristics*.

7.1.2 Input Voltage

The INA133 and INA2133 can accurately measure differential signals that are above and below the supply rails. Linear common-mode range extends from 2 × (V+)−3V to 2 × (V−) +3V (nearly twice the supplies). See Figure 5-5.

7.1.3 Offset Voltage Trim

The INA133 and INA2133 are laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 7-1 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal is summed with the output signal. This can be used to null offset voltage as shown in Figure 7-1. To maintain good common-mode rejection, keep the source impedance of a signal applied to the Ref terminal less than 10Ω.

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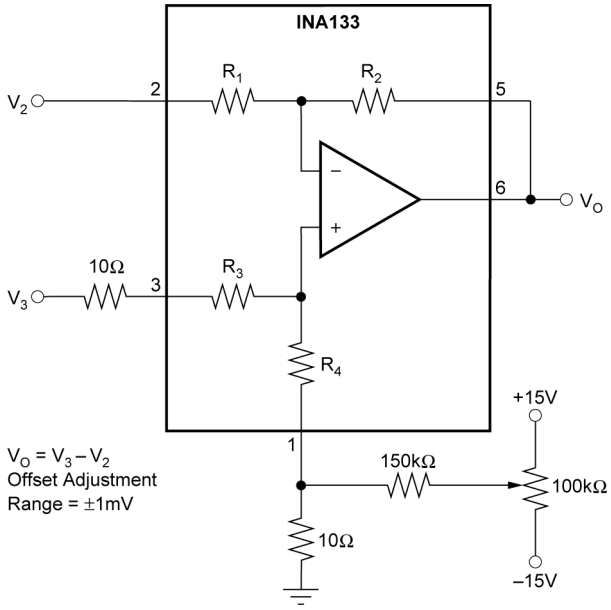

Figure 7-1. Offset Adjustment

7.2 Typical Application

The INAx133 can be used in a variety of applications. Figure 7-2 shows one example.

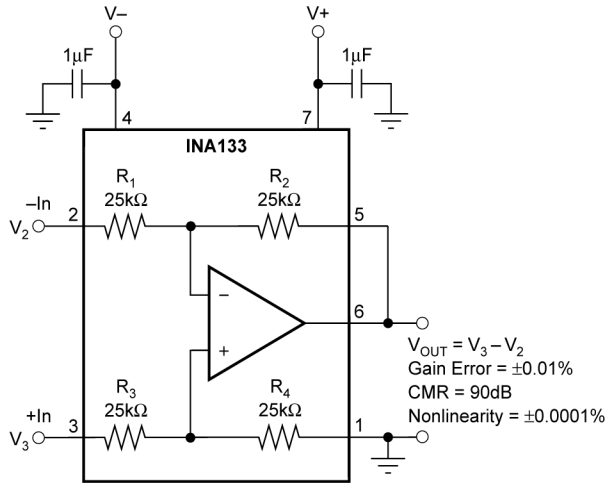

Figure 7-2. Precision Difference Amplifier (Basic Power Supply and Signal Connections)

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7.3 Additional Applications

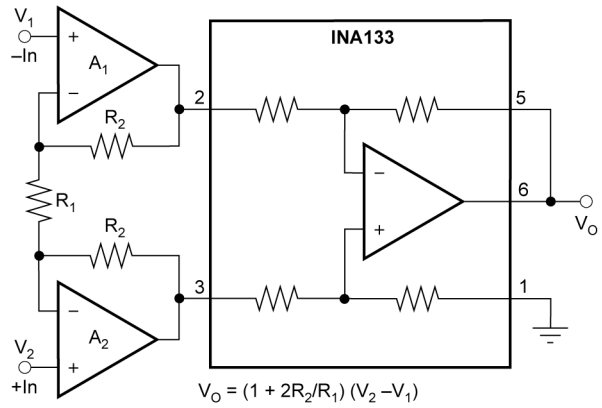
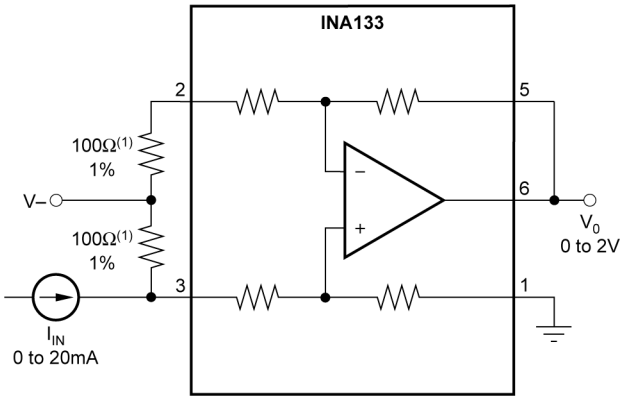


Figure 7-3. Precision Instrumentation Amplifier



NOTE: (1) Input series resistors should be less than 250Ω (1% max mismatch) to maintain excellent CMR. With 100Ω resistors, gain error is increased to 0.5%.

Figure 7-4. Current Receiver With Compliance to Rails

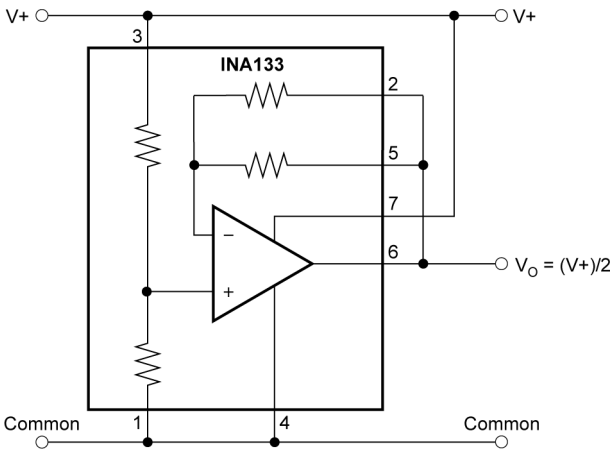


Figure 7-5. Pseudoground Generator

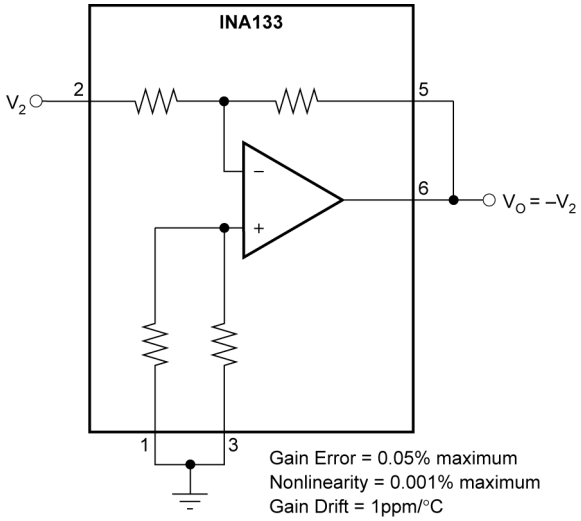


Figure 7-6. Precision Unity-Gain Inverting Amplifier

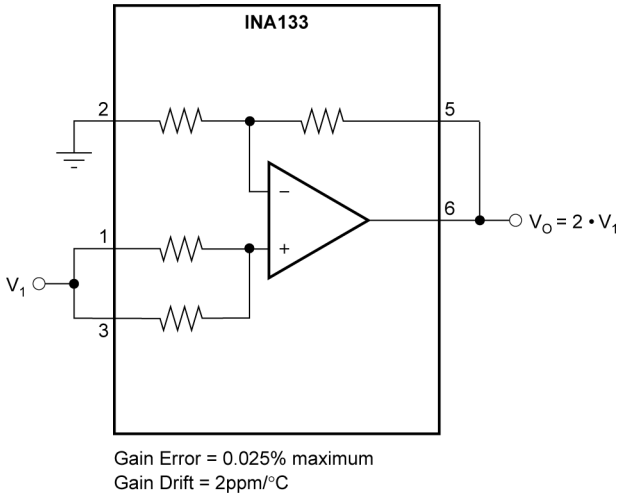


Figure 7-7. Precision Gain = 2 Amplifier

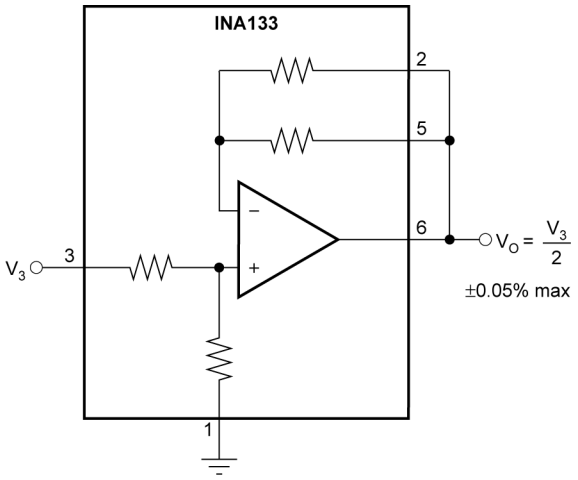


Figure 7-8. Precision Gain = 1/2 Amplifier

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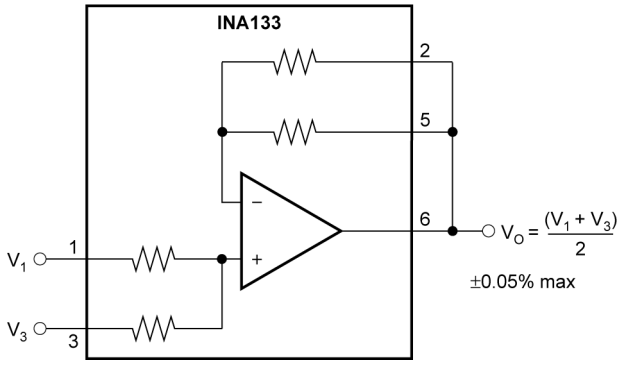

Figure 7-9. Precision Average Value Amplifier

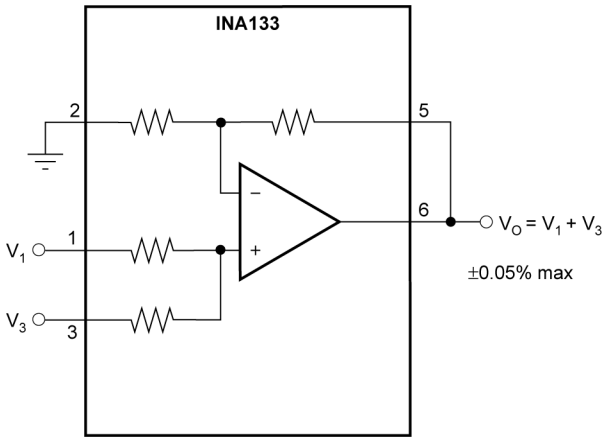

Figure 7-10. Precision Summing Amplifier

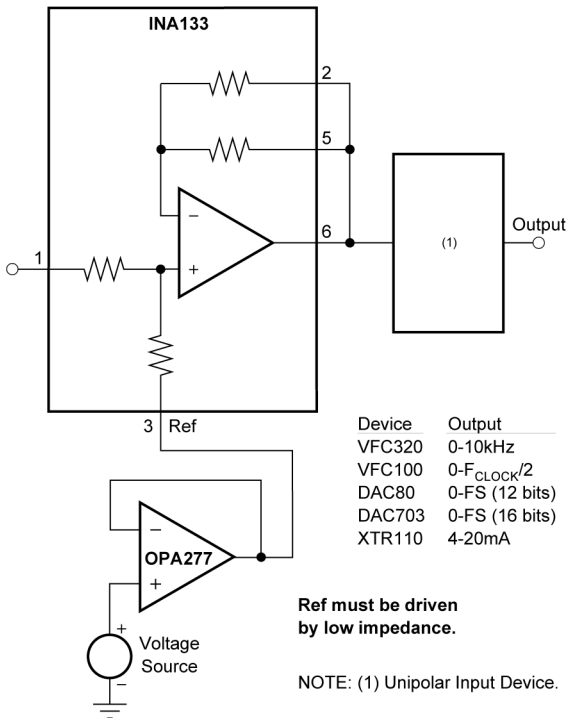

Figure 7-11. Precision Bipolar Offsetting

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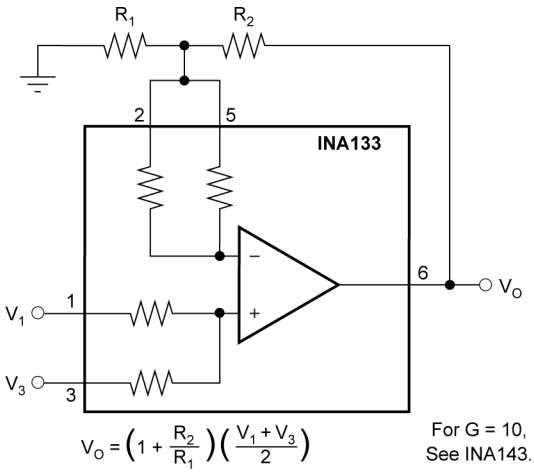

Figure 7-12. Precision Summing Amplifier With Gain

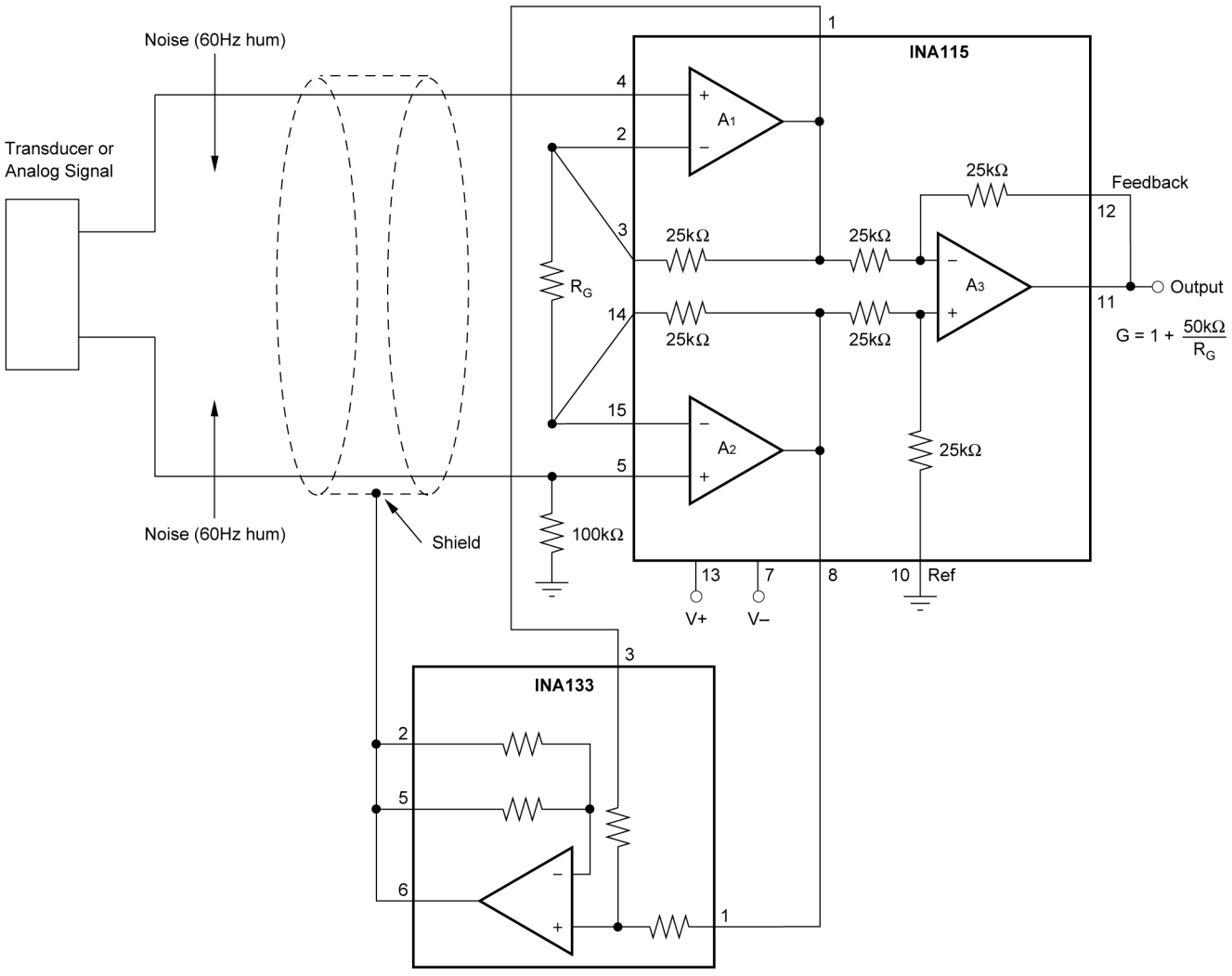

Figure 7-13. Instrumentation Amplifier Guard Drive Generator

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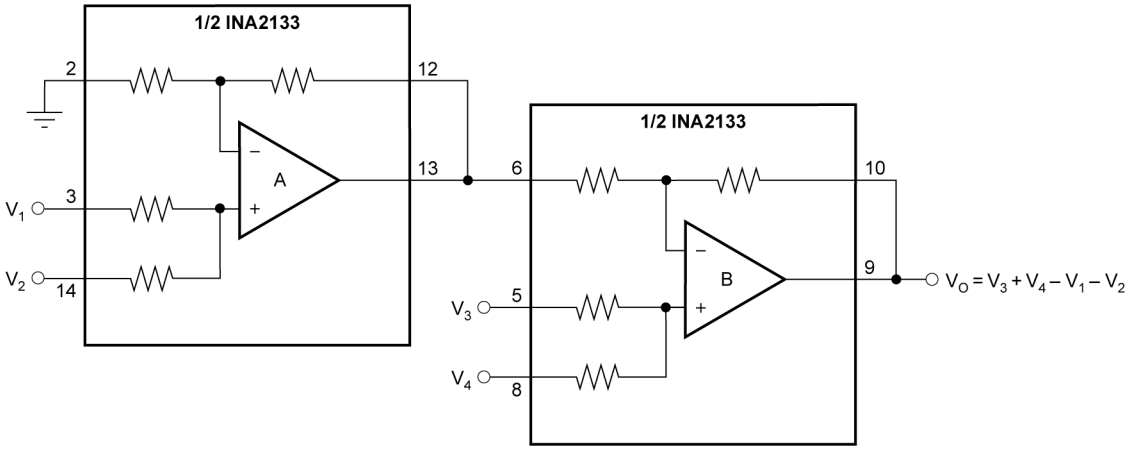

Figure 7-14. Precision Summing Instrumentation Amplifier

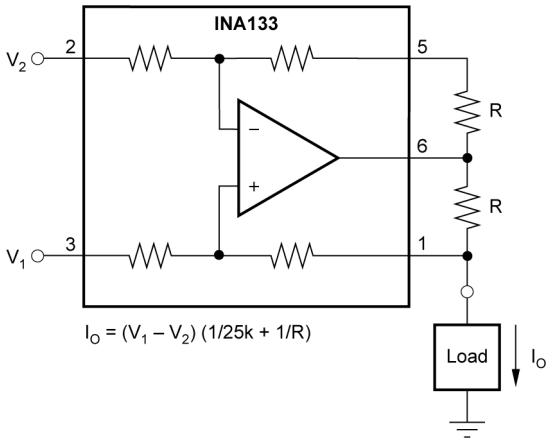

Figure 7-15. Precision Voltage-to-Current Converter With Differential Inputs

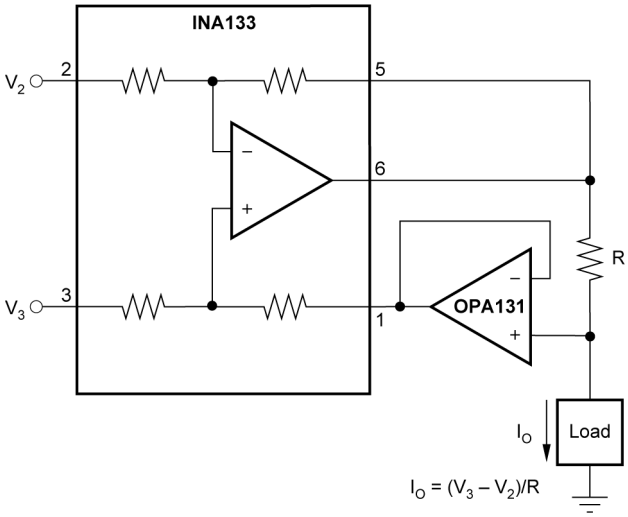

Figure 7-16. Differential Input Voltage-to-Current Converter for Low I_{OUT}

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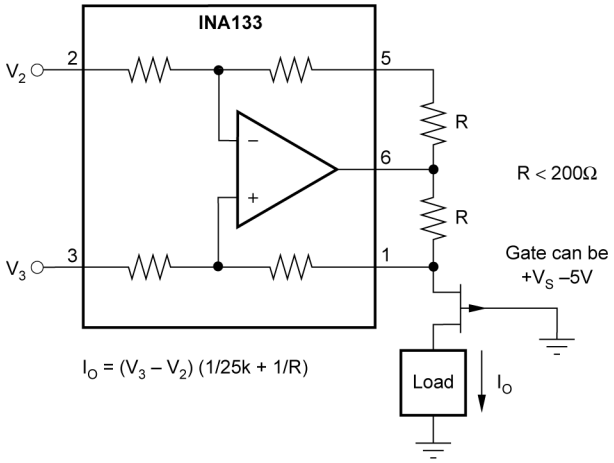

Figure 7-17. Isolating Current Source

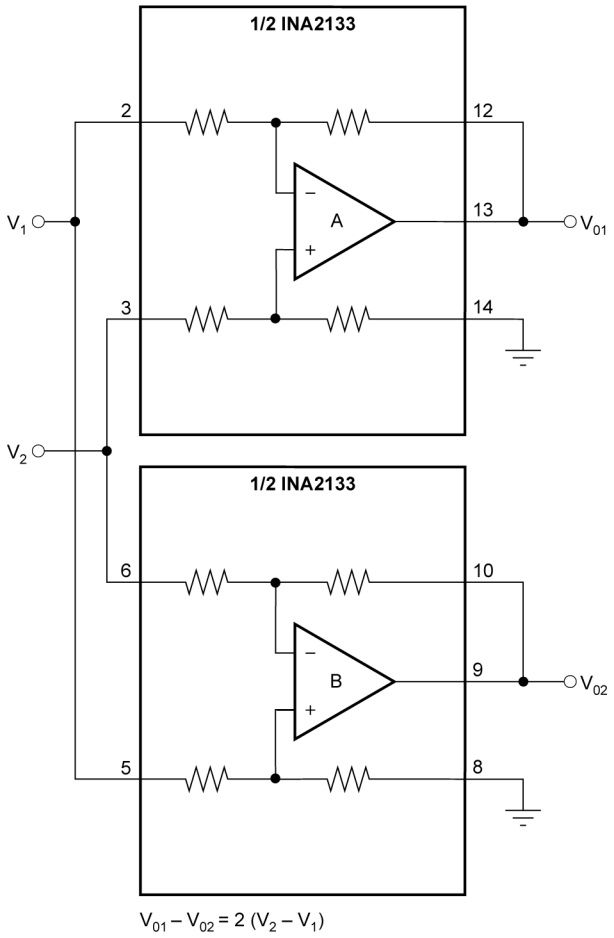

Figure 7-18. Differential Output Difference Amplifier

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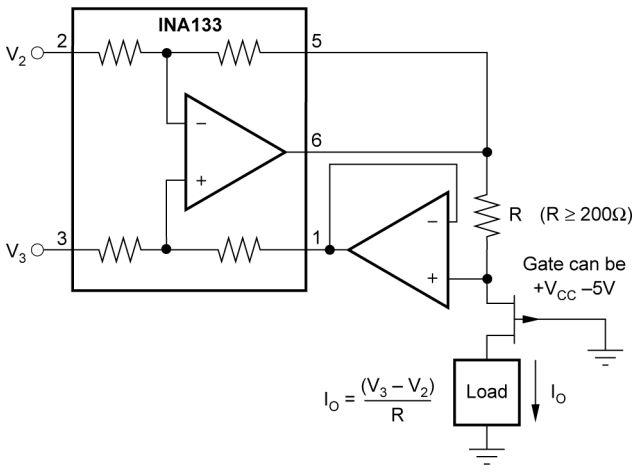

Figure 7-19. Isolating Current Source With Buffering Amplifier for Greater Accuracy

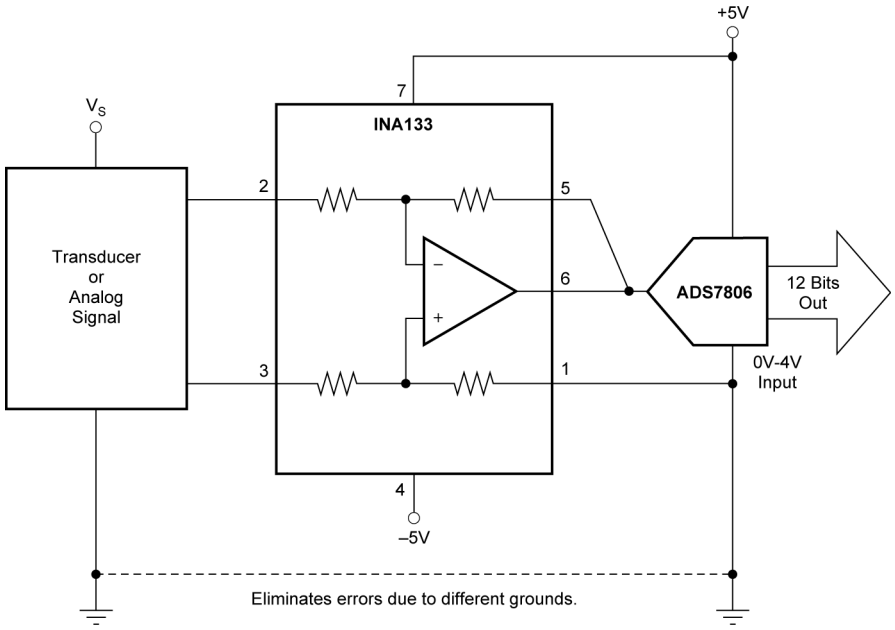

Figure 7-20. Differential Input Data Acquisition

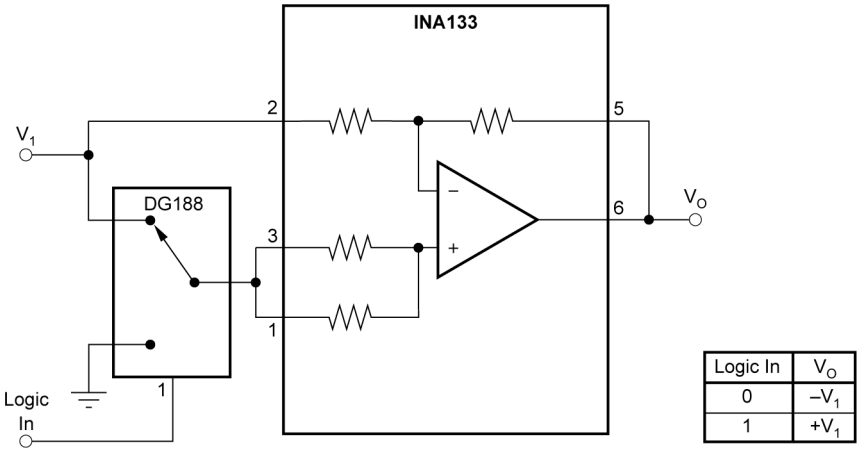

Figure 7-21. Digitally Controlled Gain of ±1 Amplifier

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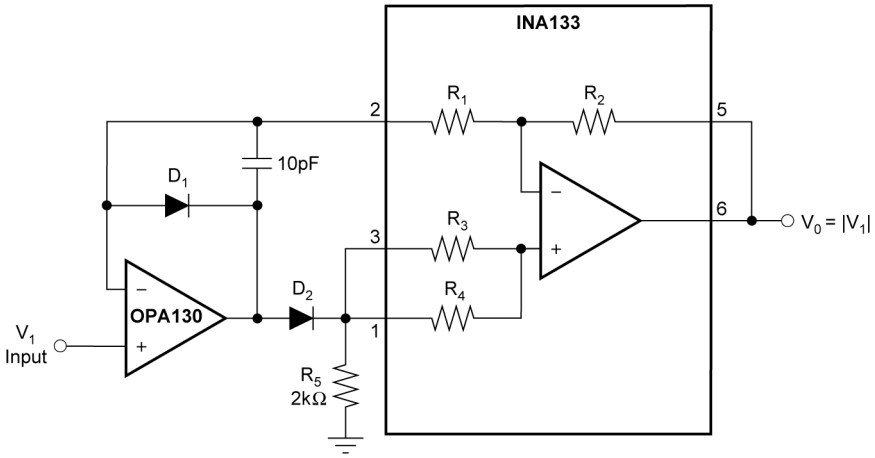

Figure 7-22. Precision Absolute Value Buffer

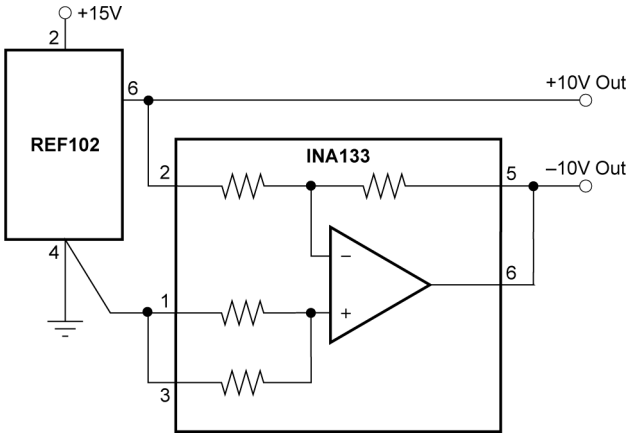

Figure 7-23. ±10V Precision Voltage Reference

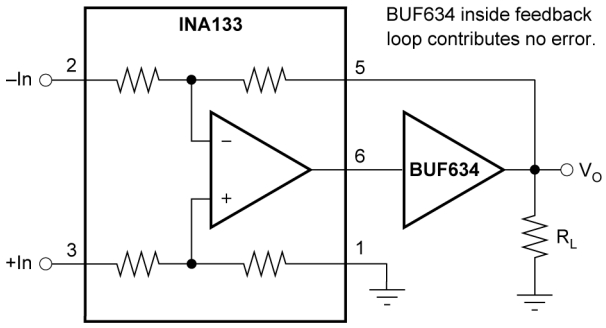

Figure 7-24. High Output Current Precision Difference Amplifier

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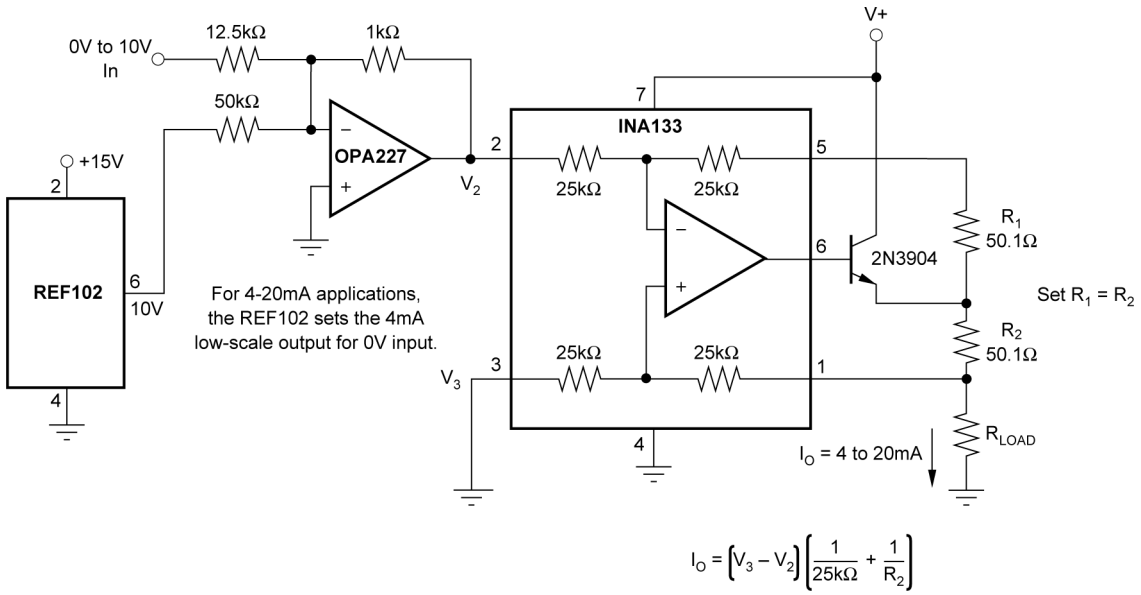

Figure 7-25. Precision Voltage-to-Current Conversion

7.4 Power Supply Recommendations

The nominal performance of the INA133 is specified with a supply voltage of ±15V or ±5V. The device operates using power supplies from ±2.25V to ±18V with varying performance. Parameters varying across the operating voltage and reference voltage range can be referenced in the *Typical Characteristics*.

TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Place the C_{BYP} as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Route the power supply trace through C_{BYP} before reaching the device power supply terminals. For more information, see *Layout Guidelines*.

7.5 Layout

7.5.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, route the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is preferred over crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

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7.5.2 Layout Examples

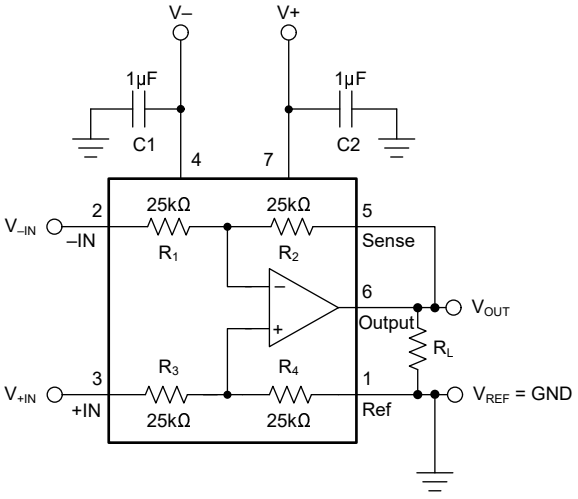

Figure 7-26. Example Schematic

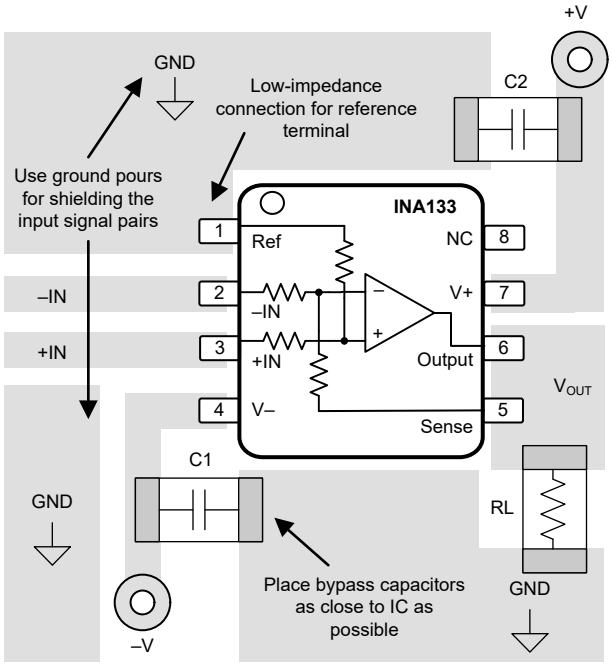

Figure 7-27. Associated PCB Layout for SOIC-8 Package

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

Part Number	Definition
INA133U/2K5 INA133UA/2K5	The die is manufactured in CSO: SHE or CSO: RFB.
INA133U INA133UA INA2133U INA2133UA	The die is manufactured in CSO: SHE.

8.1.2 Development Support

For development support on this product, see the following:

8.1.2.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.2.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2025) to Revision B (January 2025) — **Page**

- Added different fabrication process specification for slew rate in the *Features* 1
- Added description of device flow information in *Specifications* 4
- Added all chip site origins (CSO) condition to the typical test conditions in the *Electrical Characteristics* 5
- Changed output voltage typical from "(V+) - 0.8" to "(V-) - 0.8" in the *Electrical Characteristics* 5
- Added different fabrication process specifications for short circuit current, sinking and sourcing, in the *Electrical Characteristics* 5
- Separated sinking and sourcing for short circuit current in the Electrical Characteristics 5
- Changed 0.01% settling time test condition from "C_L = 1000pF" to "C_L = 100pF" in the Electrical Characteristics 5
- Changed quiescent current test condition from "I_O = 0V" to "I_O = 0A" in the *Electrical Characteristics* 5
- Added "CSO:SHE" to Total Harmonic Distortion + Noise vs Frequency, Voltage Noise Density vs Frequency, Slew Rate vs Temperature, Short-Circuit Current vs Temperature, Output Voltage Swing vs Output Current, and Large-Signal Step Response in the *Typical Characteristics* 7
- Added Total Harmonic Distortion + Noise vs Frequency, Voltage Noise Density vs Frequency, Output Voltage Swing vs Output Current (Sinking), Output Voltage Swing vs Output Current (Sourcing), and Large-Signal Step Response in the *Typical Characteristics* 7
- Added all chip site origins (CSO) condition to the typical test conditions in the *Typical Characteristics* 7
- Change and added INA133 Internal Schematic for each fabrication process in the *Functional Block Diagram* 12
- Changed "INA105" to "INA133" in the *Power Supply Recommendations* 25

Changes from Revision * (June 1999) to Revision A (March 2025) — **Page**

- Updated the numbering and format for tables, figures, and cross-references throughout the document 1
- Added the Pin Configuration and Functions, Specifications, Recommended Operating Conditions, Thermal Information, Detailed Description, Overview, Functional Block Diagram, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Layout Guidelines, Layout Example, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections 1
- Changed the Package Information table 1
- Added *Pin Functions* table for INA133 and INA2133 3
- Added test conditions to *Electrical Characteristics* table 5
- Combined V_S=±15V and V_S=±5V specification table in *Electrical Characteristics* 5

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- Changed parameter name in *Electrical Characteristics* from *Offset Voltage Initial vs Temperature* to *Offset voltage drift* 5
- Changed parameter name in *Electrical Characteristics* from *Offset Voltage Initial vs Power Supply* to *Power supply rejection ratio* 5
- Changed parameter name in *Electrical Characteristics* from *Offset Voltage vs Time* to *Long-term stability* 5
- Changed parameter name in *Electrical Characteristics* from *Current Limit, Continous-to-Common* to *Short-circuit current* and added test condition 5
- Moved the power supply and temperature ranges from the *Electrical Characteristics* table to the *Recommended Operating Conditions* and *Absolute Maximum Ratings* table..... 5
- Changed the Applications section..... 15

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA133U	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 133U
INA133U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA 133U
INA133U/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 133U
INA133UA	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-	INA 133U A
INA133UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	INA (133U, 133UA) A
INA133UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA (133U, 133UA) A
INA2133U	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-55 to 125	INA2133U
INA2133U.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-55 to 125	INA2133U
INA2133UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-55 to 125	INA2133U A
INA2133UA.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-55 to 125	INA2133U A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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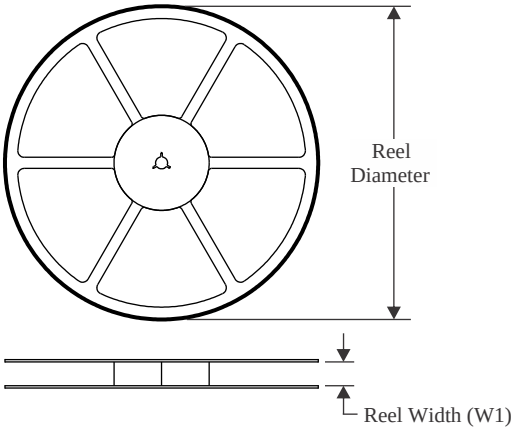
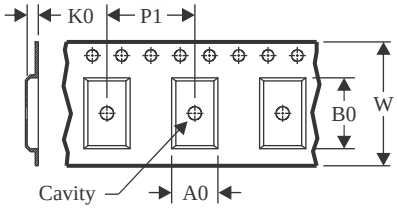
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

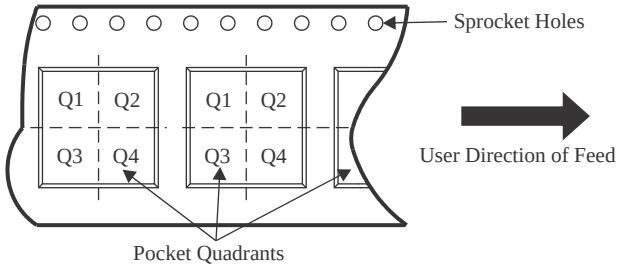


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

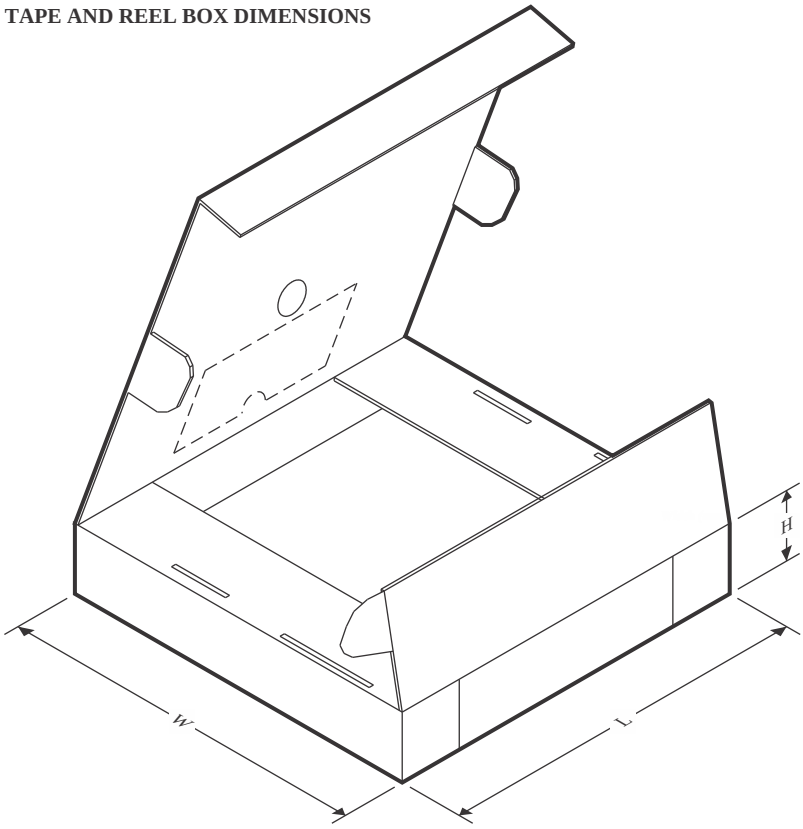
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA133U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA133UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

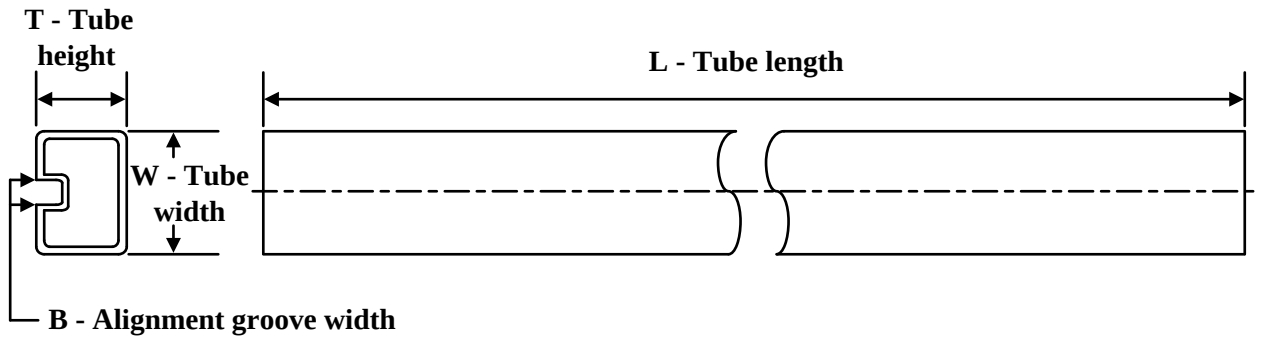
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

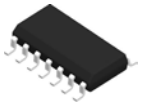
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA133U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA133UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA133U	D	SOIC	8	75	506.6	8	3940	4.32
INA133UA	D	SOIC	8	75	506.6	8	3940	4.32
INA2133U	D	SOIC	14	50	506.6	8	3940	4.32
INA2133U.A	D	SOIC	14	50	506.6	8	3940	4.32
INA2133UA	D	SOIC	14	50	506.6	8	3940	4.32
INA2133UA.A	D	SOIC	14	50	506.6	8	3940	4.32

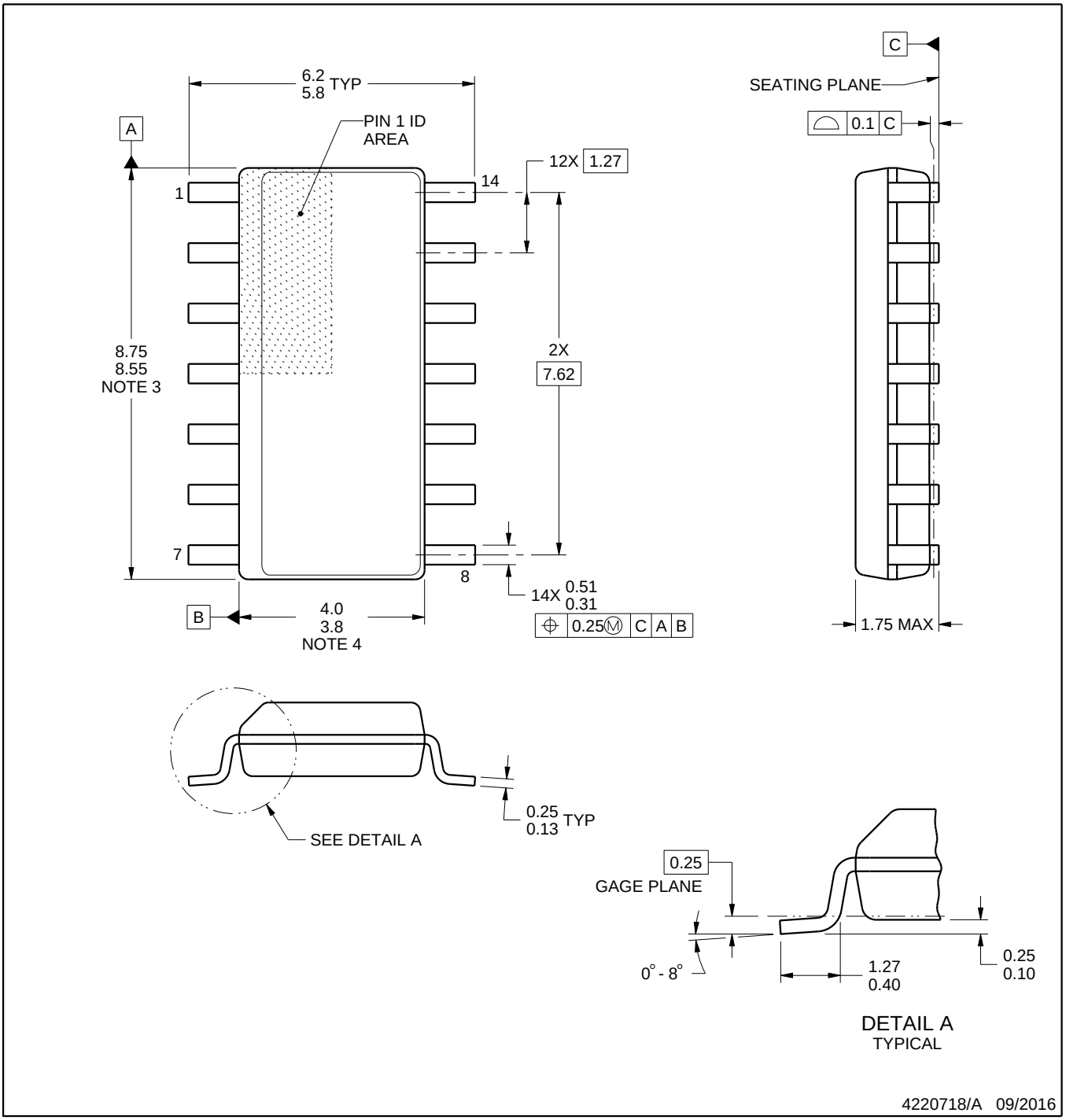


PACKAGE OUTLINE

D0014A

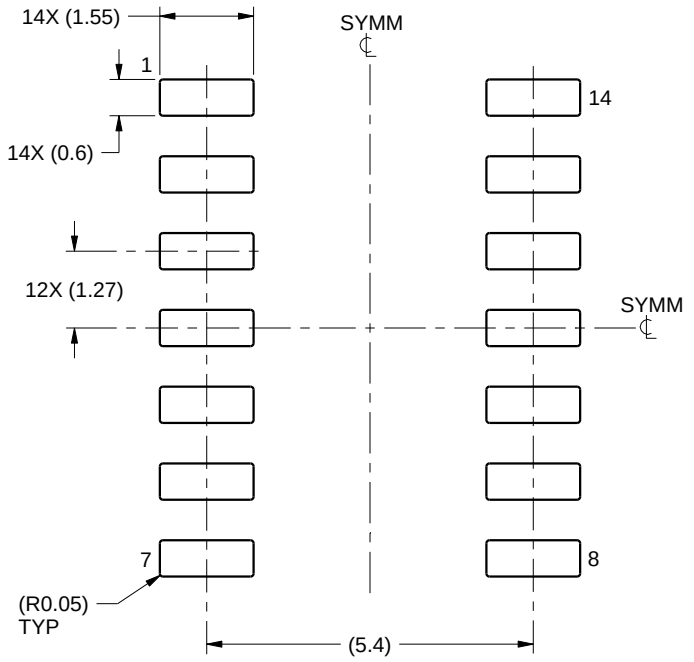
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

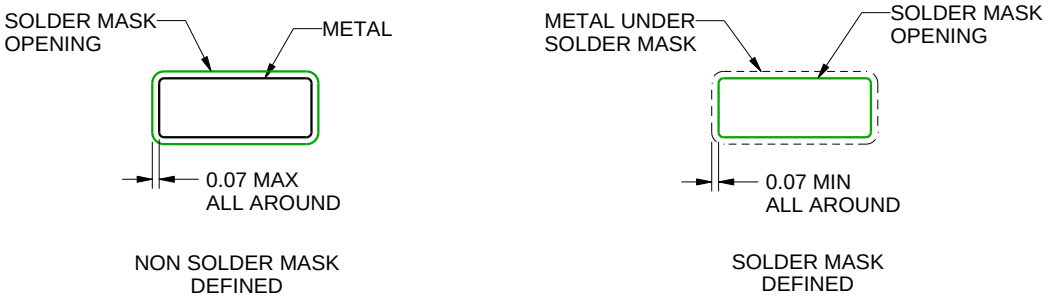


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

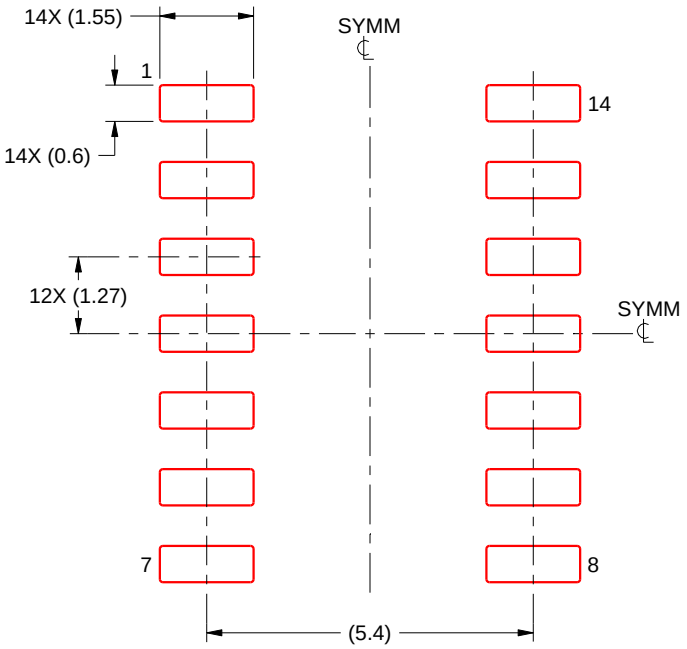
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

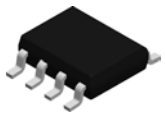


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

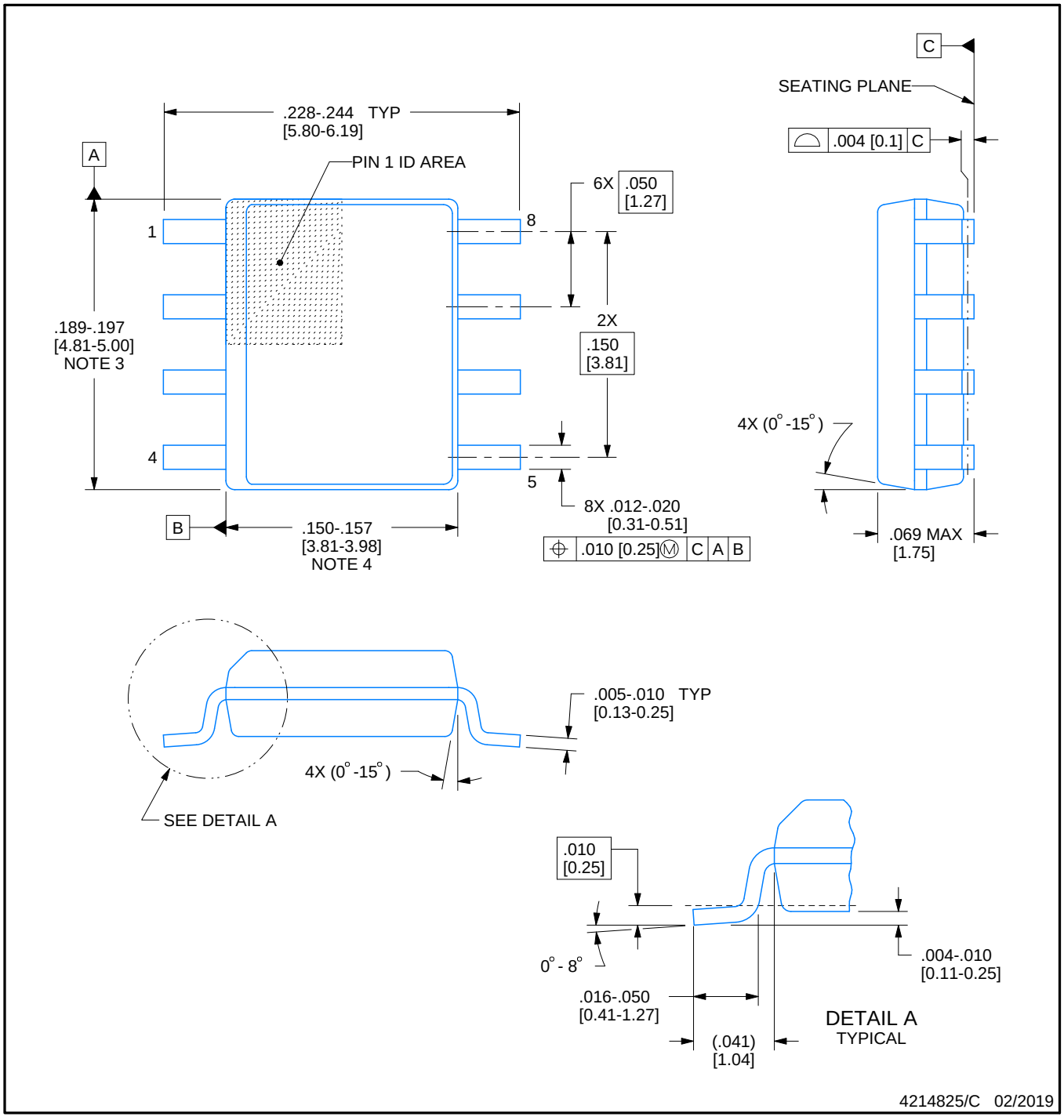


PACKAGE OUTLINE

D0008A

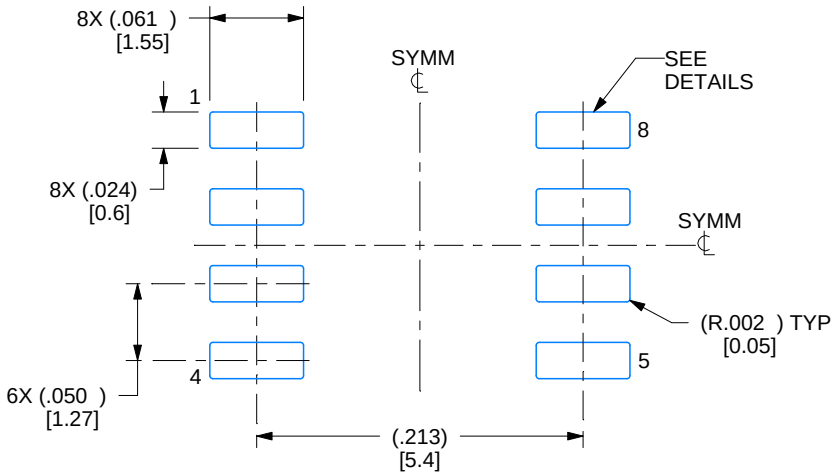
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

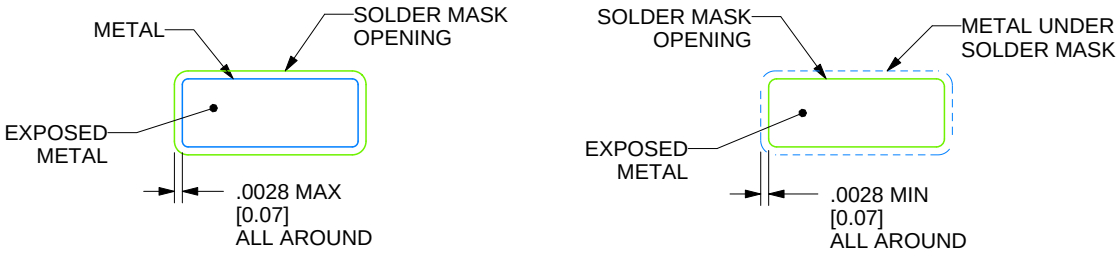


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

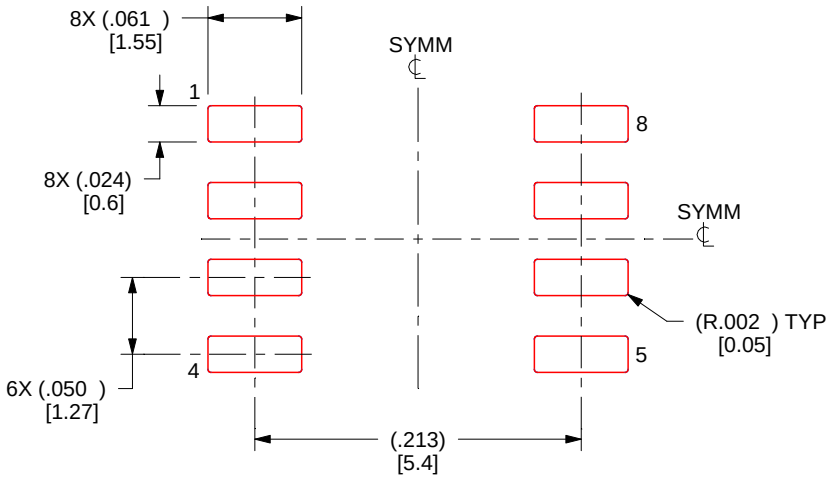
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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