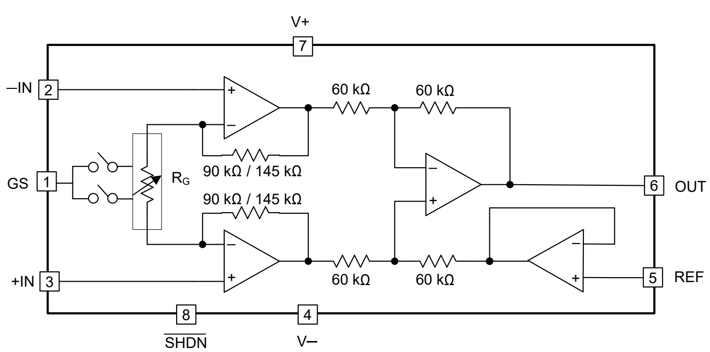
INA351 Cost and Size Optimized, Low Power, 1.8V to 5.5V Selectable Gain Instrumentation Amplifier with Integrated Reference Buffer

1 Features

- Designed for size, cost, and power conscious applications
- Selectable gain options with integrated reference buffer
  - G = 10 or G = 20 (INA351ABS)
  - G = 30 or G = 50 (INA351CDS)
- Space saving ultra-small package options
  - 10-pin X2QFN (RUG) – $3mm^2$
  - 8-pin WSON (DSG) – $4mm^2$
  - 8-pin SOT23-THN (DDF) – $4.64mm^2$
- Optimized performance for 10-bit to 14-bit systems
  - CMRR: 95dB (typical) across all gains
  - Offset voltage: 0.2mV (typical) across all gains
  - Gain error (typical):
    - 0.015% for G = 10, G = 50
    - 0.020% for G = 20, G = 30
- Bandwidth: 100kHz for G = 10 (typical)
- Drives 500pF with less than 20% overshoot (typical)
- Optimized quiescent current: 110μA (typical)
- Shutdown option for power conscious applications
- Supply range: 1.8V (±0.9V) to 5.5V (±2.75V)
- Specified temperature range: –40°C to 125°C

2 Applications

- Bridge network sensing
- Differential to single-ended conversion
- Weigh scale
- Analog input module
- Flow transmitter
- Wearable fitness and activity monitor
- Blood glucose monitor
- Pressure and temperature sensing



Note: 90kΩ for INA351ABS and 145kΩ for INA351CDS

Simplified Internal Schematic

3 Description

The INA351 is a selectable-gain instrumentation amplifier with integrated reference buffer that offers four gain options across the INA351ABS and INA351CDS variants available in small packages. The INA351ABS has gain options of 10 or 20 and the INA351CDS has gain options of 30 or 50. These gain options can be selected by toggling the gain select (GS) pin. The INA351 is an excellent choice for bridge-type sensing and for differential to single-ended conversion applications.

Built with precision matched integrated resistors, the INA351 saves on BOM costs, pick-and-place machine handling costs, and board space by removing the need for precise or closely-matched external resistors. The INA351 can interface directly to low-speed, 10-bit to 14-bit, analog-to-digital converters (ADCs) and is an excellent choice for replacing discrete implementation of instrumentation amplifiers built with commodity amplifiers and discrete resistors.

Designed with the three-amplifier architecture, the INA351 is optimized for delivering performance. The device achieves 86dB of minimum CMRR and an accurate 0.1% of maximum gain error, along with 1.3mV of maximum offset across all gain options, while consuming just 135μA of maximum quiescent current. The INA351 has an integrated shutdown option to turn off the amplifier when idle for additional power savings in battery-powered applications.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE (3)
INA351ABS	DSG (WSON, 8)	2mm × 2mm
	DDF (SOT-23, 8)	1.6mm × 2.9mm
	RUG (X2QFN, 10)	1.5mm × 2 mm
INA351CDS	DSG (WSON, 8)	2mm × 2mm
	DDF (SOT-23, 8)	1.6mm × 2.9mm
	RUG (X2QFN, 10)	1.5mm × 2mm

(1) See Section 4
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS		
		SOT-23-8 DDF	WSON DSG	X2QFN RUG
INA351ABS	1	8	8	8
INA351CDS	1	8	8	8

5 Pin Configuration and Functions

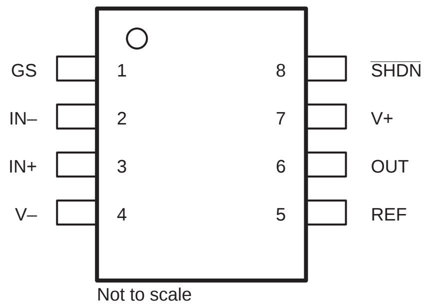
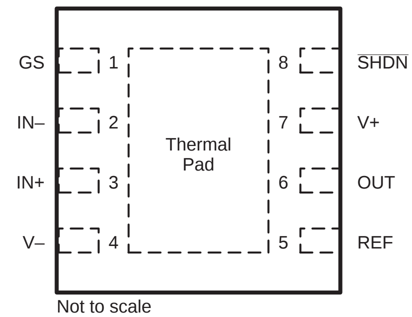


Figure 5-1. DDF Package, 8-Pin SOT-23 (Top View)



Note: Connect Thermal Pad to (V−)

Figure 5-2. DSG Package, 8-Pin WSON With Exposed Thermal Pad (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN–	2	I	Negative (inverting) input
IN+	3	O	Positive (noninverting) input
OUT	6	—	Output
REF	5	—	Reference input. This pin internally connects to a reference buffer amplifier in G = 1, unity gain follower configuration.
GS	1	I	Gain select – logic low (G = 10 for INA351ABS and G = 30 for INA351CDS) Gain select – logic high (G = 20 for INA351ABS and G = 50 for INA351CDS) Gain select – no connect (G = 20 for INA351ABS and G = 50 for INA351CDS)
SHDN	8	I	Shutdown – logic high (device enabled) Shutdown – logic low (device disabled) Shutdown – no connect (device enabled)
V–	4	—	Negative supply
V+	7	—	Positive supply

(1) I = input, O = output

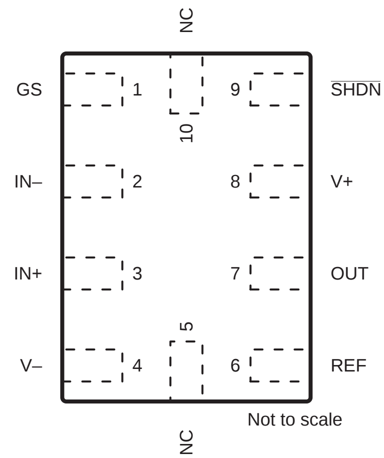


Figure 5-3. RUG Package, 10-Pin X2QFN (Top View)

Table 5-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN–	2	I	Negative (inverting) input
IN+	3	O	Positive (noninverting) input
OUT	7	—	Output
REF	6	—	Reference input. This pin internally connects to a reference buffer amplifier in G = 1, unity gain follower configuration.
GS	1	I	Gain select – logic low (G = 10 for INA351ABS and G = 30 for INA351CDS) Gain select – logic high (G = 20 for INA351ABS and G = 50 for INA351CDS) Gain select – no connect (G = 20 for INA351ABS and G = 50 for INA351CDS)
$\overline{SHDN}$	9	I	Shutdown – logic high (device enabled) Shutdown – logic low (device disabled) Shutdown – no connect (device enabled)
V–	4	—	Negative supply
V+	8	—	Positive supply
NC	5, 10	—	No connect

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	6	V
Signal input pins	Common mode voltage[2]	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage[3]		V_S + 0.2	V
	Current[2]	–10	10	mA
Output short-circuit[4]		Continuous		
Operating Temperature, T_A		–55	150	°C
Junction Temperature, T_J			150	°C
Storage Temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less
(3) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.
(4) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S = (V+) – (V–)	Single-supply	1.8	5.5	V
	Dual-supply	±0.9	±2.75	
Input Voltage Range		(V–)	(V+)	V
Specified temperature	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA351ABS, INA351CDS			UNIT
		DDF (SOT-23-THN)	DSG (WSON)	RUG (X2QFN)	
		8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	172.1	80.3	174.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.1	100.4	63.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	88.2	46.4	99.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.3	5.3	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	88.0	46.4	99.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	21.9	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, V_{REF} = V_S/2, G = 10, R_L = 10 kΩ connected to V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Offset Voltage, RTI[1]	V_S = 5.5 V, G = 10, 20, 30, 50	T_A = 25°C		±0.2	±1.3	mV
V_{OSI}	Offset Voltage over T, RTI[1]	V_S = 5.5 V, G = 10, 20, 30, 50	T_A = –40°C to 125°C			±1.4	mV
V_{OSI}	Offset temp drift, RTI[2]	V_S = 5.5 V, G = 10, 20, 30, 50	T_A = –40°C to 125°C		±0.65		µV/°C
PSRR	Power-supply rejection ratio	G = 10, 20, 30, 50	T_A = 25°C		20	75	µV/V
Z_{IN-DM}	Differential Impedance				100 || 5		GΩ || pF
Z_{IN-CM}	Common Mode Impedance				100 || 9		GΩ || pF
V_{CM}	Input Stage Common Mode Range[3]			(V–)		(V+)	V
CMRR DC	Common-mode rejection ratio, RTI	G = 10, 20, 30, 50, V_{CM} = (V–) + 0.1 V to (V+) – 1 V, High CMRR Region	V_S = 5.5 V, V_{REF} = V_S/2	86	95		dB
		G = 10, 20, 30, 50, V_{CM} = (V–) + 0.1 V to (V+) – 1 V, High CMRR Region	V_S = 3.3 V, V_{REF} = V_S/2		94		dB
		G = 10, 20, 30, 50, V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	V_S = 5.5 V, V_{REF} = V_S/2	62	75		dB
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			±0.65		pA
I_{OS}	Input offset current	V_{CM} = V_S / 2			±0.25		pA
NOISE VOLTAGE							
e_{NI}	Input referred voltage noise density[5]	G = 10, 20, 30, 50	f = 1 kHz		36		nV/√Hz
		G = 10, 20, 30, 50	f = 10 kHz		35		nV/√Hz
E_{NI}	Input referred voltage noise[5]	G = 10, f_B = 0.1 Hz to 10 Hz			3.2		$µV_{PP}$
i_n	Input current noise	f = 1 kHz			22		fA/√Hz
GAIN							
GE	Gain error[4]	G = 10, V_{REF} = V_S/2	V_O = (V–) + 0.1 V to (V+) – 0.1V		±0.015	±0.10	%
		G = 20, V_{REF} = V_S/2			±0.020	±0.10	%
	Gain error[4]	G = 30, V_{REF} = V_S/2			±0.020	±0.10	%
		G = 50, V_{REF} = V_S/2			±0.015	±0.10	%
OUTPUT							
V_{OH}	Positive rail headroom	R_L = 10 kΩ to V_S/2			15	30	mV
V_{OL}	Negative rail headroom	R_L = 10 kΩ to V_S/2			15	30	mV
C_L Drive	Load capacitance drive	V_O = 100 mV step, Overshoot < 20%			500		pF
Z_O	Closed-loop output impedance	f = 10 kHz			51		Ω
I_{SC}	Short-circuit current	V_S = 5.5 V			±20		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 10	V_{IN} = 10 mV_{pk-pk}		100		kHz
		G = 20			50		kHz
	Bandwidth, –3 dB	G = 30			40		kHz
		G = 50			25		kHz
THD + N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.75 V, V_O = 1 V_{RMS}, G = 10, R_L = 100 kΩ *f* = 1 kHz, 80-kHz measurement BW			0.035		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1 GHz, V_{IN_EMIRR} = 100 mV			96		dB
SR	Slew rate	V_S = 5 V, V_O = 2 V step, G = 10, 20, 30, 50			0.20		V/µs

6.5 Electrical Characteristics (continued)

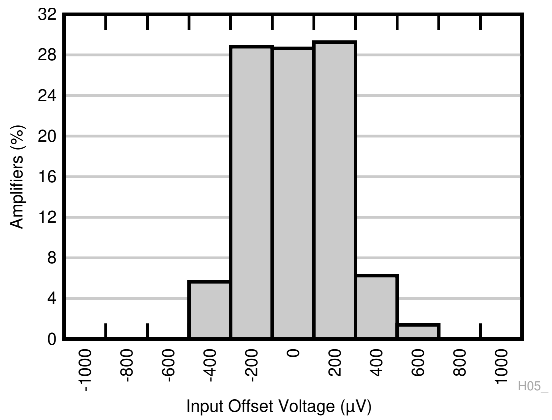
For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, V_{REF} = V_S/2, G = 10, R_L = 10 kΩ connected to V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_S	Settling time	G = 10, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		14		μs
		G = 10, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		24		
		G = 20, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		20		
		G = 20, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		30		
	Settling time	G = 30, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		30		
		G = 30, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		40		
		G = 50, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		45		
		G = 50, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF		55		
	Overload recovery	V_{IN} = 1 V, G = 10		8		μs
REFERENCE BUFFER						
REF - V_{IN}	Linear input voltage range	V_S = 5.5 V	(V–) + 0.1		(V+) – 0.1	V
REF - G	Reference gain to output			1		V/V
REF - GE	Reference gain error(4)	V_S = 5.5 V		±0.015	±0.10	%
REF - Z_{IN}	Input impedance	V_S = 5.5 V		100 || 5		GΩ || pF
REF - I_B	Reference pin bias current	V_S = 5.5 V		±0.65		pA
POWER SUPPLY						
V_S	Power-supply voltage	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
I_Q	Quiescent current	V_{IN} = 0 V		110	135	μA
		T_A = –40°C to 125°C			147	
I_{QSD}	Quiescent current per amplifier	All amplifiers disabled, $\overline{SHDN}$ = V–		0.85	1.5	μA
V_{IL}	Logic low threshold voltage (Gain Select)	G = 10 for INA351ABS, G = 30 for INA351CDS			(V–) + 0.2 V	V
V_{IH}	Logic high threshold voltage (Gain Select)	G = 20 for INA351ABS, G = 50 for INA351CDS	(V–) + 1 V			V
t_{ON}	Amplifier enable time (full shutdown) (6)	G = 10, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–		100		μs
t_{OFF}	Amplifier disable time (6)	G = 10, V_{CM} = V_S / 2, V_O = 0.1 × V_S / 2, R_L connected to V–		5		μs
	$\overline{SHDN}$ pin input bias current (per pin)	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 1 V		10		nA
	$\overline{SHDN}$ pin input bias current (per pin)	(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.2 V		175		nA

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}{}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Input common-mode voltage range of the just the input stage of the instrumentation amplifier. The entire INA351 input range depends on the combination input common-mode voltage, differential voltage, gain, reference voltage and power supply voltage. *Typical Characteristic* curves will be added with more information.
(4) Minimum and Maximum values are specified by characterization.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}{}^2 + (e_{NO} / G)^2]}$
(6) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

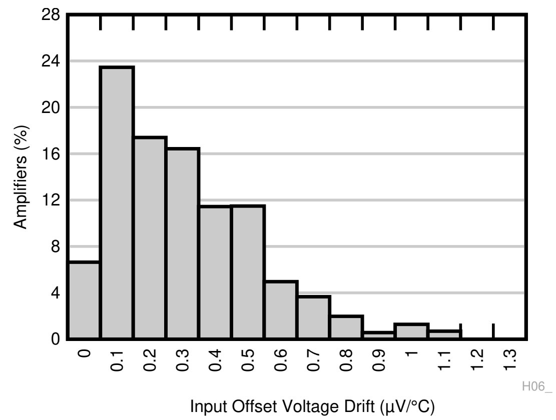
6.6 Typical Characteristics

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



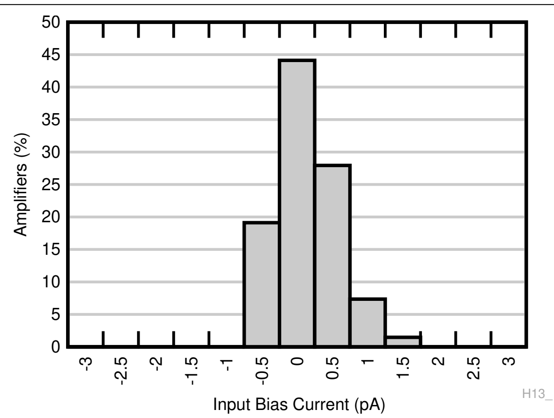
G = 10, 20, 30, 50 N = 36 μ = 23 μV σ = 0.180 mV

Figure 6-1. Typical Distribution of Input Referred Offset Voltage



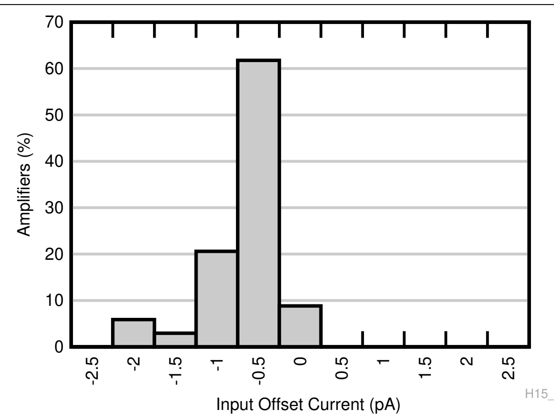
G = 10, 20, 30, 50 N = 36 μ = 0.23 μV/°C σ = 0.36 μV/°C

Figure 6-2. Typical Distribution of Input Referred Offset Drift



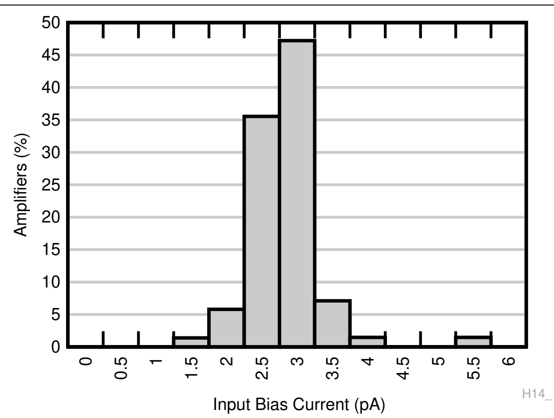
T_A = 25°C N = 72 μ = 0.33 pA σ = 0.43 pA

Figure 6-3. Typical Distribution of Input Bias Current



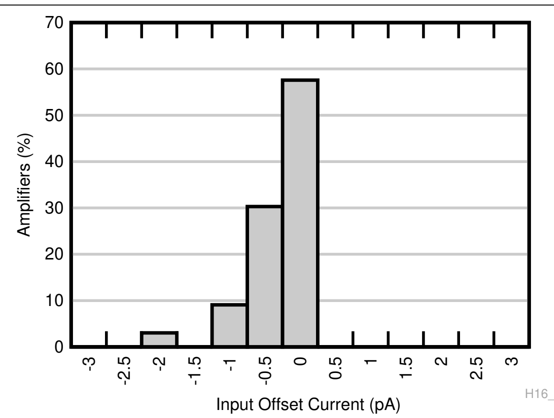
T_A = 25°C N = 36 μ = –0.40 pA σ = 0.47 pA

Figure 6-4. Typical Distribution of Input Offset Current



T_A = 85°C N = 72 μ = 3.3 pA σ = 0.53 pA

Figure 6-5. Typical Distribution of Input Bias Current

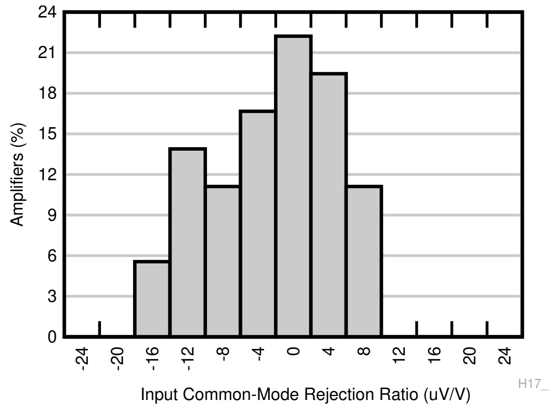


T_A = 85°C N = 36 μ = 0.05 pA σ = 0.30 pA

Figure 6-6. Typical Distribution of Input Offset Current

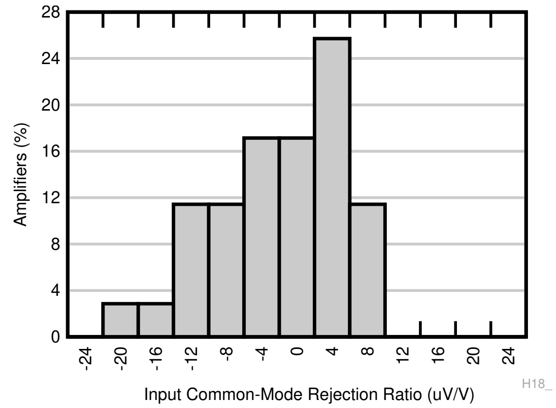
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



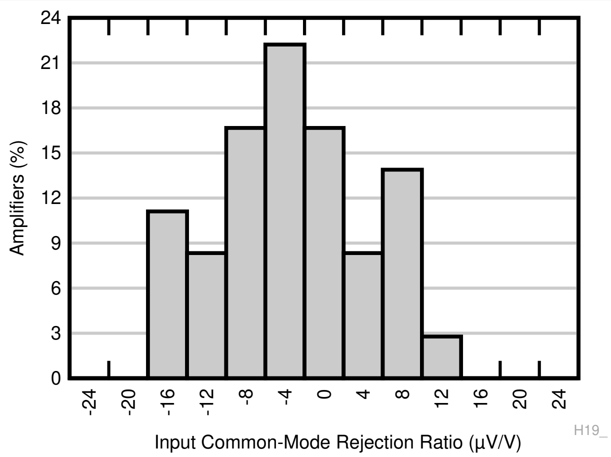
G = 10 N = 36 μ = -0.30 μV/V σ = 7.10 μV/V

Figure 6-7. Typical Distribution of CMRR



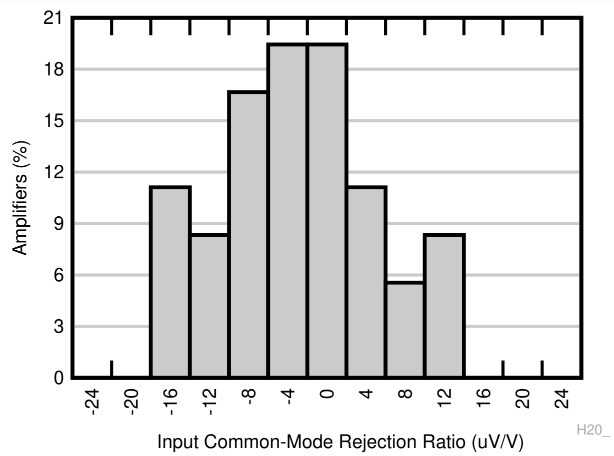
G = 20 N = 36 μ = -0.27 μV/V σ = 7.20 μV/V

Figure 6-8. Typical Distribution of CMRR



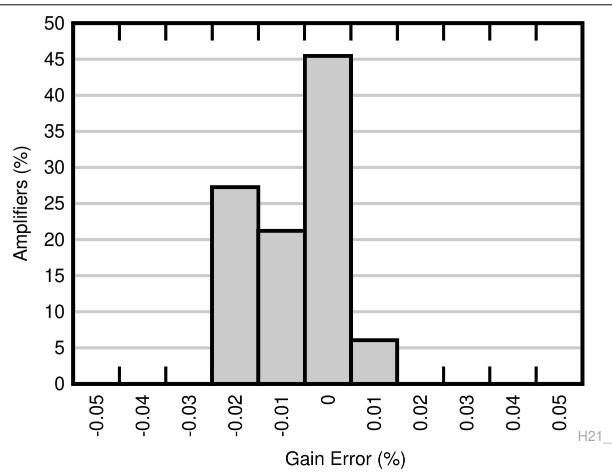
G = 30 N = 36 μ = –1.23 μV/V σ = 7.52 μV/V

Figure 6-9. Typical Distribution of CMRR



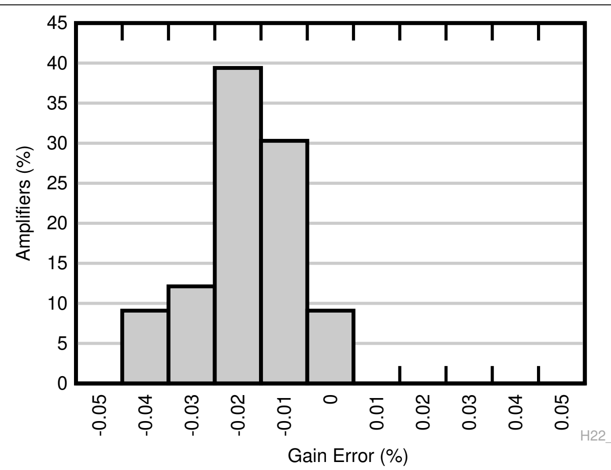
G = 50 N = 36 μ = –1.16 μV/V σ = 7.62 μV/V

Figure 6-10. Typical Distribution of CMRR



G = 10 N = 36 μ = 0.002 % σ = 0.02 %

Figure 6-11. Typical Distribution of Gain Error

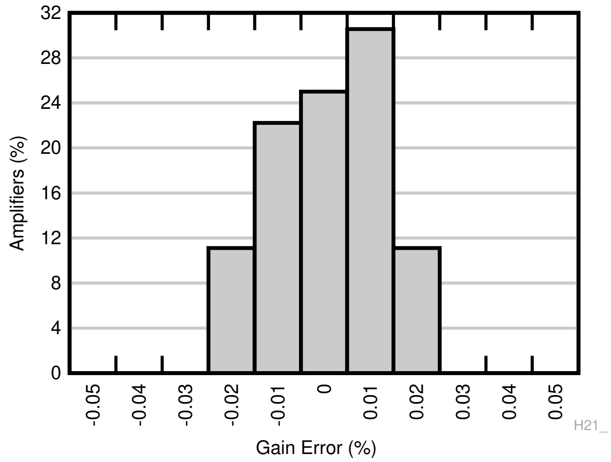


G = 20 N = 36 μ = -0.02 % σ = 0.02 %

Figure 6-12. Typical Distribution of Gain Error

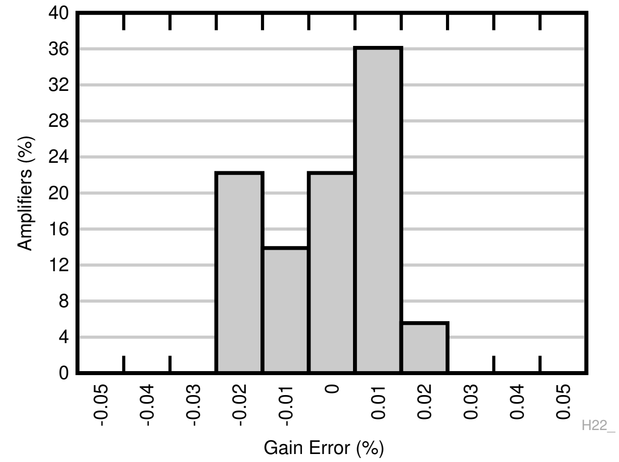
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – (V_{IN-}) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



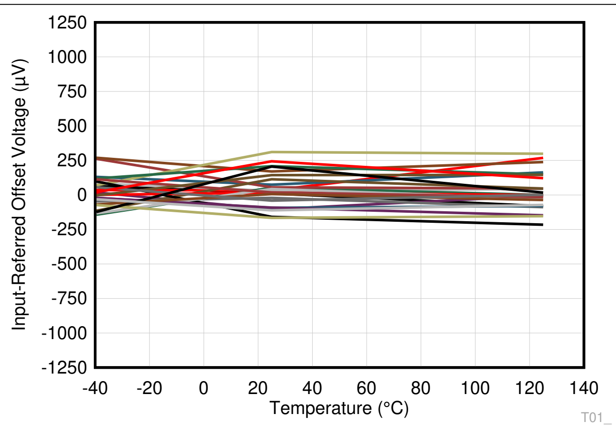
G = 30 N = 36 μ = 0.0067 % σ = 0.011 %

Figure 6-13. Typical Distribution of Gain Error



G = 50 N = 36 μ = 0.0035 % σ = 0.012 %

Figure 6-14. Typical Distribution of Gain Error



G = 10, 20, 30, 50

Figure 6-15. Input Referred Offset Voltage vs Temperature

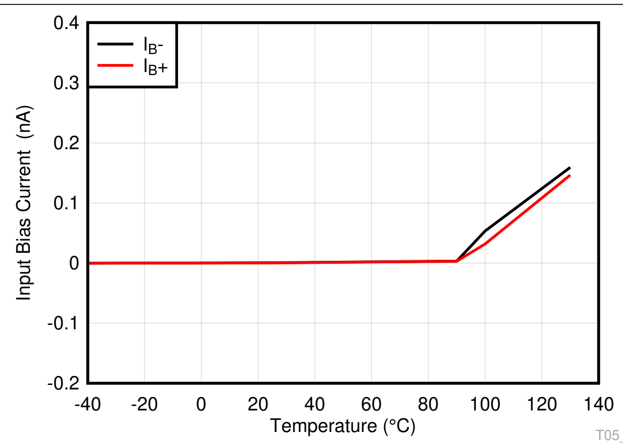


Figure 6-16. Input Bias Current vs Temperature

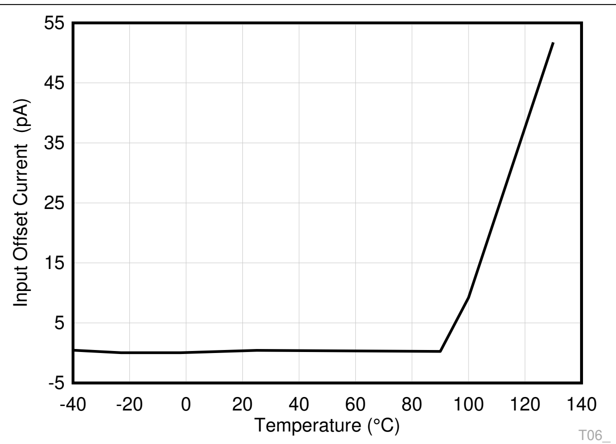


Figure 6-17. Input Offset Current vs Temperature

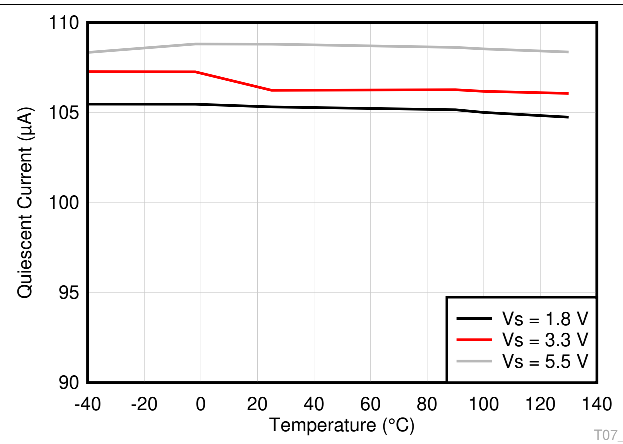


Figure 6-18. Quiescent Current vs Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)

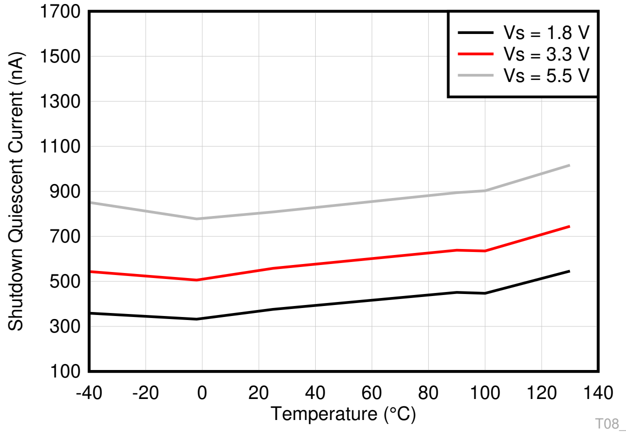


Figure 6-19. Shutdown Quiescent Current vs Temperature

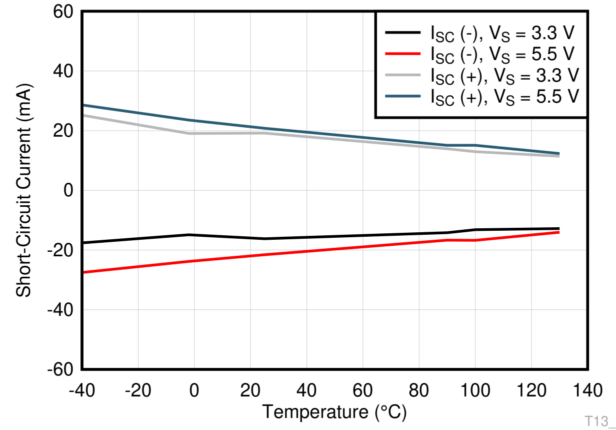


Figure 6-20. Short Circuit Current vs Temperature

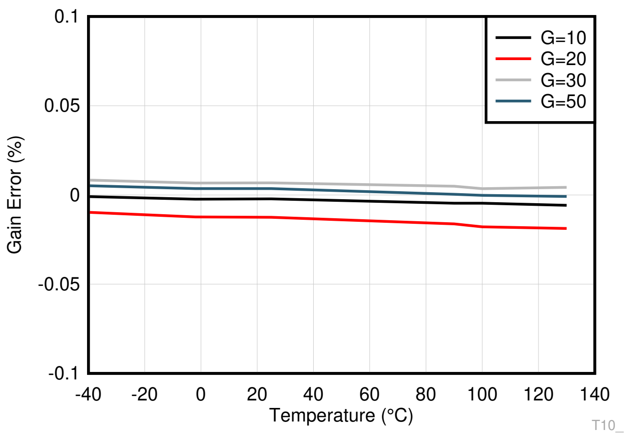


Figure 6-21. Gain Error vs Temperature

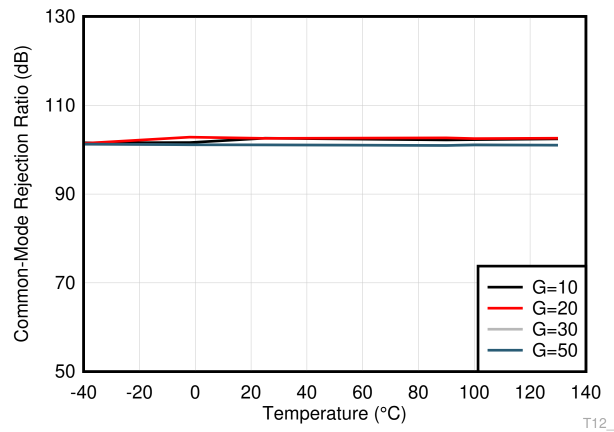
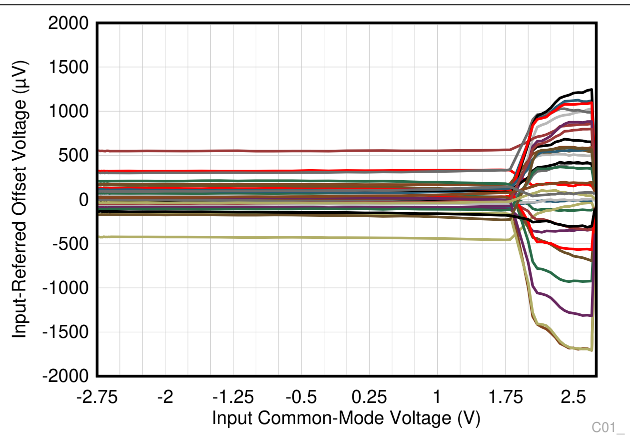
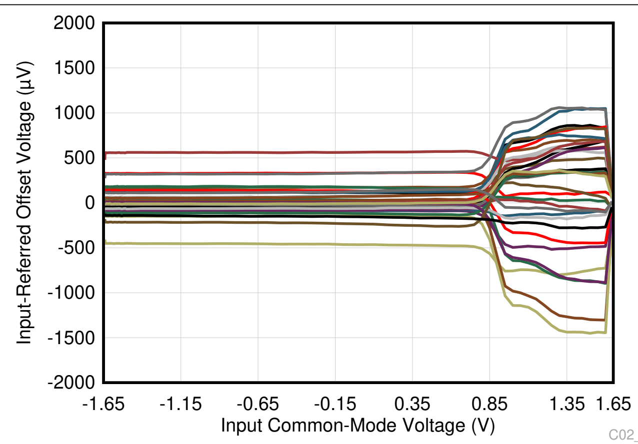


Figure 6-22. CMRR vs Temperature



V+ = 2.75 V and V– = –2.75 V

Figure 6-23. Input Referred Offset Voltage vs Input Common-Mode Voltage

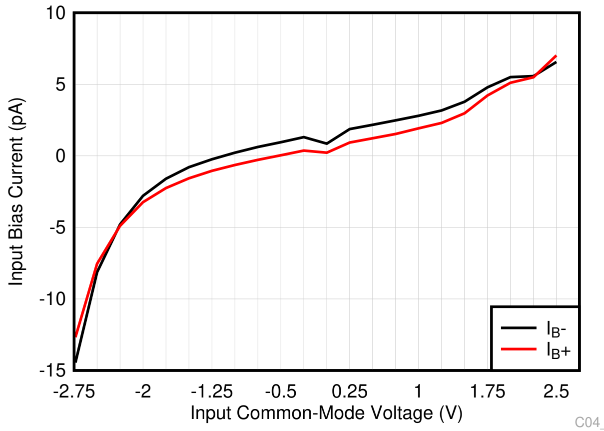


V+ = 1.65 V and V– = –1.65 V

Figure 6-24. Input Referred Offset Voltage vs Input Common-Mode Voltage

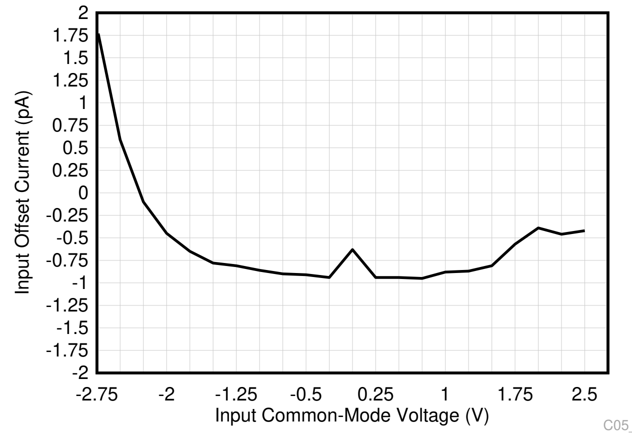
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



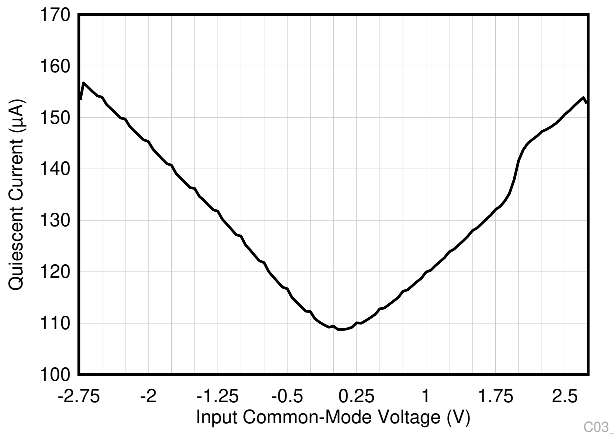
V+ = 2.75 V and V– = –2.75 V

Figure 6-25. Input Bias Current vs Input Common-Mode Voltage



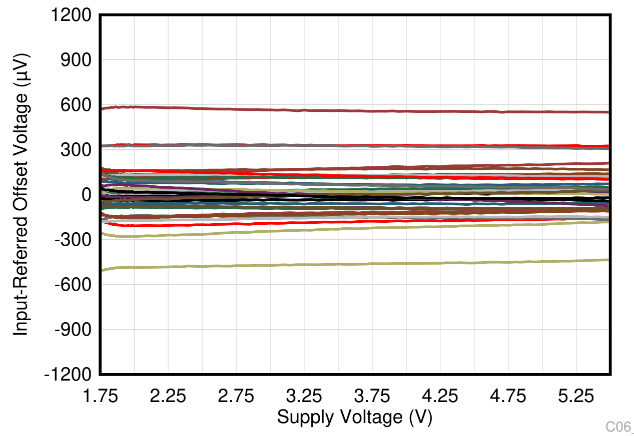
V+ = 2.75 V and V– = –2.75 V

Figure 6-26. Input Offset Current vs Input Common-Mode Voltage



V+ = 2.75 V and V– = –2.75 V

Figure 6-27. Quiescent Current vs Input Common-Mode Voltage



G = 10

Figure 6-28. Input Referred Offset Voltage vs Supply Voltage

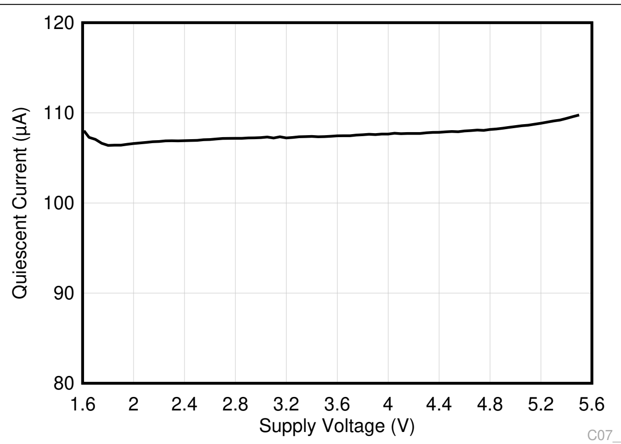


Figure 6-29. Quiescent Current vs Supply Voltage

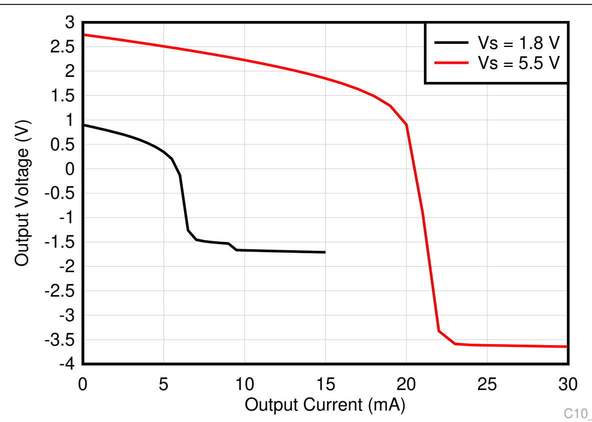


Figure 6-30. Output Voltage vs Output Current (Sourcing)

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)

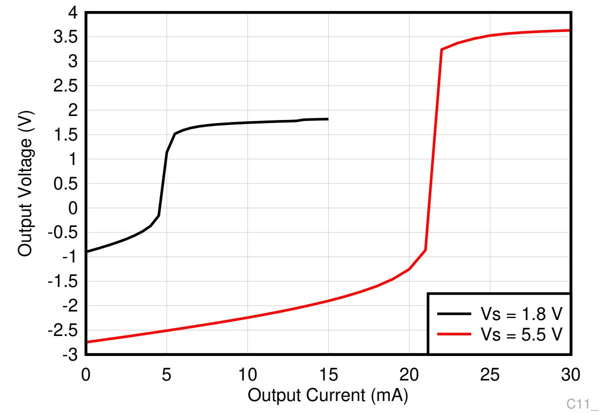


Figure 6-31. Output Voltage vs Output Current (Sinking)

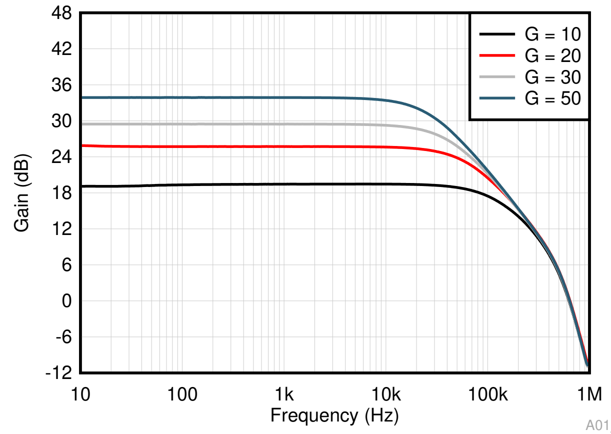


Figure 6-32. Closed-Loop Gain vs Frequency

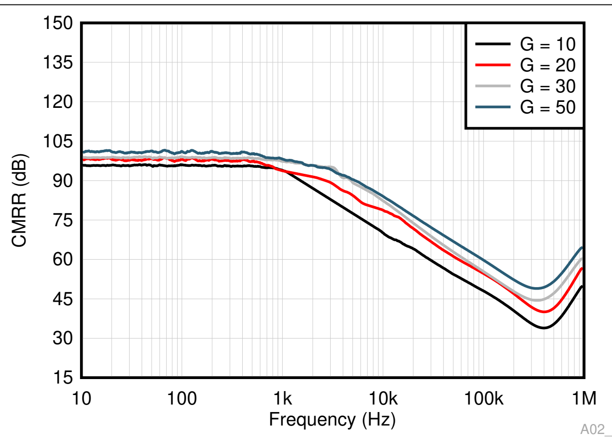


Figure 6-33. CMRR (Referred to Input) vs Frequency

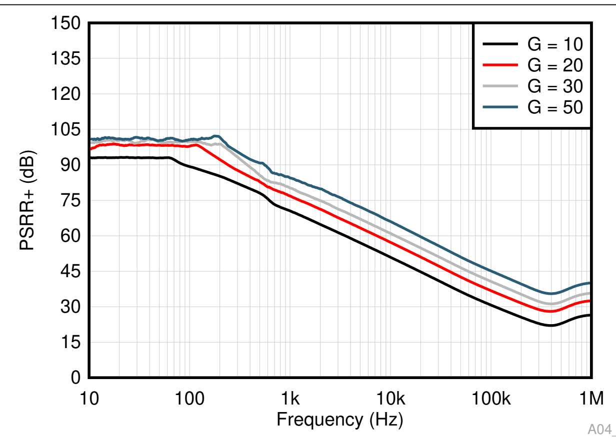


Figure 6-34. PSRR+ (Referred to Input) vs Frequency

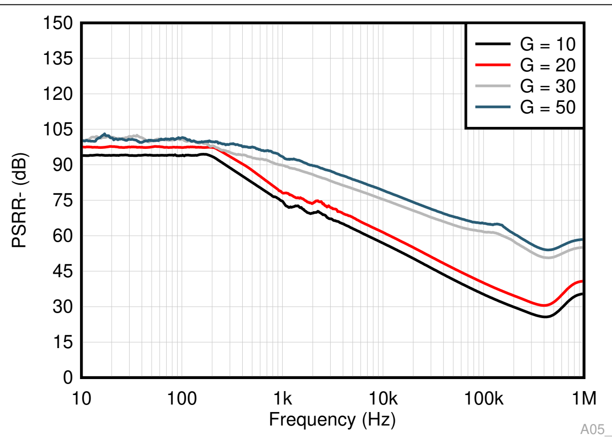


Figure 6-35. PSRR– (Referred to Input) Vs Frequency

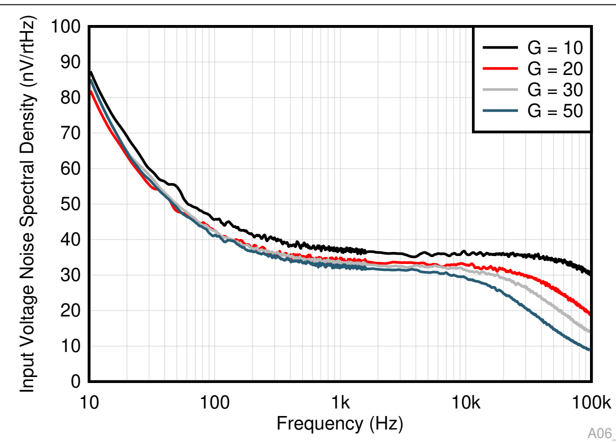


Figure 6-36. Input Referred Voltage Noise Spectral Density

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)

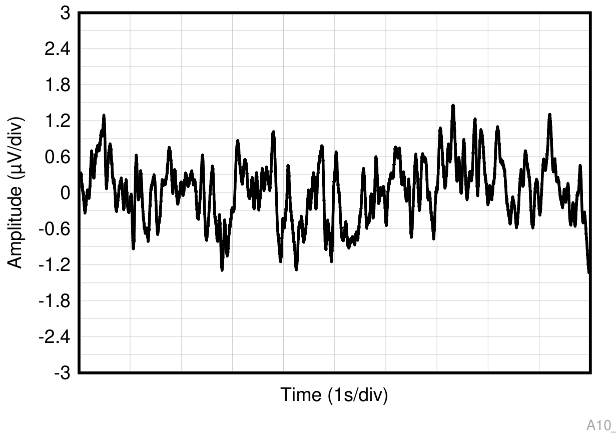


Figure 6-37. 0.1 Hz to 10 Hz Voltage Noise in Time Domain

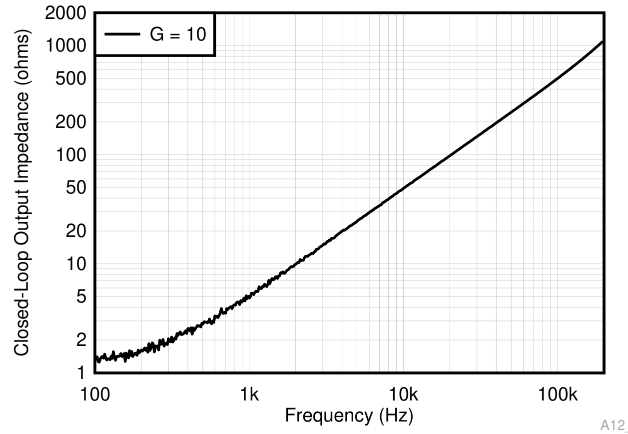


Figure 6-38. Closed-Loop Output Impedance vs Frequency

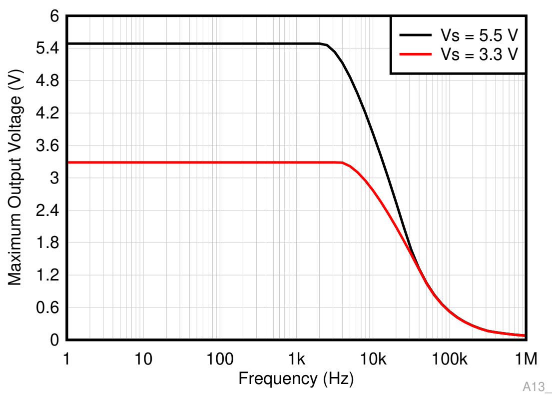
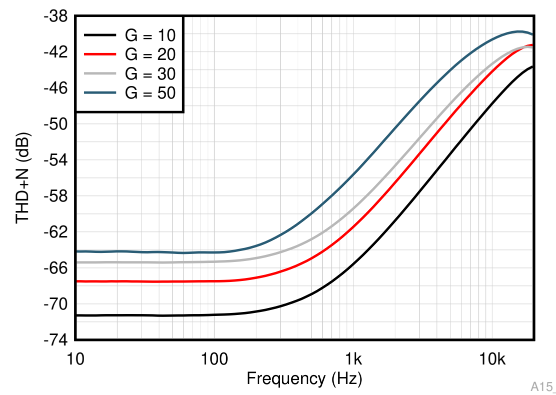
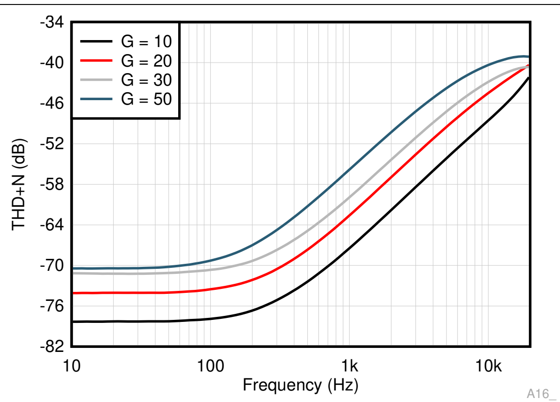


Figure 6-39. Maximum Output Voltage vs Frequency



V_S = 5.5 V BW = 80 kHz V_{CM} = 2.75 V
R_L = 10 kΩ V_{OUT} = 0.5 V_{RMS}

Figure 6-40. THD + N Frequency



V_S = 5.5 V BW = 80 kHz V_{CM} = 2.75 V
R_L = 100 kΩ V_{OUT} = 1 V_{RMS}

Figure 6-41. THD + N Frequency

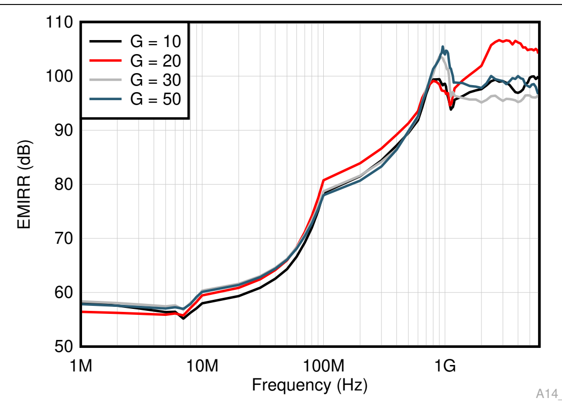
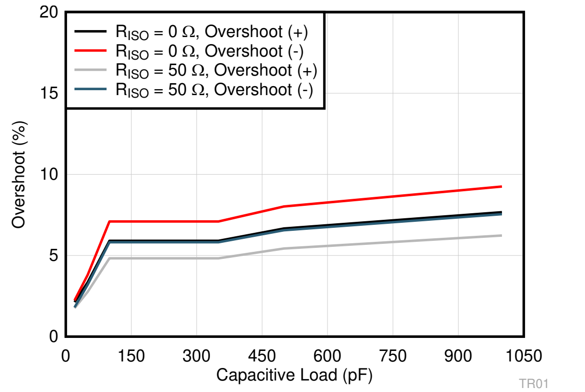


Figure 6-42. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

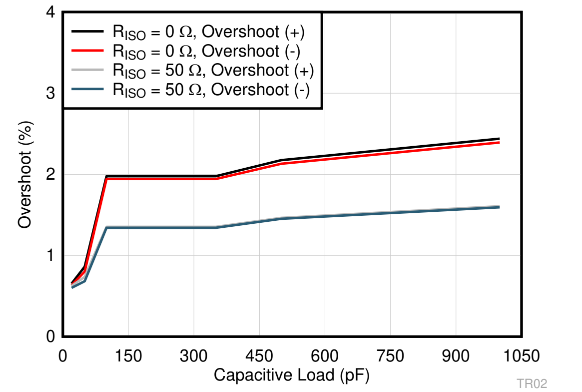
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



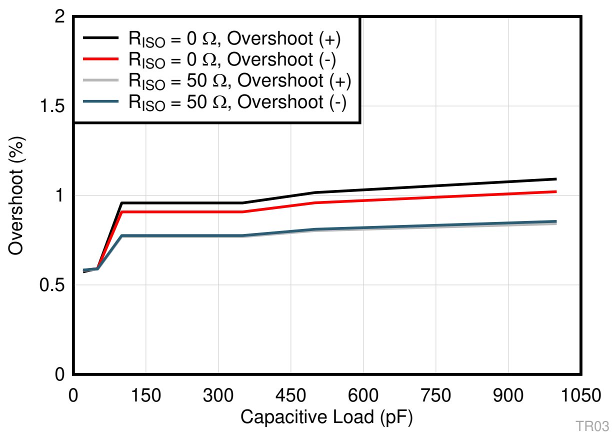
V_S = 5.5 V G = 10 V_{OUT} = 100 mV_{PP}

Figure 6-43. Small-Signal Overshoot vs Capacitive Load



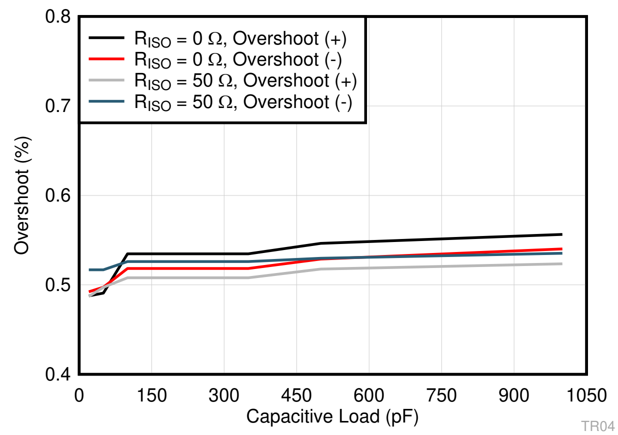
V_S = 5.5 V G = 20 V_{OUT} = 100 mV_{PP}

Figure 6-44. Small-Signal Overshoot vs Capacitive Load



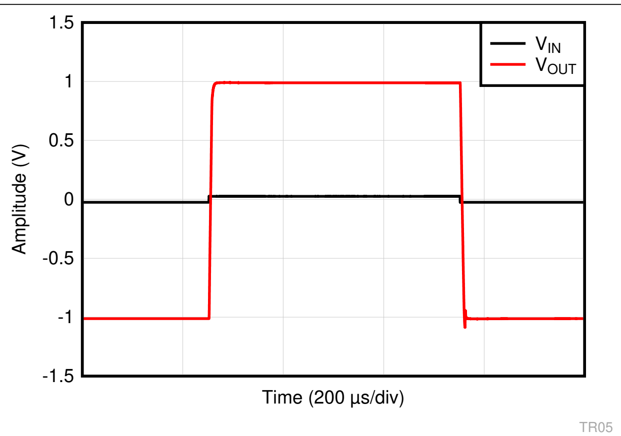
V_S = 5.5 V G = 30 V_{OUT} = 100 mV_{PP}

Figure 6-45. Small-Signal Overshoot vs Capacitive Load



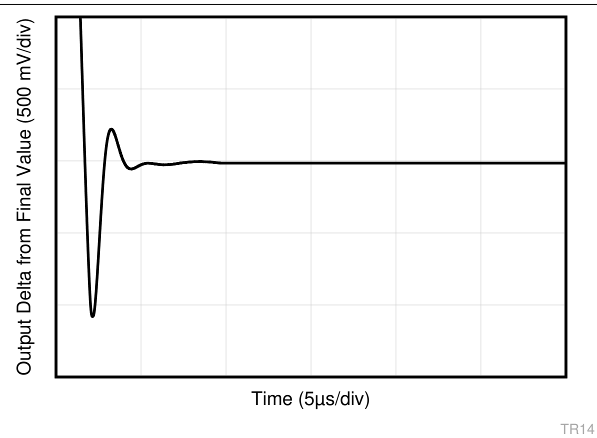
V_S = 5.5 V G = 50 V_{OUT} = 100 mV_{PP}

Figure 6-46. Small-Signal Overshoot vs Capacitive Load



V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 2 V_{PP}

Figure 6-47. Large Signal Step Response

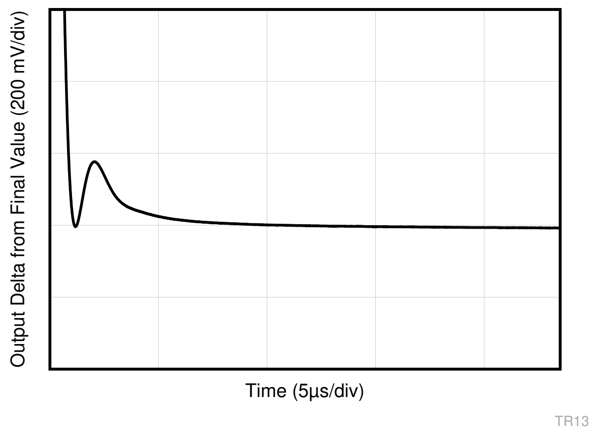


V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 2 V_{PP}

Figure 6-48. Large Signal Settling Time (Falling Edge)

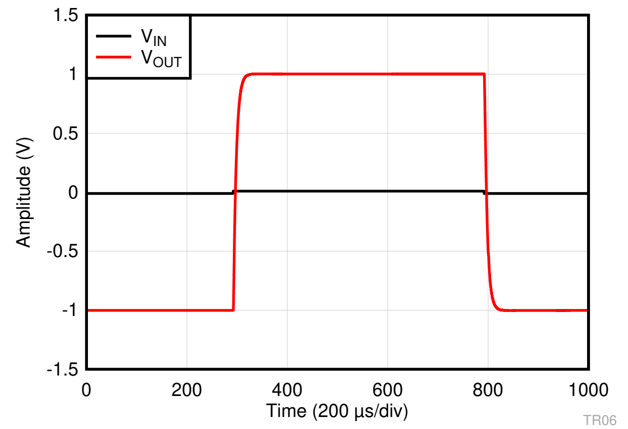
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



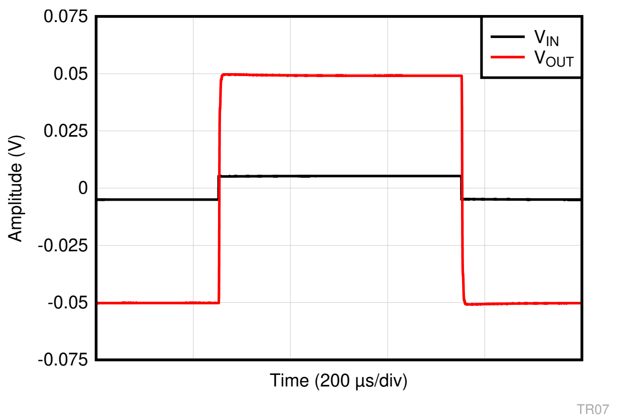
V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 2 V_{PP}

Figure 6-49. Large Signal Settling Time (Rising Edge)



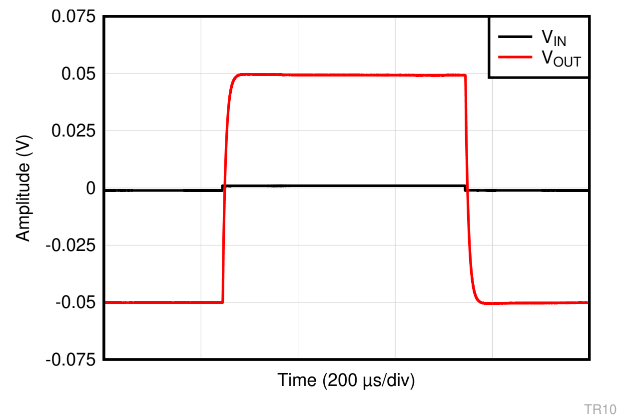
V+ = 2.75 V V– = –2.75 V G = 50 V_{OUT} = 2 V_{PP}

Figure 6-50. Large Signal Step Response



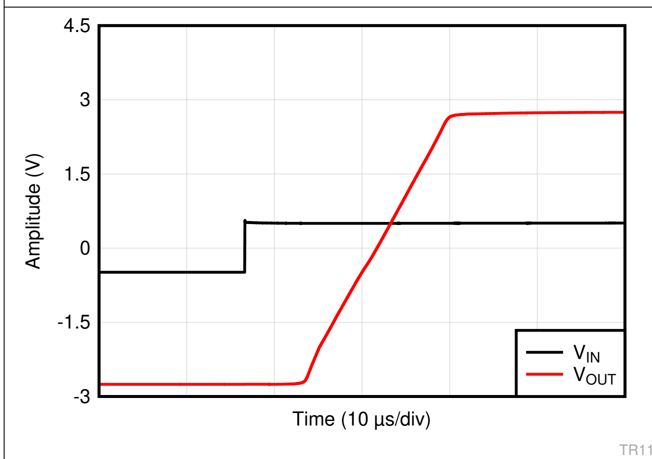
V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 0.1 V_{PP}

Figure 6-51. Small-Signal Step Response



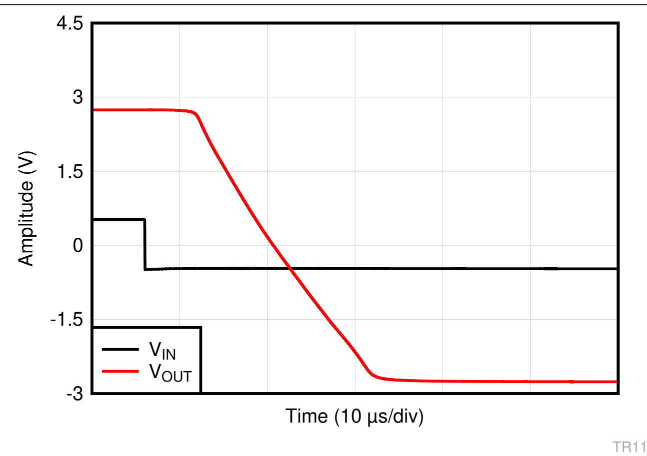
V+ = 2.75 V V– = –2.75 V G = 50 V_{OUT} = 0.1 V_{PP}

Figure 6-52. Small-Signal Step Response



V+ = 2.75 V V– = –2.75 V G = 10 V_{IN} = 1 V_{PP}

Figure 6-53. Over-Load Recovery (Rising Edge)

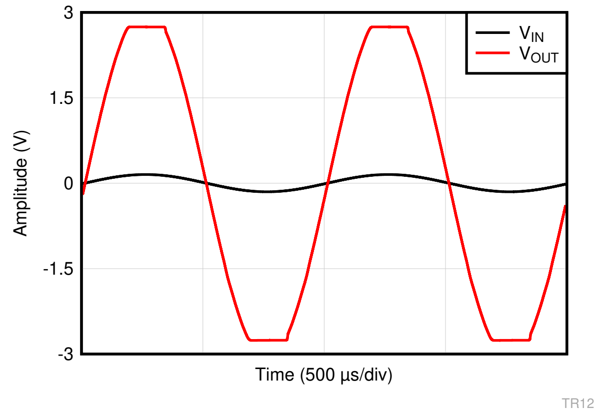


V+ = 2.75 V V– = –2.75 V G = 10 V_{IN} = 1 V_{PP}

Figure 6-54. Over-Load Recovery (Falling Edge)

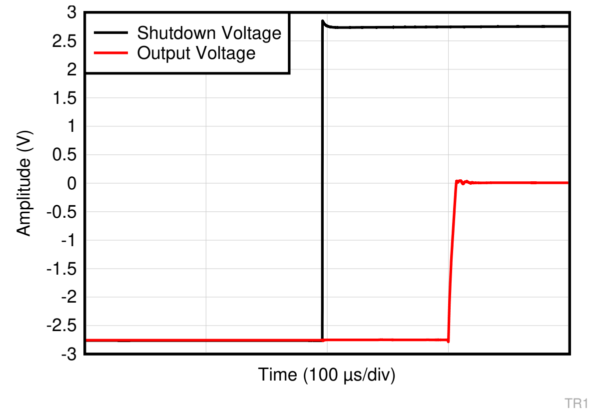
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



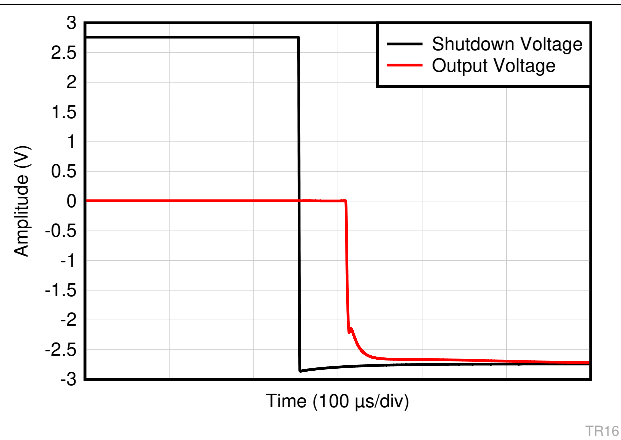
V+ = 2.75 V V– = –2.75 V G = 10 V_{IN} = 0.6 V_{PP}

Figure 6-55. No Phase Reversal



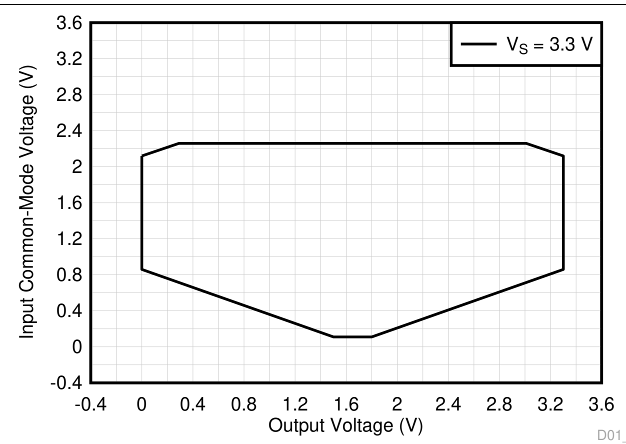
V+ = +2.75 V V– = –2.75 V G = 10

Figure 6-56. Enable Response



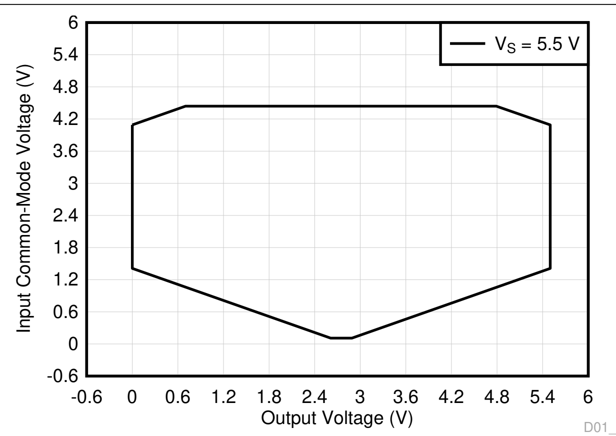
V+ = +2.75 V V– = –2.75 V G = 10

Figure 6-57. Disable Response



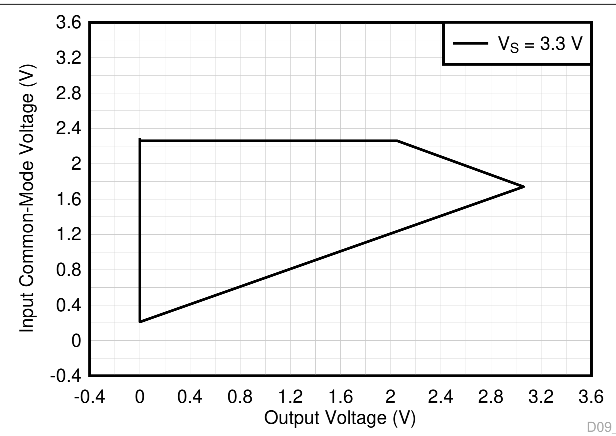
V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

Figure 6-58. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

Figure 6-59. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

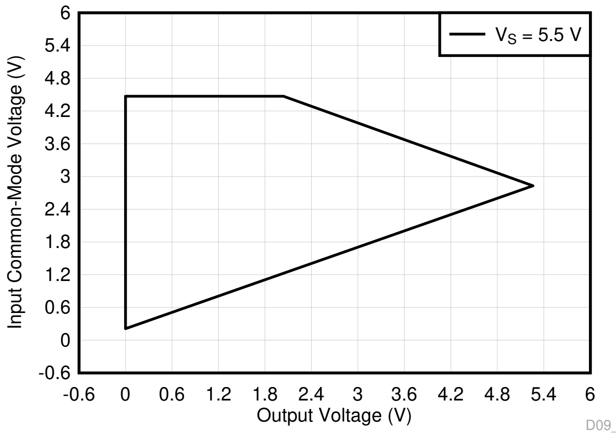


V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 6-60. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

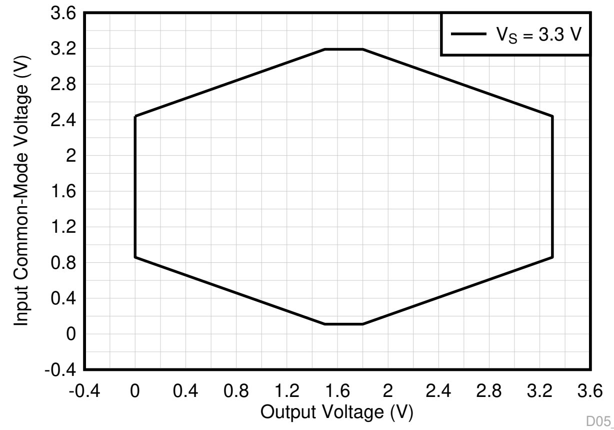
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



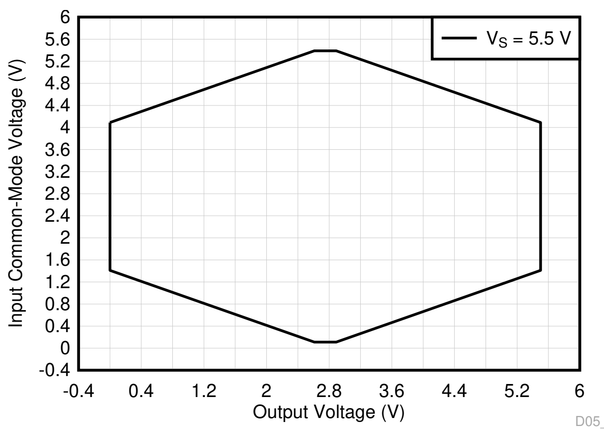
V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 6-61. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



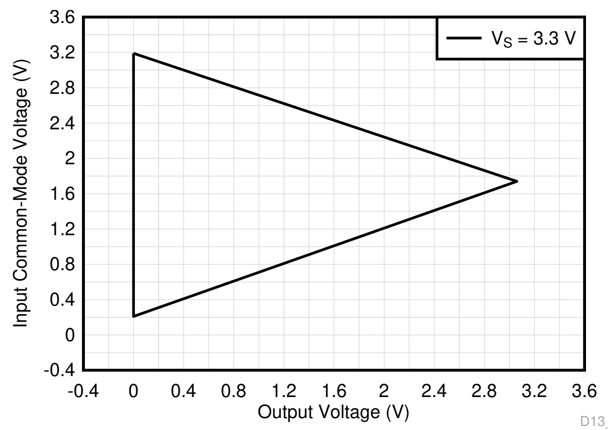
V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

Figure 6-62. Input Common-Mode Voltage vs Output Voltage



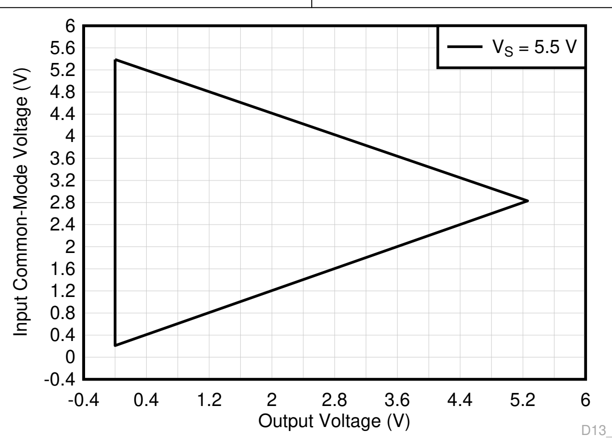
V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

Figure 6-63. Input Common-Mode Voltage vs Output Voltage



V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 6-64. Input Common-Mode Voltage vs Output Voltage



V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 6-65. Input Common-Mode Voltage vs Output Voltage

7 Detailed Description

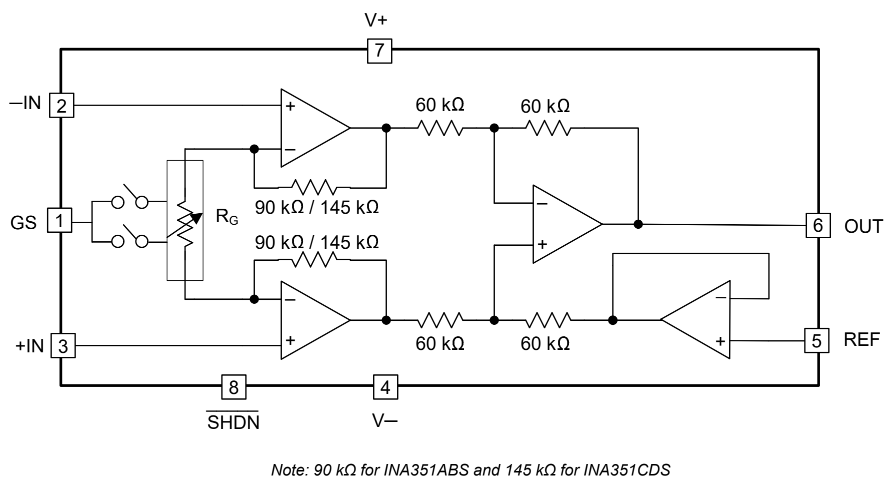
7.1 Overview

The INA351 is a selectable gain instrumentation amplifier with integrated reference buffer designed to provide an integrated, small size, cost-effective solution for applications employing general purpose INAs or discrete implementation of INAs using commodity amplifiers and resistors. The device incorporates a three op amp INA architecture integrating three operational amplifiers and seven precision matched integrated resistors. The INA351 is designed for 10-bit to 14-bit systems without any additional effort, but calibrating offset and gain error at a system level can further improve system resolution and accuracy, enabling use in precision applications.

One of the key features of the INA351 is that the device does not need any external resistors to set the gain. Often these external resistors require tighter tolerance and careful routing, which adds to system complexity and cost. The INA351 is offered in four gain options across two variants. The INA351ABS has two gain options of 10 and 20. The INA351CDS has two other gain options of 30 and 50. Gains can be selected by connecting the GS pin to logic high or logic low. Note that the GS pin can be left floating as well, as the pin is designed with an internal pull up to default to the same configuration as GS tied logic high.

The INA351 is designed for industrial applications leveraging pressure and temperature sensing via bridge-type sensor networks and load cells. The device can also be used in space-constrained applications such as patient monitoring, sleep diagnostics, electronic hospital beds, and blood glucose monitoring for voltage sensing and differential to single-ended conversion. The INA351 can enable these applications to reduce the overall size through the use of tiny packages, including a 2-mm × 1.5-mm X2QFN package and a 2-mm × 2-mm WSON package.

7.2 Functional Block Diagram



Simplified Internal Schematic

7.3 Feature Description

7.3.1 Gain-Setting

Equation 1 is the gain equation for INA351ABS:

$$G = 1 + \frac{180\ k\Omega}{R_G} \tag{1}$$

The value of the internal gain resistor R_G for INA351ABS can then be derived from the gain equation:

$$R_G = \frac{180\ k\Omega}{G - 1} \tag{2}$$

Similarly, Equation 3 is the gain equation for INA351CDS:

$$G = 1 + \frac{290\ k\Omega}{R_G} \tag{3}$$

The value of the internal gain resistor R_G for INA351CDS can then be derived from the gain equation:

$$R_G = \frac{290\ k\Omega}{G - 1} \tag{4}$$

Table 7-1 provides how to choose different gain options across the INA351ABS and INA351CDS. The 60-kΩ, 90-kΩ, and 145-kΩ resistors mentioned are all typical values of the on-chip resistors.

Table 7-1. Gain Selection Table

DEVICE	GAIN SELECT (GS)	SELECTED GAIN
INA351ABS	High or No Connect	20
	Low	10
INA351CDS	High or No Connect	50
	Low	30

7.3.1.1 Gain Error and Drift

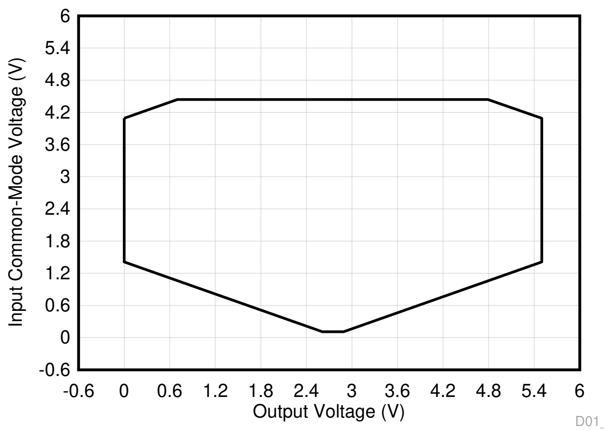
Gain error in the INA351 is limited by the mismatch of the integrated precision resistors and is specified based on characterization results. Gain error of maximum 0.1% can be expected for all gains of 10, 20, 30 and 50. Gain drift in the INA351 is limited by the slight mismatch of the temperature coefficient of the integrated resistors. Since these integrated resistors are precision matched with low temperature coefficient resistors to begin with, the overall gain drift is much better in comparison to discrete implementation of the instrumentation amplifiers built using external resistors.

7.3.2 Input Common-Mode Voltage Range

The INA351 has two gain stages, the first stage has a common-mode gain of 1 and a differential gain set by the GS pin. The second stage is configured in a difference-amplifier configuration with differential gain of 1 and ideally rejects all of the input common mode completely. The second stage also provides a gain of 1 from REF pin to set the output common-mode voltage.

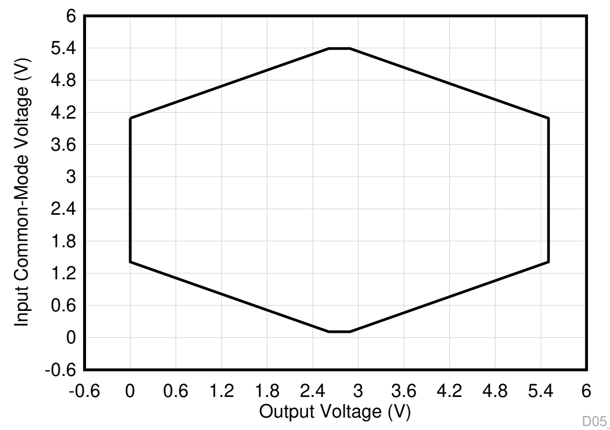
The linear input voltage range of the INA351, even for a rail-to-rail first stage, is dictated by both the signal swing at output of the first stage as well as the input common-mode voltage range output swing of the second stage. To maximize performance, it is critical to keep the INA351 within the linear range for a given combination of gain, reference, and input common-mode voltage for a particular input differential. Input common-mode voltage (V_{CM}) vs output voltage graphs (V_{OUT}) in this section show a particular reference voltage and gain configuration to outline the linear performance region of the INA351. A good common-mode rejection can be expected when operating with in the limits of the V_{CM} vs V_{OUT} graph. Note that the INA351 linear input voltage cannot be close to or extend beyond the supply rails, as the output of the first stage is driven into saturation.

The common-mode range for the most common operating conditions is outlined as follows. Figure 7-1 shows the region of operation where a minimum of 86 dB can be achieved. Figure 7-2 has much wider region of operation with a lower minimum CMRR of 62 dB, because the input signal crosses over the transition region of the input pairs to achieve rail-to-rail operation. The common-mode range for other operating conditions is best calculated with the INA V_{CM} vs V_{OUT} tool located under the *Amplifiers and Comparators* section of the Analog Engineer's Calculator on ti.com. The INA351-HCM model can be specifically used for applications requiring high CMRR and corresponds to performance shown in Figure 7-1. The INA351xxS model can be used for applications where the input common mode can be expected to vary rail-to-rail and the model corresponds to performance shown in Figure 7-2 where CMRR drops to 62-dB minimum.



V_S = 5.5 V G = 10, 20, 30, 50 $V_{REF} = V_S / 2$

Figure 7-1. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V_S = 5.5 V G = 10, 20, 30, 50 $V_{REF} = V_S / 2$

Figure 7-2. Input Common-Mode Voltage vs Output Voltage

7.3.3 EMI Rejection

The INA351 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the INA351 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 7-3 shows the results of this testing on the INA351. Table 7-2 provides the EMIRR IN+ values for the INA351 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

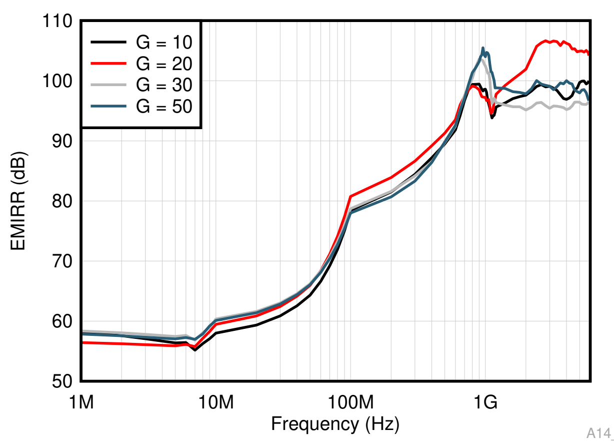


Figure 7-3. EMIRR Testing

Table 7-2. INA351 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	92 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	96 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	100 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	108 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	106.5 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105 dB

7.3.4 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guard band their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

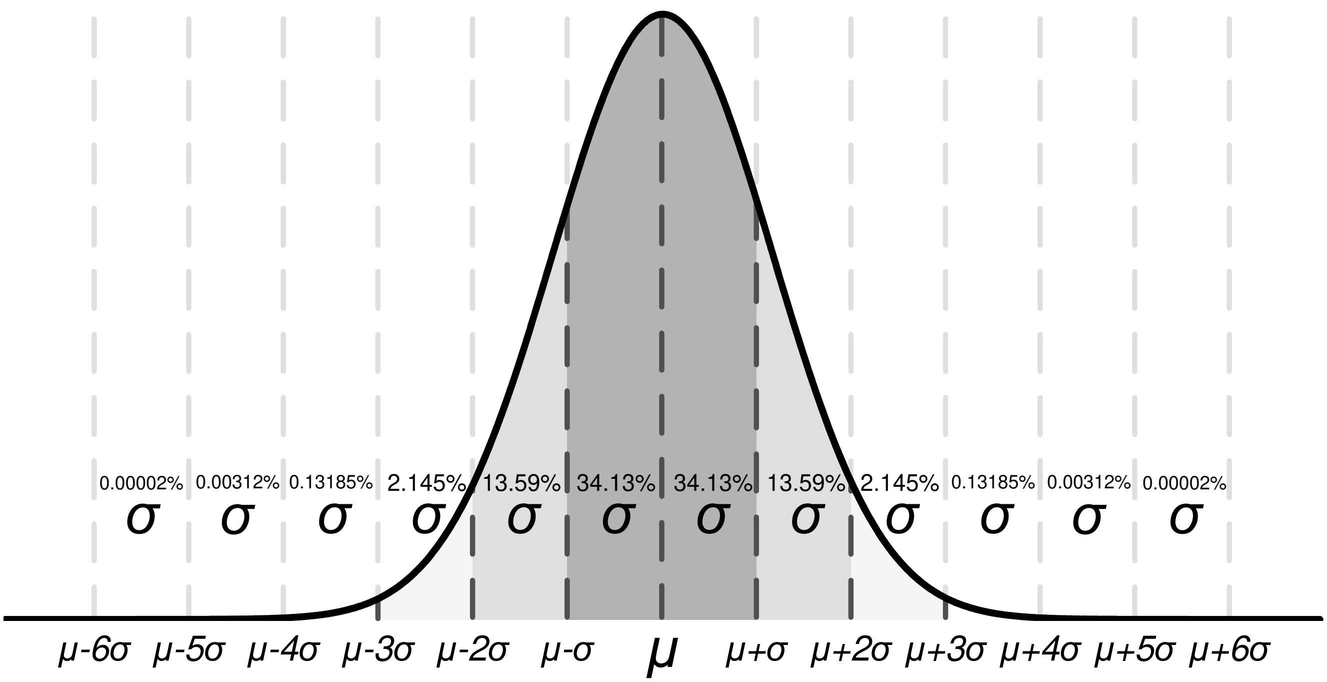


Figure 7-4. Ideal Gaussian Distribution

Figure 7-4 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, the INA351 typical input voltage offset is 200 μV, so 68.2% of all INA351 devices are expected to have an offset from –200 μV to +200 μV. At 4 *σ* (±800 μV), 99.9937% of the distribution has an offset voltage less than ±800 μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are verified by TI, and units outside these limits are removed from production material. For example, the INA351 family has a maximum offset voltage of 1.3 mV at 25°C, and even though this corresponds to 6 σ (≈1 in 500 million units), which is extremely unlikely, TI verifies that any unit with larger offset than 1.3 mV are removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for your application, and design worst-case conditions using this value. As stated earlier, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guard band to design a system around. In this case, the INA351 family does not have a maximum or minimum for offset voltage drift, but based on Figure 6-2 and the typical value of 0.65 μV/°C in the *Electrical Characteristics* table, the 6-σ value for offset voltage drift can be calculated to 3.9 μV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset drift without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot verify the performance of a device. This information must be used only to estimate the performance of a device.

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 7-5 shows the ESD circuits contained in the INA351 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where these diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

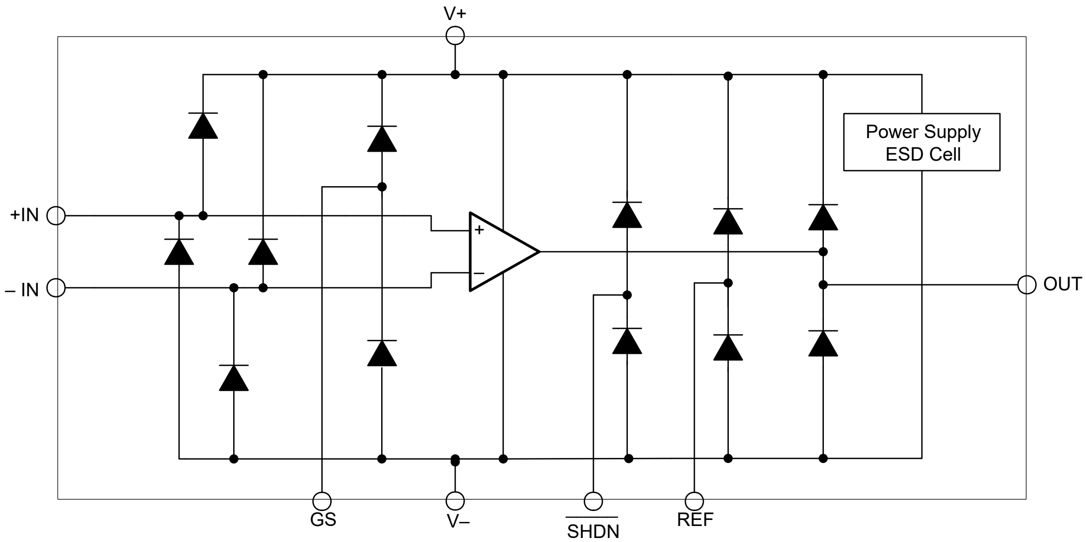


Figure 7-5. Equivalent Internal ESD Circuitry

7.4 Device Functional Modes

The INA351 has a shutdown or disable mode to enable power savings in battery powered applications. The shutdown mode has a maximum quiescent current of just 1.25 µA, which is 100 times lower from the quiescent current when the amplifier is powered-on or enabled.

The INA351 enters disable mode when the $\overline{\text{SHDN}}$ pin is tied low. The INA351 is enabled when the $\overline{\text{SHDN}}$ pin is tied high. A no connection or a floating $\overline{\text{SHDN}}$ pin enables or powers-on the INA as the pin has an internal pull up current to default to the same configuration as $\overline{\text{SHDN}}$ pin tied high.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Reference Pin

The output voltage of the INA351 is developed with respect to the voltage on the reference pin (REF). Often in dual-supply operation, REF pin connects to the system ground. However, In single-supply operation, offsetting the output signal to a precise mid-supply level is useful and required (for example, 2.75-V in a 5.5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA can drive a single-supply ADC. Traditionally, this is accomplished using an external reference buffer as shown in Figure 8-1.

The INA351 has an integrated reference buffer amplifier configured in unity gain, voltage follower configuration internal to the amplifier as shown in Simplified Internal Schematic. This allows designers to directly connect the INA351 to a resistive divider without any need for an external reference buffer amplifier as shown in Figure 8-2.

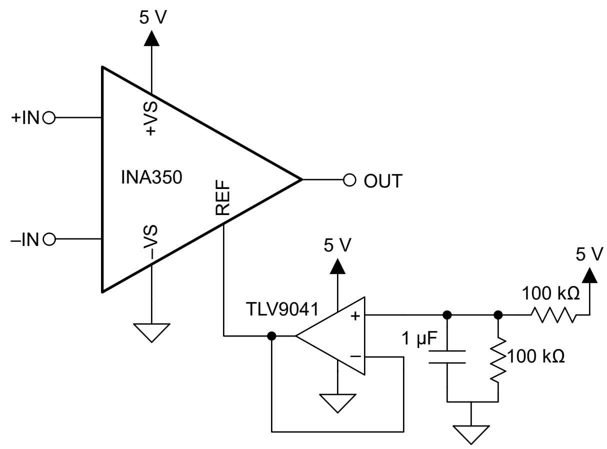


Figure 8-1. INA350 / Traditional INA – External Reference Buffer Required

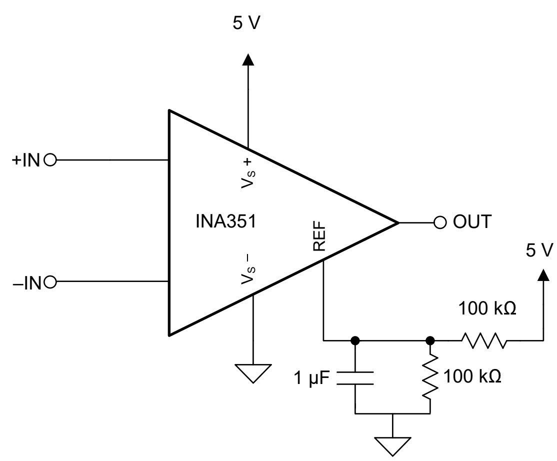


Figure 8-2. INA351 with Integrated Reference Buffer – No External Reference Buffer Required

8.1.2 Input Bias Current Return Path

The input impedance of the INA351 is extremely high, but a path must be provided for the input bias current of both inputs. This input bias current is typically a few pico amps but at high temperature this can be a few nano amps. High input impedance means that the input bias current changes little with varying input voltage.

For proper operation, input circuitry must provide a path for this input bias current. Figure 8-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA351, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in Figure 8-3). With a higher source impedance, use two equal resistors to provide a balanced input, with the possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection.

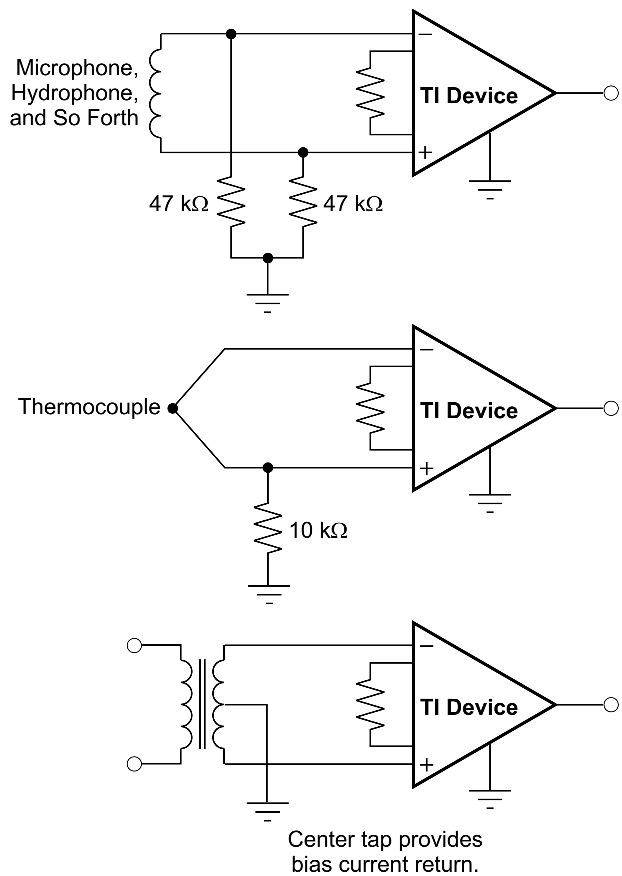


Figure 8-3. Providing an Input Common-Mode Current Path

8.2 Typical Applications

8.2.1 Resistive-Bridge Pressure Sensor

The INA351 is an integrated instrumentation amplifier that measures small differential voltages while simultaneously rejecting larger common-mode voltages. The device offers a low power consumption of 110 µA (typical) and has a smaller form factor.

The device is designed for portable applications where sensors measure physical parameters, such as changes in fluid, pressure, temperature, or humidity. An example of a pressure sensor used in the medical sector is in portable infusion pumps or dialysis machines.

The pressure sensor is made of a piezo-resistive element that can be derived as a classical 4-resistor Wheatstone bridge.

Occlusion (infusion of fluids, medication, or nutrients) happens only in one direction, and therefore can only cause the resistive element (R) to expand. This expansion causes a change in voltage on one leg of the Wheatstone bridge, which induces a differential voltage V_{DIFF}.

Figure 8-4 shows an example circuit for an occlusion pressure sensor application, as required in infusion pumps. When blockage (occlusion) occurs against a set-point value, the tubing depresses, thus causing the piezo-resistive element to expand (Node AD: R + ΔR). The signal chain connected to the bridge downstream processes the pressure change and can trigger an alarm.

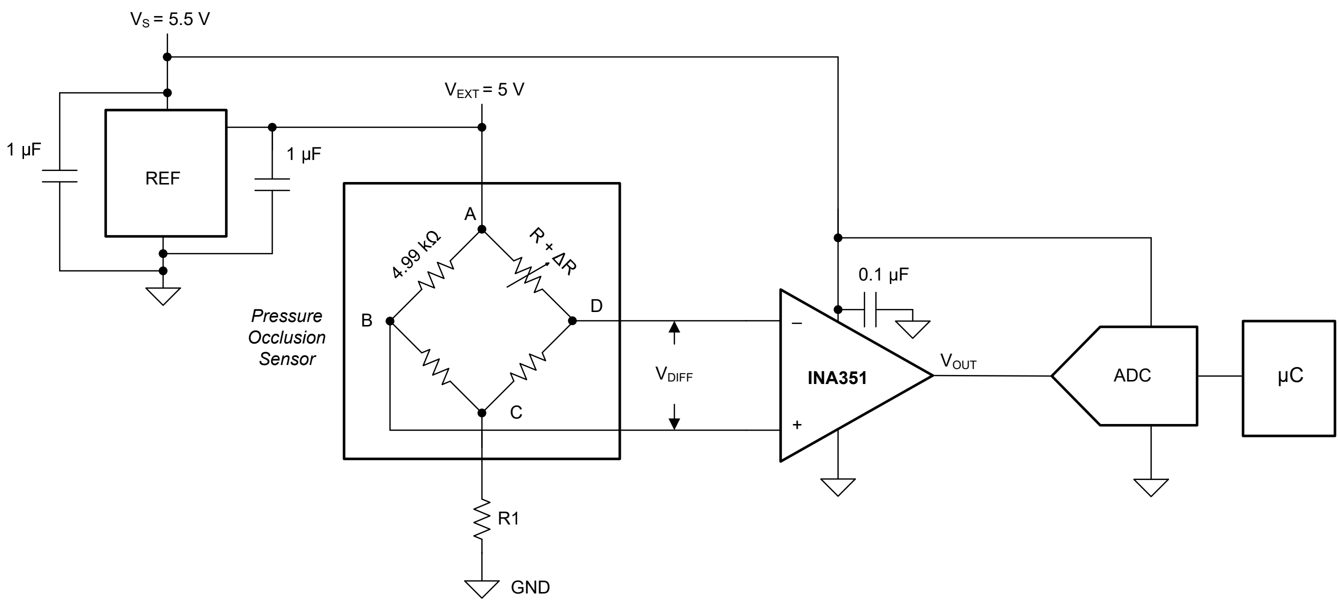


Figure 8-4. Resistive-Bridge Pressure Sensor

Low-tolerance bridge resistors must be used to minimize the offset and gain errors.

Given that there is only a positive differential voltage applied, this circuit is laid out in single-ended supply mode. The excitation voltage, V_{EXT}, to the bridge must be precise and stable; otherwise, measurement errors can be introduced.

8.2.1.1 Design Requirements

For this application, the design requirements are as provided in Table 8-1.

Table 8-1. Design Requirements

DESCRIPTION	VALUE
Single supply voltage	V_S = 5.5 V
Excitation voltage	V_{EXT} = 5.0 V
Occlusion pressure range	P = 1 psi to 12 psi, increments of P = 0.5 psi
Occlusion pressure sensitivity	S = 2 ±0.5 (25%) mV/V/psi
Occlusion pressure impedance (R)	R = 4.99 kΩ ±50 Ω (0.1%)
Total pressure sampling rate	Sr = 20 Hz
Full-scale range of ADC	$V_{ADC(fs)}$ = V_{OUT} = 3.0 V

8.2.1.2 Detailed Design Procedure

This section provides basic calculations to lay out the instrumentation amplifier with respect to the given design requirements.

One of the key considerations in resistive-bridge sensors is the common-mode voltage, V_{CM}. If the bridge is balanced (no pressure, thus no voltage change), $V_{CM(zero)}$ is half of the bridge excitation (V_{EXT}). In this example $V_{CM\ (zero)}$ is 2.5 V. For the maximum pressure of 12 psi, the bridge common-mode voltage, $V_{CM(MAX)}$, is calculated by:

$$V_{CM(MAX)} = \frac{V_{DIFF}}{2} + V_{CM(zero)} \tag{5}$$

where

$$V_{DIFF} = S_{MAX} \times V_{EXT} \times P_{MAX} = 2.5\,\frac{mV}{V \times psi} \times 5\,V \times 12\,psi = 150\,mV \tag{6}$$

Thus, the maximum common-mode voltage applied results in:

$$V_{CM(MAX)} = \frac{150\,mV}{2} + 2.5\,V = 2.575\,V \tag{7}$$

Similarly, the minimum common-mode voltage can be calculated as,

$$V_{CM(MIN)} = \frac{-150\,mV}{2} + 2.5\,V = 2.425\,V \tag{8}$$

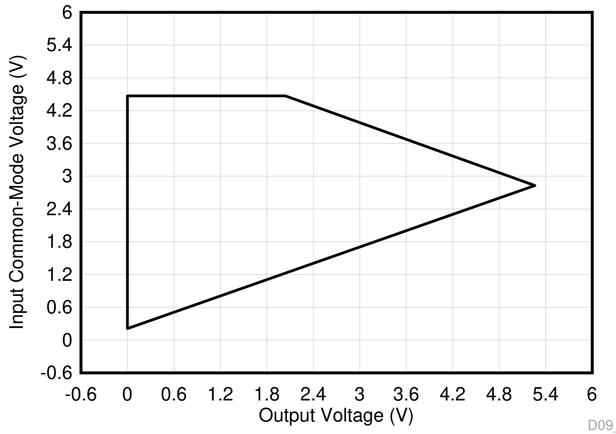
The next step is to calculate the gain required for the given maximum sensor output voltage span, V_{DIFF}, in respect to the required V_{OUT}, which is the full-scale range of the ADC.

The following equation calculates the gain value using the maximum input voltage and the required output voltage:

$$G = \frac{V_{OUT}}{V_{DIFF(MAX)}} = \frac{3.0\,V}{150\,mV} = 20\,V/V \tag{9}$$

Considering the INA351 is a selectable gain INA with gain options of 10, 20, 30, 50, the INA351ABS with GS tied high enables G = 20 maintaining the maximum output signal swing for the ADC.

Next, let us make sure that the INA351 can operate within this range checking the *Input Common-Mode Voltage vs Output Voltage* curves in the *Typical Characteristics* section. The relevant figure is also in this section for convenience. Looking at Figure 8-5, we can confirm that a output signal swing of 3 V is supported for the input signal swing between 2.425 V and 2.575 V, thus making sure of the linear operation.



V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 8-5. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

An additional series resistor in the Wheatstone bridge string (R1) may or may not be required, and can be decided based on the intended output voltage swing for a particular combination of supply voltage, reference voltage and the selected gain for an input common-mode voltage range. R1 helps adjust the input common-mode voltage range, and thus can help accommodate the intended output voltage swing. In this particular example, it is not required and can be shorted out.

8.2.1.3 Application Curves

The following typical characteristic curve is for the circuit in Figure 8-4.

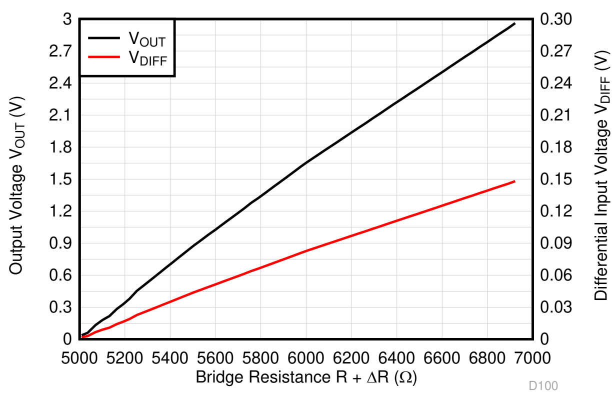


Figure 8-6. Input Differential Voltage, Output Voltage vs Bridge Resistance

8.3 Power Supply Recommendations

The nominal performance of the INA351 is specified with a supply voltage of ±2.75 V and midsupply reference voltage. The device also operates using power supplies from ±0.85 V (1.7 V) to ±2.75 V (5.5 V) and non-midsupply reference voltages with excellent performance. Parameters can vary significantly with operating voltage and reference voltage.

8.4 Layout

8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use the following PCB layout practices:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Route the input traces as far away from the supply or output traces as possible to reduce parasitic coupling. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

8.4.2 Layout Example

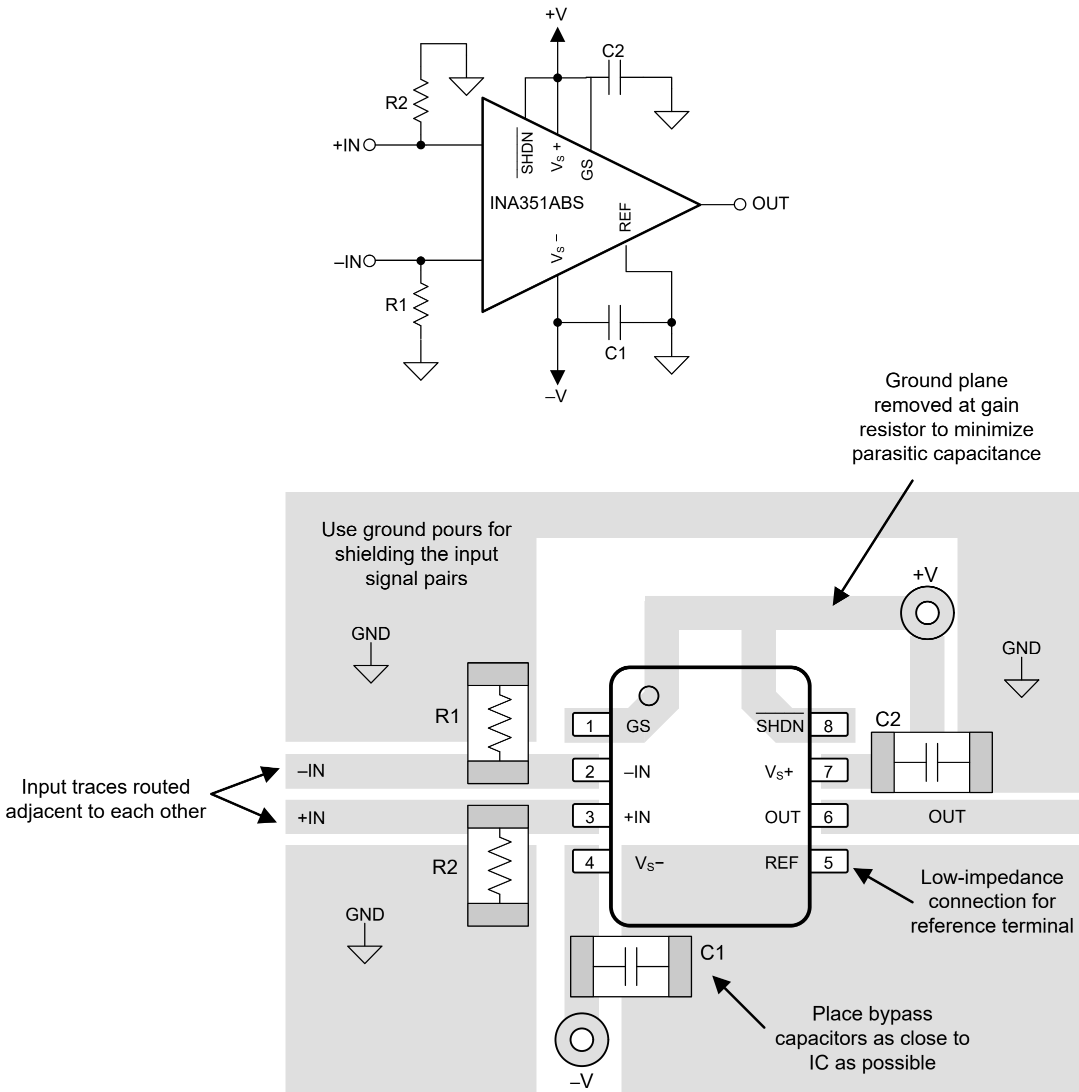


Figure 8-7. Example Schematic and Associated PCB Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

- *SPICE-based analog simulation program — TINA-TI software folder*
- *Analog Engineers Calculator*

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2023) to Revision D (November 2024) **Page**

- Deleted the preview tag from *Package Information* for INA351 DDF RTM.. 1
- Deleted the preview tag from *Device Comparison Table* for INA351 DDF RTM.. 3
- Deleted preview footnote from *Thermal Information* table for INA351 SOT-23-THIN (DDF) RTM..................... 5

Changes from Revision B (February 2023) to Revision C (May 2023)	Page
• Deleted the preview tag from *Package Information* for INA351 RUG RTM	1
• Deleted the preview tag from *Device Comparison Table* for INA351 RUG RTM	3
• Deleted preview footnote from *Thermal Information* table for INA351 X2QFN (RUG) RTM	5

Changes from Revision A (December 2022) to Revision B (February 2023)	Page
• Deleted the preview tag from *Package Information* for INA351CDSIDSGR RTM	1
• Deleted the preview tag from *Device Comparison Table* for INA351CDSIDSGR RTM	3
• Deleted preview footnote from *Electrical Characteristics* and *Thermal Information* table for INA351CDSIDSGR RTM	5

Changes from Revision * (December 2022) to Revision A (December 2022)	Page
• Added footnote for Reference gain error specification in *Electrical Characteristics* table	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA351ABSIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	351AB	Samples
INA351ABSIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2TMH	Samples
INA351ABSIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NU	Samples
INA351CDSIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	351CD	Samples
INA351CDSIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2TNH	Samples
INA351CDSIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

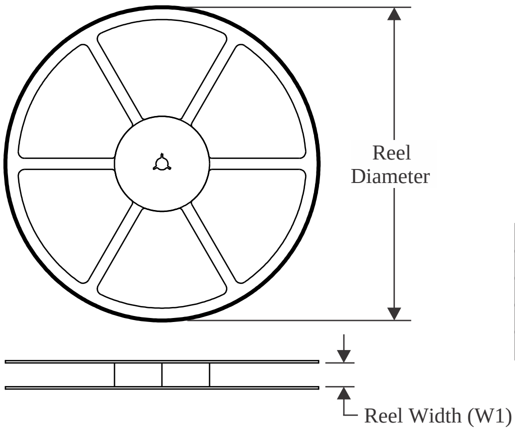
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

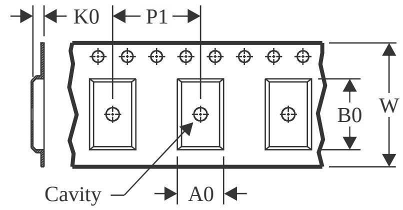
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

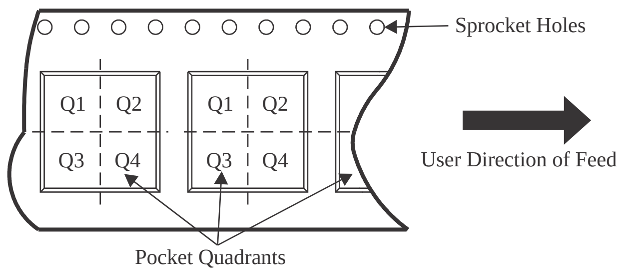


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

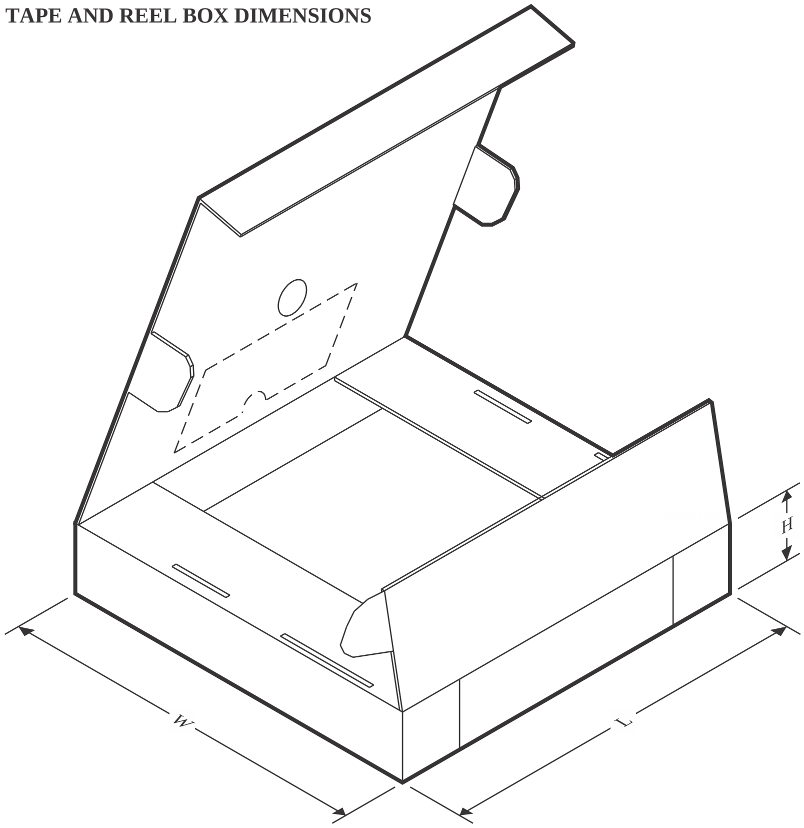
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA351ABSIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA351ABSIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA351ABSIRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
INA351CDSIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA351CDSIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA351CDSIRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



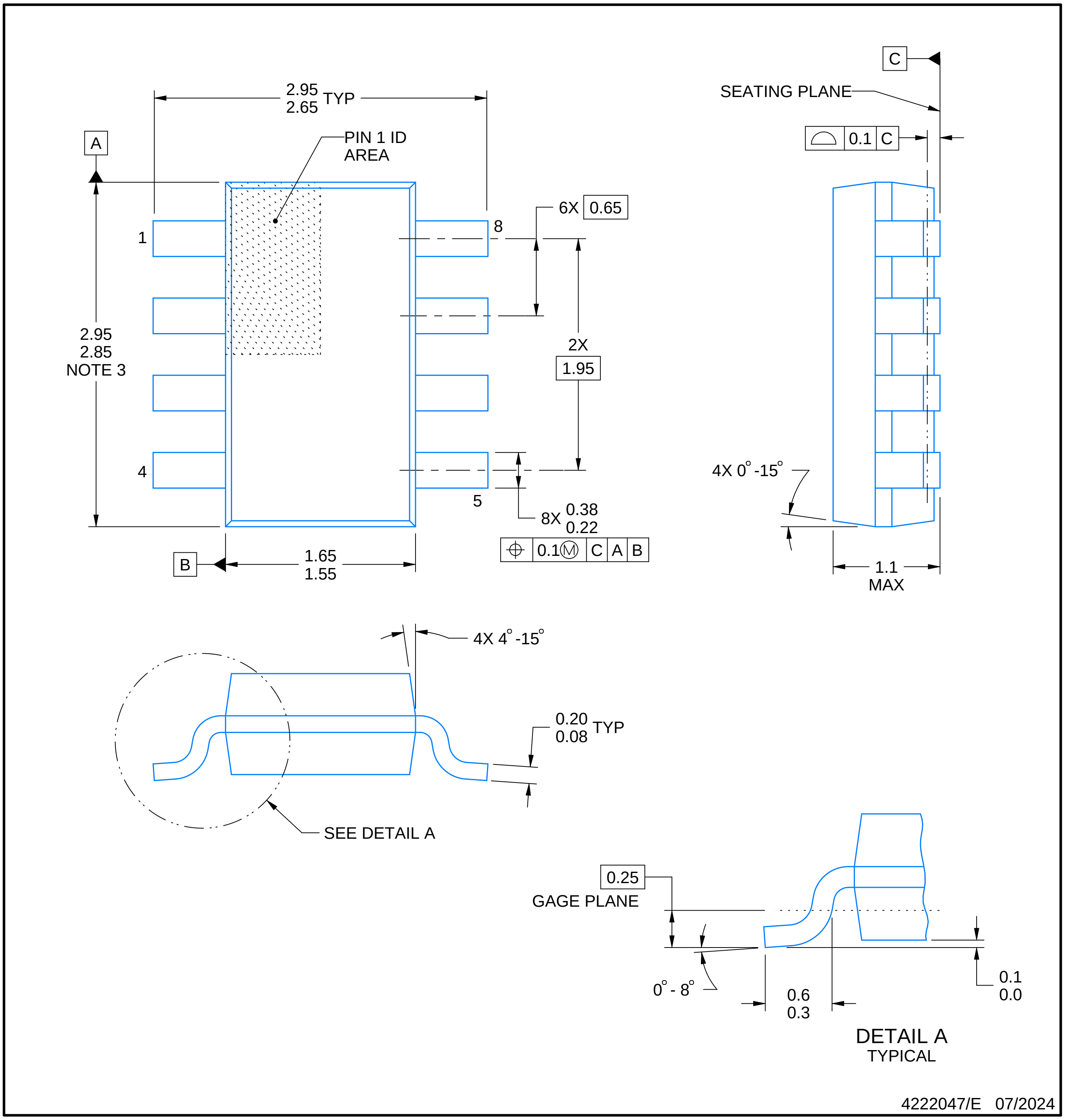
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA351ABSIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA351ABSIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA351ABSIRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
INA351CDSIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA351CDSIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA351CDSIRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

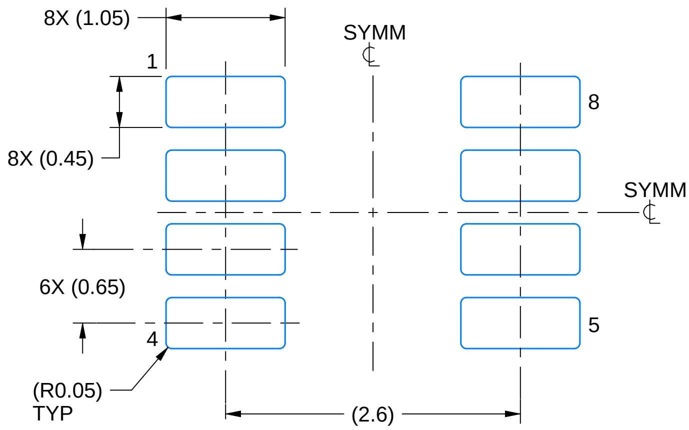
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

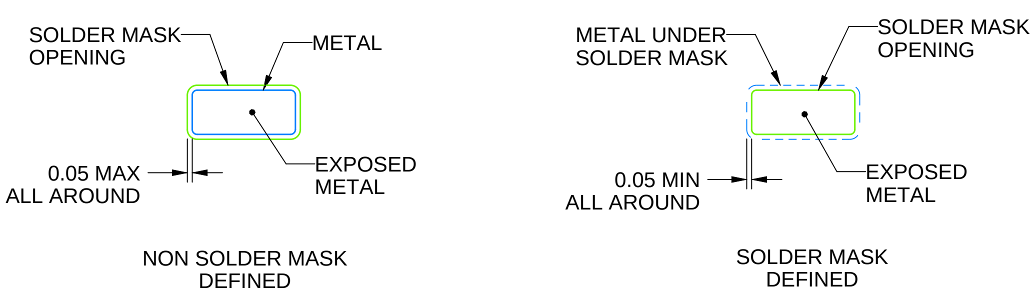


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

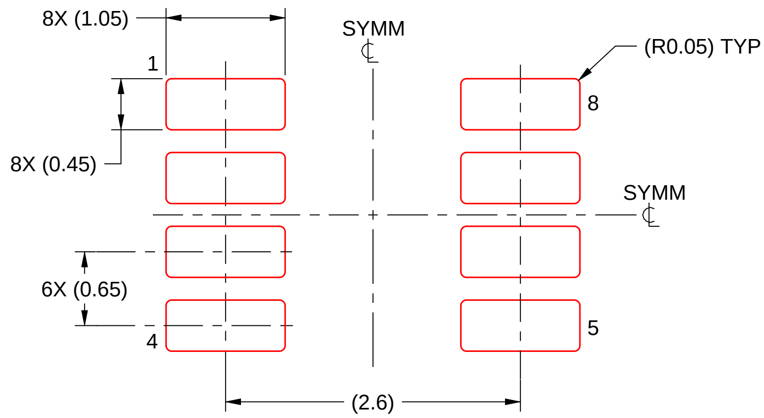


SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



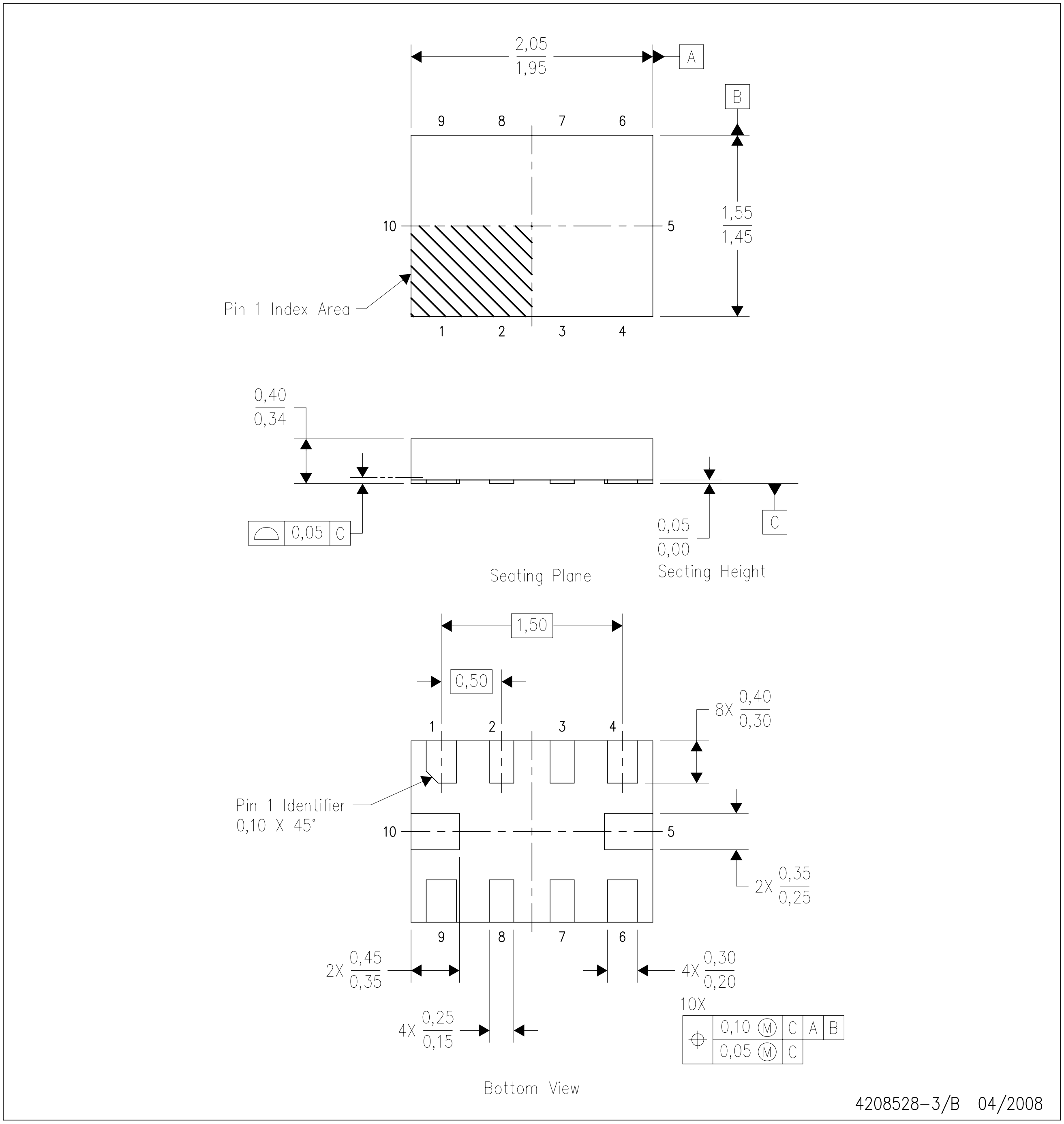
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

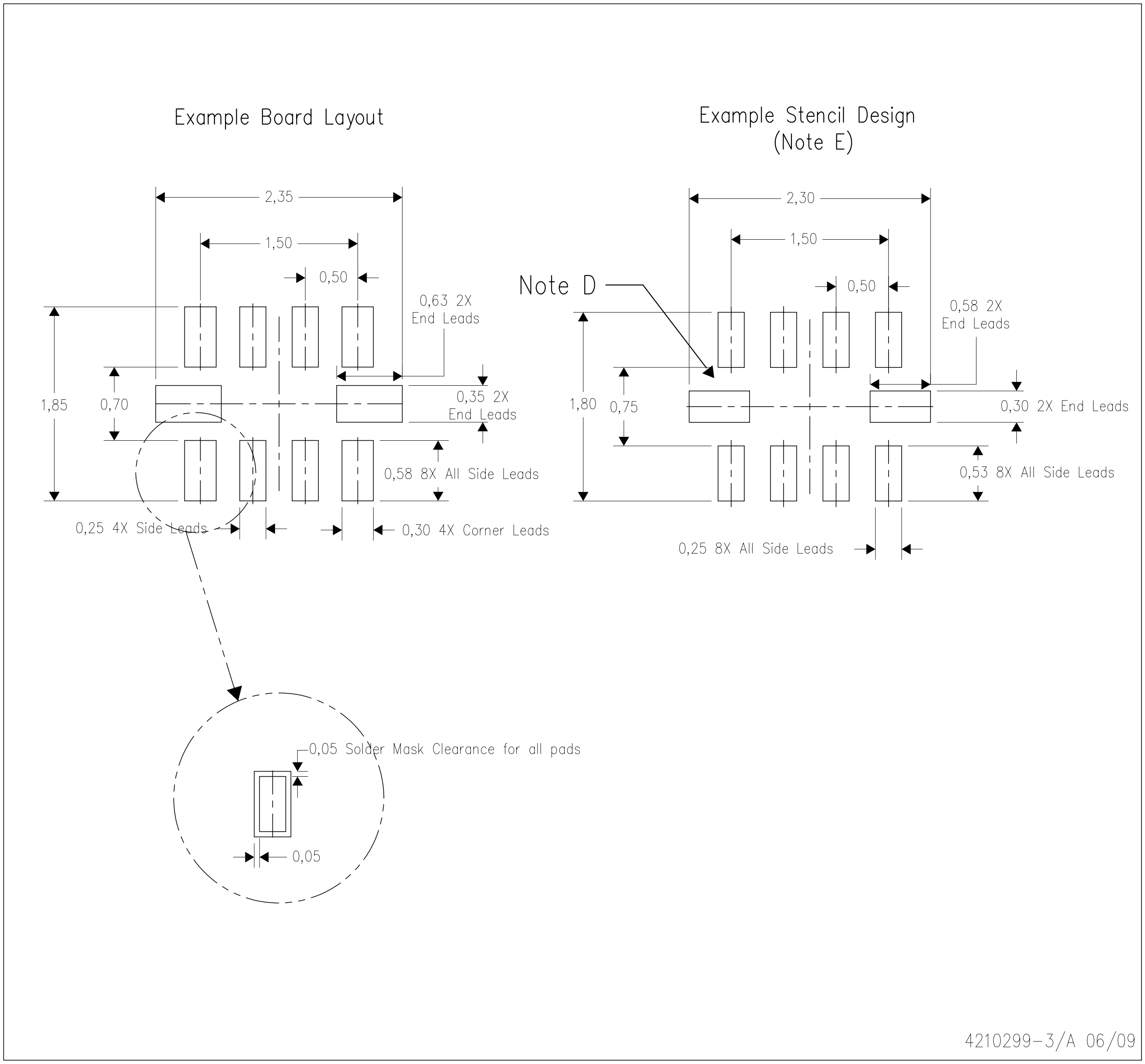
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

RUG (R-PQFP-N10) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

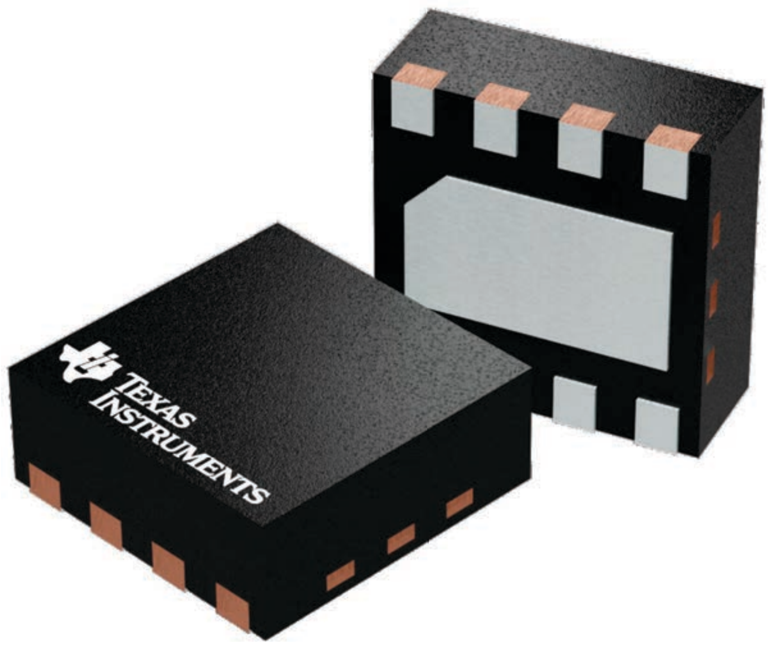
DSG 8

WSON - 0.8 mm max height

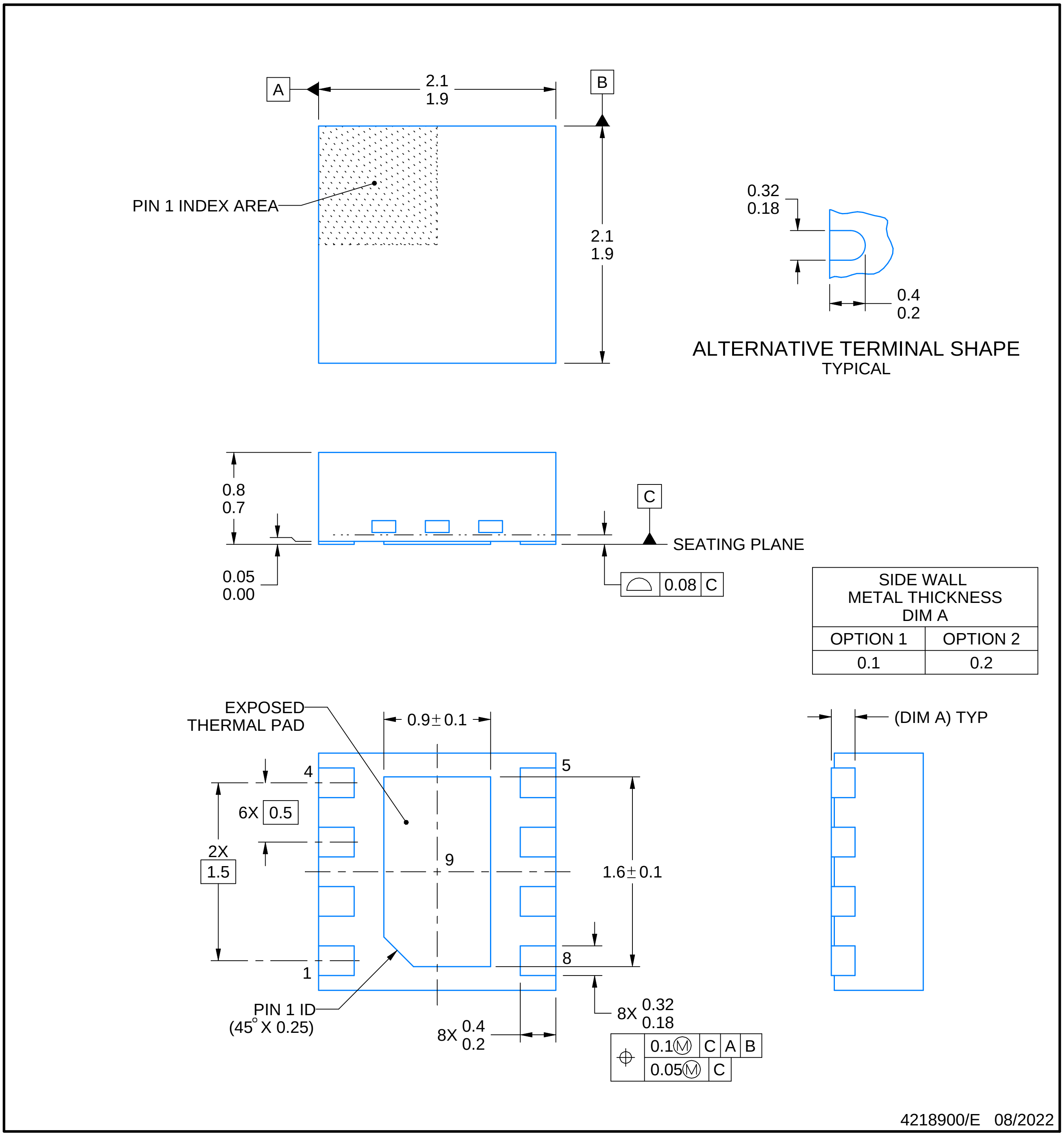
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



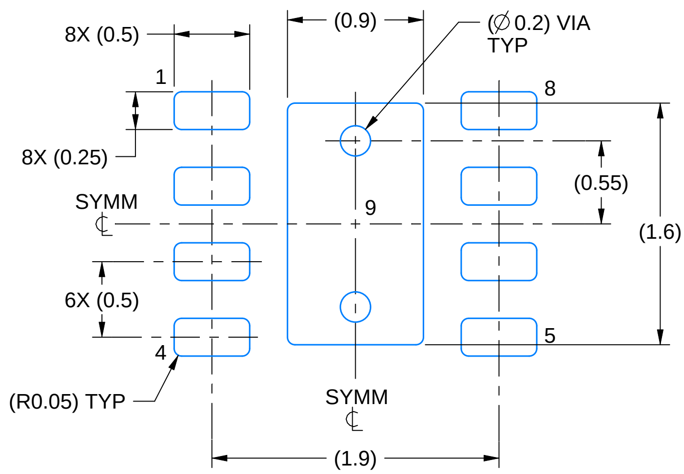
4224783/A



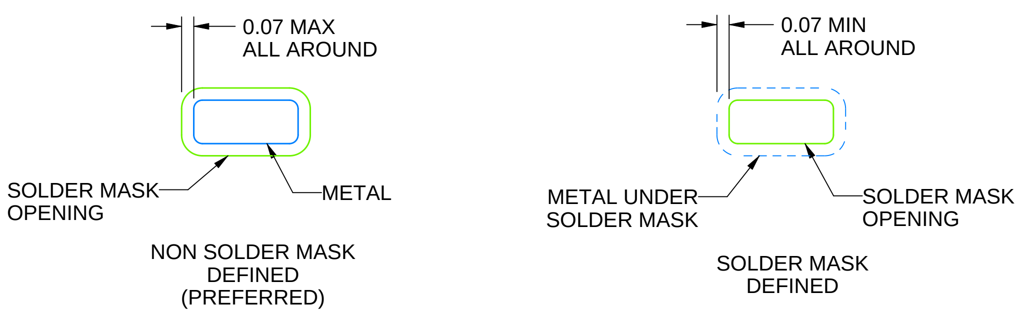
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

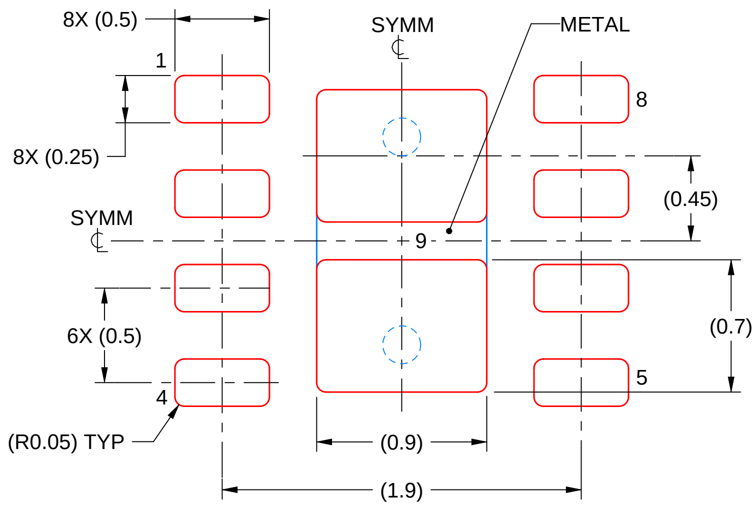


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.