

ISO654x-Q1 Automotive General Purpose Quad-Channel Functional Isolators

1 Features

- AEC-Q100 qualified with the following results:
 - Device temperature Grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature range
- Up to 50Mbps data rate
- Robust SiO_2 isolation barrier
- Functional Isolation (DBQ-16):
 - 400V_{RMS} , 566V_{DC} working voltage
 - 707V_{RMS} , 1000V_{DC} transient voltage (60s)
- Wide temperature range: -40°C to 125°C
- $\pm 150\text{kV}/\mu\text{s}$ typical CMTI
- Supply range: 1.71V to 5.5V
- Default output *high* (ISO654x-Q1) and *low* (ISO654xF-Q1) options
- 1.5mA per channel typical at 1Mbps and 3.3V (ISO6540-Q1)
- Low propagation delay: 11ns typical at 3.3V
- Robust electromagnetic compatibility (EMC)
 - System-level ESD, EFT, and surge immunity
 - Low emissions
- SSOP (DBQ-16) Package

2 Applications

- [Hybrid, electric and power train system \(EV/HEV\)](#)
 - [Battery management system \(BMS\)](#)
 - [On-board charger](#)
 - [DC/DC converter](#)
 - [Inverter and motor control](#)

3 Description

The ISO654x-Q1 devices are general purpose functional isolators for cost sensitive, space constrained applications that require isolation for non-safety applications. The isolation barrier supports a working voltage of 400V_{RMS} / 566V_{DC} and transient over voltages of 707V_{RMS} / 1000V_{DC} .

The ISO654x-Q1 devices provide high EMC performance while isolating CMOS or LVCMOS digital I/Os. ISO654x-Q1 uses SiO_2 as the isolation barrier. Each isolation channel has a logic input and output buffer separated by the insulation barrier. These devices come with enable pins that can be used to put the respective outputs in high impedance.

The ISO6540-Q1 and ISO6540F-Q1 devices have all channels in the forward direction. The ISO6541-Q1 and ISO6541F-Q1 devices have one reverse-direction channel. The ISO6542-Q1 and ISO6542F-Q1 devices have two reverse-direction channels.

In the event of input power or signal loss, the default output is *high* for devices without the suffix F and *low* for devices with the suffix F. See [Section 7.4](#) for further details.

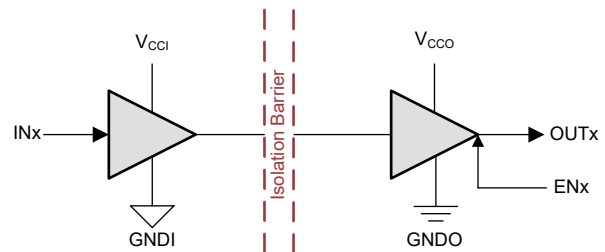
These devices help prevent noise currents on GPIOs or data buses such as SPI, UART and CAN from causing data corruption or damaging sensitive circuitry. Through chip design and layout techniques, the electromagnetic compatibility of the devices have been significantly enhanced to ease system-level design.

Package Information

PART NUMBER ⁽¹⁾	PACKAGE	PACKAGE SIZE ⁽²⁾
ISO6540-Q1 , ISO6540F-Q1	SSOP (DBQ-16)	6mm × 4.9mm
ISO6541-Q1 , ISO6541F-Q1		
ISO6542-Q1 , ISO6542F-Q1		

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{CCI} =Input supply, V_{CCO} =Output supply
 GNDI =Input ground, GNDO =Output ground

Simplified Schematic

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4 Pin Configuration and Functions

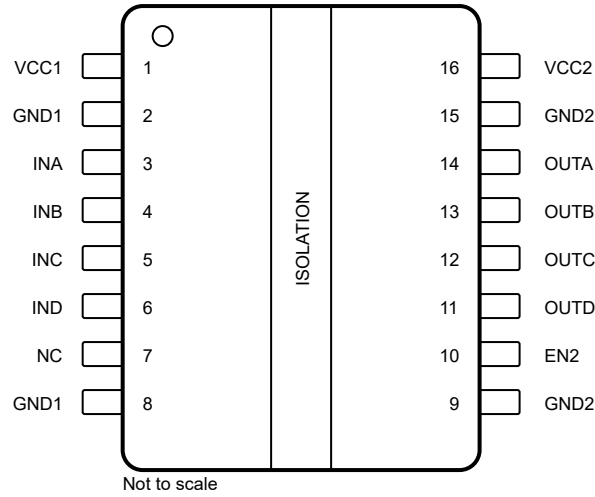


Figure 4-1. ISO6540-Q1 and ISO6540F-Q1 Top View

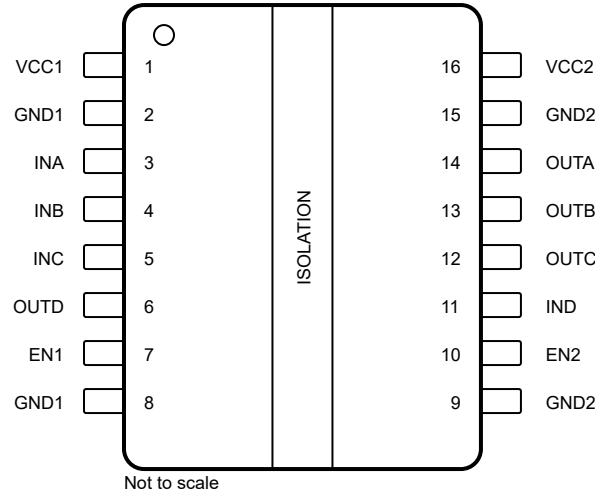


Figure 4-2. ISO6541-Q1 and ISO6541F-Q1 Top View

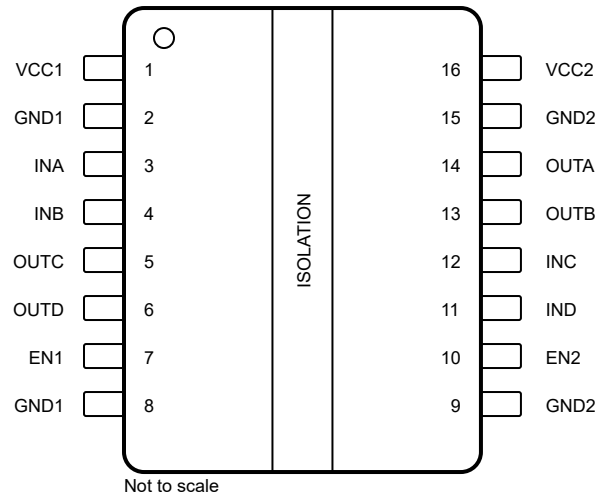


Figure 4-3. ISO6542-Q1 and ISO6542F-Q1 Top View

Table 4-1. Pin Functions

NAME	PIN			Type ⁽¹⁾	DESCRIPTION
	ISO6540-Q1 , ISO6540F-Q1	ISO6541-Q1 , ISO6541F-Q1	ISO6542-Q1 , ISO6542F-Q1		
EN1	-	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	2,8	2,8	—	Ground connection for V _{CC1}
GND2	9, 15	9,15	9,15	—	Ground connection for V _{CC2}
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	11	I	Input, channel D
NC	7	-	-		Not connected
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	6	O	Output, channel D
V _{CC1}	1	1	1	—	Power supply, side 1
V _{CC2}	16	16	16	—	Power supply, side 2

(1) I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

See⁽¹⁾

		MIN	MAX	UNIT
Supply voltage ⁽²⁾	V _{CC1} to GND1	-0.5	6	V
	V _{CC2} to GND2	-0.5	6	
Input/Output Voltage	IN _x to GND _x	-0.5	V _{CCX} + 0.5 ⁽³⁾	V
	OUT _x to GND _x	-0.5	V _{CCX} + 0.5 ⁽³⁾	
Output current	I _o	-15	15	mA
Temperature	Operating junction temperature, T _J		150	°C
	Storage temperature, T _{stg}	-65	150	°C
Transient Isolation Voltage (SSOP-16)	AC Voltage, t=60s		707	V _{RMS}
	DC Voltage, t=60s		1000	V _{DC}

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6V.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC1} ⁽¹⁾	Supply Voltage Side 1	V _{CC} = 1.8V ⁽³⁾	1.71		1.89	V
V _{CC1} ⁽¹⁾	Supply Voltage Side 1	V _{CC} = 2.5V to 5V ⁽³⁾	2.25		5.5	V
V _{CC2} ⁽¹⁾	Supply Voltage Side 2	V _{CC} = 1.8V ⁽³⁾	1.71		1.89	V
V _{CC2} ⁽¹⁾	Supply Voltage Side 2	V _{CC} = 2.5V to 5V ⁽³⁾	2.25		5.5	V
V _{CC} (UVLO+)	UVLO threshold when supply voltage is rising			1.53	1.71	V
V _{CC} (UVLO-)	UVLO threshold when supply voltage is falling		1.1	1.41		V
V _{hys} (UVLO)	Supply voltage UVLO hysteresis		0.08	0.13		V
V _{IH}	High level Input voltage		0.7 × V _{CCI} ⁽²⁾		V _{CCI}	V
V _{IL}	Low level Input voltage		0	0.3 × V _{CCI}		V
I _{OH}	High level output current	V _{CCO} = 5V ⁽²⁾	-4			mA
		V _{CCO} = 3.3V	-2			mA
		V _{CCO} = 2.5V	-1			mA
		V _{CCO} = 1.8V	-1			mA
I _{OL}	Low level output current	V _{CCO} = 5V			4	mA
		V _{CCO} = 3.3V			2	mA
		V _{CCO} = 2.5V			1	mA
		V _{CCO} = 1.8V			1	mA
DR	Data Rate		0		50	Mbps
T _A	Ambient temperature		-40	25	125	°C
T _A	Functional Isolation Working Voltage (SSOP-16)	AC Voltage (sine wave)			400	V _{RMS}
		DC Voltage			566	V _{DC}

(1) V_{CC1} and V_{CC2} can be set independent of one another

(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

(3) The channel outputs are in undetermined state when 1.89V < V_{CC1}, V_{CC2} < 2.25V and 1.05V < V_{CC1}, V_{CC2} < 1.71V

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO654x	UNIT
		DBQ (SSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [no.](#)

5.5 Package Characteristics

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DBQ-16	
CLR	External clearance ⁽¹⁾	Side 1 to side 2 distance through air	>3.7	mm
CPG	External creepage ⁽¹⁾	Side 1 to side 2 distance across package surface	>3.7	mm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material group	According to IEC 60664-1	I	
C _{IO}	Barrier capacitance, input to output ⁽²⁾	V _{IO} = 0.4 x sin(2πft), f = 1MHz	≅1	pF
R _{IO}	Isolation resistance ⁽²⁾	T _A = 25°C	>10 ¹²	Ω

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) All pins on each side of the barrier tied together creating a two-terminal device.

5.6 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4\text{mA}$; See Section 6	$V_{CCO} - 0.4$ ⁽¹⁾			V
V_{OL}	Low-level output voltage	$I_{OH} = 4\text{mA}$; See Section 6			0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ ⁽¹⁾		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at ENx			28	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at ENx	-28			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200\text{ V}$; See Section 6	100	150		$\text{kV}/\mu\text{A}$
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2\text{ MHz}$, $V_{CC} = 5\text{ V}$		2.8		pF

(1) $V_{CCI} =$ Input-side V_{CC} ; $V_{CCO} =$ Output-side V_{CC}

(2) Measured from input pin to same side ground.

5.7 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6540-Q1							
Supply current - DC signal (2)	$V_I = V_{CC1}$ (1)(ISO6540); $V_I = 0\text{ V}$ (ISO6540 with F suffix)	I_{CC1}		1.6	2.4	mA	
		I_{CC2}		2.1	3.7		
	$V_I = 0\text{ V}$ (ISO6540); $V_I = V_{CC1}$ (ISO6540 with F suffix)	I_{CC1}		5.8	8		
		I_{CC2}		2.3	4.0		
Supply current - AC signal (3)	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.7		5.1
			I_{CC2}		2.4		4.1
		10 Mbps	I_{CC1}		3.8		5.3
			I_{CC2}		4.8		6.6
		50 Mbps	I_{CC1}		4.4	6	
			I_{CC2}		15	18.1	
ISO6541-Q1							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1)(ISO6541); $V_I = 0\text{ V}$ (ISO6541 with F suffix)	I_{CC1}		1.9	2.9	mA	
		I_{CC2}		2.2	3.8		
	$V_I = 0\text{ V}$ (ISO6541); $V_I = V_{CCI}$ (ISO6541 with F suffix)	I_{CC1}		5.1	7.2		
		I_{CC2}		3.4	5.2		
Supply current - AC signal (3)	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.6		5.1
			I_{CC2}		3		4.7
		10 Mbps	I_{CC1}		4.2		5.8
			I_{CC2}		4.8		6.5
		50 Mbps	I_{CC1}		7.3	9.3	
			I_{CC2}		12.6	15.3	
ISO6542-Q1							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1)(ISO6542); $V_I = 0\text{ V}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		2.2	3.5	mA	
	$V_I = 0\text{ V}$ (ISO6542); $V_I = V_{CCI}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		4.4	6.3		
Supply current - AC signal (3)	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		3.4		5
			10 Mbps	I_{CC1}, I_{CC2}			4.7
		50 Mbps		I_{CC1}, I_{CC2}			10.2

- (1) $V_{CCI} = \text{Input-side } V_{CC}$
- (2) Supply current valid for $ENx = V_{CCx}$ and $ENx = 0\text{ V}$
- (3) Supply current valid for $ENx = V_{CCx}$

5.8 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{mA}$; See Section 6	$V_{CCO} - 0.2$ ⁽¹⁾			V
V_{OL}	Low-level output voltage	$I_{OH} = 2\text{mA}$; See Section 6			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ ⁽¹⁾		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at ENx			30	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at ENx	-30			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200\text{ V}$; See Section 6	100	150		$\text{kV}/\mu\text{A}$
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t)$, $f = 2\text{ MHz}$, $V_{CC} = 3.3\text{ V}$		2.8		pF

(1) $V_{CCI} = \text{Input-side } V_{CC}$; $V_{CCO} = \text{Output-side } V_{CC}$

(2) Measured from input pin to same side ground.

5.9 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6540-Q1							
Supply current - DC signal ⁽²⁾	$V_I = V_{CC1}$ ⁽¹⁾ (ISO6540); $V_I = 0\text{ V}$ (ISO6540 with F suffix)	I_{CC1}		1.6	2.3	mA	
		I_{CC2}		2.1	3.7		
	$V_I = 0\text{ V}$ (ISO6540); $V_I = V_{CC1}$ (ISO6540 with F suffix)	I_{CC1}		5.7	8		
		I_{CC2}		2.3	4.0		
Supply current - AC signal ⁽³⁾	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.7		5.1
			I_{CC2}		2.4		4.0
		10 Mbps	I_{CC1}		3.8		5.2
			I_{CC2}		4		5.8
		50 Mbps	I_{CC1}		4.2	5.7	
			I_{CC2}		11.2	13.8	
ISO6541-Q1							
Supply current - DC signal ⁽²⁾	$V_I = V_{CCI}$ ⁽¹⁾ (ISO6541); $V_I = 0\text{ V}$ (ISO6541 with F suffix)	I_{CC1}		1.9	2.9	mA	
		I_{CC2}		2.2	3.7		
	$V_I = 0\text{ V}$ (ISO6541); $V_I = V_{CCI}$ (ISO6541 with F suffix)	I_{CC1}		5	7.1		
		I_{CC2}		3.4	5.1		
Supply current - AC signal ⁽³⁾	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.5		5
			I_{CC2}		2.9		4.6
		10 Mbps	I_{CC1}		4		5.5
			I_{CC2}		4.2		5.9
		50 Mbps	I_{CC1}		6.1	8	
			I_{CC2}		9.7	12.1	
ISO6542-Q1							
Supply current - DC signal ⁽²⁾	$V_I = V_{CCI}$ ⁽¹⁾ (ISO6542); $V_I = 0\text{ V}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		2.2	3.4	mA	
	$V_I = 0\text{ V}$ (ISO6542); $V_I = V_{CCI}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		4.4	6.3		
Supply current - AC signal ⁽³⁾	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		3.4		4.9
			10 Mbps	I_{CC1}, I_{CC2}			4.2
		50 Mbps		I_{CC1}, I_{CC2}			8.2

(1) $V_{CCI} = \text{Input-side } V_{CC}$

(2) Supply current valid for $ENx = V_{CCx}$ and $ENx = 0\text{V}$

(3) Supply current valid for $ENx = V_{CCx}$

5.10 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1\text{mA}$; See Section 6	$V_{CCO} - 0.1$ ⁽¹⁾			V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{mA}$; See Section 6			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ ⁽¹⁾		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at ENx			30	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at ENx	-30			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200\text{ V}$; See Section 6	100	150		$\text{kV}/\mu\text{A}$
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t)$, $f = 2\text{ MHz}$, $V_{CC} = 2.5\text{ V}$		2.8		pF

(1) $V_{CCI} = \text{Input-side } V_{CC}$; $V_{CCO} = \text{Output-side } V_{CC}$

(2) Measured from input pin to same side ground.

5.11 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6540-Q1							
Supply current - DC signal (2)	$V_I = V_{CC1}$ (1)(ISO6540); $V_I = 0\text{ V}$ (ISO6540 with F suffix)	I_{CC1}		1.6	2.3	mA	
		I_{CC2}		2.1	3.7		
	$V_I = 0\text{ V}$ (ISO6540); $V_I = V_{CC1}$ (ISO6540 with F suffix)	I_{CC1}		5.7	7.9		
		I_{CC2}		2.3	4.0		
Supply current - AC signal (3)	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.7		5.1
			I_{CC2}		2.3		4.0
		10 Mbps	I_{CC1}		3.7		5.1
			I_{CC2}		3.5		5.3
		50 Mbps	I_{CC1}		4.1	5.6	
			I_{CC2}		9	11.5	
ISO6541-Q1							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1)(ISO6541); $V_I = 0\text{ V}$ (ISO6541 with F suffix)	I_{CC1}		1.9	2.9	mA	
		I_{CC2}		2.2	3.7		
	$V_I = 0\text{ V}$ (ISO6541); $V_I = V_{CCI}$ (ISO6541 with F suffix)	I_{CC1}		5	7.1		
		I_{CC2}		3.4	5.1		
Supply current - AC signal (3)	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.5		5
			I_{CC2}		2.9		4.5
		10 Mbps	I_{CC1}		3.9		5.4
			I_{CC2}		3.8		5.5
		50 Mbps	I_{CC1}		5.5	7.2	
			I_{CC2}		8.1	10.2	
ISO6542-Q1							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1)(ISO6542); $V_I = 0\text{ V}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		2.2	3.4	mA	
	$V_I = 0\text{ V}$ (ISO6542); $V_I = V_{CCI}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		4.3	6.3		
Supply current - AC signal (3)	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		3.3		4.8
			10 Mbps	I_{CC1}, I_{CC2}			4
		50 Mbps		I_{CC1}, I_{CC2}			7

- (1) $V_{CCI} = \text{Input-side } V_{CC}$
- (2) Supply current valid for $ENx = V_{CCx}$ and $ENx = 0\text{V}$
- (3) Supply current valid for $ENx = V_{CCx}$

5.12 Electrical Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1\text{mA}$; See Section 6	$V_{CCO} - 0.1$ ⁽¹⁾			V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{mA}$; See Section 6			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ ⁽¹⁾		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at ENx			30	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at ENx	-30			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200\text{ V}$; See Section 6	100	150		$\text{kV}/\mu\text{A}$
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2\text{ MHz}$, $V_{CC} = 1.8\text{ V}$		2.8		pF

(1) $V_{CCI} = \text{Input-side } V_{CC}$; $V_{CCO} = \text{Output-side } V_{CC}$

(2) Measured from input pin to same side ground.

5.13 Supply Current Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6540-Q1							
Supply current - DC signal ⁽²⁾	$V_I = V_{CC1}$ ⁽¹⁾ (ISO6540); $V_I = 0\text{ V}$ (ISO6540 with F suffix)	I_{CC1}		1.2	1.8	mA	
		I_{CC2}		2	3.7		
	$V_I = 0\text{ V}$ (ISO6540); $V_I = V_{CC1}$ (ISO6540 with F suffix)	I_{CC1}		5.1	7.6		
		I_{CC2}		2.2	4.0		
Supply current - AC signal ⁽³⁾	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.1		4.7
			I_{CC2}		2.2		4.0
		10 Mbps	I_{CC1}		3.2		4.8
			I_{CC2}		3.1		4.9
		50 Mbps	I_{CC1}		3.4	5.1	
			I_{CC2}		7	9.7	
ISO6541-Q1							
Supply current - DC signal ⁽²⁾	$V_I = V_{CCI}$ ⁽¹⁾ (ISO6541); $V_I = 0\text{ V}$ (ISO6541 with F suffix)	I_{CC1}		1.5	2.5	mA	
		I_{CC2}		2	3.6		
	$V_I = 0\text{ V}$ (ISO6541); $V_I = V_{CCI}$ (ISO6541 with F suffix)	I_{CC1}		4.5	6.9		
		I_{CC2}		3.2	5		
Supply current - AC signal ⁽³⁾	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.1		4.7
			I_{CC2}		2.7		4.4
		10 Mbps	I_{CC1}		3.3		5
			I_{CC2}		3.4		5.1
		50 Mbps	I_{CC1}		4.5	6.3	
			I_{CC2}		6.4	8.7	
ISO6542-Q1							
Supply current - DC signal ⁽²⁾	$V_I = V_{CCI}$ ⁽¹⁾ (ISO6542); $V_I = 0\text{ V}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		1.9	3.2	mA	
	$V_I = 0\text{ V}$ (ISO6542); $V_I = V_{CCI}$ (ISO6542 with F suffix)	I_{CC1}, I_{CC2}		4	6.1		
Supply current - AC signal ⁽³⁾	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		3		4.7
			10 Mbps	I_{CC1}, I_{CC2}			3.5
		50 Mbps		I_{CC1}, I_{CC2}			5.6

- (1) $V_{CCI} = \text{Input-side } V_{CC}$
- (2) Supply current valid for $ENx = V_{CCx}$ and $ENx = 0\text{V}$
- (3) Supply current valid for $ENx = V_{CCx}$

5.14 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 6		11	18	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0.2	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				6	ns
t_r	Output signal rise time	See Section 6		2.6	4.5	ns
t_f	Output signal fall time			2.6	4.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 6		18.6	25.8	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			18.6	25.8	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO654x			14.2	21.1	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO654x			14.2	21.1	ns
t_{PU}	Time from UVLO to valid output data				300	μ s
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Section 6		0.1	0.3	μ s
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.15 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay time	at 100kbps		11	18	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $	See Figure 1-1		0.5	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				7	ns
t_r	Output signal rise time	See Section 6		1.6	3.2	ns
t_f	Output signal fall time			1.6	3.2	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 6		23.2	34.4	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			23.2	34.4	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO654x			16.6	23	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO654x			16.6	23	ns
t_{PU}	Time from UVLO to valid output data				300	μ s
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Section 6		0.1	0.3	μ s
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.16 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Figure 1-1		12	20.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0.6	7.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				7	ns
t_r	Output signal rise time	See Section 6		2	4	ns
t_f	Output signal fall time			2	4	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 6		28.1	43	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			28.1	43	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO654x			20.4	36.3	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO654x			20.4	36.3	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Section 6		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.17 Switching Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Figure 1-1		15	24	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0.7	8.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				8.8	ns
t_r	Output signal rise time	See Section 6		2.7	5.3	ns
t_f	Output signal fall time			2.7	5.3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 6		40.3	63	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			40.3	63	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO654x			30	51.4	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO654x			30	51.4	ns
t_{PU}	Time from UVLO to valid output data				300	μ s
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Section 6		0.1	0.3	μ s
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.18 Typical Characteristics

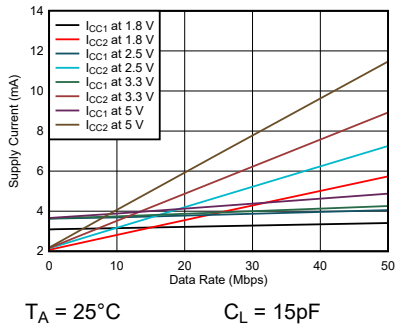


Figure 5-1. ISO6540-Q1 or ISO6540F-Q1 Supply Current vs Data Rate (With 15pF Load)

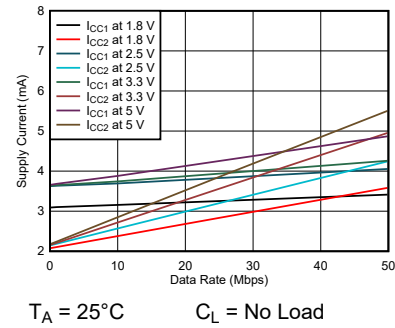


Figure 5-2. ISO6540-Q1 or ISO6540F-Q1 Supply Current vs Data Rate (With No Load)

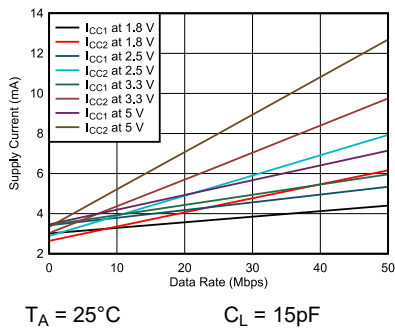


Figure 5-3. ISO6541-Q1 or ISO6541F-Q1 Supply Current vs Data Rate (With 15pF Load)

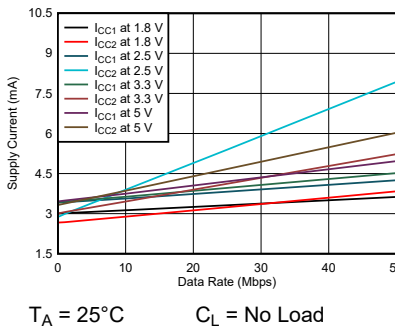


Figure 5-4. ISO6541-Q1 or ISO6541F-Q1 Supply Current vs Data Rate (With No Load)

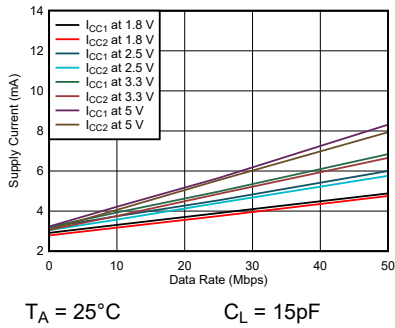


Figure 5-5. ISO6542-Q1 or ISO6542F-Q1 Supply Current vs Data Rate (With 15pF Load)

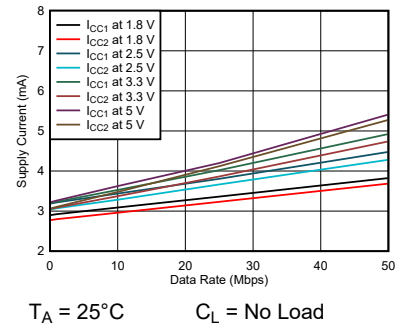


Figure 5-6. ISO6542-Q1 or ISO6542F-Q1 Supply Current vs Data Rate (With No Load)

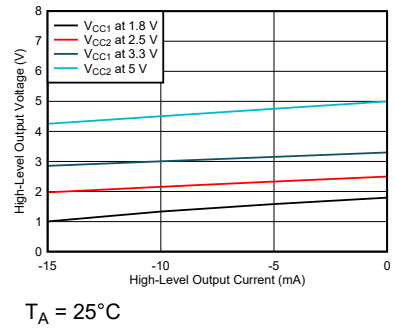


Figure 5-7. High-Level Output Voltage vs High-level Output Current

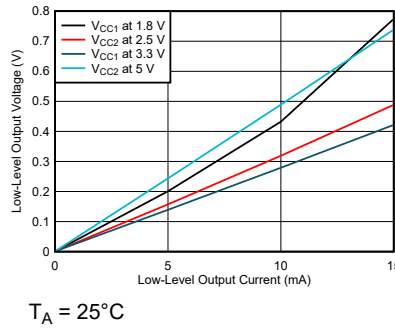


Figure 5-8. Low-Level Output Voltage vs Low-Level Output Current

5.18 Typical Characteristics (continued)

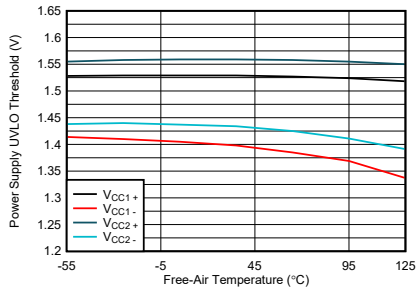


Figure 5-9. Power Supply Undervoltage Threshold vs Free-Air Temperature

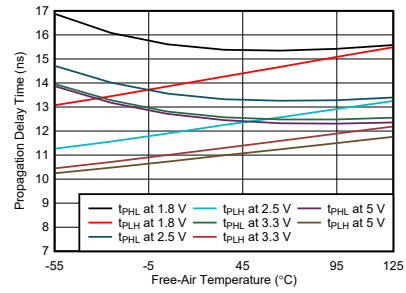
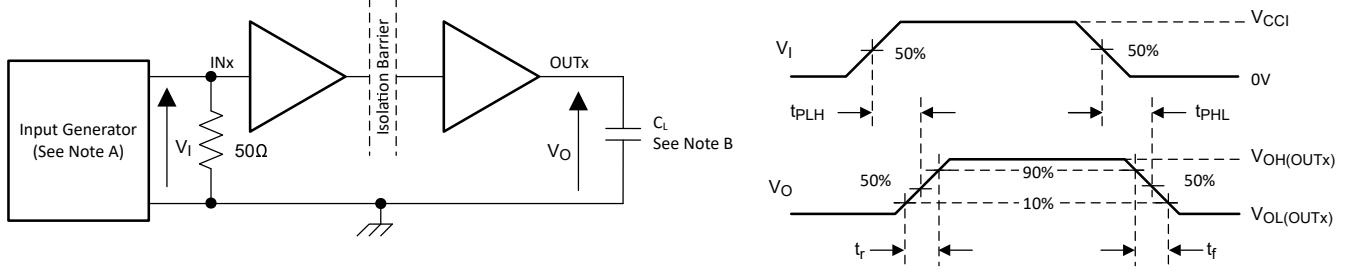


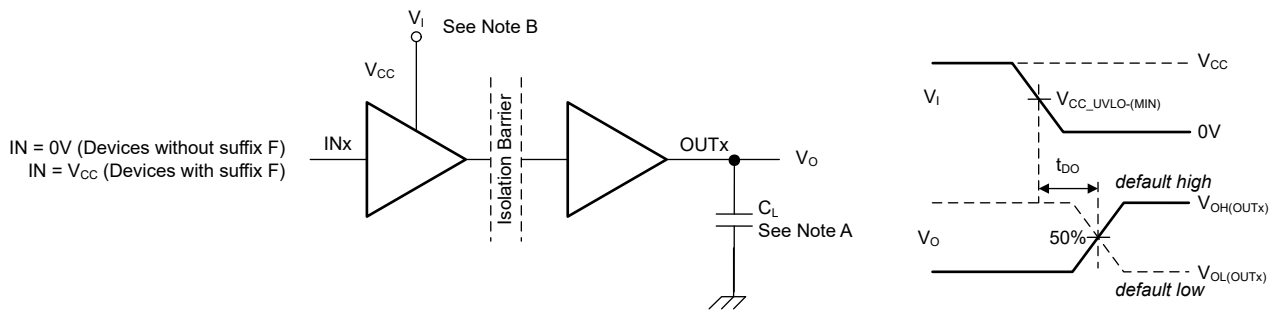
Figure 5-10. Propagation Delay Time vs Free-Air Temperature

6 Parameter Measurement Information



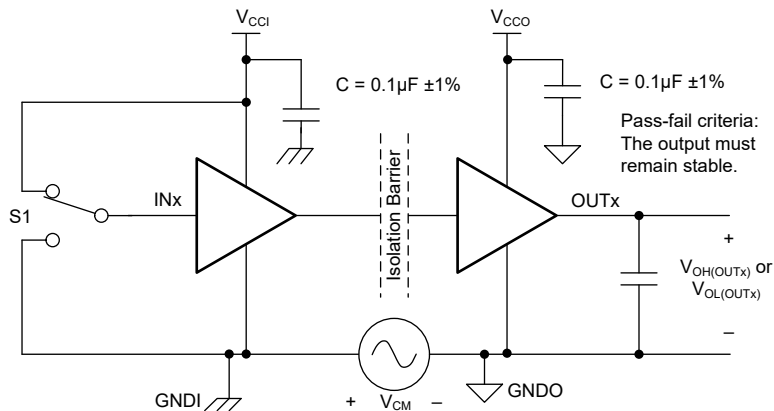
- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50kHz, 50% duty cycle, $t_r \leq$ 3ns, $t_f \leq$ 3ns, $Z_0 = 50\Omega$. At the input, 50Ω resistor is required to terminate INx (input) generator signal. The 50Ω resistor is not needed in the actual application.
- B. $C_L = 15\text{pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



- A. $C_L = 15\text{pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. Power Supply Ramp Rate = 10mV/ns

Figure 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15\text{pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. $ENx = V_{CC}$, channels are enabled during CMTI test.

Figure 6-3. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO654x-Q1 family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier.

The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO654x-Q1 devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching.

7.2 Functional Block Diagram

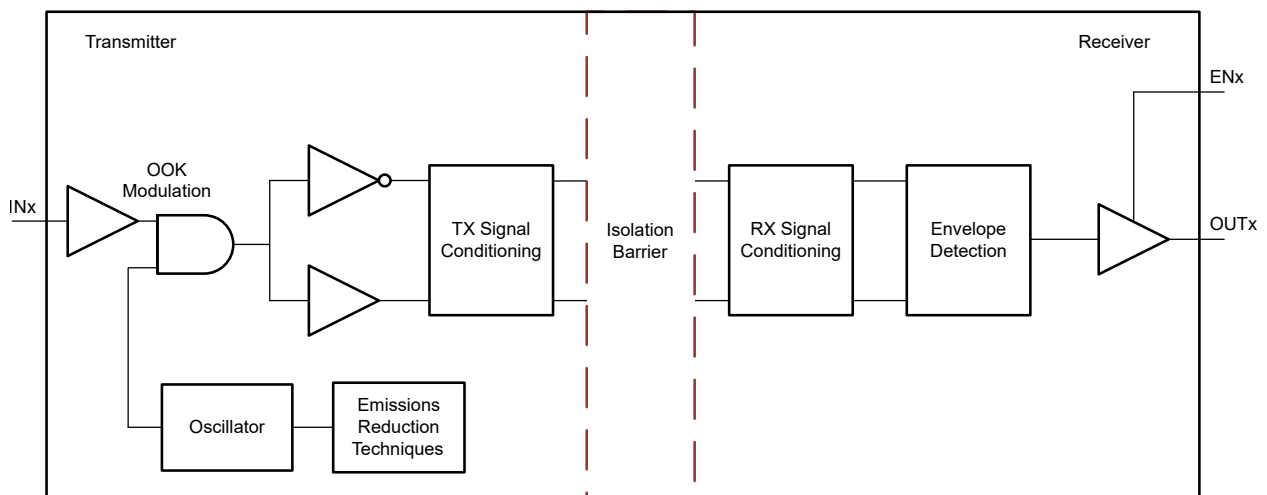


Figure 7-1. Conceptual Block Diagram of an OOK Based Digital Isolator

Figure 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

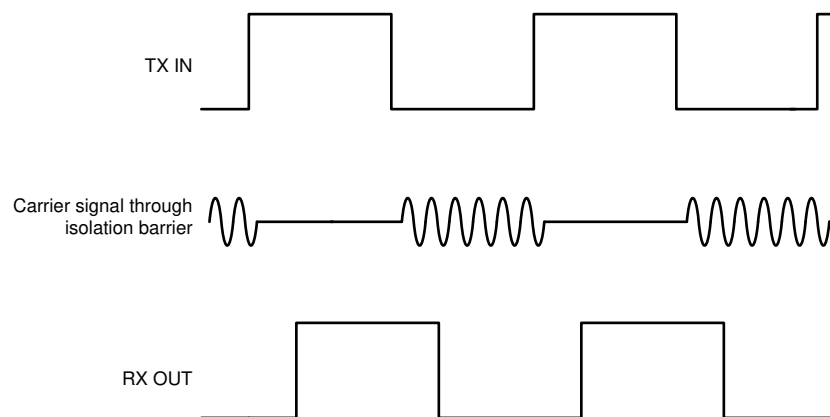


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

Table 7-1 provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE
ISO6540-Q1	4 Forward 0 Reverse	50Mbps	High	DBQ-16
ISO6540F-Q1	4 Forward 0 Reverse	50Mbps	Low	DBQ-16
ISO6541-Q1	3 Forward 1 Reverse	50Mbps	High	DBQ-16
ISO6541F-Q1	3 Forward 1 Reverse	50Mbps	Low	DBQ-16
ISO6542-Q1	2 Forward 2 Reverse	50Mbps	High	DBQ-16
ISO6542F-Q1	2 Forward 2 Reverse	50Mbps	Low	DBQ-16

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are defined and tested by international standards such as IEC 61000-4-x and CISPR 25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO654x-Q1 family of devices incorporates many chip-level design techniques to help overall system robustness.

7.4 Device Functional Modes

Table 7-2 lists the functional modes for the ISO654x-Q1 devices.

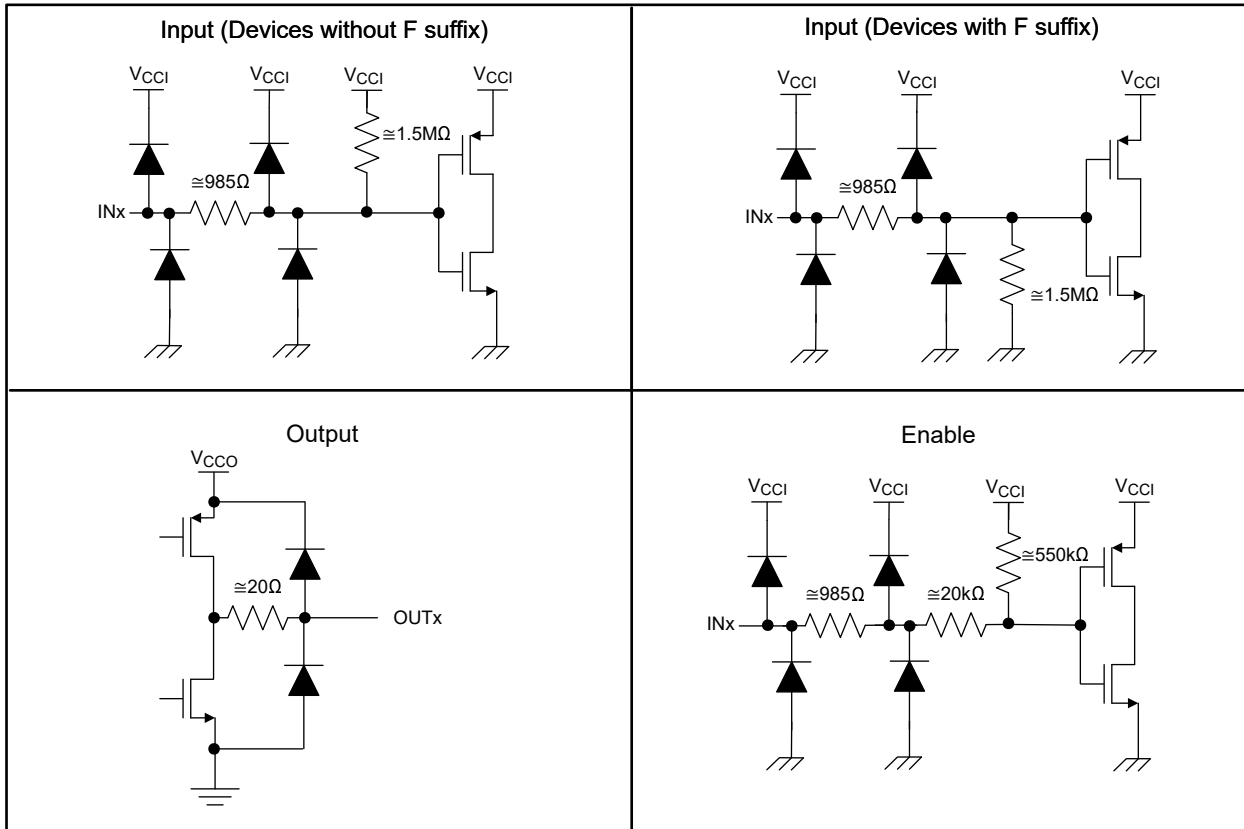
Table 7-2. Function Table

V _{CCI} (1)	V _{CCO}	INPUT (IN _x)	OUTPUT ENABLE (EN _x)	OUTPUT (OUT _x)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When IN _x is open, the corresponding channel output goes to the default logic state. Default is <i>High</i> for ISO654x-Q1 and <i>Low</i> for ISO654xF-Q1 (with F suffix).
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V _{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is <i>High</i> for ISO654x-Q1 and <i>Low</i> for ISO654xF-Q1 (with F suffix). When V _{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V _{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V _{CCO} is unpowered, a channel output is undetermined ⁽²⁾ . When V _{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ V_{CC_RO(MIN)}); PD = Powered down (V_{CC} ≤ V_{CC_UVLO-}); X = Irrelevant; H = High level; L = Low level; Z = High Impedance

(2) The outputs are in undetermined state when V_{CC_UVLO-} ≤ V_{CCI} or V_{CCO} < V_{CC} ≥ V_{CC_RO(MIN)}.

7.5 Device I/O Schematics



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO654x-Q1 devices are high-performance, low power, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for parallel (multiple) driver applications. The ISO654x-Q1 devices use single-ended CMOS-logic switching technology.

The supply voltage range is from 1.71V to 5.5V for both supplies, V_{CC1} and V_{CC2} . Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, supplying ISO654x-Q1 V_{CC1} with 3.3V (which is within 1.71V to 5.5V) and V_{CC2} with 5V (which is also within 1.71V to 5.5V) is possible. You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

Note

ISO654x-Q1 is a functional isolator, and is not certified for isolation by standard bodies. For applications that require certified isolation by standard bodies, customers must choose [ISO644x-Q1](#), [ISO674x-Q1](#) or [ISO774x-Q1](#) families of digital isolators.

8.2 Typical Application

Figure 8-1 shows an isolated dual CAN interface implementation.

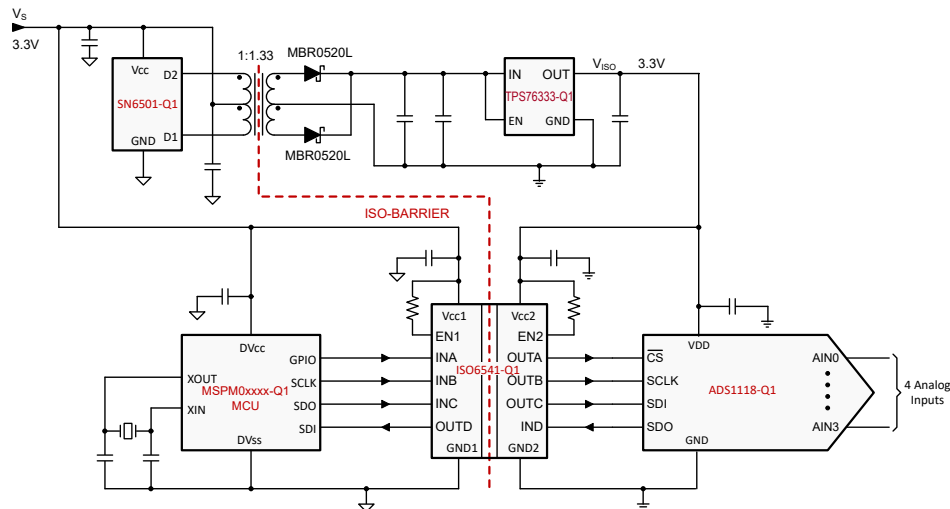


Figure 8-1. Isolated SPI for an Analog Measurement With 4 Inputs

Figure 8-2 shows an isolated dual CAN interface implementation.

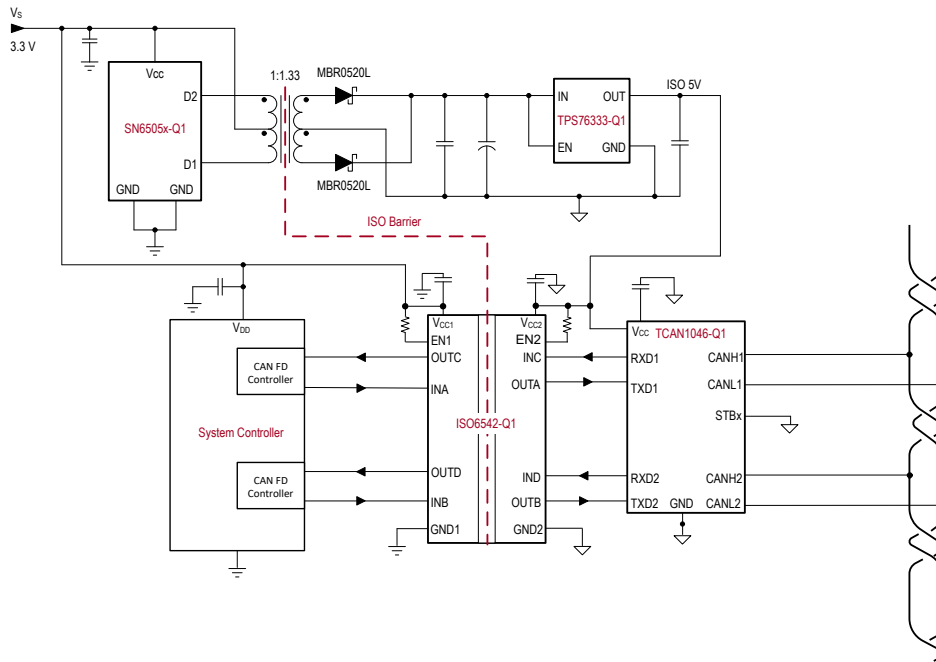


Figure 8-2. Typical Isolated Dual CAN Application Circuit

8.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 8-1](#).

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO654x-Q1 family of devices only require two external bypass capacitors to operate.

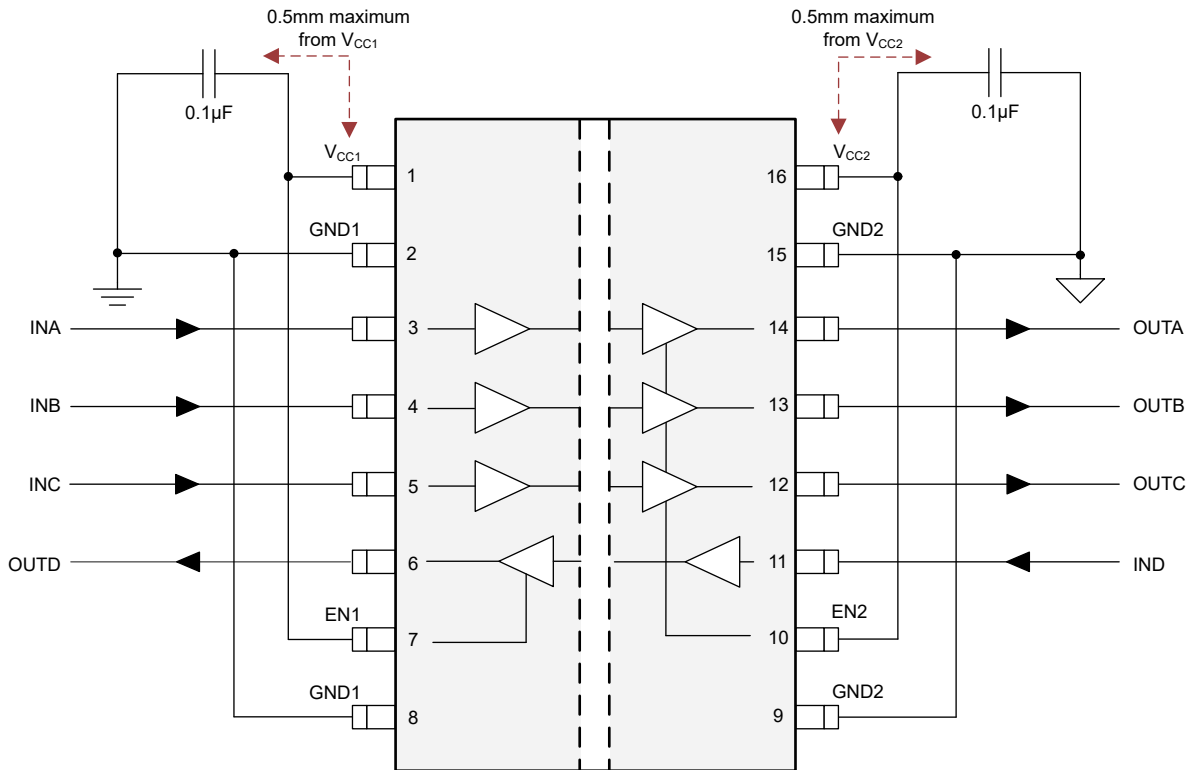
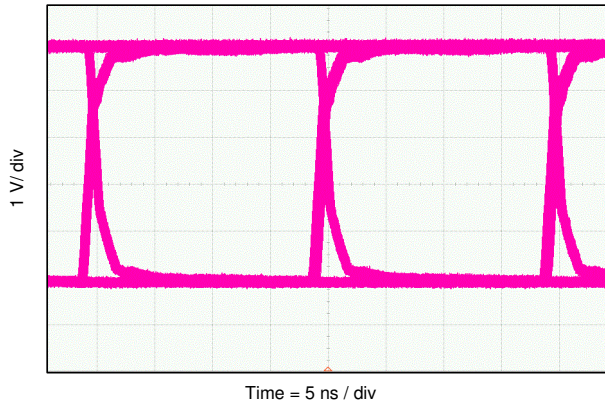


Figure 8-3. Typical ISO654x-Q1 Circuit

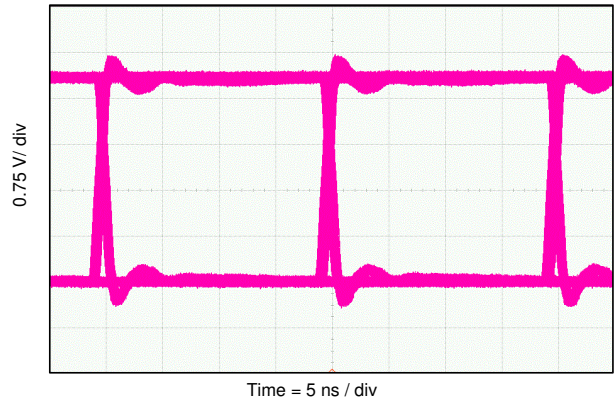
8.2.3 Application Curve

The following typical eye diagrams of the ISO654x-Q1 family of devices indicates low jitter and wide open eye at the maximum data rate of 50Mbps.



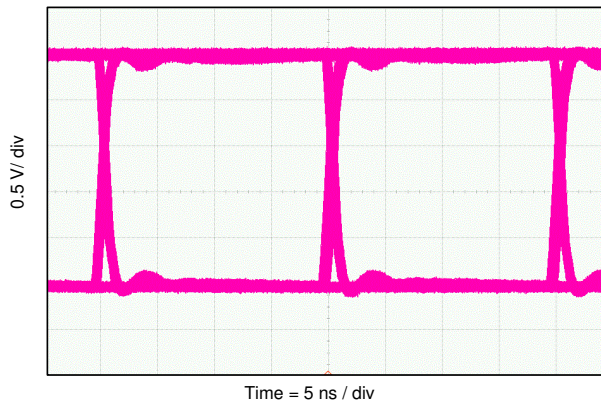
Horizontal 5ns / division, Vertical 1V / division.

Figure 8-4. ISO654x-Q1 Eye Diagram at 50Mbps PRBS $2^{16} - 1$, 5V and 25°C



Horizontal 5ns / division, Vertical 750mV / division.

Figure 8-5. ISO654x-Q1 Eye Diagram at 50Mbps PRBS $2^{16} - 1$, 3.3V and 25°C



Horizontal 5ns / division, Vertical 500mV / division.

Figure 8-6. ISO654x-Q1 Eye Diagram at 50Mbps PRBS $2^{16} - 1$, 2.5V and 25°C

8.3 Power Supply Recommendations

To provide reliable operation at data rates and supply voltages, a 0.1 μ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For automotive applications, please use [SN6501-Q1](#) or [SN6505B-Q1](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501-Q1 Transformer Driver for Isolated Power Supplies](#) or [SN6505B-Q1 Automotive, low-noise, 1-A, 420-kHz transformer driver with soft start for isolated power supplies](#).

8.4 Layout

8.4.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see [Layout Example Schematic](#)). Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#) application note.

8.4.2 Layout Example

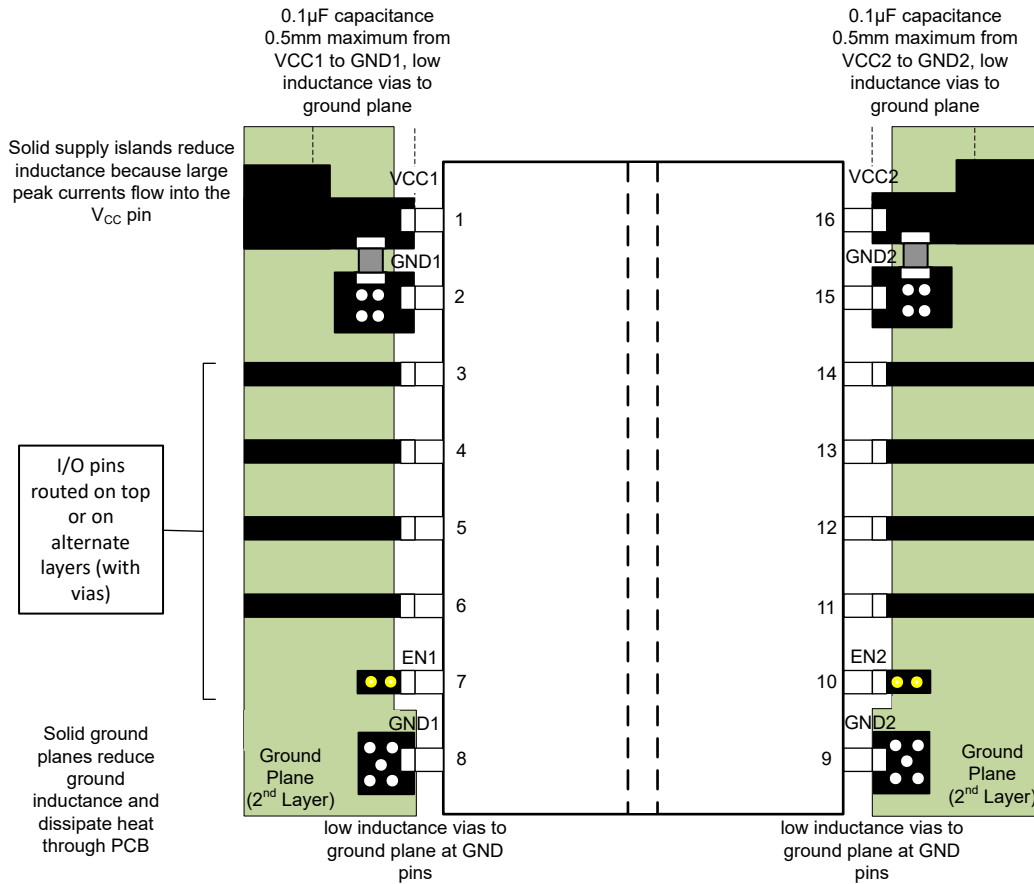


Figure 8-7. Layout Example

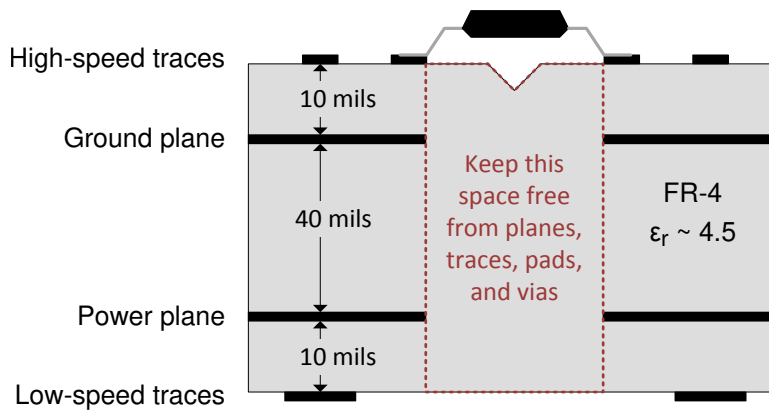


Figure 8-8. Layout Example PCB cross section

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ISO6540-Q1 Technical Documents](#)
- Texas Instruments, [ISO6541-Q1 Technical Documents](#)
- Texas Instruments, [ISO6542-Q1 Technical Documents](#)
- Texas Instruments, [Digital Isolator Design Guide](#), application note
- Texas Instruments, [Digital Isolator Design Guide](#), application note
- Texas Instruments, [Isolation Glossary](#), application note
- Texas Instruments, [How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems](#), application note
- Texas Instruments, [SN6505x-Q1 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#), data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO6540FQDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6540F
ISO6540FQDBQRQ1.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6540F
ISO6540QDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6540
ISO6541FQDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6541F
ISO6541FQDBQRQ1.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6541F
ISO6541QDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6541
ISO6541QDBQRQ1.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6541
ISO6542FQDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6542F
ISO6542FQDBQRQ1.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6542F
ISO6542QDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6542
ISO6542QDBQRQ1.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6542

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO6540-Q1, ISO6541-Q1, ISO6542-Q1 :

- Catalog : [ISO6540](#), [ISO6541](#), [ISO6542](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6540FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6540QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6541FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6541QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6542FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6542QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

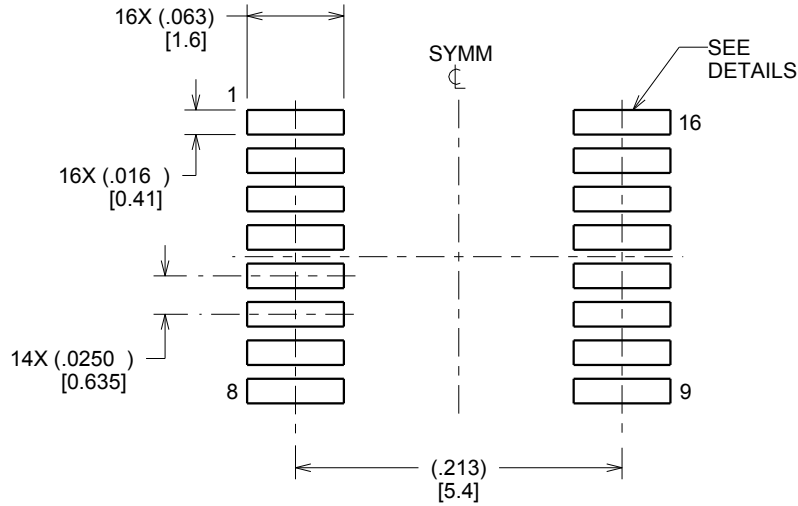
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6540FQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6540QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6541FQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6541QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6542FQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6542QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0

EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

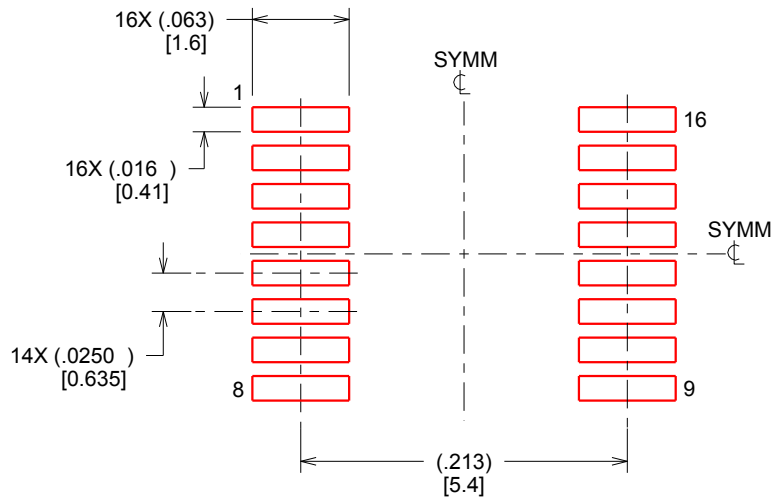
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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