

IWRL6432AOP Single-Chip 57 to 63.5GHz Industrial Radar Sensor with Antenna On Package (AOP)

1 Features

- FMCW Transceiver
 - Integrated PLL, transmitter, receiver, baseband and ADC
 - 57GHz to 63.5GHz coverage with 6.5GHz continuous bandwidth
 - Range typically up to 20m
 - FMCW operation
 - 5MHz IF bandwidth, real-only Rx channels
 - Ultra-accurate chirp engine based on fractional-N PLL
- Integrated 3 receive channels and 2 transmit channels Antennas-On-Package (AOP)
- Processing elements
 - Arm® M4F® core with single precision FPU (160MHz)
 - TI Radar Hardware Accelerator (HWA 1.2) for FFT, log magnitude, and CFAR operations (80MHz)
- Supports multiple low-power modes
 - Idle mode and deep sleep mode
- Power management
 - 1.8V and 3.3V IO support
 - Built-in LDO network for enhanced PSRR
 - BOM-Optimized and Power-Optimized modes
 - One or two power rails for 1.8V IO mode, two or three power rails for 3.3V IO mode
- Built-in calibration
 - Built-in Firmware (ROM)
 - Self-contained on-chip calibration system
- Host Interface
 - UART
 - CAN-FD
 - SPI
- RDIF (Radar Data Interface) for raw ADC sample capture
- Other interfaces available to user application
 - QSPI
 - I2C
 - JTAG
 - GPIOs
 - PWM Interface
- Internal memory
 - 1MB of On-chip RAM
 - Configurable L3 shared memory for Radar Cube
 - Data and Code RAM of (512/640/768KB)
- Easy hardware design
 - 0.5mm pitch, 101-BGA 10.9mm× 6.7mm AMY package for easy assembly and low-cost PCB design
 - Small size
- Clock source
 - 40.0MHz crystal for primary clock
 - Supports externally driven clock (Square/Sine) at 40.0MHz
 - 32kHz internal oscillator for low power operations
- Supports temperature operating range
 - Operating junction temperature range: –40°C to 105°C



2 Applications

- Automated door/gate
- Motion detector
- Occupancy detection / people tracking / people counting
- Video doorbell
- IP network camera
- Thermostat
- Air conditioner
- Refrigerators and freezers
- Vacuum robot
- Lawn mover
- PC/Notebooks
- Portable electronics
- Televisions
- Tablets
- Earphones
- Smart watches
- Gaming
- Home theater & entertainment

3 Description

The IWRL6432AOP mmWave Sensor device is an Antenna-on-Package (AOP) device that is an evolution within integrated single chip mmWave sensors that simplifies the board design. The device is based on FMCW radar technology. The device is capable of operation in the 57GHz to 63.5GHz band and is partitioned into mainly four power domains:

- **RF/Analog Sub-System:** This block includes all the RF and Analog components required to transmit and receive the RF signals.
- **Front-End Controller sub-System (FECSS):** FECSS contains processor ARM Cortex M3, responsible for radar front-end configuration, control, and calibration.
- **Application Sub-System (APPSS):** APPSS is where the device implements a user programmable ARM Cortex M4 allowing for custom control and interface applications. Top Sub-System (TOPSS) is part of the APPSS power domain and contains the clocking and power management sub-blocks.
- **Hardware Accelerator (HWA):** HWA block supplements the APPSS by offloading common radar processing such as FFT, Constant False Alarm rate (CFAR), scaling, and compression.

IWRL6432AOP is specifically designed to have separate control for each of the above-mentioned power domains to control states (power ON or OFF) based on use case requirements. The device also features the capability to exercise various low-power states like sleep and deep sleep, where low-power sleep mode is achieved by clock gating and by turning off some of the internal IP blocks of the device. The device also provides the option of keeping some contents of the device, like Application image or RF profile retained in such scenarios.

Additionally, the device is built with TI's low power 45nm RF CMOS process and enables unprecedented levels of integration in an extremely small form factor. IWRL6432AOP is designed for low power, self-monitored, ultra-accurate radar systems in the industrial (and personal electronics) space for applications such as building/factory automation, commercial/residential security, personal electronics, presence/motion detection, and gesture detection/recognition for human machine interfaces

Packaging Information

| PRE-PRODUCTION PART NUMBER (1) | PACKAGE ⁽³⁾ | BODY/ PACKAGE SIZE ⁽²⁾ | TRAY / TAPE AND REEL | DESCRIPTION |
|-----------------------------------|------------------------|---|-------------------------|------------------------------|
| XI6432BRQAAMY | AMY (FCCSP, 101) | 10.9mmx 6.7 mm | Tray | Pre-production; Generic Part |

| PRODUCTION PART NUMBER (1) | PACKAGE ⁽³⁾ | BODY/ PACKAGE SIZE ⁽²⁾ | TRAY / TAPE AND REEL | DESCRIPTION |
|----------------------------|------------------------|---|-------------------------|---|
| IWRL6432BRQGAMYR | AMY (FCCSP, 101) | 10.9mmx 6.7 mm | Tape & Reel | Production; Deep sleep enabled; Generic Part |
| IWRL6432BRQAAMYR | AMY (FCCSP, 101) | 10.9mmx 6.7 mm | Tape & Reel | Production; Deep sleep enabled; Authenticated Boot capable |
| IWRL6432BRQAAMY | AMY (FCCSP, 101) | 10.9mmx 6.7 mm | Tray | Production; Deep sleep enabled; Authenticated boot capable |

(1) For more information, see [Device Nomenclature](#)

- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) For more information, see [Mechanical, Packaging, and Orderable Information](#)

4 Functional Block Diagram

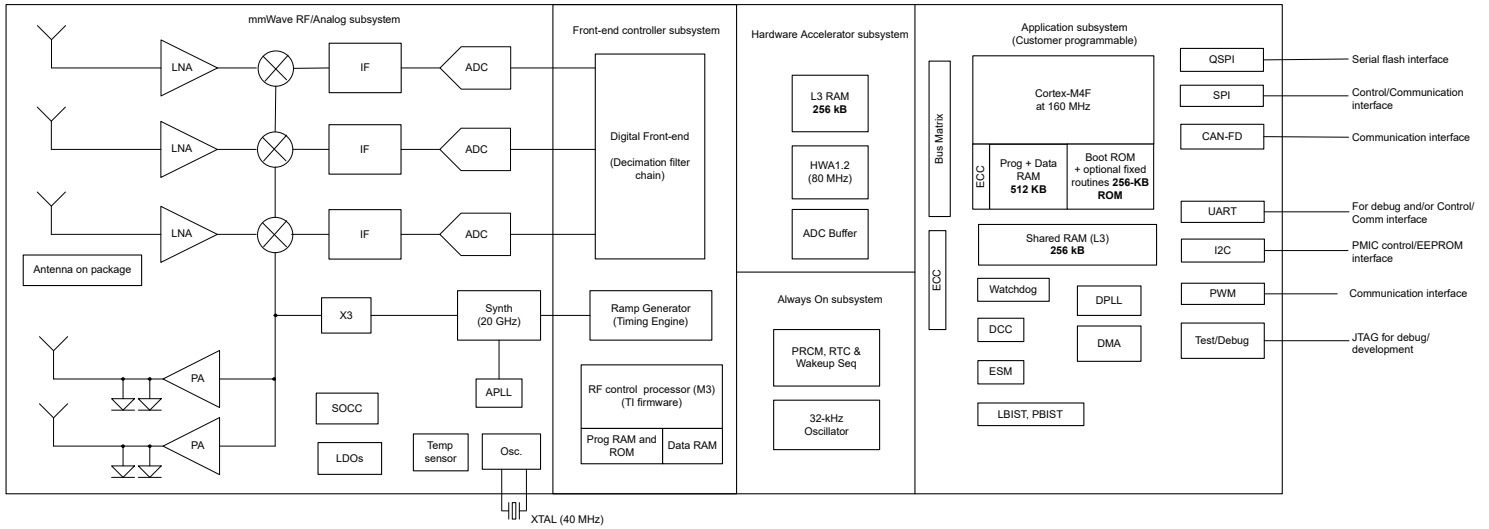


Figure 4-1. Functional Block Diagram

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5 Device Comparison

The following table compares the features of radar devices.

Table 5-1. Device Features Comparison

| FUNCTION | IWR6432AOP | IWR6432 | IWR6432 WCSP | IWR6843AOP ⁽¹⁾ | IWR6843 ⁽¹⁾ | IWR6443 | IWR1432 |
|---|---------------|-------------|--------------|---------------------------|------------------------|------------------|-------------------------------|
| Antenna on Package (AOP) | Yes | - | - | Yes | - | - | - |
| Number of receivers | 3 | 3 | 3 | 4 | 4 | 4 | 3 |
| Number of transmitters | 2 | 2 | 2 | 3 ⁽²⁾ | 3 ⁽²⁾ | 3 ⁽²⁾ | 2 |
| RF frequency range | 57 to 63.5GHz | 57 to 64GHz | 57 to 64GHz | 60 to 64GHz | 60 to 64GHz | 60 to 64GHz | 76 to 81GHz |
| On-chip memory | 1MB | 1MB | 1MB | 1.75MB | 1.75MB | 1.4MB | 1MB |
| Max I/F (Intermediate Frequency) (MHz) | 5 | 5 | 5 | 10 | 10 | 10 | 5 |
| Max real sampling rate (Msps) | 12.5 | 12.5 | 12.5 | 25 | 25 | 25 | 12.5 |
| Max complex sampling rate (Msps) | - | - | - | 12.5 | 12.5 | 12.5 | - |
| Safety and Security | | | | | | | |
| Functional Safety -Compliance | - | SIL-2 | - | SIL-2 | SIL-2 | - | SIL-2 Targeted ⁽³⁾ |
| Device Security ⁽⁴⁾ | - | - | - | Yes | Yes | Yes | - |
| Processors | | | | | | | |
| MCU | M4F | M4F | M4F | R4F | R4F | R4F | M4F |
| DSP | - | - | - | C674x | C674x | - | - |
| HWA | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Peripherals | | | | | | | |
| Serial Peripheral Interface (SPI) ports | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Quad Serial Peripheral Interface (QSPI) | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Inter-Integrated Circuit (I ² C) interface | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Controller Area Network (DCAN) interface | - | - | - | - | - | - | - |

Table 5-1. Device Features Comparison (continued)

| FUNCTION | IWRL6432AOP | IWRL6432 | IWRL6432 WCSP | IWR6843AOP ⁽¹⁾ | IWR6843 ⁽¹⁾ | IWR6443 | IWRL1432 |
|---|-------------------|-------------------|-------------------|---------------------------|------------------------|--------------------|-------------------|
| Controller Area Network (CAN-FD) interface | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Trace | - | - | - | Yes | Yes | - | - |
| PWM | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| DMM Interface | - | - | - | Yes | Yes | Yes | - |
| Hardware In Loop (HIL/ DMM) | - | - | - | Yes | Yes | Yes | - |
| GPADC | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ADC Raw Data Capture | RDIF | RDIF | RDIF | LVDS | LVDS | LVDS | RDIF |
| UART | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1V bypass mode | N/A | N/A | N/A | Yes | Yes | Yes | N/A |
| JTAG | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Number of TX that can be used simultaneously | 1 | 2 | 2 | 3 | 3 | 3 | 2 |
| Per Chirp configurable TX phase shifter | - | BPM only | BPM only | Yes ⁽⁵⁾ | Yes ⁽⁵⁾ | Yes ⁽⁵⁾ | BPM only |
| Package Variant | Under- Mount | FCCSP | WCSP | Under- Mount | FCCSP | FCCSP | FCCSP |
| Product Preview (PP), Advance Information (AI), or Production Data (PD) | PD ⁽⁶⁾ | PD ⁽⁶⁾ | PD ⁽⁶⁾ | PD ⁽⁶⁾ | PD ⁽⁶⁾ | PD ⁽⁶⁾ | PD ⁽⁶⁾ |

- (1) Developed for Functional Safety applications, the device supports hardware integrity up to SIL-2. Refer to the related documentation for more details. Non-Functional Safety Variants are also available for these devices.
- (2) 3 Tx Simultaneous operation on the applicable devices is supported only with 1V LDO bypass and PA LDO disable mode. In this mode, the 1V supply needs to be fed on the V_{OUT} PA pin.
- (3) As the certification may get secured at different times and post certificate the target would be updated to “compliant” from “compliance targeted” only in related datasheets, please refer to the respective datasheets for most recent compliance status.
- (4) Device security features including Secure Boot and Customer Programmable Keys are available in select devices for only select part variants as indicated by the Device Type identifier in Section 3, Device Information table.
- (5) 6 bits linear Phase Shifter.
- (6) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty.

5.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave sensors TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for Industrial applications.

mmWave IWR The Texas Instruments IWRxxxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 57- to 63.5GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from short to ultra short range can be realized using these devices.

Companion products for IWRL6432AOP Review products that are similar to this product.

Reference designs for IWRL6432AOP The IWRL6432AOP TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/reference-designs.

6 Terminal Configurations and Functions

6.1 Pin Diagrams

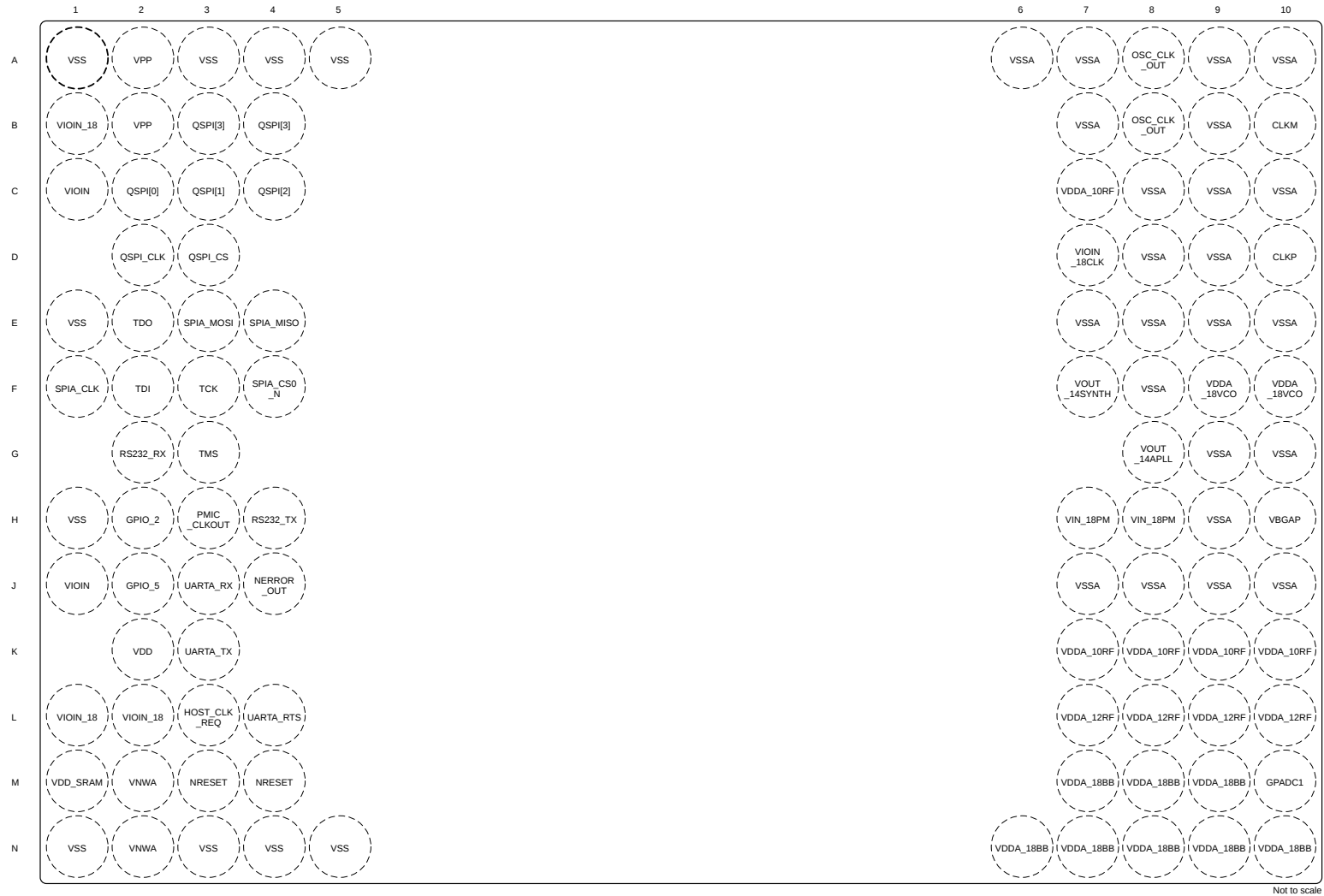


Figure 6-1. Pin Diagram (Top View)

Table 6-1. Pin Attributes (AMY0101A Package)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | BALL STATE DURING RST ⁽⁸⁾ | BALL RESET AFTER RST ⁽⁹⁾ | PULL UP/DOWN TYPE ⁽¹⁰⁾ |
|--------------------------------|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|--------------------------------------|-------------------------------------|-----------------------------------|
| B10 | CLKM | CLKM | | | | A | | | |
| D10 | CLKP | CLKP | | | | A | | | |
| M10 | GPADC1 | GPADC1 | | | | A | | | |
| H2 | GPIO_2 | GPIO_2 | PADAL_CFG_REGISTER | 0x5A00 002C | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | LIN_RX | | | 1 | I | | | |
| | | WARM_RESET_OUT | | | 2 | O | | | |
| | | I2C_SDA | | | 3 | IO | | | |
| | | SPIA_CS1_N | | | 4 | IO | | | |
| | | WU_REQIN | | | 5 | I | | | |
| | | RTC_CLK_IN | | | 6 | I | | | |
| | | MDO_D0 | | | 7 | O | | | |
| J2 | GPIO_5 | GPIO_5 | PADAV_CFG_REGISTER | 0x5A00 0054 | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | SYNC_IN | | | 1 | I | | | |
| | | LIN_RX | | | 2 | I | | | |
| | | EPWMB | | | 3 | O | | | |
| | | EPWM_SYNC_IN | | | 4 | I | | | |
| | | MDO_D3 | | | 5 | O | | | |
| L3 | HOST_CLK_REQ | HOST_CLK_REQ | PADAX_CFG_REGISTER | 0x5A00 005C | 0 | O | Off / Off / Off | Off / SS / Off | PU/PD |
| | | GPIO_7 | | | 1 | IO | | | |
| | | MCU_CLKOUT | | | 2 | O | | | |
| | | LIN_TX | | | 3 | O | | | |
| | | WU_REQIN | | | 4 | I | | | |
| | | SPIB_MISO | | | 5 | IO | | | |
| | | I2C_SCL | | | 6 | IO | | | |
| | | MDO_D3 | | | 8 | O | | | |
| | | MDO_FRM_CLK | | | 9 | O | | | |
| | | J4 | | | NERROR_OUT | NERROR_OUT | | | |
| GPIO_4 | 1 | | IO | | | | | | |
| SYNC_IN | 2 | | I | | | | | | |
| SPIB_CS0_N | 3 | | IO | | | | | | |
| WU_REQIN | 4 | | I | | | | | | |
| RTC_CLK_IN | 5 | | I | | | | | | |
| MCU_CLKOUT | 6 | | O | | | | | | |
| MDO_D3 | 7 | | O | | | | | | |
| M3, M4 | NRESET | NRESET | | | | A | | | |
| A8, B8 | OSC_CLK_OUT | OSC_CLK_OUT | | | | A | | | |

Table 6-1. Pin Attributes (AMY0101A Package) (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | BALL STATE DURING RST ⁽⁸⁾ | BALL RESET AFTER RST ⁽⁹⁾ | PULL UP/DOWN TYPE ⁽¹⁰⁾ |
|--------------------------------|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|--------------------------------------|-------------------------------------|-----------------------------------|
| H3 | PMIC_CLKOUT | SOP[1] | PADAK_CFG_REG | 0x5A00 0028 | During Power-up | I | Off / Off / Off | Off / Off / Off | PU/PD |
| | | PMIC_CLKOUT | | | 0 | O | | | |
| | | LIN_TX | | | 1 | O | | | |
| | | SPIA_CS1_N | | | 2 | IO | | | |
| | | MDO_FRM_CLK | | | 3 | O | | | |
| C2 | QSPI[0] | QSPI[0] | PADAC_CFG_REG | 0x5A00 0008 | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | SPIB_MOSI | | | 1 | IO | | | |
| | | MDO_D0 | | | 2 | O | | | |
| C3 | QSPI[1] | QSPI[1] | PADAD_CFG_REG | 0x5A00 000C | 0 | I | Off / Off / Off | Off / Off / Off | PU/PD |
| | | SPIB_MISO | | | 1 | IO | | | |
| | | RTC_CLK_IN | | | 2 | I | | | |
| | | MDO_D3 | | | 3 | O | | | |
| C4 | QSPI[2] | QSPI[2] | PADAE_CFG_REG | 0x5A00 0010 | 0 | I | Off / Off / Off | Off / Off / Off | PU/PD |
| | | I2C_SCL | | | 1 | IO | | | |
| | | WU_REQIN | | | 2 | I | | | |
| | | MDO_D1 | | | 3 | O | | | |
| B3, B4 | QSPI[3] | QSPI[3] | PADAF_CFG_REG | 0x5A00 0014 | 0 | I | Off / Off / Off | Off / Off / Off | PU/PD |
| | | I2C_SDA | | | 1 | IO | | | |
| | | SYNC_IN | | | 2 | I | | | |
| | | MDO_D2 | | | 3 | O | | | |
| D2 | QSPI_CLK | QSPI_CLK | PADAA_CFG_REG | 0x5A00 0000 | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | SPIB_CLK | | | 1 | IO | | | |
| | | MDO_CLK | | | 2 | O | | | |
| D3 | QSPI_CS | QSPI_CS | PADAB_CFG_REG | 0x5A00 0004 | 0 | O | Off / Off / Off | Off / Off / Off | PU/PD |
| | | SPIB_CS0_N | | | 1 | IO | | | |
| | | MDO_FRM_CLK | | | 2 | O | | | |
| G2 | RS232_RX | RS232_RX | PADAP_CFG_REG | 0x5A00 003C | 0 | I | Off / Off / Up | On / Off / Up | PU/PD |
| | | I2C_SDA | | | 1 | IO | | | |
| | | UARTB_RX | | | 2 | I | | | |
| | | LIN_RX | | | 3 | I | | | |
| | | MDO_D2 | | | 4 | O | | | |
| | | SPIB_MISO | | | 5 | IO | | | |

Table 6-1. Pin Attributes (AMY0101A Package) (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | BALL STATE DURING RST ⁽⁸⁾ | BALL RESET AFTER RST ⁽⁹⁾ | PULL UP/DOWN TYPE ⁽¹⁰⁾ |
|--------------------------------|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|--------------------------------------|-------------------------------------|-----------------------------------|
| H4 | RS232_TX | RS232_TX | PADA0_CFG_REG | 0x5A00 0038 | 0 | O | Off / Off / Off | Off / SS / Off | PU/PD |
| | | I2C_SCL | | | 1 | IO | | | |
| | | UARTB_TX | | | 2 | O | | | |
| | | LIN_TX | | | 3 | O | | | |
| | | EPWM_SYNC_IN | | | 4 | I | | | |
| | | MDO_D1 | | | 5 | O | | | |
| | | SPIB_CS1_N | | | 6 | IO | | | |
| F1 | SPIA_CLK | SPIA_CLK | PADAG_CFG_REG | 0x5A00 0018 | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | EPWMB | | | 1 | O | | | |
| | | I2C_SCL | | | 2 | IO | | | |
| | | SPIB_CLK | | | 3 | IO | | | |
| | | MDO_CLK | | | 4 | O | | | |
| F4 | SPIA_CS0_N | SPIA_CS0_N | PADAH_CFG_REG | 0x5A00 001C | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | EPWMA | | | 1 | O | | | |
| | | I2C_SDA | | | 2 | IO | | | |
| | | SPIB_CS0_N | | | 3 | IO | | | |
| | | MDO_D3 | | | 4 | O | | | |
| E4 | SPIA_MISO | SPIA_MISO | PADAJ_CFG_REG | 0x5A00 0024 | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | GPIO_1 | | | 1 | IO | | | |
| | | EPWMA | | | 2 | O | | | |
| | | SPIB_MISO | | | 3 | IO | | | |
| | | MDO_D2 | | | 4 | O | | | |
| E3 | SPIA_MOSI | SPIA_MOSI | PADAI_CFG_REG | 0x5A00 0020 | 0 | IO | Off / Off / Off | Off / Off / Off | PU/PD |
| | | GPIO_0 | | | 1 | IO | | | |
| | | EPWMB | | | 2 | O | | | |
| | | SPIB_MOSI | | | 3 | IO | | | |
| | | MDO_D1 | | | 4 | O | | | |
| F3 | TCK | TCK | PADAT_CFG_REG | 0x5A00 004C | 0 | I | Off / Off / Down | On / Off / Down | PU/PD |
| | | EPWMB | | | 1 | O | | | |
| | | SPIB_CS1_N | | | 2 | IO | | | |
| | | SPIB_MOSI | | | 3 | IO | | | |
| | | MDO_D0 | | | 4 | O | | | |
| F2 | TDI | TDI | PADAR_CFG_REG | 0x5A00 0044 | 0 | I | Off / Off / Down | On / Off / Down | PU/PD |
| | | EPWMA | | | 1 | O | | | |
| | | SPIB_CS0_N | | | 2 | IO | | | |

Table 6-1. Pin Attributes (AMY0101A Package) (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | BALL STATE DURING RST ⁽⁸⁾ | BALL RESET AFTER RST ⁽⁹⁾ | PULL UP/DOWN TYPE ⁽¹⁰⁾ |
|--------------------------------|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|--------------------------------------|-------------------------------------|-----------------------------------|
| E2 | TDO | SOP[0] | PADAS_CFG_REG | 0x5A00 0048 | During Power-up | I | Off / Off / Off | Off / SS / Off | PU/PD |
| | | TDO | | | 0 | O | | | |
| | | MDO_FRM_CLK | | | 1 | O | | | |
| G3 | TMS | TMS | PADAQ_CFG_REG | 0x5A00 0040 | 0 | I | Off / Off / Up | On / Off / Up | PU/PD |
| | | WARM_RESET_OUT | | | 1 | O | | | |
| | | SPIA_CS1_N | | | 2 | IO | | | |
| | | SYNC_IN | | | 3 | I | | | |
| | | SPIB_MISO | | | 4 | IO | | | |
| | | SPIB_CLK | | | 5 | IO | | | |
| | | RTC_CLK_IN | | | 6 | I | | | |
| | | EPWM_SYNC_IN | | | 7 | I | | | |
| | | EPWM_SYNC_OUT | | | 8 | O | | | |
| L4 | UARTA_RTS | UARTA_RTS | PADAW_CFG_REG | 0x5A00 0058 | 0 | O | Off / Off / Off | Off / Off / Off | PU/PD |
| | | GPIO_6 | | | 1 | IO | | | |
| | | LIN_TX | | | 2 | O | | | |
| | | SPIB_CLK | | | 3 | IO | | | |
| | | WU_REQIN | | | 4 | I | | | |
| | | EPWMA | | | 5 | O | | | |
| | | RTC_CLK_IN | | | 6 | I | | | |
| | | MDO_CLK | | | 7 | O | | | |
| J3 | UARTA_RX | UARTA_RX | PADAM_CFG_REG | 0x5A00 0030 | 0 | I | Off / Off / Off | Off / Off / Off | PU/PD |
| | | GPIO_3 | | | 1 | IO | | | |
| | | LIN_RX | | | 2 | I | | | |
| | | CAN_FD_RX | | | 3 | I | | | |
| | | SYNC_IN | | | 4 | I | | | |
| | | UARTB_RX | | | 5 | I | | | |
| | | I2C_SDA | | | 6 | IO | | | |
| | | MDO_D1 | | | 7 | O | | | |
| K3 | UARTA_TX | UARTA_TX | PADAN_CFG_REG | 0x5A00 0034 | 0 | O | Off / Off / Off | Off / Off / Off | PU/PD |
| | | LIN_TX | | | 1 | O | | | |
| | | CAN_FD_TX | | | 2 | O | | | |
| | | SPIB_MOSI | | | 3 | IO | | | |
| | | WU_REQIN | | | 4 | I | | | |
| | | UARTB_TX | | | 5 | O | | | |
| | | I2C_SCL | | | 6 | IO | | | |
| | | MDO_D2 | | | 7 | O | | | |
| H10 | VBGAP | VBGAP | | | | A | | | |

Table 6-1. Pin Attributes (AMY0101A Package) (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | BALL STATE DURING RST ⁽⁸⁾ | BALL RESET AFTER RST ⁽⁹⁾ | PULL UP/DOWN TYPE ⁽¹⁰⁾ |
|---|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|--------------------------------------|-------------------------------------|-----------------------------------|
| K2 | VDD | VDD | | | | PWR | | | |
| C7, K10, K7, K8, K9 | VDDA_10RF | VDDA_10RF | | | | PWR | | | |
| L10, L7, L8, L9 | VDDA_12RF | VDDA_12RF | | | | PWR | | | |
| M7, M8, M9, N10, N6, N7, N8, N9 | VDDA_18BB | VDDA_18BB | | | | PWR | | | |
| F10, F9 | VDDA_18VCO | VDDA_18VCO | | | | PWR | | | |
| M1 | VDD_SRAM | VDD_SRAM | | | | PWR | | | |
| H7, H8 | VIN_18PM | VIN_18PM | | | | PWR | | | |
| C1, J1 | VIOIN | VIOIN | | | | PWR | | | |
| B1, L1, L2 | VIOIN_18 | VIOIN_18 | | | | PWR | | | |
| D7 | VIOIN_18CLK | VIOIN_18CLK | | | | PWR | | | |
| M2, N2 | VNWA | VNWA | | | | PWR | | | |
| G8 | VOUT_14APLL | VOUT_14APLL | | | | PWR | | | |
| F7 | VOUT_14SYNTH | VOUT_14SYNTH | | | | PWR | | | |
| A2, B2 | VPP | VPP | | | | PWR | | | |
| A1, A3, A4, A5, E1, H1, N1, N3, N4, N5 | VSS | VSS | | | | GND | | | |
| A10, A6, A7, A9, B7, B9, C10, C8, C9, D8, D9, E10, E7, E8, E9, F8, G10, G9, H9, J10, J7, J8, J9 | VSSA | VSSA | | | | GND | | | |

(1) **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.

(2) **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).

(3) **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

(4) **PINCNTL_REGISTER:** APPSS Register name for PinMux Control

(5) **PINCNTL_ADDRESS:** APPSS Address for PinMux Control

(6) **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.

(7) **TYPE:** Signal type and direction:

- I = Input
- O = Output
- IO = Input or Output

(8) **BALL STATE DURING RST:** State of Ball during reset in the format of RX/TX/Pull Status

- RX (Input buffer)
 - Off: The input buffer is **disabled**.
 - On: The input buffer is **enabled**.
- TX (Output buffer)
 - Off: The output buffer is **disabled**.
 - Low: The output buffer is **enabled** and drives V_{OL} .

- Pull Status (Internal pull resistors)
 - Off: Internal pull resistors are turned **off**.
 - Up: Internal **pull-up** resistor is turned on.
 - Down: Internal **pull-down** resistor is turned on.
 - NA: No internal pull resistor.
 - An empty box, or "-" means Not Applicable.
- (9) **BALL STATE AFTER RST:** State of Ball after reset in the format of RX/TX/Pull Status
- RX (Input buffer)
 - Off: The input buffer is **disabled**.
 - On: The input buffer is **enabled**.
 - TX (Output buffer)
 - Off: The output buffer is **disabled**.
 - SS: The subsystem selected with MUXMODE determines the output buffer state.
 - Pull status (Internal pull resistors)
 - Off: Internal pull resistors are turned **off**.
 - Up: Internal **pull-up resistor** is turned on.
 - Down: Internal **pull-down resistor** is turned on.
 - NA: No internal pull resistor.
 - An empty box, NA, or "-" means Not Applicable.
- (10) **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
- Pull Up: Internal pullup
 - Pull Down: Internal pulldown
 - An empty box means No pull.
- (11) Pin Mux Control Value maps to lower 4 bits of register.

6.2 Signal Descriptions

Note

All digital IO pins of the device (except NRESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

Table 6-2. Analog Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|-------------------------|----------|---------|
| CLKM | XTAL CLKM pin | A | B10 |
| CLKP | XTAL CLKP pin | A | D10 |
| GPADC1 | GPADC input 1 | A | M10 |
| NRESET | NRESET input | A | M3, M4 |
| OSC_CLK_OUT | Oscillator Clock output | A | A8, B8 |
| VBGAP | BandGap reference pin | A | H10 |

Table 6-3. CAN Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|-------------------|----------|---------|
| CAN_FD_RX | CAN Receive Data | I | J3 |
| CAN_FD_TX | CAN Transmit Data | O | K3 |

Table 6-4. Clock Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|---|----------|--------------------|
| MCU_CLKOUT | MCU clock output | O | J4, L3 |
| PMIC_CLKOUT | PMIC clock output This also serves as a Sense On Power Line. Impacts boot mode SOP1. | O | H3 |
| RTC_CLK_IN | RTC clock input This is used as wakeup source for exiting from deep sleep. For more details, refer to the Technical Reference Manual | I | C3, G3, H2, J4, L4 |

Table 6-5. EPWM Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|---------------|------------------|----------|----------------|
| EPWMA | EPWM Output A | O | E4, F2, F4, L4 |
| EPWMB | EPWM Output B | O | E3, F1, F3, J2 |
| EPWM_SYNC_IN | EPWM Sync Input | I | G3, H4, J2 |
| EPWM_SYNC_OUT | EPWM Sync output | O | G3 |

Table 6-6. GPIO Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|------------------------------|----------|---------|
| GPIO_0 | General Purpose Input/Output | IO | E3 |
| GPIO_1 | General Purpose Input/Output | IO | E4 |
| GPIO_2 | General Purpose Input/Output | IO | H2 |
| GPIO_3 | General Purpose Input/Output | IO | J3 |
| GPIO_4 | General Purpose Input/Output | IO | J4 |
| GPIO_5 | General Purpose Input/Output | IO | J2 |
| GPIO_6 | General Purpose Input/Output | IO | L4 |
| GPIO_7 | General Purpose Input/Output | IO | L3 |

Table 6-7. I2C Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|-------------|----------|--------------------|
| I2C_SCL | I2C Clock | IO | C4, F1, H4, K3, L3 |
| I2C_SDA | I2C Data | IO | B4, F4, G2, H2, J3 |

Table 6-8. JTAG Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|-----------------------------|----------|---------|
| TCK | JTAG Test Clock Input | I | F3 |
| TDI | JTAG Test Data Input | I | F2 |
| TDO | JTAG Test Data Output | O | E2 |
| TMS | JTAG Test Mode Select Input | I | G3 |

Table 6-9. MDO Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|-----------------|----------|--------------------|
| MDO_CLK | MDO Clock | O | D2, F1, L4 |
| MDO_D0 | MDO data 0 | O | C2, F3, H2 |
| MDO_D1 | MDO data 1 | O | C4, E3, H4, J3 |
| MDO_D2 | MDO data 2 | O | B4, E4, G2, K3 |
| MDO_D3 | MDO data 3 | O | C3, F4, J2, J4, L3 |
| MDO_FRM_CLK | MDO Frame Clock | O | D3, E2, H3, L3 |

Table 6-10. Power Supply Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|--------------|--|----------|---|
| VDD | 1.2V Core supply | PWR | K2 |
| VDDA_10RF | 1.0V RF Supply | PWR | C7, K10, K7, K8, K9 |
| VDDA_12RF | 1.2V RF Supply | PWR | L10, L7, L8, L9 |
| VDDA_18BB | 1.8V analog supply | PWR | M7, M8, M9, N10, N6, N7, N8, N9 |
| VDDA_18VCO | 1.8V analog supply | PWR | F10, F9 |
| VDD_SRAM | 1.2V SRAM supply | PWR | M1 |
| VIN_18PM | 1.8V core supply | PWR | H7, H8 |
| VIOIN | 1.8V analog supply | PWR | C1, J1 |
| VIOIN_18 | 1.8V analog supply | PWR | B1, L1, L2 |
| VIOIN_18CLK | 1.8V analog supply | PWR | D7 |
| VNWA | 1.2V VNWA supply. Always connected to SRAM supply. | PWR | M2, N2 |
| VOUT_14APLL | 1.4V analog supply | PWR | G8 |
| VOUT_14SYNTH | 1.4V analog supply | PWR | F7 |
| VPP | 1.7V VPP supply. Voltage supply for fuse chain. | PWR | A2, B2 |
| VSS | Ground | GND | A1, A3, A4, A5, E1, H1, N1, N3, N4, N5 |
| VSSA | Ground | GND | A10, A6, A7, A9, B7, B9, C10, C8, C9, D8, D9, E10, E7, E8, E9, F8, G10, G9, H9, J10, J7, J8, J9 |

Table 6-11. QSPI Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|-----------------|----------|---------|
| QSPI_D0 | QSPI Data bit 0 | IO | C2 |

Table 6-11. QSPI Signal Descriptions (continued)

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|------------------|----------|---------|
| QSPI_D1 | QSPI Data bit 1 | I | C3 |
| QSPI_D2 | QSPI Data bit 2 | I | C4 |
| QSPI_D3 | QSPI Data bit 3 | I | B3, B4 |
| QSPI_SCLK | QSPI clock | IO | D2 |
| QSPI_CS | QSPI Chip select | O | D3 |

Table 6-12. RS232 Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|---------------------|----------|---------|
| RS232_RX | RS232 Receive Data | I | G2 |
| RS232_TX | RS232 Transmit Data | O | H4 |

Table 6-13. SPIA Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|--------------------|----------|------------|
| SPIA_CLK | SPIA Clock | IO | F1 |
| SPIA_CS0_N | SPIA Chip Select 0 | IO | F4 |
| SPIA_CS1_N | SPIA Chip Select 1 | IO | G3, H2, H3 |
| SPIA_MISO | SPIA MISO | IO | E4 |
| SPIA_MOSI | SPIA MOSI | IO | E3 |

Table 6-14. SPIB Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|--------------------|----------|--------------------|
| SPIB_CLK | SPIB Clock | IO | D2, F1, G3, L4 |
| SPIB_CS0_N | SPIB Chip Select 0 | IO | D3, F2, F4, J4 |
| SPIB_CS1_N | SPIB Chip Select 1 | IO | F3, H4 |
| SPIB_MISO | SPIB MISO | IO | C3, E4, G2, G3, L3 |
| SPIB_MOSI | SPIB MOSI | IO | C2, E3, F3, K3 |

Table 6-15. System Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|----------------|---------------------------|----------|------------------------|
| HOST_CLK_REQ | Host clock request output | O | L3 |
| NERROR_OUT | NERROR output signal | O | J4 |
| SYNC_IN | Sync input | I | B4, G3, J2, J3, J4 |
| WARM_RESET_OUT | Warm reset output | O | G3, H2 |
| WU_REQIN | Wakeup Request input | I | C4, H2, J4, K3, L3, L4 |

Table 6-16. UARTA Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|---------------------|----------|---------|
| UARTA_RTS | UARTA RTS output | O | L4 |
| UARTA_RX | UARTA Receive Data | I | J3 |
| UARTA_TX | UARTA Transmit Data | O | K3 |

Table 6-17. UARTB Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|--------------------|----------|---------|
| UARTB_RX | UARTB Receive Data | I | G2, J3 |

Table 6-17. UARTB Signal Descriptions (continued)

| SIGNAL NAME | DESCRIPTION | PIN TYPE | AMY PIN |
|-------------|---------------------|----------|---------|
| UARTB_TX | UARTB Transmit Data | O | H4, K3 |

7 Specifications

7.1 Absolute Maximum Ratings

| PARAMETERS ^{(1) (2)} | | MIN | MAX | UNIT |
|--------------------------------|---|--|-------------|------|
| VDD | 1.2Vdigital power supply | -0.5 | 1.4 | V |
| VIOIN | I/O supply (3.3V or 1.8 V): All CMOS I/Os operate on the same VIOIN voltage level | -0.5 | 3.8 | V |
| VIOIN_18 | 1.8Vsupply for CMOS IO | -0.5 | 2 | V |
| VIN_18CLK | 1.8Vsupply for clock module | -0.5 | 2 | V |
| VIN_18BB | 1.8V Analog baseband power supply | -0.5 | 2 | V |
| VIN_18VCO supply | 1.8V RF VCO supply | -0.5 | 2 | V |
| VPP | Voltage supply for fuse chain | -0.5 | 2 | V |
| Input and output voltage range | Dual-voltage LVCMOS inputs, 3.3V or 1.8V(Steady State) | -0.3V | VIOIN + 0.3 | V |
| | Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8V(Transient Overshoot/Undershoot) or external oscillator input | VIOIN + 20% up to 20% of signal period | | |
| CLKP, CLKM | Input ports for reference crystal | -0.5 | 2 | V |
| Clamp current | Input or Output Voltages 0.3V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O. | -20 | 20 | mA |
| T _J | Operating junction temperature range | -40 | 105 | °C |
| T _{STG} | Storage temperature range after soldered onto PC board | -55 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS}, unless otherwise noted.

7.2 ESD Ratings

| | | | VALUE | UNIT | |
|--------------------|-------------------------|---|-------------|-------|---|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | All Pins | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All Pins | ±500 | |
| | | | Corner Pins | ±750 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Power-On Hours (POH)

| JUNCTION TEMPERATURE (T _J) ⁽¹⁾ | OPERATING CONDITION | NOMINAL CVDD VOLTAGE (V) | POWER-ON HOURS [POH] (HOURS) |
|---|---------------------|--------------------------|------------------------------|
| 105°C T _J | 50% RF duty cycle | 1.2 | 100,000 |

7.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|--------------------|--|-------------|-----|-----------|--------|
| VDD | 1.2Vdigital power supply | 1.14 | 1.2 | 1.26 | V |
| VIOIN | I/O supply (3.3V or 1.8V): All CMOS I/Os operate on the VIOIN supply voltage level. | 3.135 | 3.3 | 3.465 | V |
| | | 1.71 | 1.8 | 1.89 | |
| VIOIN_18 | 1.8Vsupply for CMOS IO | 1.71 | 1.8 | 1.89 | V |
| VIN_18CLK | 1.8Vsupply for clock module | 1.71 | 1.8 | 1.89 | V |
| VIN18BB | 1.8V Analog baseband power supply | 1.71 | 1.8 | 1.89 | V |
| VIN_18VCO | 1.8V RF VCO supply | 1.71 | 1.8 | 1.89 | V |
| V _{IH} | Voltage Input High (1.8Vmode) | 1.17 | | | V |
| | Voltage Input High (3.3Vmode) | 2.25 | | | |
| V _{IL} | Voltage Input Low (1.8Vmode) | | | 0.3*VIOIN | V |
| | Voltage Input Low (3.3Vmode) | | | 0.62 | |
| V _{OH} | High-level output threshold (I _{OH} = 6mA) | VIOIN – 450 | | | mV |
| V _{OL} | Low-level output threshold (I _{OL} = 6mA) | | | | 450 mV |
| NRESET SOP[1:0] | V _{IL} (1.8V Mode) | | | 0.2 | V |
| | V _{IH} (1.8V Mode) | 0.96 | | | |
| | V _{IL} (3.3V Mode) | | | 0.3 | |
| | V _{IH} (3.3V Mode) | 1.57 | | | |

7.5 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for authenticated boot devices. During the process of writing the customer specific keys or other fields like software version etc. in the efuse, the user needs to provide the VPP supply.

7.5.1 Recommended Operating Conditions for OTP eFuse Programming

| PARAMETER | DESCRIPTION | MIN | NOM | MAX | UNIT |
|-------------------------------------|--|------|-------------------|------|-------|
| VPP | Supply voltage range for the eFuse ROM domain during normal operation | | NC ⁽²⁾ | | |
| | Supply voltage range for the eFuse ROM domain during OTP programming ⁽¹⁾ | 1.65 | 1.7 | 1.75 | V |
| Duration of VPP Supply | If VPP voltage is supplied for more than recommended Hours, it can cause reliability issue | | | 24 | Hours |
| I(VPP) | | | | 50 | mA |
| Decoupling Capacitor ⁽³⁾ | | | 0.1 | 0.5 | uF |

- (1) During normal operation, no voltage should be applied to VPP. This can be typically achieved by disabling the external regulator attached to the VPP terminal.
- (2) NC: No Connect
- (3) The decoupling capacitor specification is applicable for the BOM optimized topology.

Note

Power up sequence: VPP must be ramped up at the end i.e after all other rails ramp up is done

7.5.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.

7.5.3 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, in these cases of faulty EFUSE programmability, TI WILL HAVE NO LIABILITY.

7.6 Power Supply Specifications

7.6.1 Power Optimized 3.3V I/O Topology

Table 7-1 describes the power rails from an external power supply block to the device via a 3.3V I/O topology.

Table 7-1. Power Supply Rails Characteristics: Power Optimized 3.3V I/O Topology

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOs IN THE DEVICE |
|--------|---|--|
| 3.3V | Digital I/Os | Input: VIOIN |
| 1.8V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC | Input: VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIN_18PM LDO Output: VOUT_14SYNTH, VOUT_14APLL |
| 1.2V | Core Digital and SRAMs, RF, VNWA | Input: VDD, VDD_SRAM, VNWA, VDDA_12RF LDO Output: VDDA_10RF |

7.6.2 Power Optimized 1.8V I/O Topology

Table 7-2 describes the power rails from an external power supply block to the device via a power optimized 1.8V I/O topology.

Table 7-2. Power Supply Rails Characteristics: Power Optimized 1.8V I/O Topology

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOs IN THE DEVICE |
|--------|---|---|
| 1.8V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC | Input: VIOIN, VIN_18PM, VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18 LDO Output: VOUT_14SYNTH, VOUT_14APLL |
| 1.2V | Core Digital and SRAMs, RF, VNWA | Input: VDD, VDD_SRAM, VNWA, VDDA_12RF LDO Output: VDDA_10RF |

7.6.3 BOM Optimized 3.3V I/O Topology

Table 7-3 describes the power rails from an external power supply block to the device via a BOM Optimized 3.3V I/O Topology.

Table 7-3. Power Supply Rails Characteristics: BOM Optimized 3.3V I/O Topology

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOs IN THE DEVICE |
|--------|---|--|
| 3.3V | Digital I/Os | Input: VIOIN |
| 1.8V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC | Input: VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIN_18PM LDO Output: VOUT_14SYNTH, VDDA_10RF, VDD_SRAM, VNWA, VOUT_14APLL, VDDA_12RF, VDD, |

7.6.4 BOM Optimized 1.8V I/O Topology

Table 7-4 describes the power rails from an external power supply block to the device via a BOM optimized 1.8V I/O topology.

Table 7-4. Power Supply Rails Characteristics: BOM Optimized 1.8V I/O Topology

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOs IN THE DEVICE |
|--------|---|--|
| 1.8V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, Digital I/Os | Input: VIOIN, VDDA_18VCO, VIOIN_18CLK, VIOIN_18, VDDA_18BB, VIN_18PM, VDDA_18VCO LDO Output: VDD, VDD_SRAM, VNWA, VDDA_10RF, VDDA_12RF, VOUT_14APLL, VOUT_14SYNTH |

7.6.5 System Topologies

The following the system topologies are supported.

- Topology 1: Autonomous mode, with ability to wake-up external MCU
- Topology 2: Peripheral mode, under control of external MCU

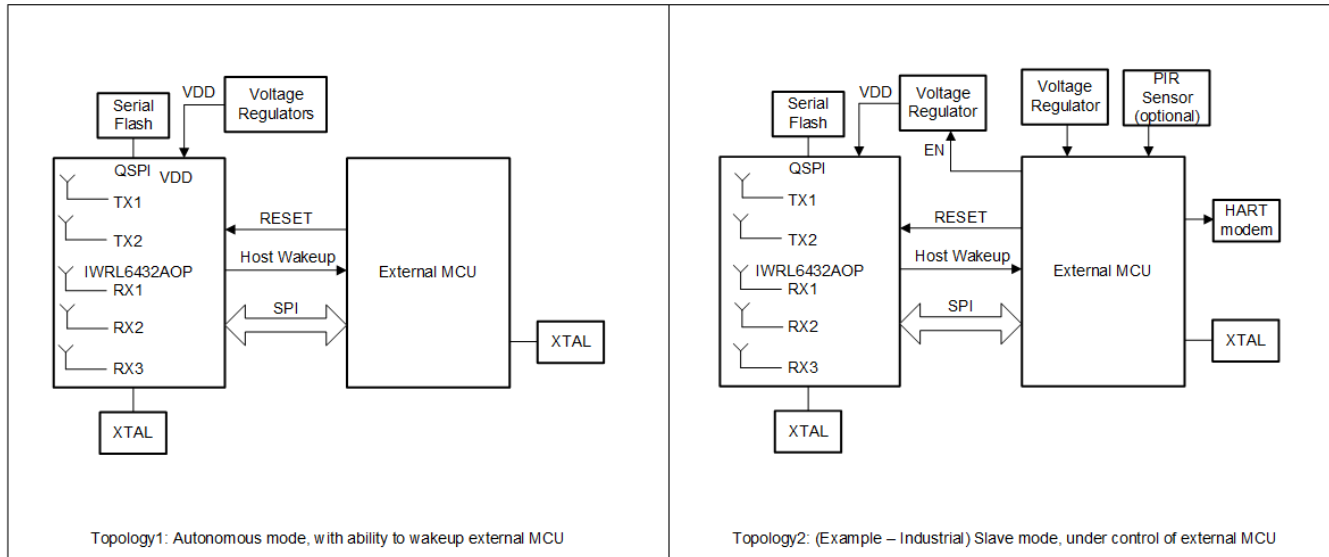


Figure 7-1. System Topologies

In Topology 1: Autonomous mode, the IWRL6432AOP can be used as full sensor along with M4F application processor. In this case the internal application processor does all the processing and interrupts the host processor to communicate to take action based on the sensor data. Most of the processing happens on the *internal* MCU of the IWRL6432AOP chip and only high level desired results are communicated to external host via LIN/CAN.

In Topology 2: Peripheral mode, the IWRL6432AOP is controlled by external MCU and most of the processing is done on *external* MCU. In this case computational and power requirements are higher and the external MCU stays active most of the time.

7.6.5.1 Power Topologies

The device supports two unique power topologies for BOM optimized and Power Optimized modes. The tables above, from [Section 7.6.1](#) to [Section 7.6.4](#), summarize these options. Two power topologies come into account based on whether the 1.2V rail is generated internally or is provided externally.

In BOM optimized mode the device can be powered up using one rail (1.8V) or two rails (3.3V and a 1.8V) provided externally. The 1.2V rail is internally generated in BOM optimized topology.

In power optimized mode, the device can either be powered using two rails (1.8V and 1.2V) or with three rails (3.3V, 1.8V and 1.2V), all provided externally. The 1.2V rail is NOT internally generated in the Power optimized topology. The device senses the external 1.2V supply and decides which topology the device will operate on.

7.6.5.1.1 BOM Optimized Mode

In this mode, the device can be powered using a 1.8V regulator OR using a 3.3V and a 1.8V regulator mode. The choice of one rail vs two rails is dependent on the IO voltages needed.

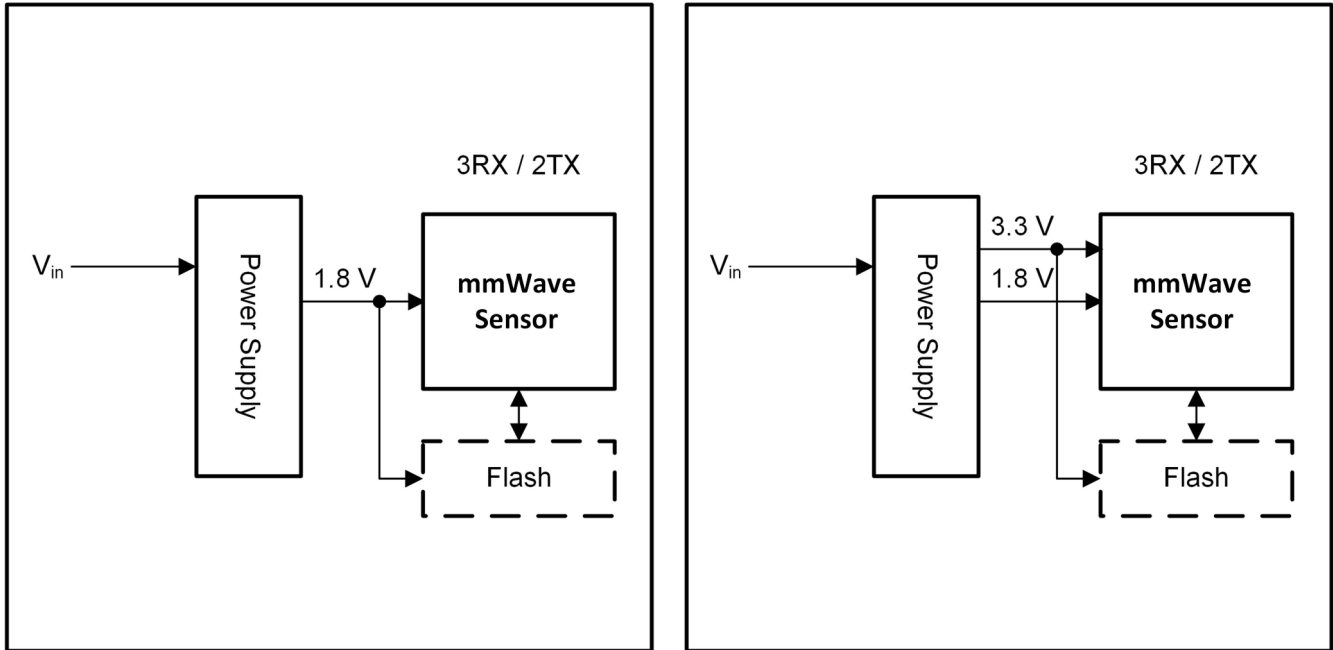


Figure 7-2. BOM Optimized Mode Power Management (Left: 1.8V I/O Topology, Right: 3.3V I/O Topology)

7.6.5.1.2 Power Optimized Mode

This mode is designed for applications needing ultra-low power applications. The device can either be powered using two rails (1.8V and 1.2V) or with three rails (3.3V, 1.8V and 1.2V).

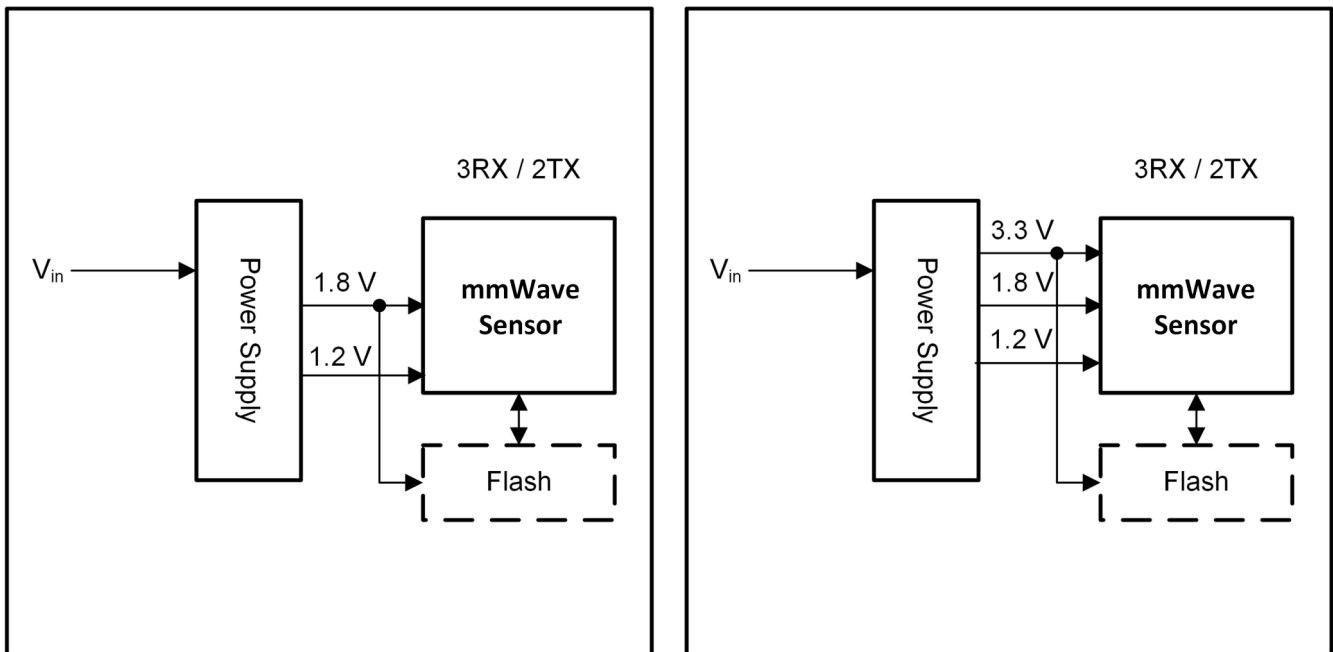


Figure 7-3. Power Optimized Mode Power Management (Left: 1.8V I/O Topology, Right: 3.3V I/O Topology)

7.6.6 Internal LDO output decoupling capacitor and layout conditions for BOM optimized topology

This section depicts the recommended values of de-coupling capacitors and range of allowable parasitic inductance and resistance in particular sections of the output path for the internal LDOs. Like all low dropout regulators, the internal LDO requires an output capacitor connected between OUTPUT and GND to stabilize the internal control loop. We recommended using X7R type capacitors which have a low variation across temperature. The minimum and maximum values of the capacitor captured in the table below. The table includes variation of a given capacitor due to DC bias, tolerance and temperature variation.

Note

1. If the parasitic values are not kept within the specified range, performance of the device can degrade.
2. Typical values of de-coupling capacitors are recommended to use. Any capacitance value taken near the edge of the range can degrade the performance. The working range of the chosen capacitor can not exceed the specified range.

7.6.6.1 Single-Capacitor Rail

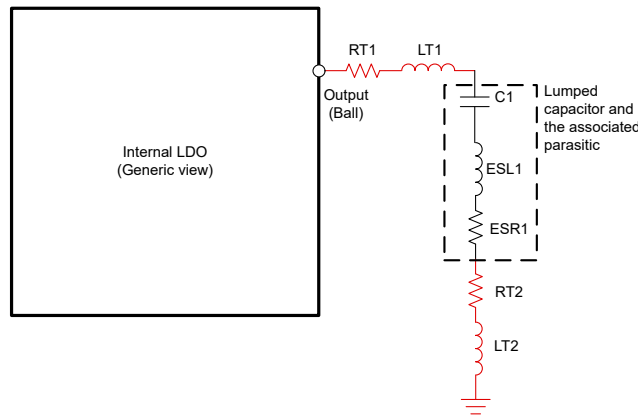


Figure 7-4. Parasitic offered by different portion of the output path (for one capacitor)

The 1.2V Digital LDO requires one decoupling capacitor with a typical value of 4.7uF. The parasitics offered by different portions of the output path is illustrated in Figure 7-4. “RT1” and “RT2” are the parasitic resistances offered by the ball to capacitor lead trace and the ground trace respectively. Similarly, “LT1” and “LT2” are parasitic inductances offered by the ball to capacitor lead trace and the ground trace respectively. “ESL1” and “ESR1” are the effective series inductance and resistance of the decoupling capacitor. Table 7-5 gives the minimum, maximum and typical values of the capacitance and the parasitics.

7.6.6.1.1 1.2V Digital LDO

Ball name: VDD

Table 7-5. 1.2V Dig LDO Output

| | Min | Typ | Max | Unit |
|--|-----|-----|-----|------|
| Recommended value of C | 3.6 | 4.7 | 5.2 | uF |
| Allowed output parasitic inductance L_p ⁽¹⁾ | 1 | 1.5 | 2 | nH |
| Allowed output parasitic resistance R_p ⁽²⁾ | 15 | 20 | 35 | mOhm |

(1) $L_p = LT1 + ESL1 + LT2$

(2) $R_p = RT1 + ESR1 + RT2$

7.6.6.2 Two-capacitor rail

The 1.2V RF LDO, 1.2V SRAM LDO and 1.0V RF LDO require two decoupling capacitors with typical values of 10uF and 2.2uF.

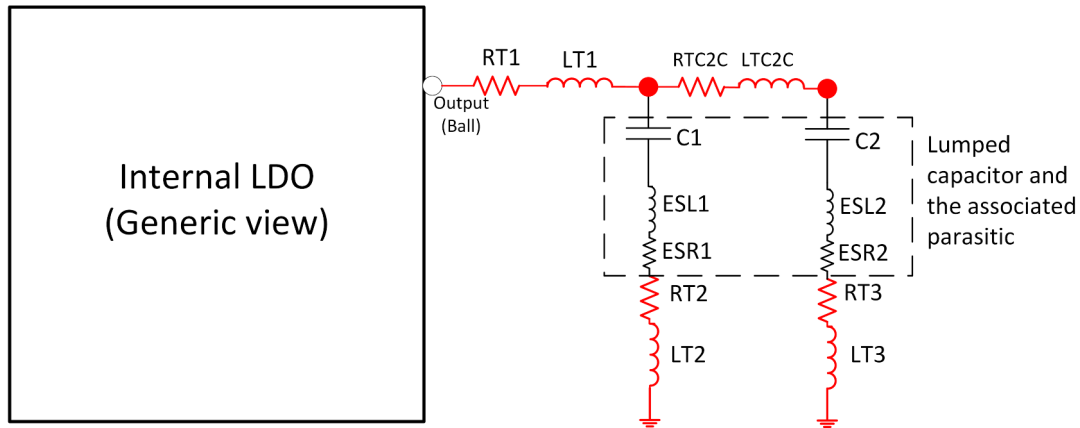


Figure 7-5. Parasitic offered by different portion of the output path (for two capacitors)

The parasitics offered by different portions of the output path is illustrated in [Figure 7-5](#). As shown in [Figure 7-5](#), the output path can be divided into four portions:

Ball to first capacitor: “RT1” and “LT1” are the parasitic resistance and inductance offered by the ball to the first capacitor lead.

Along the first capacitor: “ESL1” and “ESR1” are the effective series inductance and resistance of the first decoupling capacitor. “RT2” and “LT2” are the ground trace resistance and inductance respectively of the first capacitor ground trace.

First capacitor lead to second capacitor lead: “RTC2C” and “LTC2C” are the resistance and inductance of the trace between two capacitors.

Along the second capacitor: “ESL2” and “ESR2” are the effective series inductance and resistance of the second decoupling capacitor. “RT3” and “LT3” are the ground trace resistance and inductance respectively of the second capacitor ground trace.

Note

Both the capacitors are recommended to be placed close to the respective ball.

7.6.6.2.1 1.2V RF LDO

Ball name: VDDA_12RF

Table 7-6. 1.2V RF LDO Output

| | | Min | Typ | Max | Unit |
|-------------------------------------|--|-----|------|------|------|
| Recommended value(s) of C | C1 | 4.9 | 10.0 | 11.0 | uF |
| | C2 | 1.3 | 2.2 | 2.4 | uF |
| Allowed output parasitic inductance | Ball to 1 st Capacitor lead (LT1) | 0.3 | | 0.6 | nH |
| | Along 1 st Capacitor (ESL1 + LT2) | 0.4 | | 0.7 | |
| | Between two Capacitor leads (LTC2C) | 0.1 | | 0.3 | |
| | Along the 2 nd Capacitor (ESL2 + LT3) | 0.4 | | 0.7 | |

Table 7-6. 1.2V RF LDO Output (continued)

| | | Min | Typ | Max | Unit |
|-------------------------------------|--|-----|-----|-----|------|
| Allowed output parasitic resistance | Ball to 1 st Capacitor lead (RT1) | 1 | | 5 | mOhm |
| | Along 1 st Capacitor (ESR1 + RT2) | 15 | | 25 | |
| | Between two Capacitor leads (RTC2C) | 1 | | 5 | |
| | Along the 2 nd Capacitor (ESR2 + RT3) | 15 | | 25 | |

7.6.6.2.2 1.2V SRAM LDO

Ball name: VDD_SRAM

Table 7-7. 1.2V SRAM LDO Output

| | | Min | Typ | Max | Unit |
|-------------------------------------|--|-----|------|------|------|
| Recommended value(s) of C | C1 | 4.9 | 10.0 | 11.0 | uF |
| | C2 | 1.3 | 2.2 | 2.4 | uF |
| Allowed output parasitic inductance | Ball to 1 st Capacitor lead (LT1) | 0.5 | | 1.0 | nH |
| | Along 1 st Capacitor (ESL1 + LT2) | 1.0 | | 1.5 | |
| | Between two Capacitor leads (LTC2C) | 0.5 | | 1.0 | |
| | Along the 2 nd Capacitor (ESL2 + LT3) | 1.0 | | 1.5 | |
| Allowed output parasitic resistance | Ball to 1 st Capacitor lead (RT1) | | | 1 | mOhm |
| | Along 1 st Capacitor (ESR1 + RT2) | 15 | | 35 | |
| | Between two Capacitor leads (RTC2C) | | | 1 | |
| | Along the 2 nd Capacitor (ESR2 + RT3) | 15 | | 35 | |

7.6.6.2.3 1.0V RF LDO

Ball name: VDDA_10RF

Table 7-8. 1.0V RF LDO Output

| | | Min | Typ | Max | Unit |
|-------------------------------------|--|-----|------|------|------|
| Recommended value(s) of C | C1 | 4.9 | 10.0 | 11.0 | uF |
| | C2 | 1.3 | 2.2 | 2.4 | uF |
| Allowed output parasitic inductance | Ball to 1 st Capacitor lead (LT1) | 0.3 | 0.3 | 0.6 | nH |
| | Along 1 st Capacitor (ESL1 + LT2) | 0.3 | | 1.0 | |
| | Between two Capacitor leads (LTC2C) | 0.1 | | 0.3 | |
| | Along the 2 nd Capacitor (ESL2 + LT3) | 0.3 | | 1.0 | |
| Allowed output parasitic resistance | Ball to 1 st Capacitor lead (RT1) | 1 | | 5 | mOhm |
| | Along 1 st Capacitor (ESR1 + RT2) | 15 | | 25 | |
| | Between two Capacitor leads (RTC2C) | 1 | | 5 | |
| | Along the 2 nd Capacitor (ESR2 + RT3) | 15 | | 25 | |

7.6.7 Noise and Ripple Specifications

The 1.8V power supply ripple specifications mentioned in [Table 7-9](#) are defined to meet a target spur level of -105dBc (RF Pin = -15dBm) at the RX. The spur and ripple levels have a dB-to-dB relationship, for example, a 1dB increase in supply ripple leads to a $\approx 1\text{dB}$ increase in spur level. Values quoted are peak-peak levels for a sinusoidal input applied at the specified frequency.

Table 7-9. Noise and Ripple Specifications

| FREQ (KHZ) | NOISE SPECIFICATION | | RIPPLE SPECIFICATION | |
|------------|--|--|----------------------|----------------------------|
| | 1.8V($\mu\text{V}/\sqrt{\text{Hz}}$) | 1.2V ($\mu\text{V}/\sqrt{\text{Hz}}$) ⁽¹⁾ | 1.8V(mVpp) | 1.2V (mVpp) ⁽¹⁾ |
| 10 | 6.057 | 44.987 | 0.035 | 1.996 |
| 100 | 2.677 | 26.801 | 0.760 | 2.233 |
| 200 | 2.388 | 28.393 | 0.955 | 3.116 |
| 500 | 0.757 | 9.559 | 0.504 | 1.152 |
| 1000 | 0.419 | 1.182 | 0.379 | 0.532 |
| 2000 | 0.179 | 1.256 | 0.153 | 0.561 |
| 5000 | 0.0798 | 0.667 | 0.079 | 0.297 |
| 10000 | 0.0178 | 0.104 | 0.017 | 0.046 |

(1) 1.2V noise/ripple specification is only for power optimized supply configurations. For BOM optimized topology 1.2V noise/ripple specification is not applicable.

Note

Same 1.8V noise/ripple specification is applicable for the 1.8V supply in the BOM optimized topology

7.7 Power Save Modes

Table 7-10 lists the supported power states.

Table 7-10. Device Power States

| Power State | Details |
|-------------|---|
| Active | Active Power State is when RF/chirping activity is ongoing |
| Processing | Processing Power State is when data is being processed RF turned off ⁽¹⁾ |
| Idle | Idle Power State is during inter-frame/inter-burst/inter-chirp idle time |
| Deep Sleep | Lowest possible power state of the device where the contents of the device can be retained (Application Image, Chirp Profile etc) and device need not boot from scratch again. Device can enter this state after the frame processing is complete in order to save power significantly. Deep sleep exit can be through a number of external wakeup sources and internal timing maintenance. |

(1) The power consumed here also includes the Hardware Accelerator Power Consumption.

7.7.1 Typical Power Consumption Numbers

Table 7-11 and Table 7-12 lists the typical power consumption for each power save modes in different power topologies and antenna configurations for a nominal device at 25C ambient temperature and nominal voltage conditions.

Table 7-11. Estimated Power Consumed in 3.3V IO Mode

| Power Mode | | Power Consumption (mW) | |
|-------------------|--|------------------------|--------------------|
| | | Power Optimized Mode | BOM Optimized Mode |
| Active (1TX, 3RX) | Sampling: 12.5 MSps, BW = 2GHz RX gain = 30dB TX back off = 0dB | 803 | 1064 |
| Active (1TX, 2RX) | | 720 | 950 |
| Active (1TX, 1RX) | | 690 | 910 |
| Processing | Major motion SDK OOB chain is used for measurement. | 80 | 120 |
| Idle | APPSS CM4 = 20MHz, FECSS, HWA powered off, SPI active | 11.2 | 19.0 |
| Deep sleep | Memory Retained = 114KB | 0.66 | 0.67 |

Table 7-12. Estimated Power Consumed in 1.8V IO Mode

| Power Mode | | Power Consumption (mW) | |
|-------------------|---|------------------------|--------------------|
| | | Power Optimized Mode | BOM Optimized Mode |
| Active (1TX, 3RX) | Sampling: 12.5 MSps, | 803 | 1064 |
| Active (1TX, 2RX) | BW = 2GHz | 720 | 950 |
| Active (1TX, 1RX) | RX gain = 30dB TX back off = 0dB | 690 | 910 |
| Processing | Major motion SDK OOB chain is used for measurement. | 80 | 120 |
| Idle | APPSS CM4 = 20MHz, FECSS, HWA powered off, SPI active | 10.9 | 18.6 |
| Deep Sleep | Memory Retained = 114KB | 0.48 | 0.48 |

Table 7-13. Use-Case Power Consumed in 3.3V Power Optimized Topology

| Parameter | Condition | Typical (mW) |
|--|-----------------|--------------|
| Average Power Consumption (Presence Detection -Major Motion) | 1Hz Update Rate | 1.2 |
| RF Front End Configuration : 1TX, 1RX ADC Sampling Rate = 12.5Msps Ramp End time = 25us Chirp Idle Time = 6us Chirp Slope = 35MHz/us Number of chirps per burst = 10 Burst Periodicity = 300us Number of bursts per frame = 1 Device configured to go to deep sleep state after active operation. Memory Retained in deep sleep = 114KB | | |

7.8 Peak Current Requirement per Voltage Rail

Table 7-14 provides the max split rail current numbers.

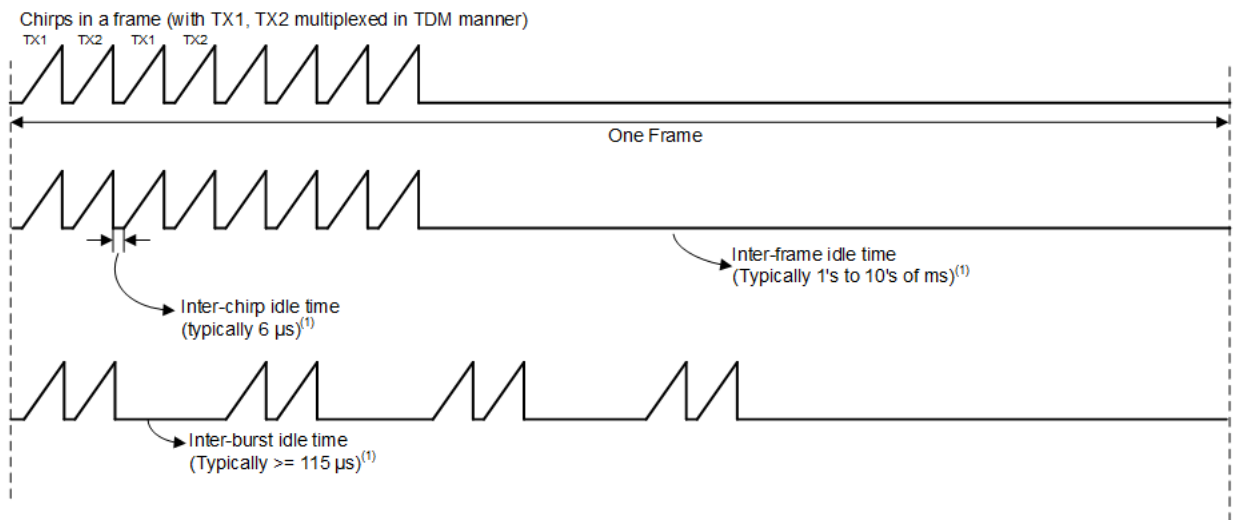
Table 7-14. Maximum Peak Current per Voltage Rail

| Mode ⁽¹⁾ | IO Voltage ⁽³⁾ | Maximum Current (mA) ⁽²⁾ | | |
|---------------------|---------------------------|--|--|--|
| | | 1.2V: total current drawn by all nodes driven by 1.2V rail | 1.8V: total current drawn by all nodes driven by 1.8V rail | 3.3V: total current drawn by all nodes driven by 3.3V rail |
| BOM Optimized | 3.3V | NA | 1360 | 90 |
| BOM Optimized | 1.8V | NA | 1450 | NA |
| Power Optimized | 3.3V | 1100 | 270 | 90 |
| Power Optimized | 1.8V | 1100 | 360 | NA |

- (1) Exercise full functionality of device, including 1TX, 3RX in TDM MIMO mode operation, HWA, M4F and various host comm/interface peripherals active (CAN, I2C, GPADC), test across full temperature range
- (2) The specified current values are at typical supply voltage level.
- (3) The exact VIOIN current depends on the peripherals used and the frequency of operation.

7.9 Supported DFE Features

- TX output back-off
 - TX back-off is supported from 0dB to 26dB in 1dB steps
- RX gain
 - Real only RX channels
 - Total RX gain range of 30 dB to 40dB, in 2dB steps
- VCO
 - Single VCO covering entire RF sweep bandwidth up to 6.5GHz.
- High-pass filter
 - Supports corner frequency options: 175kHz, 350kHz, 700kHz, 1400kHz
 - First-order high pass filter only
- Low-pass filter
 - Max IF bandwidth supported is 5MHz
 - 40dB stopband rejection, two filtering options supported
 - 90% visibility – IF bandwidth is 90% of Nyquist (has longer setting time due to larger filter length)
 - 80% visibility – IF bandwidth is 80% of Nyquist and is 30% faster due to quicker settling time, compared with 90% visibility
- Supported ADC sampling rates
 - 1.0, 1.25, 1.667, 2.0, 2.5, 4.0, 5.0, 6.667, 7.692, 10.0, 12.5Msps
- Timing Engine
 - Support for chirps, bursts and frames
 - Longer frame idle time gives more power saving than a longer burst idle time. Further, a longer chirp idle time gives lesser power saving than a longer burst idle time. For more details please refer power calculator in the [mmWave sensing estimator](#).
 - Chirp accumulation (averaging) possible across closely spaced chirps to reduce memory requirement
 - Provision for per-chirp dithering of parameters



1. Refer to DFP API documentation

Figure 7-6. Chip Profile Supported by Timing Engine

7.10 RF Specification

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | | MIN | TYP | MAX | UNIT |
|-----------------|--|---------------|-------------------|-----|------|--------|------|
| Receiver | Effective isotropic noise figure (EINF) ⁽¹⁾ | 57 to 63.5GHz | Tx Back off = 0dB | | 16 | | dB |
| | | | Tx Back off = 6dB | | 12 | | |
| | IF bandwidth ⁽²⁾ | | | | 5 | MHz | |
| | ADC sampling rate (real) | | | | 12.5 | Msp/s | |
| Transmitter | ADC resolution | | | 12 | | Bits | |
| | Single transmitter output power EIRP ⁽³⁾ | | | 17 | | dBm | |
| | Power backoff range | | | 26 | | dB | |
| Clock subsystem | Frequency range | | 57 | | 63.5 | GHz | |
| | Ramp rate | | | | 400 | MHz/μs | |
| | Phase noise at 1MHz offset | 57 to 63.5GHz | | -89 | | dBc/Hz | |

- (1) With single TX ON. EINF varies with RF and TX-RX combination. Please refer to [Tx back off and Rx gain recommendation for xWRL6432AOP](#).
- (2) The analog IF stages include high-pass filtering, with configurable first-order high-pass corner frequency. The set of available HPF corners is summarized as follows:

| Available HPF Corner Frequencies (kHz) |
|--|
| 175, 350, 700, 1400 |

- The filtering performed by the digital baseband chain is targeted to provide less than ±0.5dB pass-band ripple/droop.
- (3) For more details please refer to [Transmitter Antenna Radiation Pattern](#).

7.11 CPU Specifications

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TYP | UNIT |
|------------------------------------|---|-----|------|
| Application Subsystem (M4F Family) | Clock Speed | 160 | MHz |
| | Tightly Coupled Memory - A (Program + Data) | 512 | KB |
| Shared Memory | Shared L3 Memory ⁽¹⁾ | 256 | KB |
| | L3 Memory dedicated for HWA | 256 | KB |

- (1) L3 memory is configurable

7.12 Thermal Resistance Characteristics

Table 7-15. Thermal Resistance Characteristics for AMY Package [AMY0101A]

| THERMAL METRICS ^{(1) (4)} | | °C/W ^{(2) (3)} |
|------------------------------------|-------------------------|-------------------------|
| RO _{JC} | Junction-to-case | 6.4 |
| RO _{JB} | Junction-to-board | 18.1 |
| RO _{JA} | Junction-to-free air | 36.9 |
| Psi _{JC} | Junction-to-package top | 3.24 |
| Psi _{JB} | Junction-to-board | 17.7 |

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) °C/W = degrees Celsius per watt.
- (3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RO_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
 - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements
- (4) Test Condition: Power=1.305W at 25°C

7.13 Antenna Radiation Patterns

This section discusses transmitter and receiver antenna radiation patterns in Azimuth and Elevation planes

Note

The edge of the AOP device should be close to the edge of the PCB as done in [IWRL6432AOPEVM](#) or [IWRL6432AOP Reference Design](#) to minimize ripples in the radiation pattern caused by surface waves. For large form factor boards, trapezoidal cutouts with the PCB edge less than 0.3mm from the edge of the AOP should be implemented if permitted by design form-factor

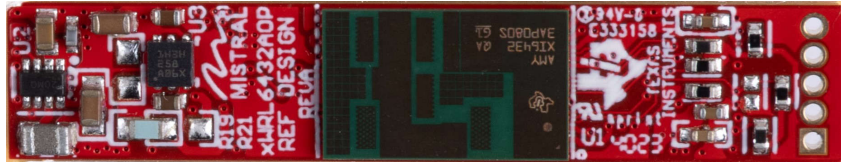


Figure 7-7. IWRL6432AOP Reference Design with PCB edge less than 0.3mm

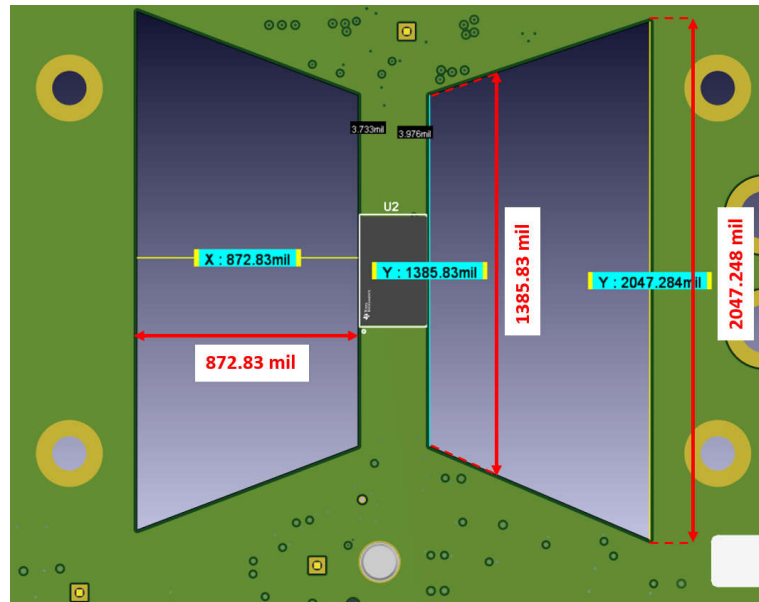
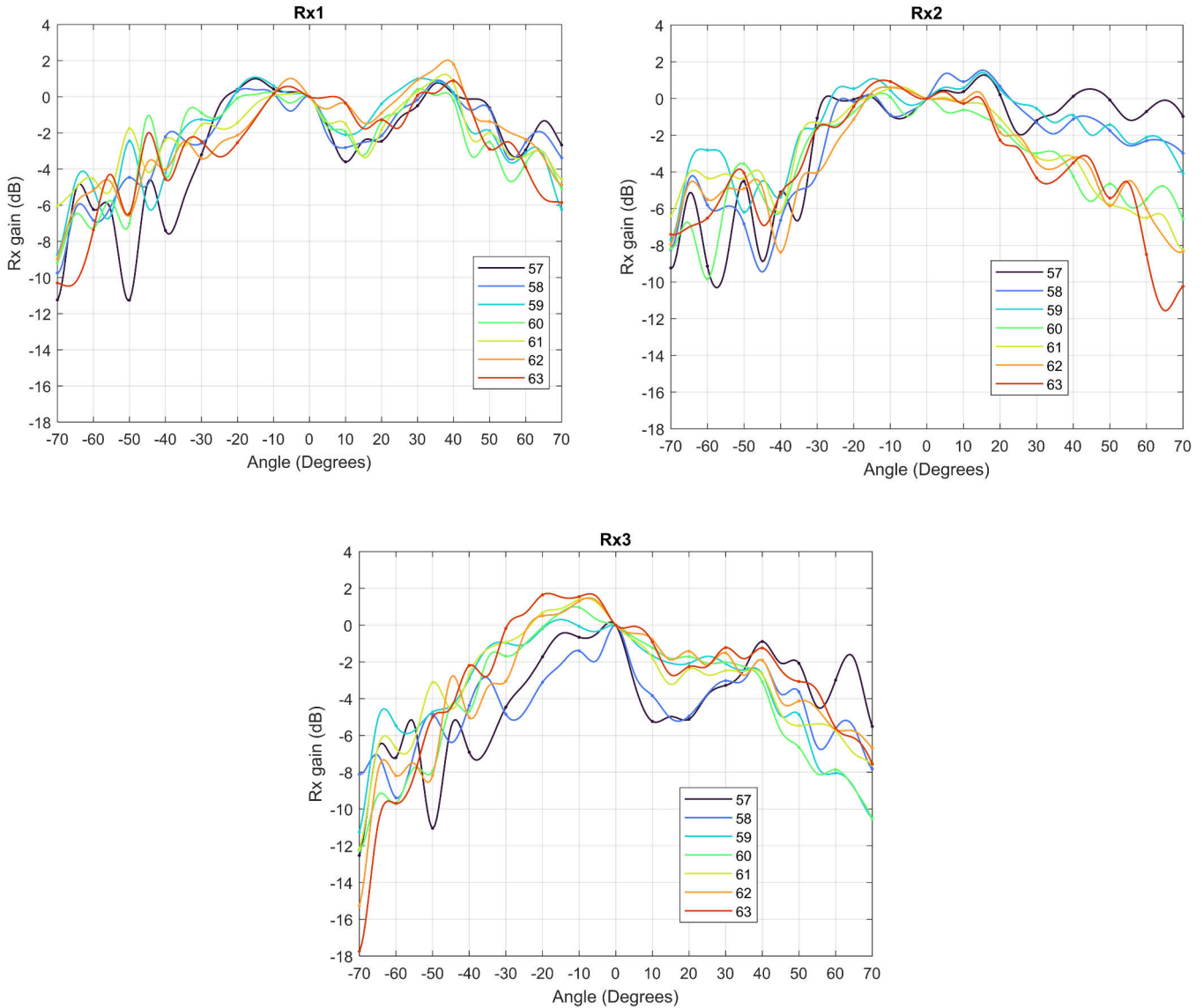


Figure 7-8. Large form factor board with trapezoidal cutout and PCB edge less than 0.3mm

7.13.1 Antenna Radiation Patterns for Receiver

Figure 7-9 shows typical antenna radiation gain plots normalized to boresight at various frequencies for the three receivers in both Azimuth and Elevation planes. The Y axis shows the Gain in dB and X axis shows the angle in degrees.

RX Gain Plot across Azimuth (normalized to boresight)



RX Gain Plot across Elevation (normalized to boresight)

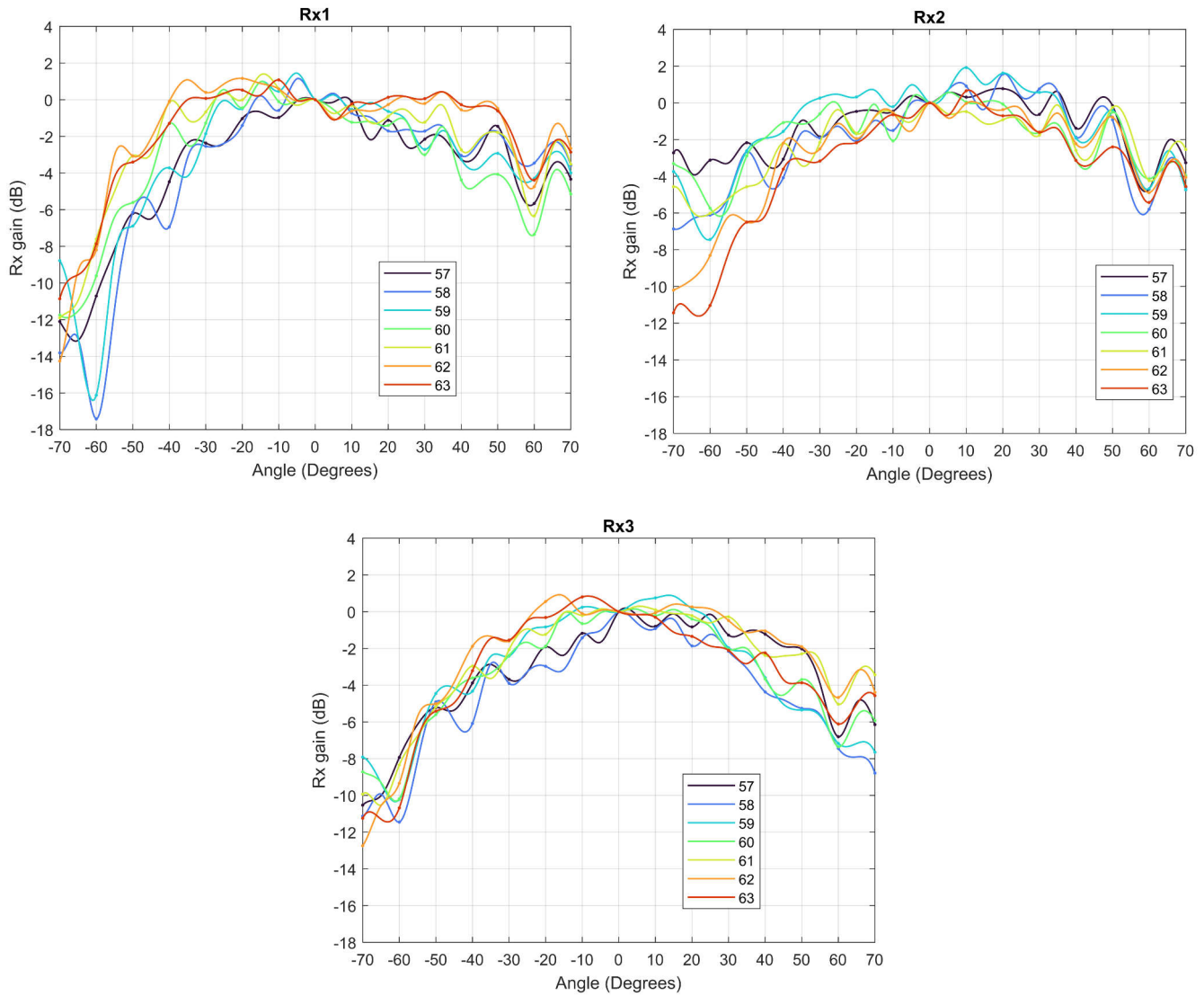


Figure 7-9. Receiver Gain Plot normalized to boresight

7.13.2 Antenna Radiation Patterns for Transmitter

Figure 7-10 shows typical antenna radiation patterns for the two transmitters in both Azimuth and Elevation planes. The Y axis shows the average EIRP in dBm for 0dB back off setting and X axis shows the angle in degrees.

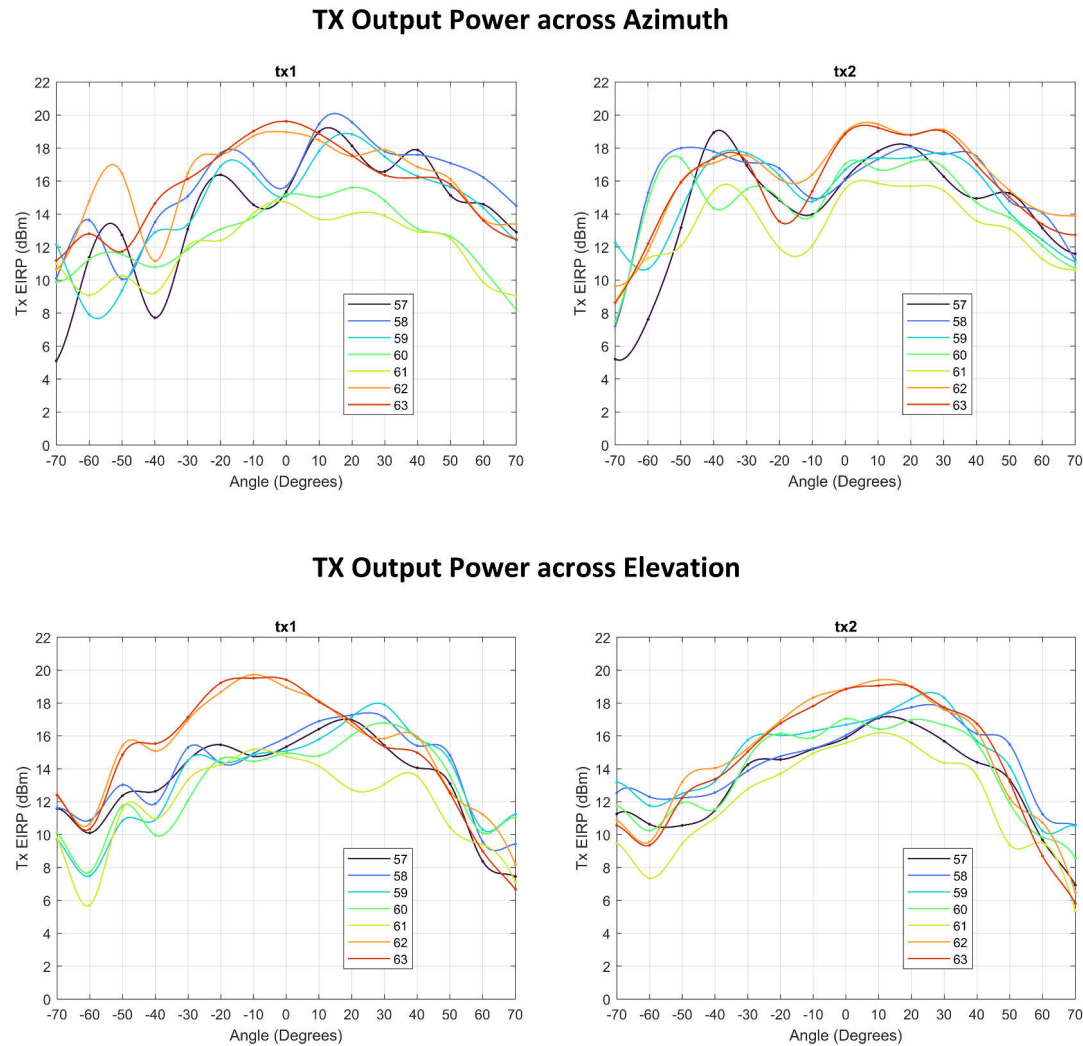


Figure 7-10. Transmitter Antenna Radiation Pattern

7.14 Antenna Positions

Figure 7-11 shows the placement and relative spacing of the antennas.

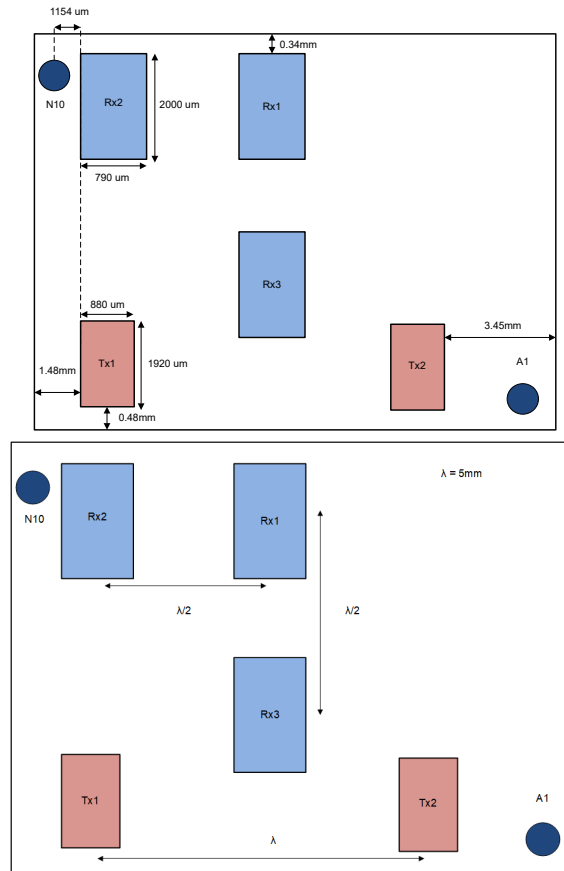
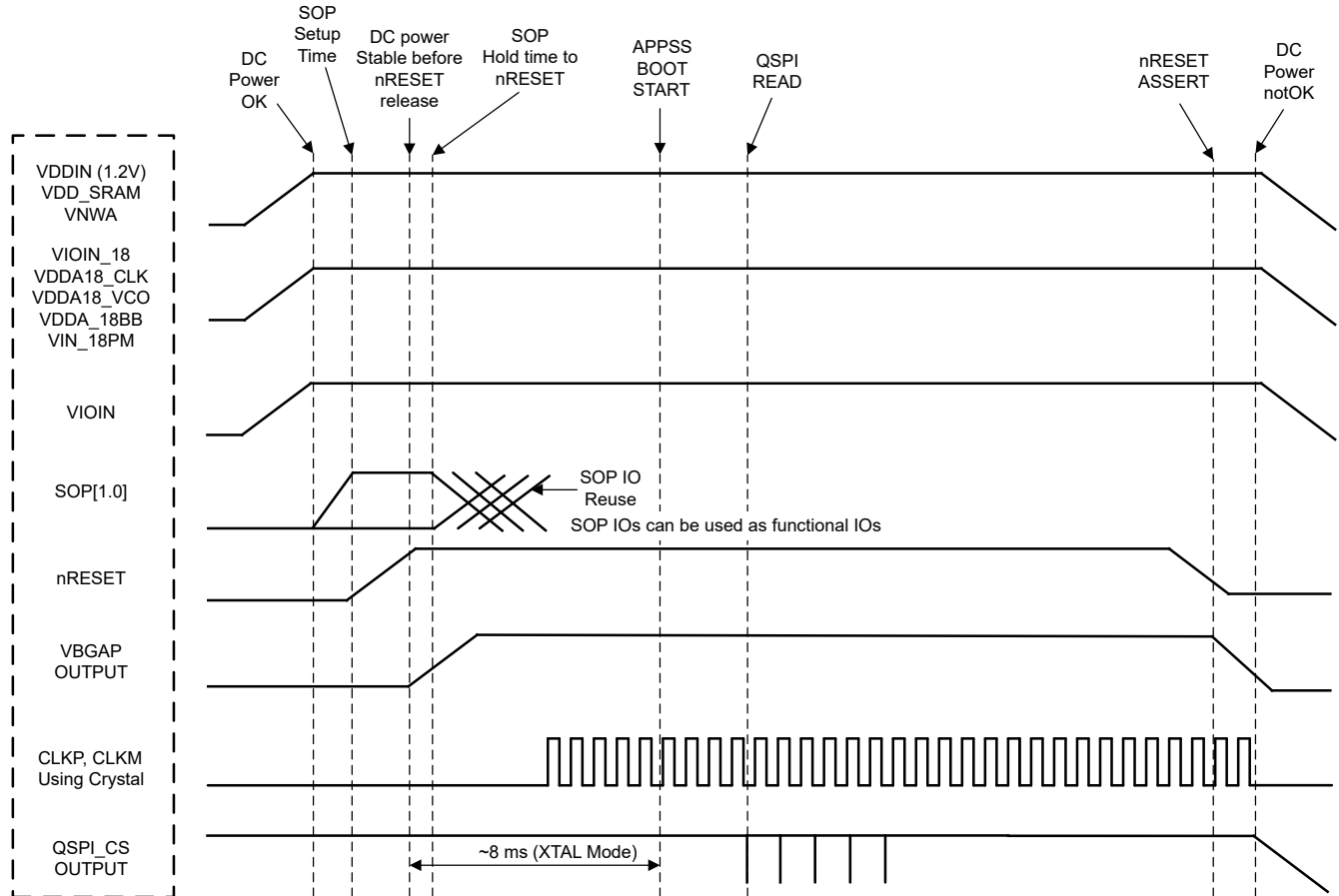


Figure 7-11. Antenna Positions (Placement and Relative Spacing)

7.15 Timing and Switching Characteristics

7.15.1 Power Supply Sequencing and Reset Timing

The IWRL6432AOP device expects all external voltage rails to be stable before reset is deasserted. [Figure 7-12](#) describes the device wake-up sequence.



- A. MCU_CLK_OUT in autonomous mode, where IWRL6432AOP application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

Figure 7-12. Device Wake-up Sequence

7.15.2 Synchronized Frame Triggering

The IWRL6432AOP device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. A software API trigger must be provided to set up the device for the hardware SYNC_IN trigger. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

The periodicity of the external SYNC_IN pulse should be always greater than the programmed frame periodicity in the frame configurations in all instances.

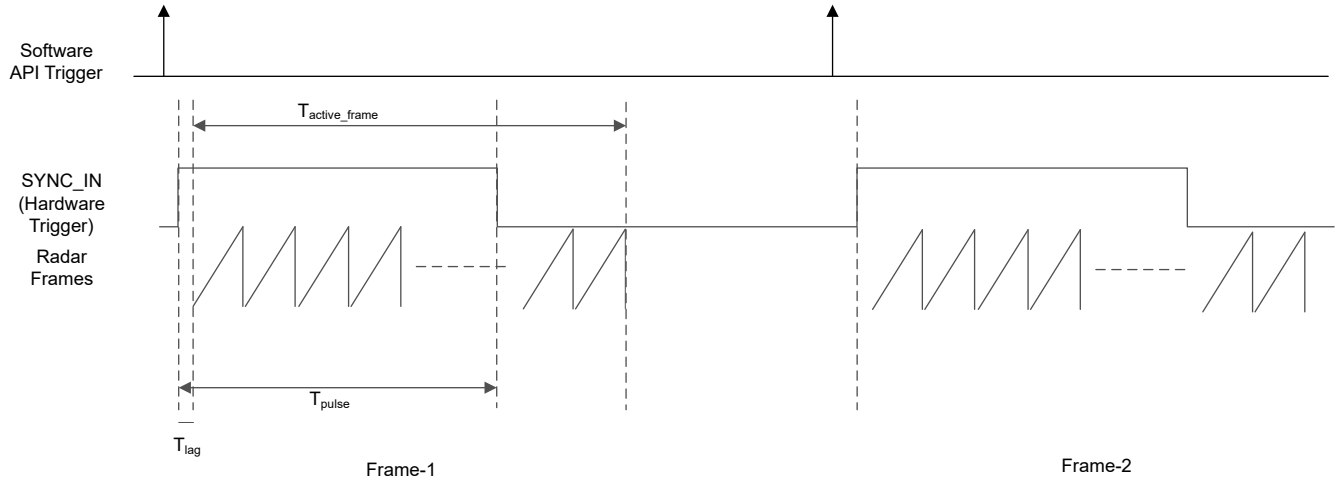


Figure 7-13. Sync In Hardware Trigger

Table 7-16. Frame Trigger Timing

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---------------------|-----------------------|--------------|-------------------------------|------|
| T_{active_frame} | Active frame duration | User defined | | ns |
| T_{pulse} | | 25 | $< T_{active_frame}$ or 4000 | |

7.15.3 Input Clocks and Oscillators

7.15.3.1 Clock Specifications

The IWRL6432AOP requires external clock source (that is, a 40MHz crystal or external oscillator to CLKP) for initial boot and as a reference for an internal APLL hosted in the device. An external crystal connected to the device pins [Figure 7-14](#) shows the crystal implementation.

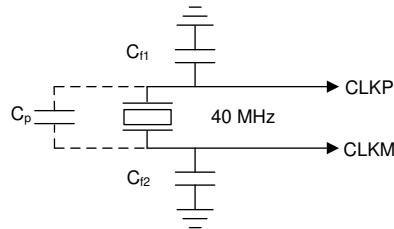


Figure 7-14. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in [Figure 7-14](#), should be chosen such that [Equation 1](#) is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

[Table 7-17](#) lists the electrical characteristics of the clock crystal.

Table 7-17. Crystal Electrical Characteristics (Oscillator Mode)

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------|--|------|-----|-----|--------------------|
| f_P | Parallel resonance crystal frequency | | 40 | | MHz |
| C_L | Crystal load capacitance | 5 | 8 | 12 | pF |
| ESR | Crystal ESR | | | 50 | Ω |
| Temperature range | Expected temperature range of operation | -40 | | 105 | $^{\circ}\text{C}$ |
| Frequency tolerance | Crystal frequency tolerance ^{(1) (2) (3)} | -200 | | 200 | ppm |
| Drive level | | | 50 | 200 | μW |

(1) The crystal manufacturer's specification must satisfy this requirement.

(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

(3) Crystal tolerance affects radar sensor accuracy.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40MHz clock is fed externally. [Table 7-18](#) lists the electrical characteristics of the external clock signal.

Table 7-18. External Clock Mode Specifications

| PARAMETER | | SPECIFICATION | | | UNIT |
|---|------------------------|---------------|-----|------|---------|
| | | MIN | TYP | MAX | |
| Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40MHz | Frequency | | 40 | | MHz |
| | AC-Amplitude | 700 | | 1200 | mV (pp) |
| | DCV _{il} | 0.00 | | 0.20 | V |
| | DCV _{ih} | 1.6 | | 1.95 | V |
| | Phase Noise at 1kHz | | | -132 | dBc/Hz |
| | Phase Noise at 10 kHz | | | -143 | dBc/Hz |
| | Phase Noise at 100 kHz | | | -152 | dBc/Hz |
| | Phase Noise at 1MHz | | | -153 | dBc/Hz |
| | Duty Cycle | 35 | | 65 | % |
| | Frequency Tolerance | -200 | | 200 | ppm |

7.15.4 MultiChannel buffered / Standard Serial Peripheral Interface (McSPI)

The McSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus

7.15.4.1 McSPI Features

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receive mode
- Controller multichannel mode:
 - Full duplex/half duplex
 - Transmit-only/receive-only/transmit-and-receive modes
 - Flexible input/output (I/O) port controls per channel
 - Programmable clock granularity
 - Per channel configuration for clock definition, polarity enabling, and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for McSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

7.15.4.2 SPI Timing Conditions

Table 7-19 presents timing conditions for McSPI

Table 7-19. McSPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t _R | Input rise time | 1 | | 3 | ns |
| t _F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C _{LOAD} | Output load capacitance | 2 | | 15 | pF |

7.15.4.3 SPI—Controller Mode

7.15.4.3.1 Timing and Switching Requirements for SPI - Controller Mode

Table 7-20 and Table 7-21 present timing requirements for SPI - Controller Mode.

Table 7-20. SPI Timing Requirements - Controller Mode

| NO. ⁽¹⁾ (8) | | | MODE | MIN | MAX | UNIT |
|---------------------------|-----------------------|--|------|-----|-----|------|
| SM4 | $t_{su(MISO-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge ⁽¹⁾ | | 5 | | ns |
| SM5 | $t_{h(SPICLK-MISO)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge ⁽¹⁾ | | 3 | | ns |

Table 7-21. SPI Switching Characteristics - Controller Mode

| NO. ⁽¹⁾ (8) | | | MODE | MIN | MAX | UNIT |
|---------------------------|----------------------|---|---|------------------------------------|-----|------|
| SM1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK ^{(1) (2)} | | 24.6 ⁽³⁾ | | ns |
| SM2 | $t_{w(SPICLKL)}$ | Typical Pulse duration, SPI_CLK low ⁽¹⁾ | | -1 + 0.5P ⁽³⁾ (4) | | ns |
| SM3 | $t_{w(SPICLKH)}$ | Typical Pulse duration, SPI_CLK high ⁽¹⁾ | | -1 + 0.5P ⁽⁴⁾ | | ns |
| SM6 | $t_{d(SPICLK-SIMO)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition ⁽¹⁾ | | -2 | 5 | ns |
| SM7 | $t_{sk(CS-SIMO)}$ | Delay time, SPI_CS[x] active to SPI_D[x] transition | | 5 | | ns |
| SM8 | $t_{d(SPICLK-CS)}$ | Delay time, SPI_CS[x] active to SPI_CLK first edge | Controller_PHA0_POL 0; Controller_PHA0_POL 1; ⁽⁵⁾ | -4 + B ⁽⁶⁾ | | ns |
| | | | Controller_PHA1_POL 0; Controller_PHA1_POL 1; ⁽⁵⁾ | -4 + A ⁽⁷⁾ | | ns |
| SM9 | $t_{d(SPICLK-CS)}$ | Delay time, SPI_CLK last edge to SPI_CS[x] inactive | Controller_PHA0_POL 0; Controller_PHA0_POL 1; ⁽⁵⁾ | -4 + A ⁽⁷⁾ | | ns |
| | | | Controller_PHA1_POL 0; Controller_PHA1_POL 1; ⁽⁵⁾ | -4 + B ⁽⁶⁾ | | ns |
| SM11 | Cb | Capacitive load for each bus line | | 3 | 15 | pF |

- (1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data
- (2) Related to the SPI_CLK maximum frequency
- (3) 20 ns cycle time = 50 MHz
- (4) P = SPICLK period
- (5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register
- (6) $B = (TCS + .5) \times TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even ≥ 2 .
- (7) When $P = 20.8$ ns, $A = (TCS + 1) \times TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register.
When $P > 20.8$ ns, $A = (TCS + 0.5) \times Fratio \times TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register.
- (8) The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.

This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data

Note

The maximum supported frequency depends on host driver capabilities (data latching edge, setup time, hold time, clock jitter, clock duty-cycle, IO delay etc.) and the system level design (PCB design, propagation delay, IO load etc.). Timing analysis for the complete path (Host to Device) needs to be performed for determining the maximum achievable frequency.

An indicative example: Supported frequency of Radar SPI Peripheral mode is 40MHz in full cycle and 20MHz in half cycle mode.

7.15.4.3.2 Timing and Switching Characteristics for SPI Output Timings—Controller Mode

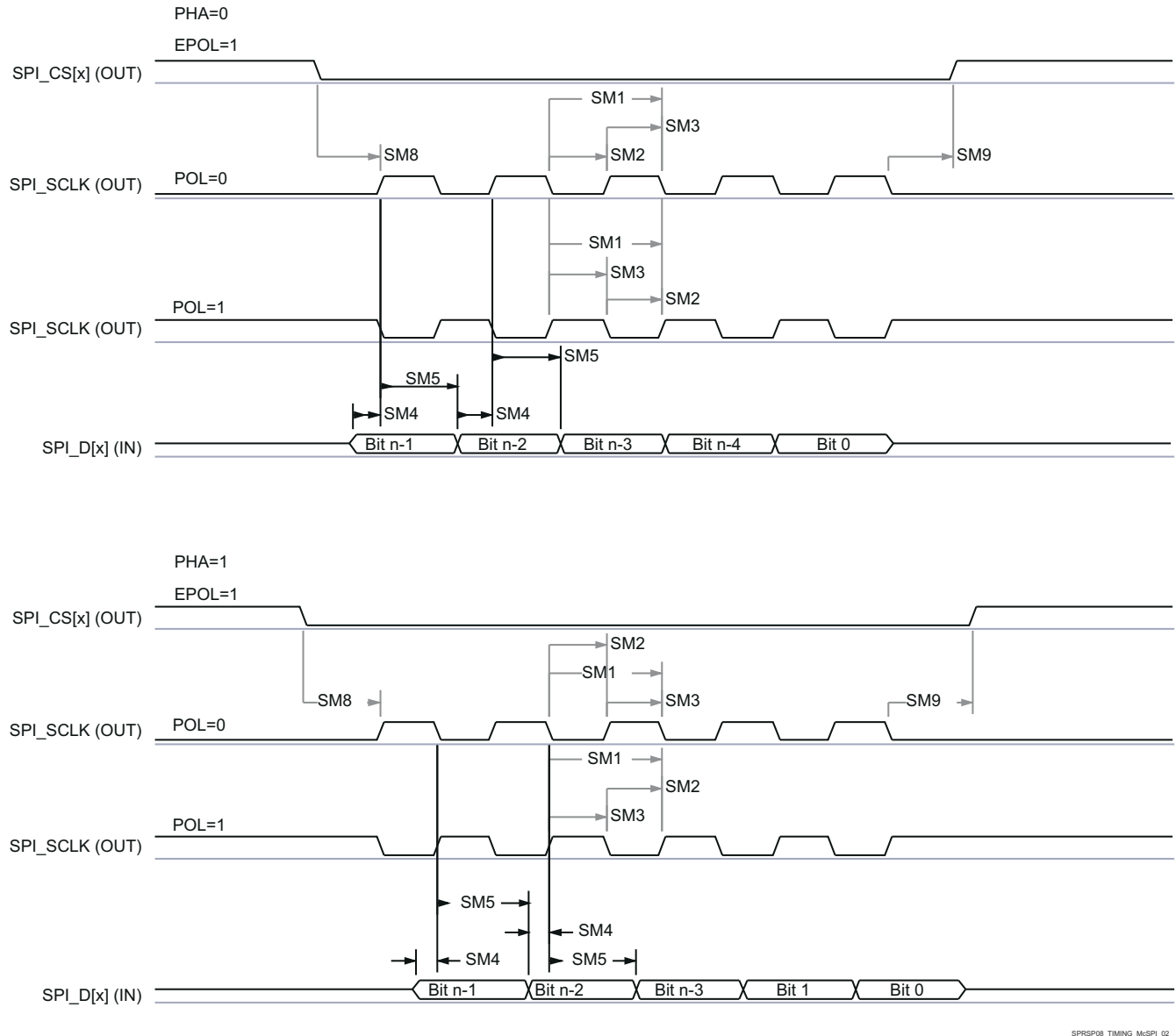
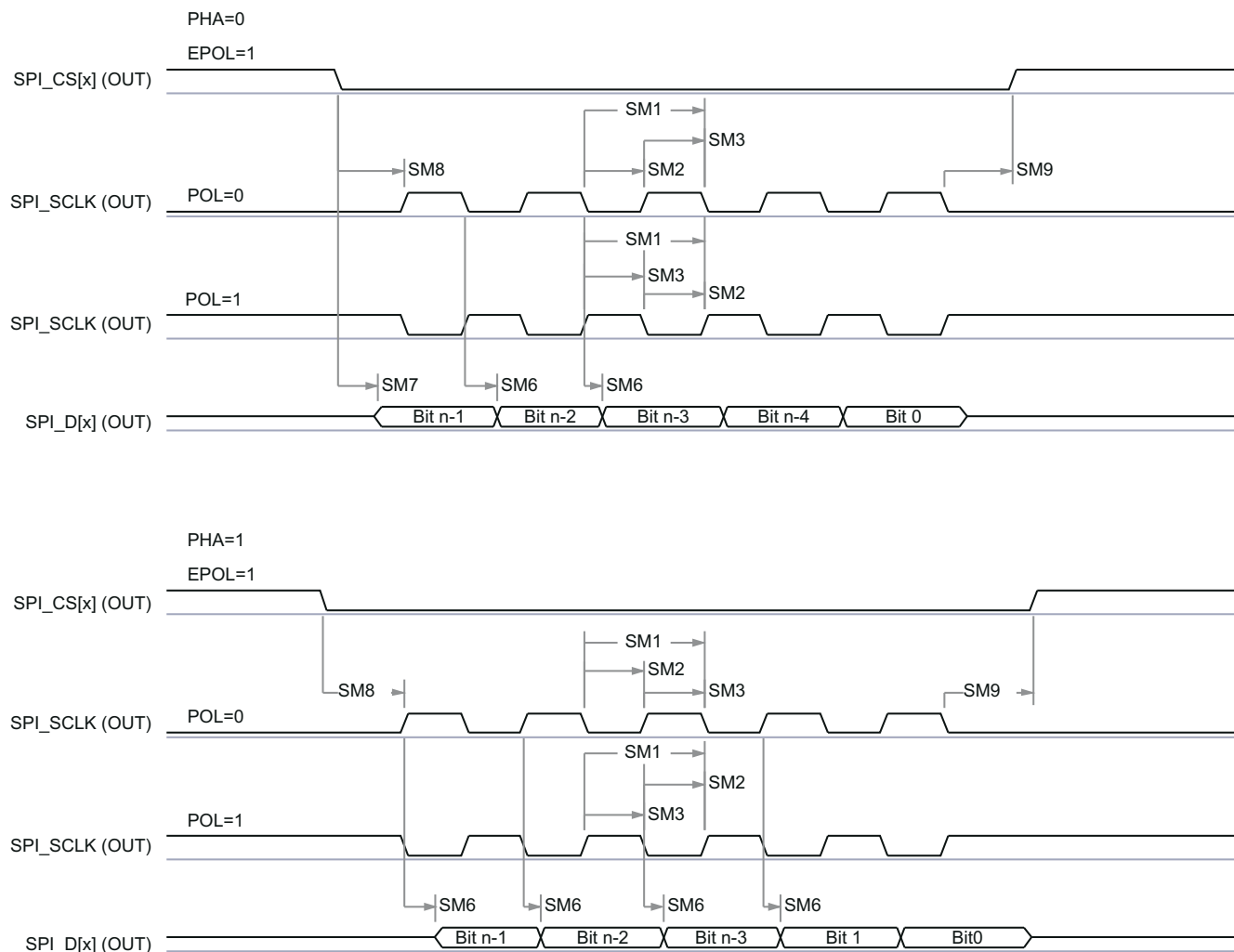


Figure 7-15. SPI Timing -Controller Mode Receive

SPIRSP08_TIMING_McSPI_02



SPRSP08_TIMING_McSPI_01

Figure 7-16. SPI Timing - Controller Mode Transmit

7.15.4.4 SPI—Peripheral Mode

7.15.4.4.1 Timing and Switching Requirements for SPI - Peripheral Mode

Table 7-22 and Table 7-23 present timing requirements for SPI -Peripheral Mode.

Table 7-22. SPI Timing Requirements - Peripheral Mode

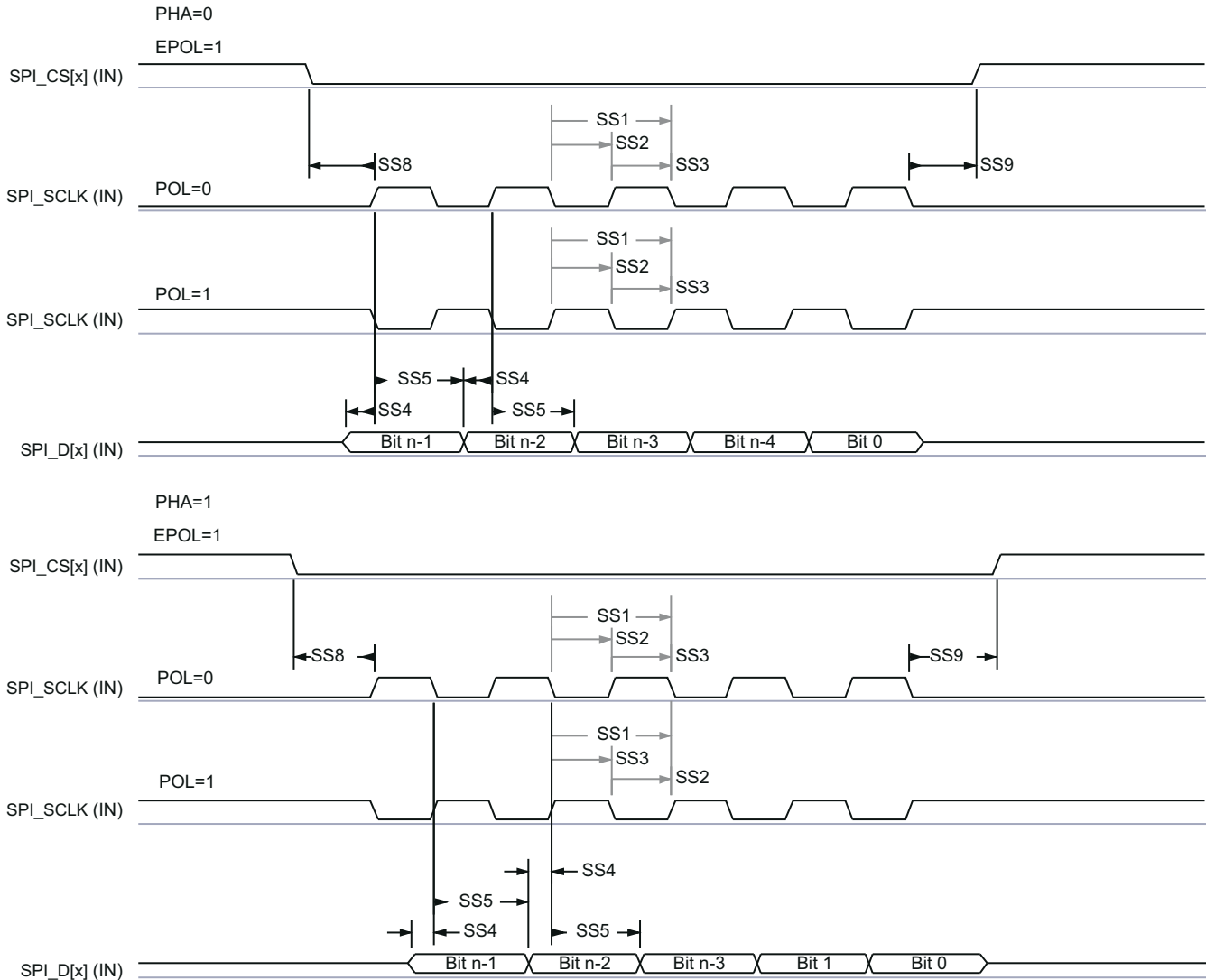
| NO.(1) (3) | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|------------|-----------------------|---|-----------------------|-----|------|
| SS1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK | 24.6 | | ns |
| SS2 | $t_{w(SPICLKL)}$ | Typical Pulse duration, SPI_CLK low | 0.45*P ⁽²⁾ | | ns |
| SS3 | $t_{w(SPICLKH)}$ | Typical Pulse duration, SPI_CLK high | 0.45*P ⁽²⁾ | | ns |
| SS4 | $t_{su(SIMO-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge | 3 | | ns |
| SS5 | $t_{h(SPICLK-SIMO)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge | 1 | | ns |
| SS8 | $t_{su(CS-SPICLK)}$ | Setup time, SPI_CS[x] valid before SPI_CLK first edge | 5 | | ns |
| SS9 | $t_{h(SPICLK-CS)}$ | Hold time, SPI_CS[x] valid after SPI_CLK last edge | 5 | | ns |
| SS10 | sr | Input Slew Rate for all pins | 1 | 3 | ns |
| SS11 | Cb | Capacitive load on D0 and D1 | 2 | 15 | pF |

Table 7-23. SPI Switching Characteristics Peripheral Mode

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|-----|----------------------|--|------|------|------|
| SS6 | $t_{d(SPICLK-SOMI)}$ | Delay time, SPI_CLK active edge to McSPI_somi transition | 0 | 5.77 | ns |
| SS7 | $t_{sk(CS-SOMI)}$ | Delay time, SPI_CS[x] active edge to McSPI_somi transition | 5.77 | | ns |

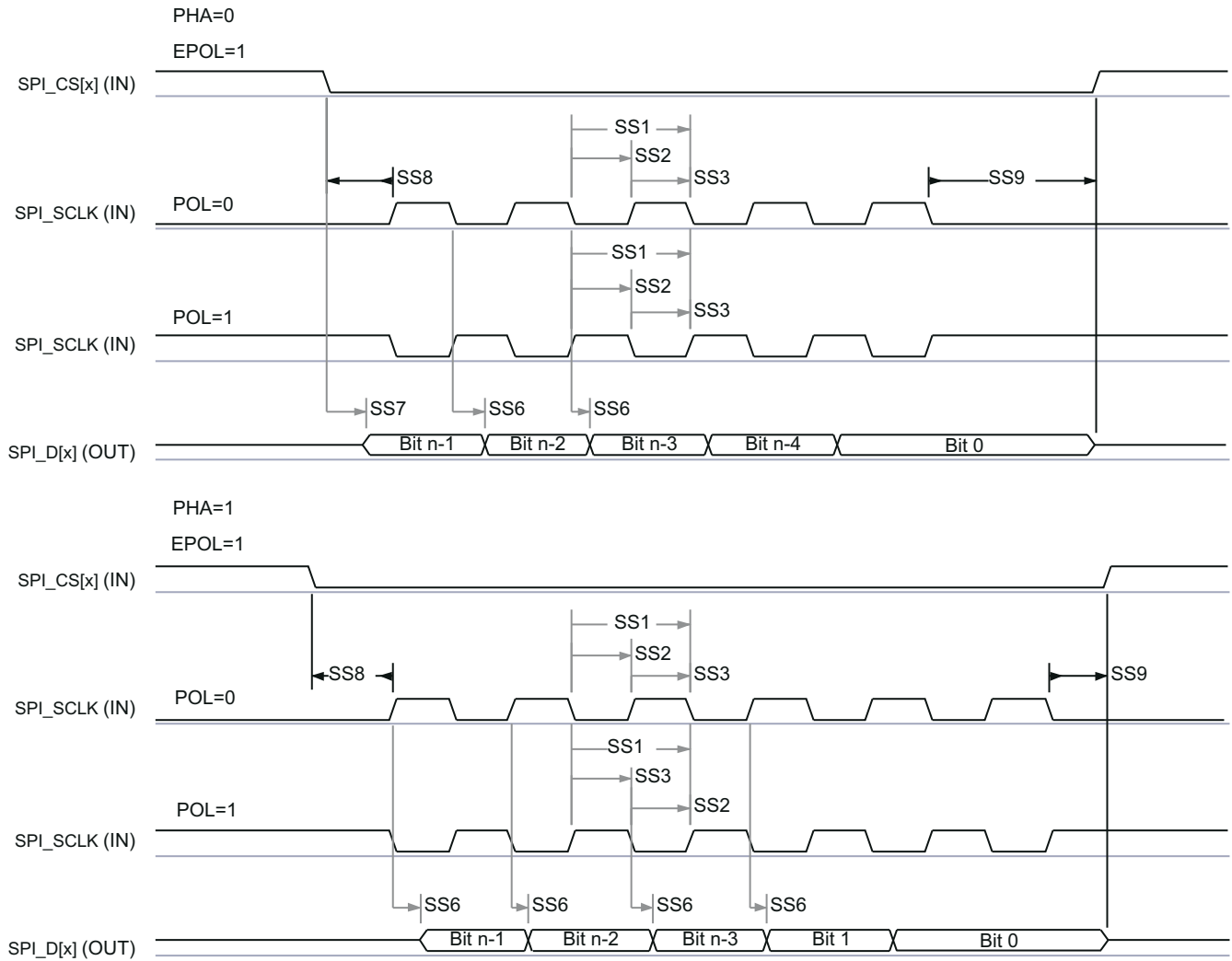
- (1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
- (2) P = SPICLK period.
- (3) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

7.15.4.4.2 Timing and Switching Characteristics for SPI Output Timings—Secondary Mode



SPRSP08_TIMING_McSPI_04

Figure 7-17. SPI Timing - Peripheral mode Receive



SPRSP08_TIMING_McSPI_03

Figure 7-18. SPI Timing - Peripheral mode Transmit

7.15.5 RDIF Interface Configuration

The supported Radar Data InterFace (RDIF) is developed as a debug interface (for example: to capture raw ADC data) and not as a production interface. The RDIF has four data lanes, one Bit Clock lane, and one Frame Clock lane. From this interface, high-speed data is sent out for debug purposes. The RDIF interface supports the following data rates¹:

- 400Mbps
- 320Mbps
- 200Mbps
- 160Mbps

7.15.5.1 RDIF Interface Timings

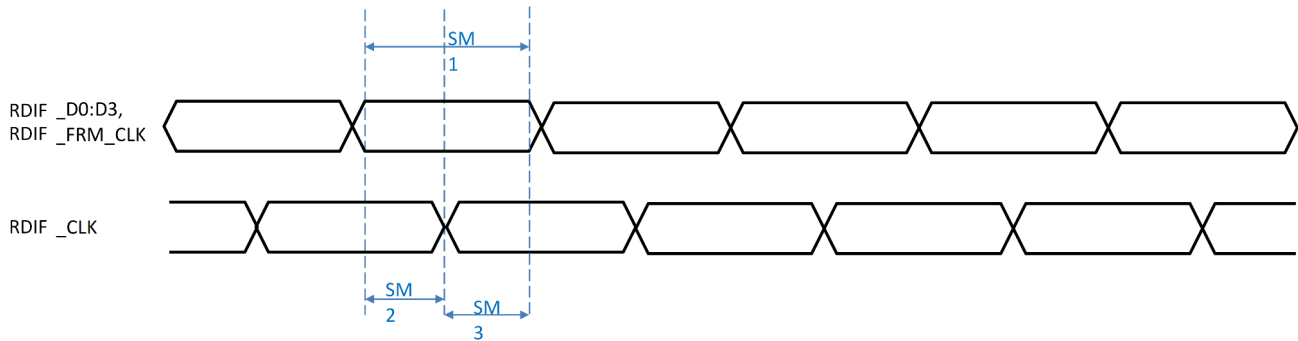


Figure 7-19. RDIF Timing Requirements

Table 7-24. Timing Requirements for RDIF Interface

| No. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|-----|--|---|----------------|-----|-----|------|
| SM1 | T _b (RDIF_D[x]) | Bit Interval, RDIF_d[x] | Internal Clock | 9.6 | | ns |
| SM2 | T _{vb} (RDIF_D[x] - RDIF_CLK) | Data valid time, RDIF_d[x] and RDIF_frm_clk valid before RDIF_clk active edge | Internal Clock | 4.8 | | ns |
| SM3 | T _{va} (RDIF_CLK - RDIF_D[x]) | Data valid time, RDIF_d[x] valid after RDIF_clk active edge | Internal Clock | 4.8 | | ns |
| SM4 | C _b | Capacitive load for each bus line | | 3 | 15 | pF |

¹ Aggregated data rate over four data lanes.

7.15.5.2 RDIF Data Format

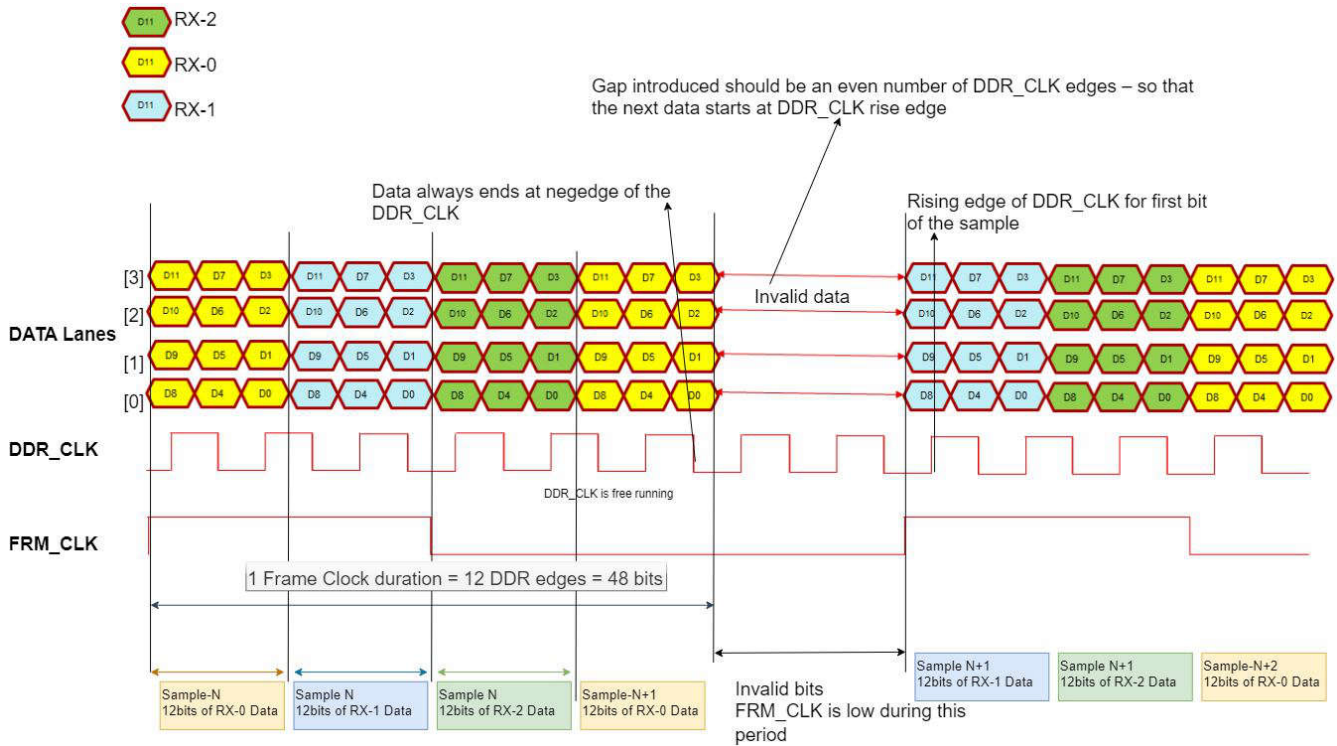


Figure 7-20. RDIF Data Format

- The samples are sent one channel by one channel as shown in the diagram above. All the 12-bits of one channel are sent on 4 data lanes in 3 DDR_CLK edges, followed by next RX channel.
- The frame clock (FRM_CLK) spans 12 DDR_CLK edges and 48 bits are sent in 1 FRM_CLK
- The FRM_CLK can have gaps in between. This is required as the interface rate is greater than the incoming rate
- DDR_CLK is continuous.
- DDR_CLK is generated from 400MHz ADC CLK (one of the ADC CLKs) - selected for the DFE. It is the same 400MHz clock selected for DFE.
- New sample always starts at the rise edge of the DDR_CLK
- The FRM_CLK is valid for the entire data bit and is meets the T_{su}/T_{th} wrt DDR_CLK.

7.15.6 General-Purpose Input/Output

7.15.6.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)

Table 7-25 lists the switching characteristics of output timing relative to load capacitance.

Table 7-25. Switching Characteristics for Output Timing versus Load Capacitance (C_L)

| PARAMETER ^{(1) (2)} | | TEST CONDITIONS | VIOIN = 1.8V | VIOIN = 3.3V | UNIT | |
|------------------------------|---------------|------------------|---------------------|--------------|------|----|
| t_r | Max rise time | Slew control = 0 | $C_L = 20\text{pF}$ | 2.8 | 3.0 | ns |
| | | | $C_L = 50\text{pF}$ | 6.4 | 6.9 | |
| | | | $C_L = 75\text{pF}$ | 9.4 | 10.2 | |
| t_f | Max fall time | | $C_L = 20\text{pF}$ | 2.8 | 2.8 | ns |
| | | | $C_L = 50\text{pF}$ | 6.4 | 6.6 | |
| | | | $C_L = 75\text{pF}$ | 9.4 | 9.8 | |
| t_r | Max rise time | Slew control = 1 | $C_L = 20\text{pF}$ | 3.3 | 3.3 | ns |
| | | | $C_L = 50\text{pF}$ | 6.7 | 7.2 | |
| | | | $C_L = 75\text{pF}$ | 9.6 | 10.5 | |
| t_f | Max fall time | | $C_L = 20\text{pF}$ | 3.1 | 3.1 | ns |
| | | | $C_L = 50\text{pF}$ | 6.6 | 6.6 | |
| | | | $C_L = 75\text{pF}$ | 9.6 | 9.6 | |

- (1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

7.15.7 Controller Area Network - Flexible Data-rate (CAN-FD)

The CAN-FD module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The CAN-FD has the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1
- Full CAN FD support (up to 64 data bytes per frame)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 11-bit filter elements
- Internal Loopback mode for self-test
- Mask-able interrupts, two interrupt lines
- Two clock domains (CAN clock / Host clock)
- Parity / ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Full Message Memory capacity (4352 words).

7.15.7.1 Dynamic Characteristics for the CANx TX and RX Pins

| PARAMETER | | MIN | TYP | MAX | UNIT |
|----------------------|---|-----|-----|-----|------|
| $t_{d(CAN_FD_tx)}$ | Delay time, transmit shift register to CAN_FD_tx pin ⁽¹⁾ | | | 15 | ns |
| $t_{d(CAN_FD_rx)}$ | Delay time, CAN_FD_rx pin to receive shift register ⁽¹⁾ | | | 15 | ns |

(1) These values do not include rise/fall times of the output buffer.

7.15.8 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions in compatibility mode
- Supports two individually enabled interrupt lines: level 0 and level 1
- Configurable frame format of 3 to 13 bits per character based on the following:
 - Data word length programmable from one to eight bits
 - Additional address bit in address-bit mode
 - Parity programmable for zero or one parity bit, odd or even parity
 - Stop programmable for one or two stop bits
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Two multiprocessor communication formats allow communication between more than two devices
- Sleep mode is available to free CPU resources during multiprocessor communication and then wake up to receive an incoming message
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Five error flags and Seven status flags provide detailed information regarding SCI events
- Two external pins: RS232_RX and RS232_TX
- Multi-buffered receive and transmit units

7.15.8.1 SCI Timing Requirements

| | | MIN | TYP | MAX | UNIT |
|---------|-----------------------------|-----|----------------------|---------------------|-------|
| f(baud) | Supported baud rate at 20pF | | 115.2 ⁽¹⁾ | 1250 ⁽²⁾ | kBaud |

- (1) Maximum supported standard baud rate.
 (2) Maximum supported custom baud rate.

7.15.9 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multi-controller communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I2C-bus™. This module will support any target or controller I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
 - Bit/Byte format transfer
 - 7-bit and 10-bit device addressing modes
 - START byte
 - Multi-controller transmitter/ target receiver mode
 - Multi-controller receiver/ target transmitter mode
 - Combined controller transmit/receive and receive/transmit mode
 - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

Note

This I2C module does not support:

- High-speed (HS) mode
 - C-bus compatibility mode
 - The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)
-

7.15.9.1 I2C Timing Requirements

| | | STANDARD MODE ⁽¹⁾ | | FAST MODE | | UNIT |
|--------------------------|---|------------------------------|---------------------|-----------|-----|---------|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | μ s |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μ s |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μ s |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | μ s |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | μ s |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| $t_{h(SCLL-SDA)}$ | Hold time, SDA valid after SCL low | 0 | 3.45 ⁽¹⁾ | 0 | 0.9 | μ s |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μ s |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | μ s |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| C_b ^{(2) (3)} | Capacitive load for each bus line | | 400 | | 400 | pF |

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins can potentially draw current when the device is powered down.
- (2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
- (3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

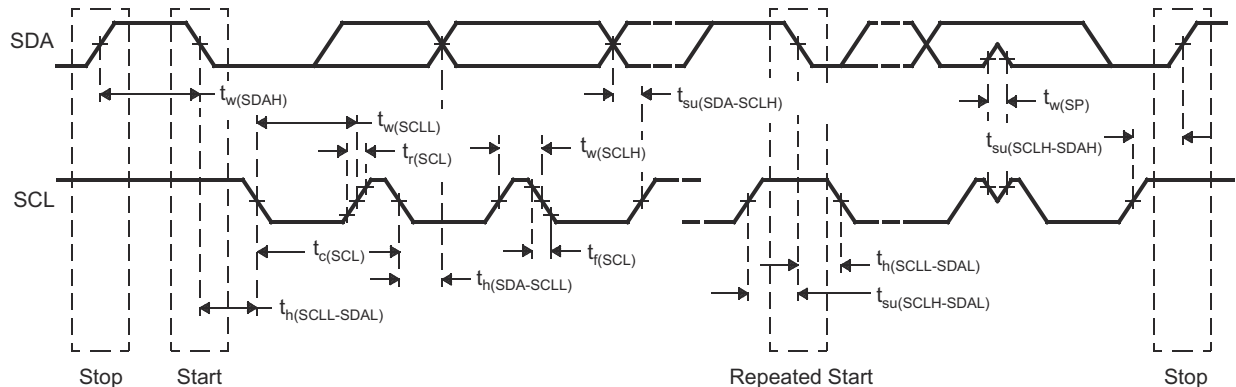


Figure 7-21. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, the device must output the next data bit to the SDA line $t_{rmax} + t_{su(SDA-SCLH)}$.

7.15.10 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a controller only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Section 7.15.10.2 and Section 7.15.10.3 assume the operating conditions stated in Section 7.15.10.1.

7.15.10.1 QSPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

7.15.10.2 Timing Requirements for QSPI Input (Read) Timings

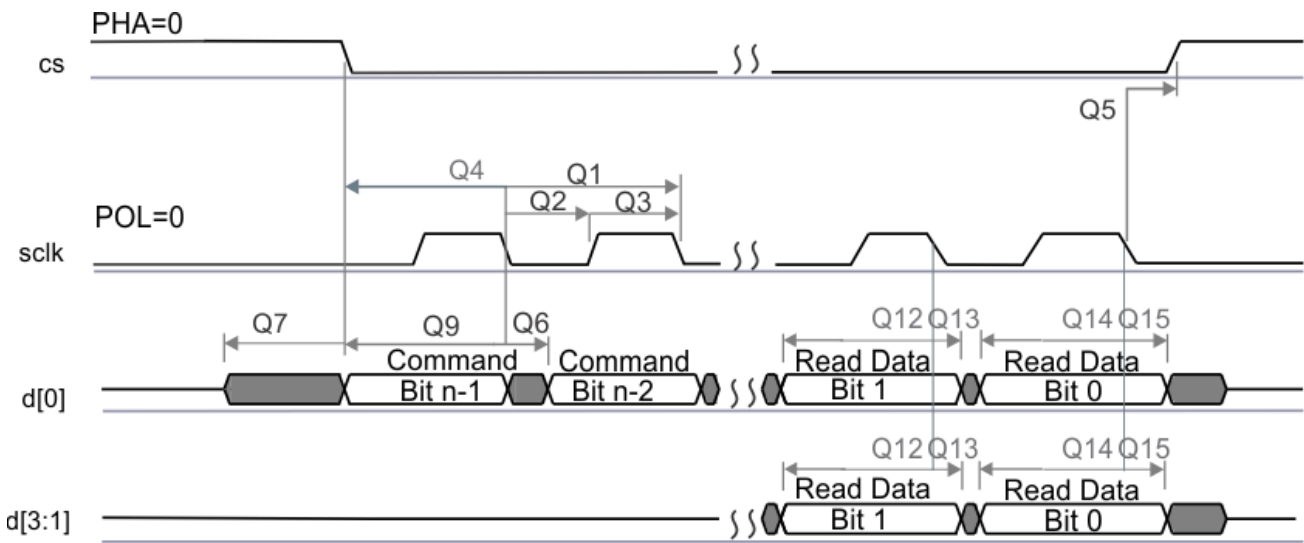
| | | MIN ^{(1) (2)} | TYP | MAX | UNIT |
|------------------|---|------------------------|-----|-----|------|
| $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge | 5 | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, d[3:0] valid after falling sclk edge | 1 | | | ns |
| $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | 5 – P ⁽³⁾ | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, final d[3:0] bit valid after final falling sclk edge | 1 + P ⁽³⁾ | | | ns |

- (1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
- (2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
- (3) P = SCLK period in ns.

7.15.10.3 QSPI Switching Characteristics

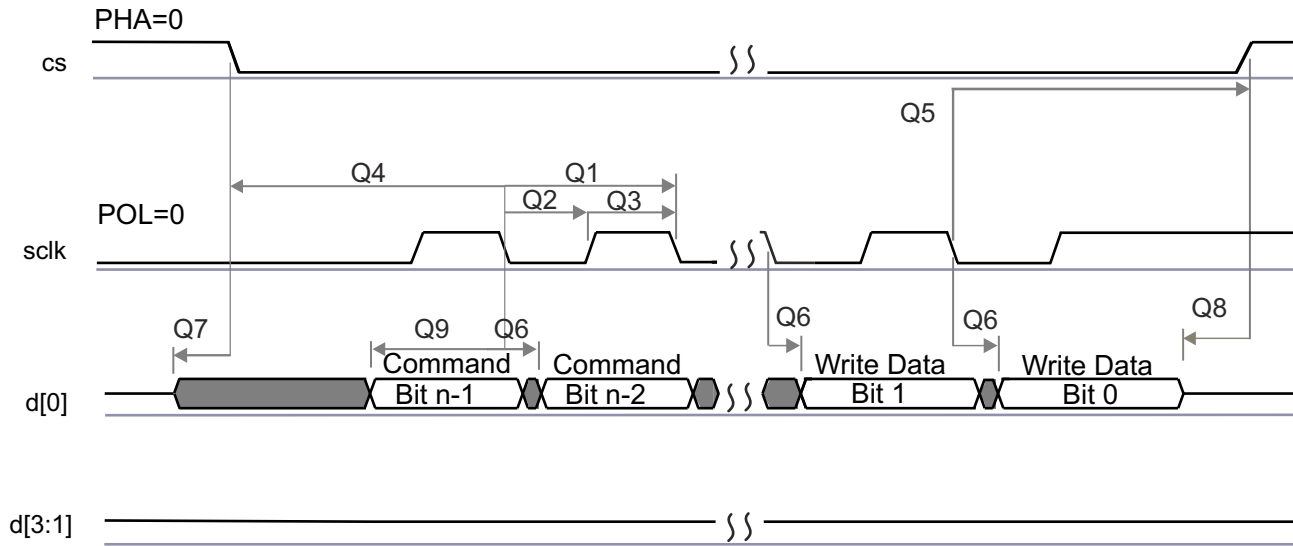
| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|----------------------------------|---|---------------------------|-----|-----------------------------|------|
| Q1 | $t_c(\text{SCLK})$ | Cycle time, sclk | 12.5 | | | ns |
| Q2 | $t_w(\text{SCLKL})$ | Pulse duration, sclk low | $Y \cdot P - 3^{(1)(2)}$ | | | ns |
| Q3 | $t_w(\text{SCLKH})$ | Pulse duration, sclk high | $Y \cdot P - 3^{(1)(2)}$ | | | ns |
| Q4 | $t_d(\text{CS-SCLK})$ | Delay time, sclk falling edge to cs active edge | $-M \cdot P - 1^{(2)(3)}$ | | $-M \cdot P + 2.5^{(2)(3)}$ | ns |
| Q5 | $t_d(\text{SCLK-CS})$ | Delay time, sclk falling edge to cs inactive edge | $N \cdot P - 1^{(2)(3)}$ | | $N \cdot P + 2.5^{(2)(3)}$ | ns |
| Q6 | $t_d(\text{SCLK-D1})$ | Delay time, sclk falling edge to d[1] transition | -2 | | 4 | ns |
| Q7 | $t_{\text{ena}}(\text{CS-D1LZ})$ | Enable time, cs active edge to d[1] driven (lo-z) | $-P - 4^{(2)}$ | | $-P + 1^{(2)}$ | ns |
| Q8 | $t_{\text{dis}}(\text{CS-D1Z})$ | Disable time, cs active edge to d[1] tri-stated (hi-z) | $-P - 4^{(2)}$ | | $-P + 1^{(2)}$ | ns |
| Q9 | $t_d(\text{SCLK-D1})$ | Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only) | $-2 - P^{(2)}$ | | $4 - P^{(2)}$ | ns |
| Q12 | $t_{\text{su}}(\text{D-SCLK})$ | Setup time, d[3:0] valid before falling sclk edge | 5 | | | ns |
| Q13 | $t_h(\text{SCLK-D})$ | Hold time, d[3:0] valid after falling sclk edge | 1 | | | ns |
| Q14 | $t_{\text{su}}(\text{D-SCLK})$ | Setup time, final d[3:0] bit valid before final falling sclk edge | $5 - P^{(2)}$ | | | ns |
| Q15 | $t_h(\text{SCLK-D})$ | Hold time, final d[3:0] bit valid after final falling sclk edge | $1 + P^{(2)}$ | | | ns |

- (1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
- (2) P = SCLK period in ns.
- (3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2



SPRS85v TIMING QSPI 02

Figure 7-22. QSPI Read (Clock Mode 0)



SPRS85v_TIMING_OSP11_04

Figure 7-23. QSPI Write (Clock Mode 0)

7.15.11 JTAG Interface

Section 7.15.11.2 and Section 7.15.11.3 assume the operating conditions stated in Section 7.15.11.1.

7.15.11.1 JTAG Timing Conditions

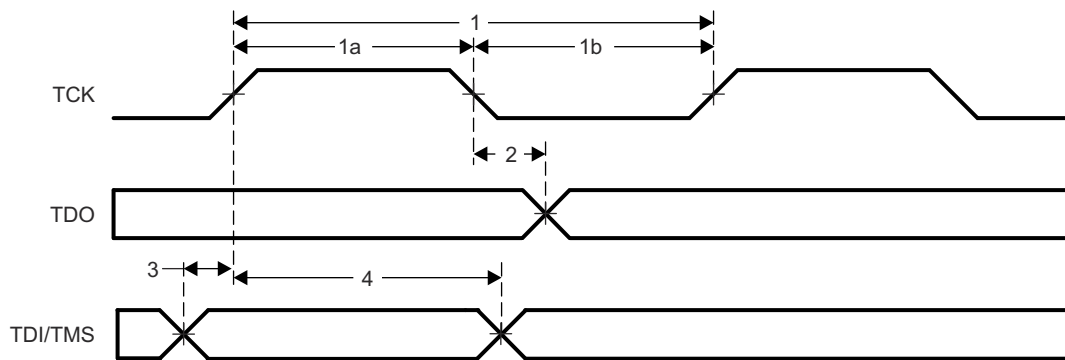
| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

7.15.11.2 Timing Requirements for IEEE 1149.1 JTAG

| NO. | PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----|-------------------|---|-------|-----|-----|------|
| 1 | $t_c(TCK)$ | Cycle time TCK | 66.66 | | | ns |
| 1a | $t_w(TCKH)$ | Pulse duration TCK high (40% of t_c) | 20 | | | ns |
| 1b | $t_w(TCKL)$ | Pulse duration TCK low(40% of t_c) | 20 | | | ns |
| 3 | $t_{su}(TDI-TCK)$ | Input setup time TDI valid to TCK high | 2.5 | | | ns |
| | $t_{su}(TMS-TCK)$ | Input setup time TMS valid to TCK high | 2.5 | | | ns |
| 4 | $t_h(TCK-TDI)$ | Input hold time TDI valid from TCK high | 18 | | | ns |
| | $t_h(TCK-TMS)$ | Input hold time TMS valid from TCK high | 18 | | | ns |

7.15.11.3 Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

| NO. | PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----|------------------|----------------------------------|-----|-----|-----|------|
| 2 | $t_d(TCKL-TDOV)$ | Delay time, TCK low to TDO valid | 0 | | 15 | ns |



SPRS91v_JTAG_01

Figure 7-24. JTAG Timing

8 Detailed Description

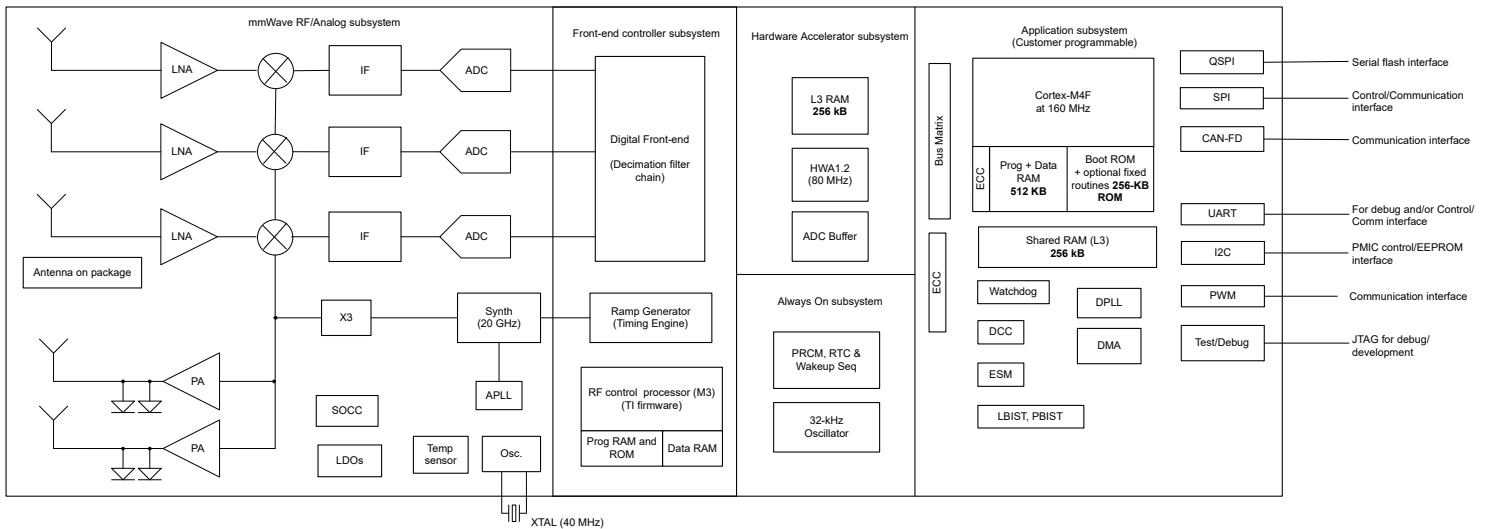
8.1 Overview

The IWRL6432AOP device is a complete SOC which include mmWave front end, customer programmable MCU and analog baseband signal chain for two transmitters and three receivers. This device is intended as a radar-on-a-chip in use-cases with quality provision for memory, processing capacity and application code size. Use-cases include cost-effective industrial radar sensing applications. Examples are:

- Industrial-level sensing
- Industrial automation sensor fusion with radar
- Traffic intersection monitoring with radar
- Industrial radar-proximity monitoring
- People counting
- Gesture detection

In terms of scalability, the IWRL6432AOP device can be paired with a low-end external MCU to address more complex applications that can require additional memory for a larger application software footprint and faster interfaces.

8.2 Functional Block Diagram



8.3 Subsystems

8.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The device supports only TDM (Time Division Multiplexed) mode but doesn't support simultaneous two TX operation. Similarly, the device allows configuring the number of receive channels based on application and power requirements. For system power saving, RF and analog subsystems can be put into low power mode configuration.

8.3.2 Clock Subsystem

The IWRL6432AOP clock subsystem generates 57 to 63.5GHz from an input reference from a crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X3 multiplier to create the required frequency in the 57 to 63.5GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

Figure 8-1 describes the clock subsystem.

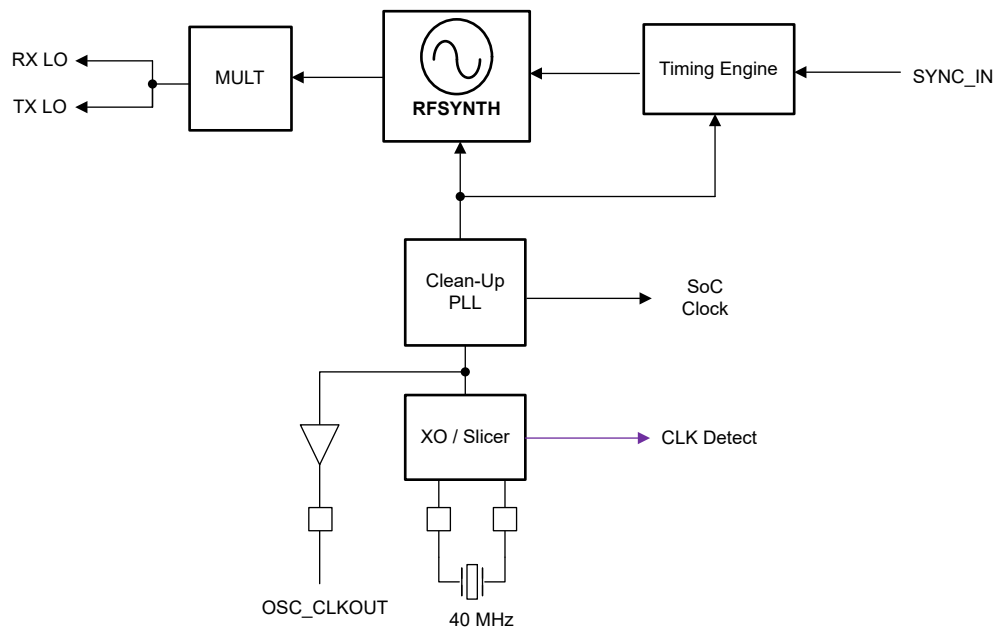


Figure 8-1. Clock Subsystem

8.3.3 Transmit Subsystem

The IWRL6432AOP transmit subsystem consists of two parallel transmit chains, each with independent phase and amplitude control.

The transmit chains also support programmable backoff for system optimization.

Figure 8-2 describes the transmit subsystem.

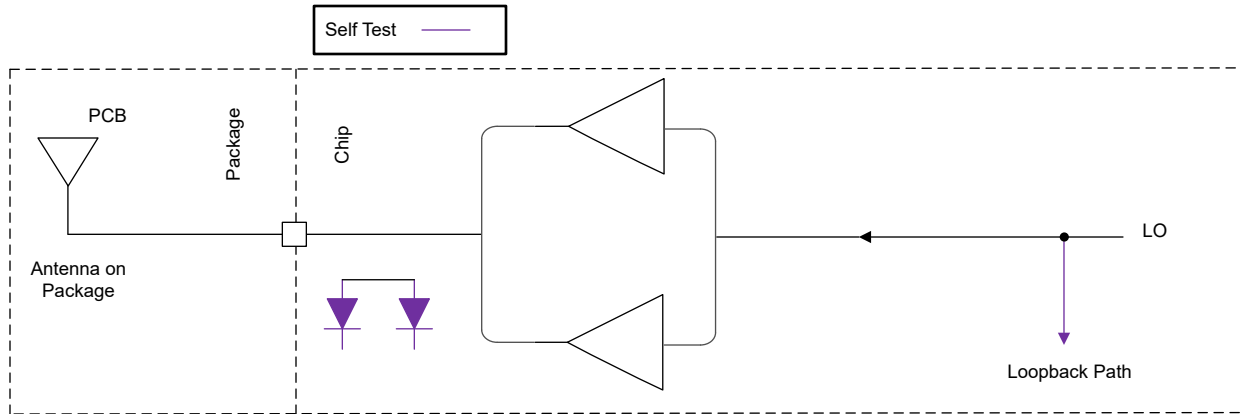


Figure 8-2. Transmit Subsystem (Per Channel)

8.3.4 Receive Subsystem

The IWRL6432AOP receive subsystem consists of three parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All three receive channels can either operate simultaneously OR can be powered down individually based on system power needs and application design.

The IWRL6432AOP device supports a real baseband architecture, which uses real mixer, single IF and ADC chains to provide output for each receiver channel. The device is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175kHz and can support bandwidths up to 5MHz.

Figure 8-3 describes the receive subsystem.

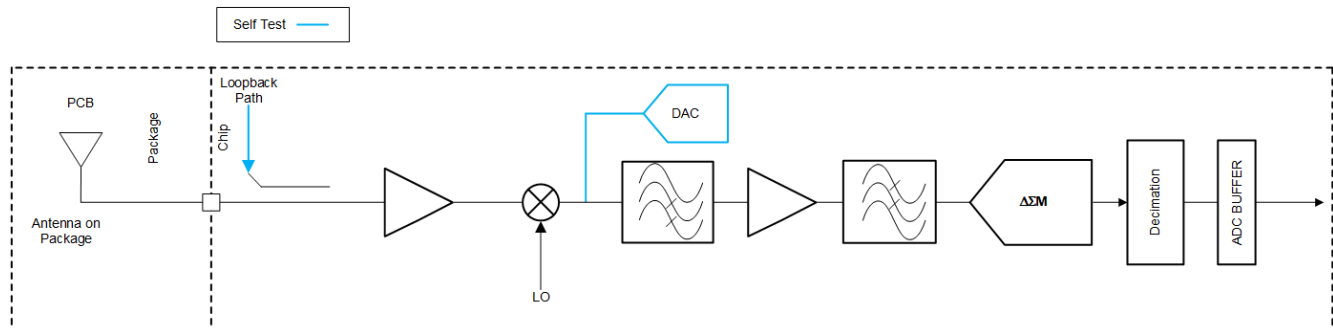


Figure 8-3. Receive Subsystem (Per Channel)

8.3.5 Processor Subsystem

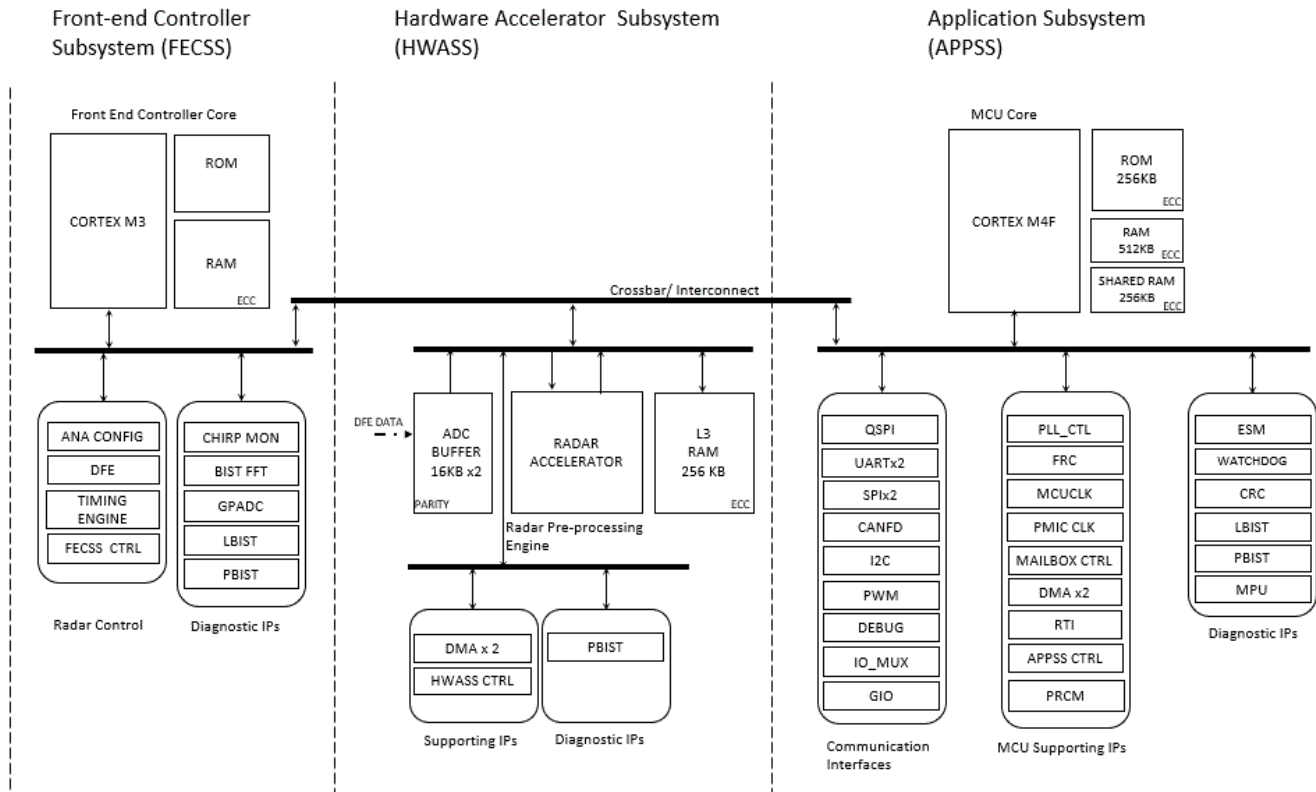


Figure 8-4. Processor Subsystem

Figure 8-4 shows the block diagram for customer programmable processor subsystems in the IWRL6432AOP device. At a high level there are two customer programmable subsystems, as shown separated by a dotted line in the diagram. The center panel shows the HWA, a high-bandwidth interconnect for high performance (64-bit, 80MHz), and associated peripherals data transfer. RDIF interface for Measurement data output, L3 Radar data cube memory, the ADC buffers, the CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Application Subsystem. The Application Subsystem is the brain of the device and controls all the device peripherals and house-keeping activities of the device. The Application Subsystem contains Cortex-M4F processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals (I²C, UART, SPIs, CAN, PMIC clocking module, PWM, and others) connected to Main Interconnect through Peripheral Central Resource (PCR interconnect).

8.3.6 Host Interface

The host interface can be provided through a SPI, UART, or CAN-FD interface. In some cases the serial interface for industrial applications is transcoded to a different serial standard.

The IWRL6432AOP device communicates with the host radar processor over the following control signals:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (peripheral) for host control . All radio control commands (and response) flow through this interface
- Reset – Active-low reset for device wakeup from host
- Host Interrupt - an indication that the mmWave sensor needs host interface
- Error – Used for notifying the host in case the radio controller detects a fault

8.3.7 Application Subsystem Cortex-M4F

The application system includes an ARM Cortex M4F processor clocked with a maximum operating frequency of 160MHz. User applications executing on this processor control the overall operation of the device, including radar control through well-defined API messages, radar signal processing (assisted by the radar hardware accelerator), and peripherals for external interfaces.

See the [Technical Reference Manual](#) for a complete description and memory map.

8.3.8 Hardware Accelerator (HWA1.2) Features

- Fast FFT computation, with programmable 2^N sizes, up to 1024-point complex FFT
- Internal FFT bit-width of 24 bits (each for I and Q) for good Signal-to-Quantization-Noise Ratio (SQNR) performance
- Fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for pre-FFT processing – Ex: DC estimation and subtraction
- DC estimation & subtraction, Interference estimation & zero-out, Real window, Complex pre-multiplication
- Magnitude (absolute value) and Log-magnitude computation
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses
- Chaining and looping mechanism to sequence a set of operations one after another with minimal intervention from the main processor
- Peak detection – CFAR (CFAR-CA, CFAR-OS) detector
- Basic statistics, including Sum and 1D Max
- Compression engine for radar cube memory optimization

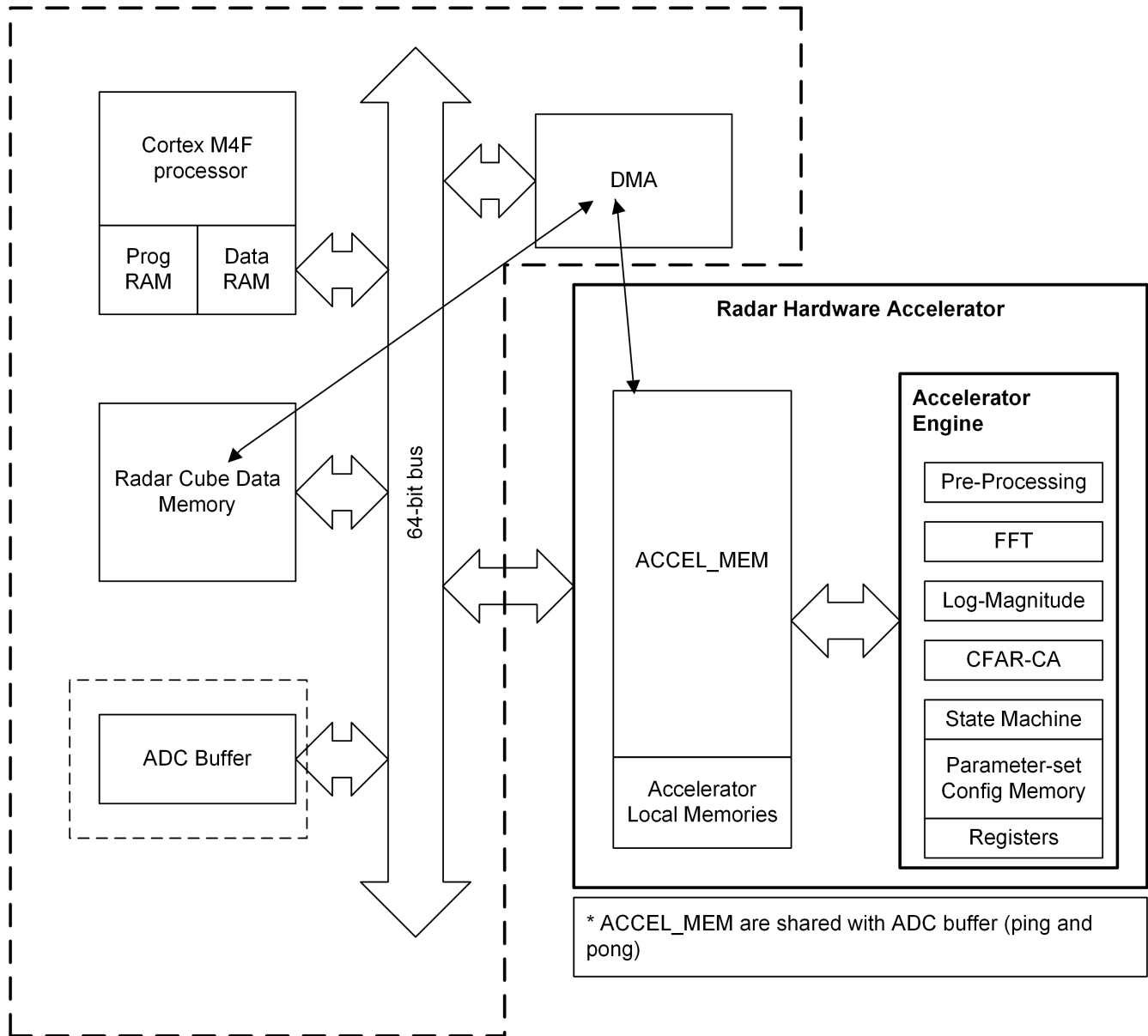


Figure 8-5. HWA 1.2 Functional Block Diagram

8.3.8.1 Hardware Accelerator Feature Differences Between HWA1.1 and HWA1.2

| Feature | HWA1.0, HWA1.1 (xWR1843, xWR6843) | HWA1.2 (xWRL6432, xWRL1432) |
|---|-----------------------------------|--|
| FFT features | FFT sizes | 1024, 512, 256, ... |
| | Internal bit-width | 24-bit I, 24-bit Q |
| | | Configurable butterfly scaling at each stage |
| | FFT stitching | up to 4096 point |
| FFT benchmark for four 256-pt FFTs | | 1312 clock cycles (6.56 μs at 200MHz) |
| No. of parameter-sets | | 16 |
| Local memory | | 64KB |

| Feature | HWA1.0, HWA1.1 (xWR1843, xWR6843) | HWA1.2 (xWRL6432, xWRL1432) |
|--|--|---|
| Input and Output formatter | <ul style="list-style-type: none"> A and B-dim addressing of local memory Programmable scaling | <ul style="list-style-type: none"> A and B-dim addressing of local memory Programmable scaling |
| Pre-FFT processing | <ul style="list-style-type: none"> Interference zero out with fixed threshold, based on magnitude Complex multiplication (7 modes) Real window coefficients | <ul style="list-style-type: none"> DC estimation and subtraction Interference zero out with adaptive statistics, based on mag, mag-diff. Interference count indication. Complex multiplication (7 modes) Real window coefficients |
| Post-FFT processing | Log-magnitude (0.3dB accuracy) | Log-magnitude (0.06dB accuracy) |
| Compression and De-compression support | Not available in HWA1.0 (xWR1843), Available in HWA1.1 (xWR6843) | Available |
| Detection | CFAR-CA (linear and log modes) | <ul style="list-style-type: none"> CFAR-CA (linear and log modes) CFAR-OS (window size up to 32 on each side) |
| Statistics | 1D Sum, 1D Max | 1D Sum, 1D Max |

8.4 Other Subsystems

8.4.1 GPADC Channels (Service) for User Application

The IWRL6432AOP device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to two external voltages. The GPADC1 is used for this purpose.

- GPADC is controlled by TI firmware running inside the FEC sub-system and access for customer's external voltage monitoring purpose is via 'APPSS' calls routed to the FEC subsystem. This API can be linked with the user application running on APPSS Cortex M4F®.
- Device Firmware package (DFP) provides APIs to configure and measure these signals. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings is reported for each of the monitored voltages.

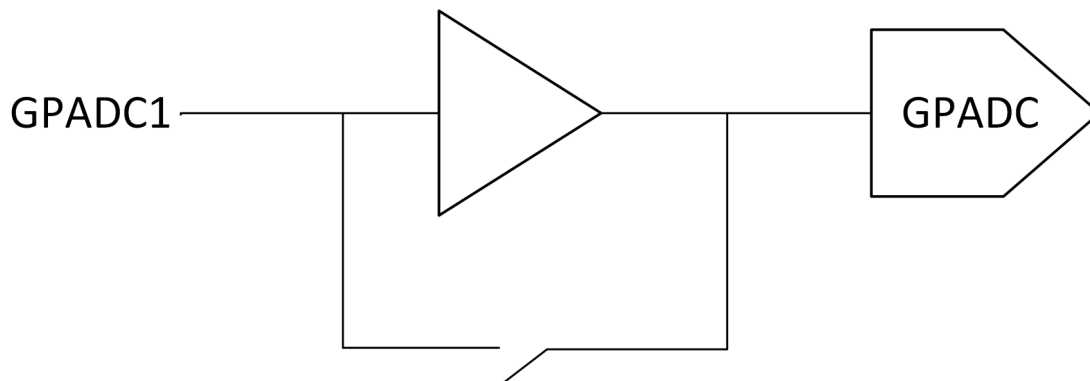


Figure 8-6. GPADC Path

GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is $\pm 7^{\circ}\text{C}$.

8.4.2 GPADC Parameters

| PARAMETER | TYP | UNIT |
|---|-----------|------|
| ADC supply | 1.8 | V |
| ADC unbuffered input voltage range | 0 – 1.8 | V |
| ADC buffered input voltage range ⁽¹⁾ | 0.4 – 1.3 | V |
| ADC resolution | 8 | bits |
| ADC offset error | ± 5 | LSB |
| ADC gain error | ± 5 | LSB |
| ADC DNL | -1/+2.5 | LSB |
| ADC INL | ± 2.5 | LSB |
| ADC sample rate ⁽²⁾ | 831 | Ksps |
| ADC sampling time ⁽²⁾ | 300 | ns |
| ADC internal cap | 10 | pF |
| ADC buffer input capacitance | 2 | pF |
| ADC input leakage current | 3 | uA |

(1) Outside of given range, the buffer output will become nonlinear.

(2) GPADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

8.5 Memory Partitioning Options

IWRL6432AOP devices will have a total memory of 1MB. The L3 memory has two memory banks and can be associated with radar cube memory or with the Cortex-M4F RAM. Please refer to the 'APPSS Memory Organization' section of the [xWRLx432 Technical Reference Manual](#) regarding the memory organization for the CPU subsystems in APPSS.

Table 8-1. Memory Partition Options

| | | Config 1 | Config 2 | Config 3 |
|----------------------------------|---|----------|----------|----------|
| Radar data memory* (L3) | Includes data cube, detection matrix, heatmap | 256KB | 384kB | 512KB |
| Application (M4F program + data) | Includes drivers, mmWavelink, BIOS | 768KB | 640KB | 512KB |
| Total memory | | 1024KB | 1024KB | 1024KB |

The entire RAM is retainable. Additionally, each memory cluster can be independently turned off (if needed). The clusters are defined as below

Table 8-2. Memory Retention Options

| RAM_1 | | | RAM_2 | | RAM_3 | Shared | HWA |
|------------------------|------------|------------|------------|------------|---------|------------|-------|
| 256KB | | | 128KB | | 128KB | 256KB | 256KB |
| BANK #1 ⁽¹⁾ | | | BANK #2 | | BANK #3 | | |
| Cluster #1 | Cluster #3 | Cluster #4 | Cluster #2 | Cluster #5 | | Cluster #6 | |
| 64kB | 64KB | 128KB | 16KB | 112KB | 128KB | 256KB | 256KB |

(1) Retention memories have power switches. These Banks represent memory configurations.

8.6 Boot Modes

As soon as device reset is de-asserted, the processor of the APPSS starts executing its bootloader from an on-chip ROM memory.

The bootloader operates in three basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as "Sense on power" (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

[Table 8-3](#) enumerates the relevant SOP combinations and how these map to bootloader operation.

Table 8-3. SOP Combinations

| SOP1 | SOP0 | BOOTLOADER MODE AND OPERATION |
|------|------|--|
| 0 | 0 | Flashing Mode Device Bootloader spins in loop to allow flashing of user application (or device firmware patch - Supplied by TI) to the serial flash. |
| 0 | 1 | Functional Mode Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it. |
| 1 | 1 | Debug Mode Bootloader is bypassed and M4F processor is halted. This allows user to connect emulator at a known point. |

9 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Application information can be found on [IWR Application web page](#).

9.2 Reference Schematic

Please check the device product page for latest Hardware design information under Design Kits - typically, at Design and Development

Listed for convenience are: Design Files, Schematics, Layouts, and Stack up for PCB

- [Altium IWR6432AOP EVM Design Files](#)
- [IWR6432AOP EVM Schematic Drawing, Assembly Drawing, and Bill of Materials](#)

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are in the following sections.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *IWRL6432AOP*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, AMY0101), the temperature range (for example, blank is the default commercial temperature range). [Figure 10-1](#) provides a legend for reading the complete device name for any *IWRL6432AOP* device.

For orderable part numbers of *IWRL6432AOP* devices in the AMY0101 package types, see the Package Option Addendum of this document (when available), the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [IWRL6432AOP Device Errata](#).

IWRL6432AOP

SWRS323B – APRIL 2024 – REVISED AUGUST 2025

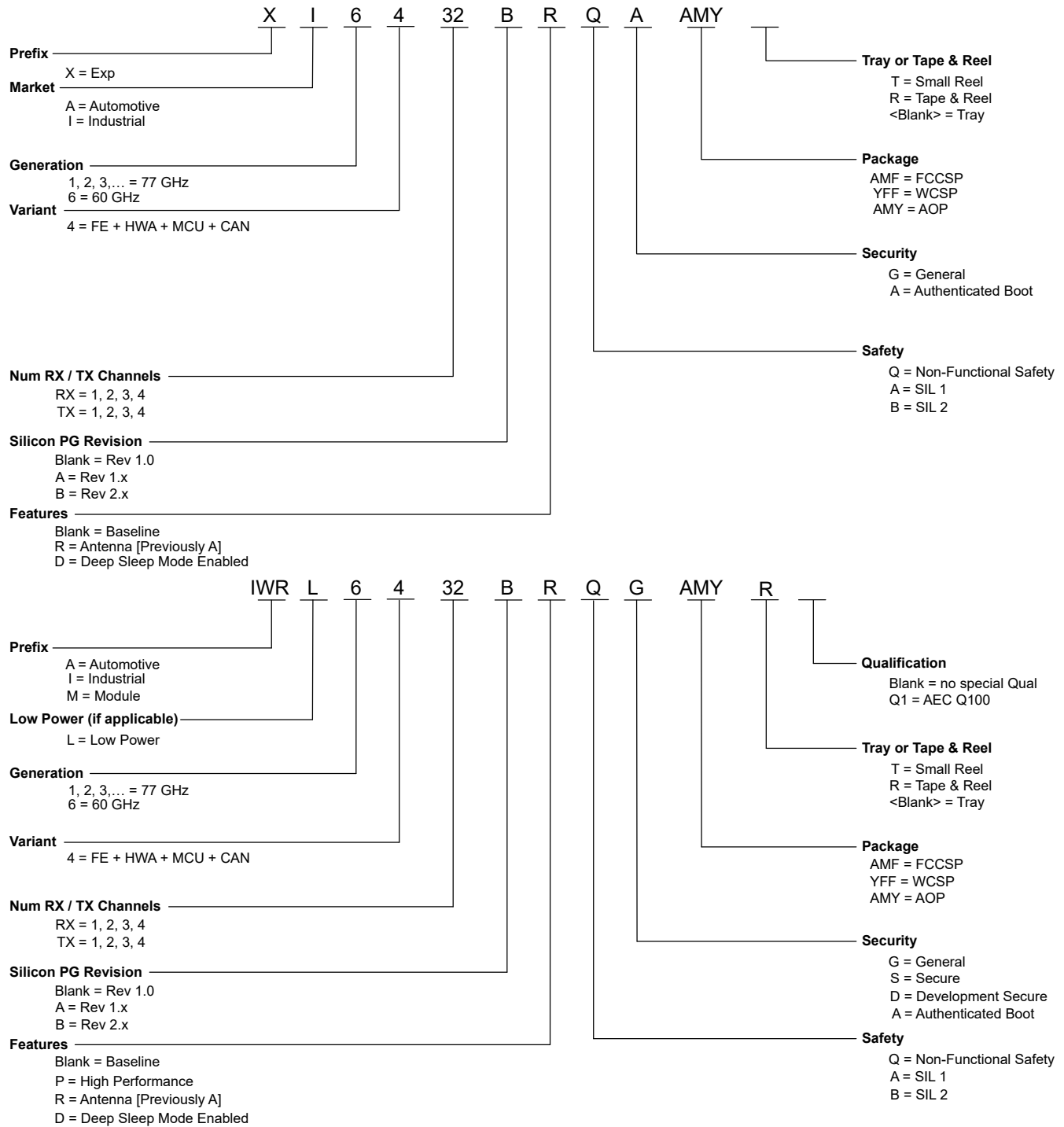


Figure 10-1. Device Nomenclature

10.2 Tools and Software

Models

[IWRL6432AOP BSDL model](#)

Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

[IWRL6432AOP IBIS model](#)

IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the peripherals, and other technical collateral follows.

Errata

- [IWRL6432AOP device errata](#)

Describes known advisories, limitations, and cautions on silicon and provides workarounds.

10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help—straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.5 Trademarks

E2E™ is a trademark of Texas Instruments.

Arm®, M4F®, and Cortex M4F® are registered trademarks of Arm Limited.

All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

| | |
|-----------------------------|--|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |
|-----------------------------|--|

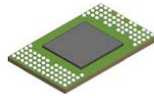
11 Revision History

Changes from April 26, 2025 to July 25, 2025 (from Revision A (April 2025) to Revision B (July 2025))

| | Page |
|---|-------------|
| • (Features) : Updated max frequency to 63.5GHz..... | 1 |
| • (Description) : Updated max frequency to 63.5GHz..... | 2 |
| • (Device feature comparison) : Updated max frequency to 63.5GHz..... | 6 |
| • (Device feature comparison) : Production status changed from AI to PD..... | 6 |
| • (Related Products) : Updated max frequency to 63.5GHz..... | 8 |
| • (Recommended Operating Conditions for OTP eFuse Programming): Added decoupling capacitor recommendation for BOM optimized mode..... | 22 |
| • (RF Specification) : Updated max frequency to 63.5GHz..... | 32 |
| • (Antenna Radiation Patterns) : Note updated for longer PCB edge..... | 33 |
| • (Antenna Radiation Patterns) : Antenna Radiation pattern updated to reflect maximum frequency of 63.5GHz..... | 33 |
| • (Antenna Positions): Updated antenna placement and relative spacing..... | 37 |
| • (Timing and Switching Requirements for SPI - Controller Mode): Note updated for McSPI supported frequency..... | 41 |
| • (Clock Subsystem) : Updated max frequency to 63.5GHz..... | 58 |
| • (Memory Partitioning Options) : Updated with reference to TRM for the CPU subsystems in APPSS..... | 64 |

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation

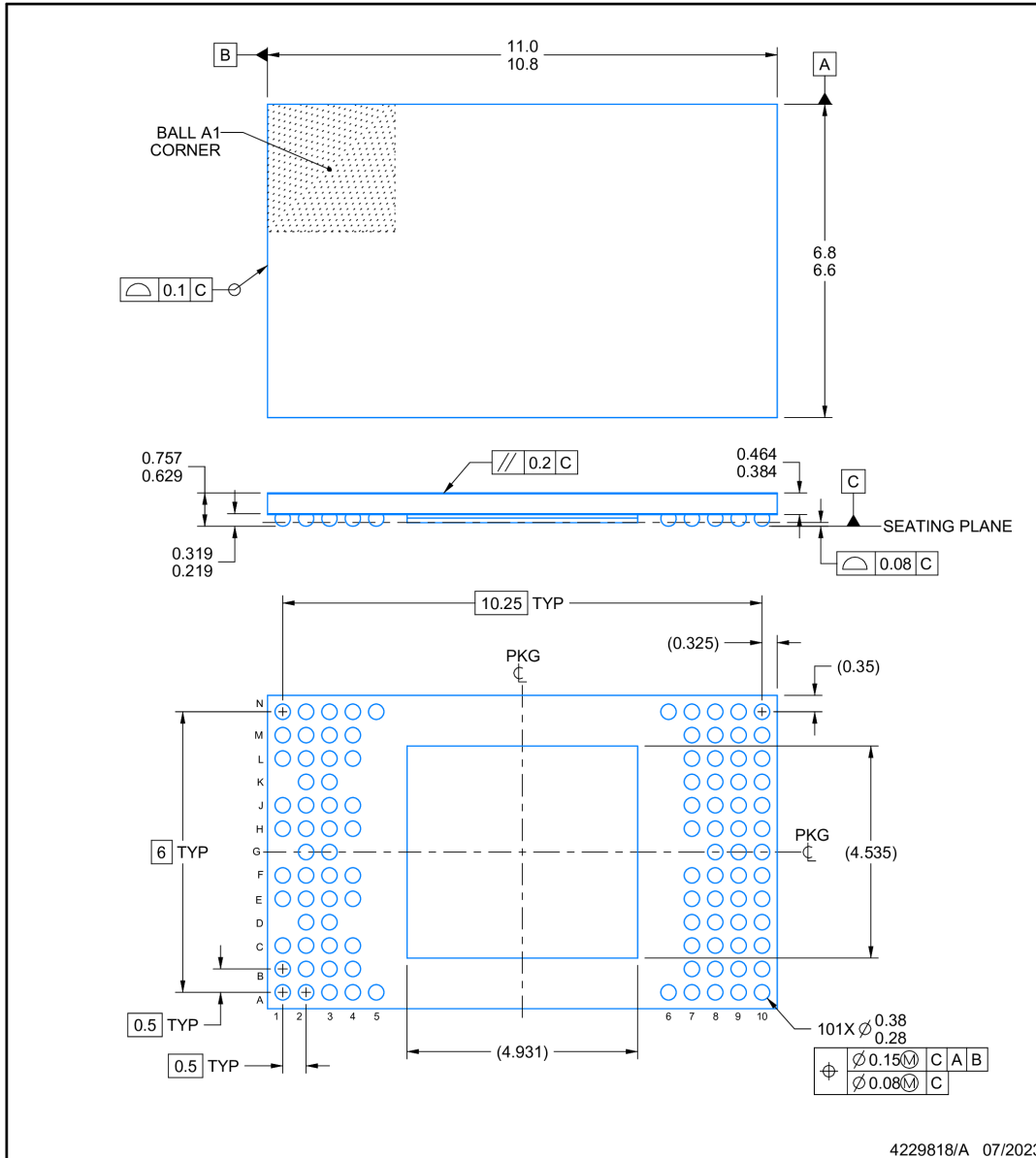


AMY0101A

PACKAGE OUTLINE

FCCSP - 0.757 mm max height

FLIP CHIP CHIP SCALE PACKAGE



NOTES:

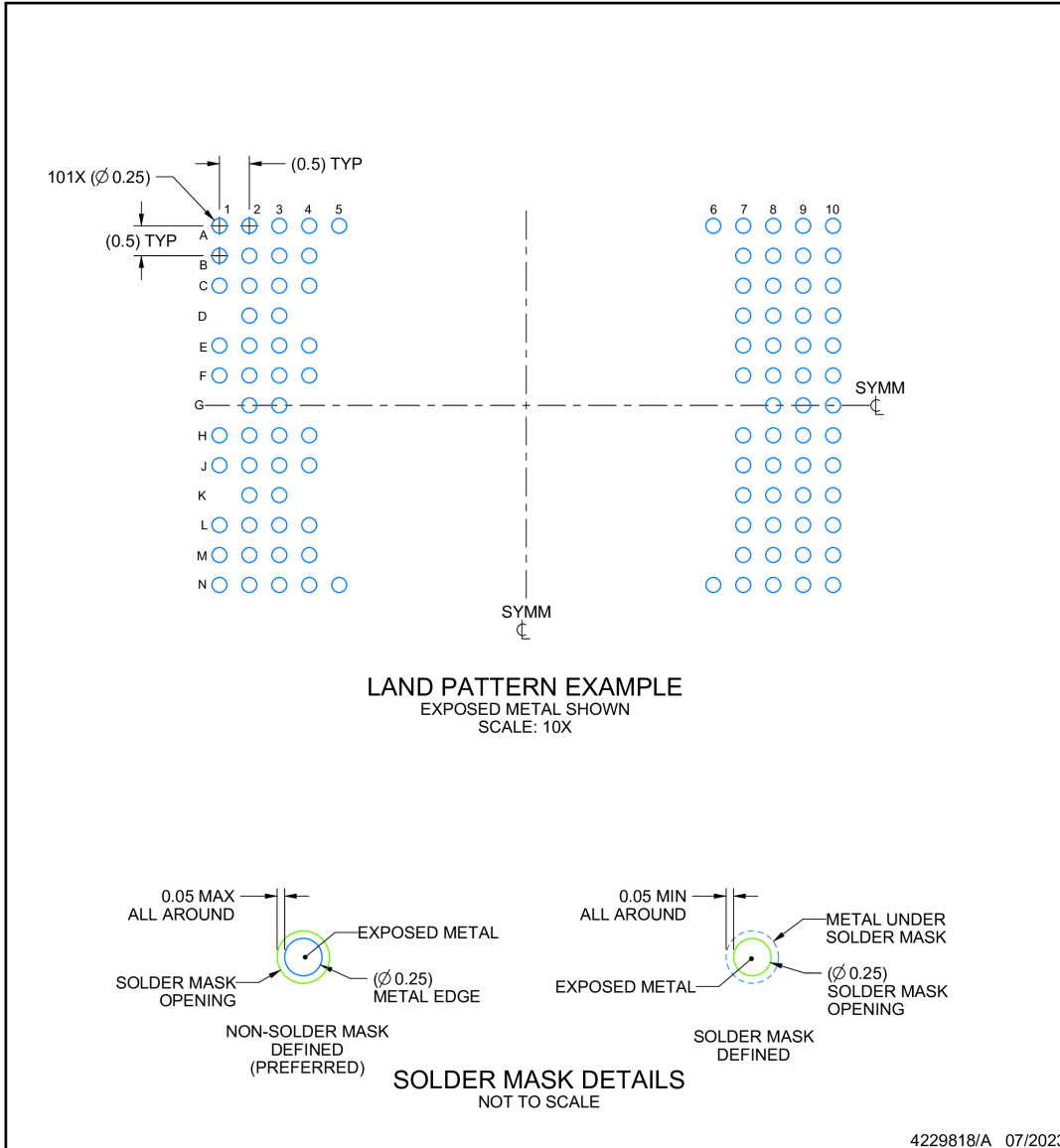
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

AMY0101A

FCCSP - 0.757 mm max height

FLIP CHIP CHIP SCALE PACKAGE



NOTES: (continued)

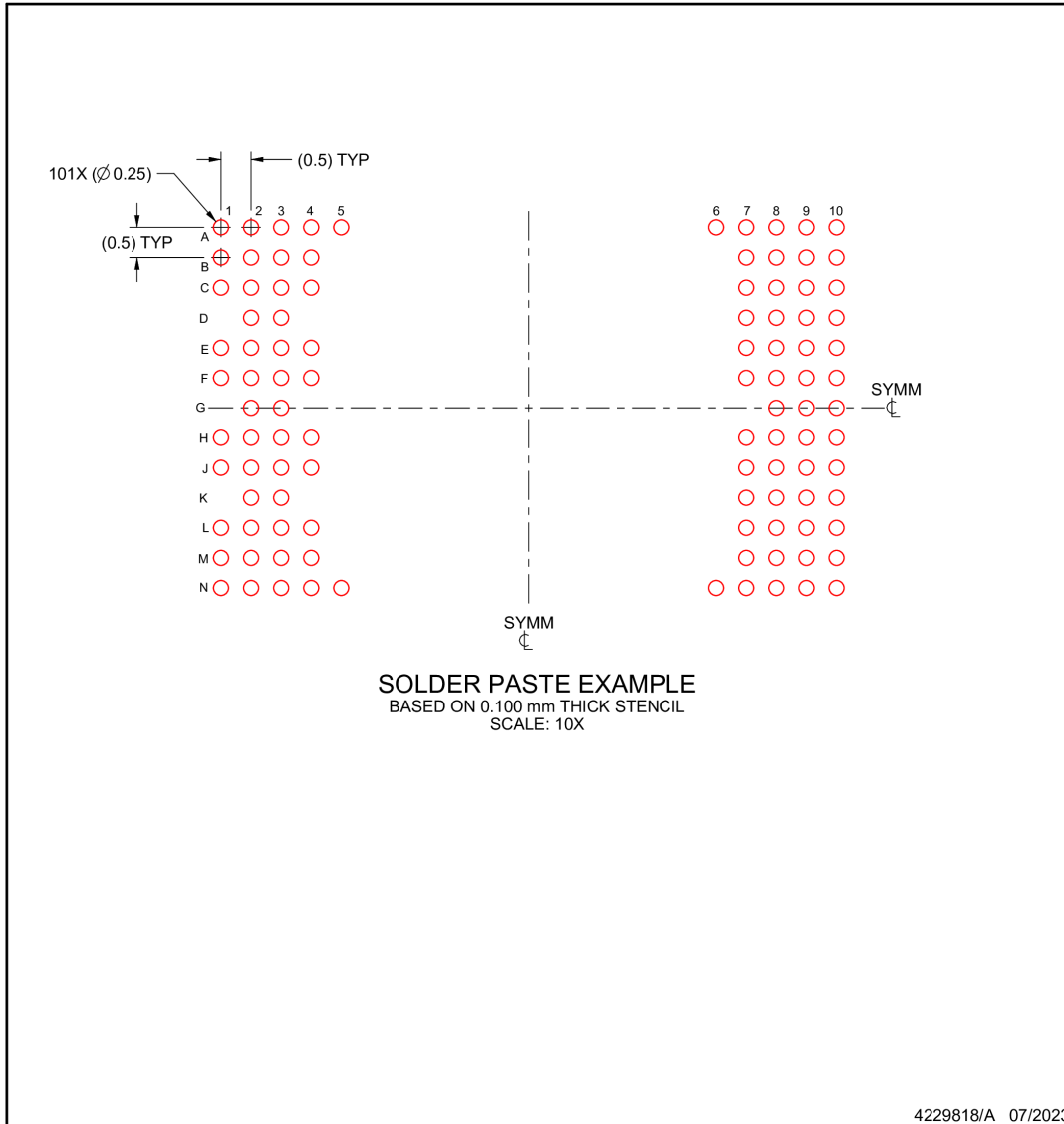
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

AMY0101A

FCCSP - 0.757 mm max height

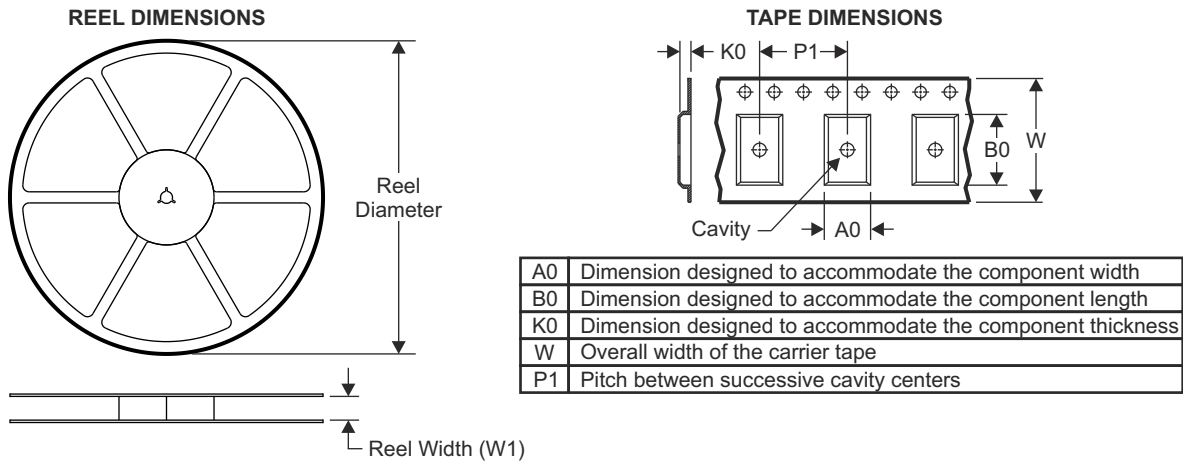
FLIP CHIP CHIP SCALE PACKAGE



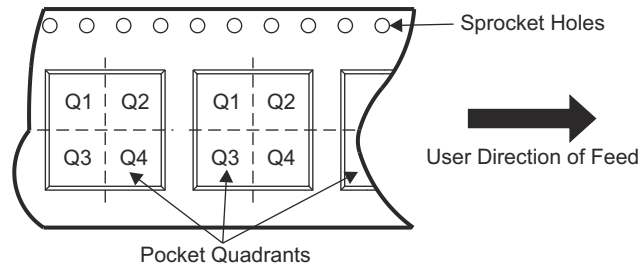
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

12.1 Tape and Reel Information

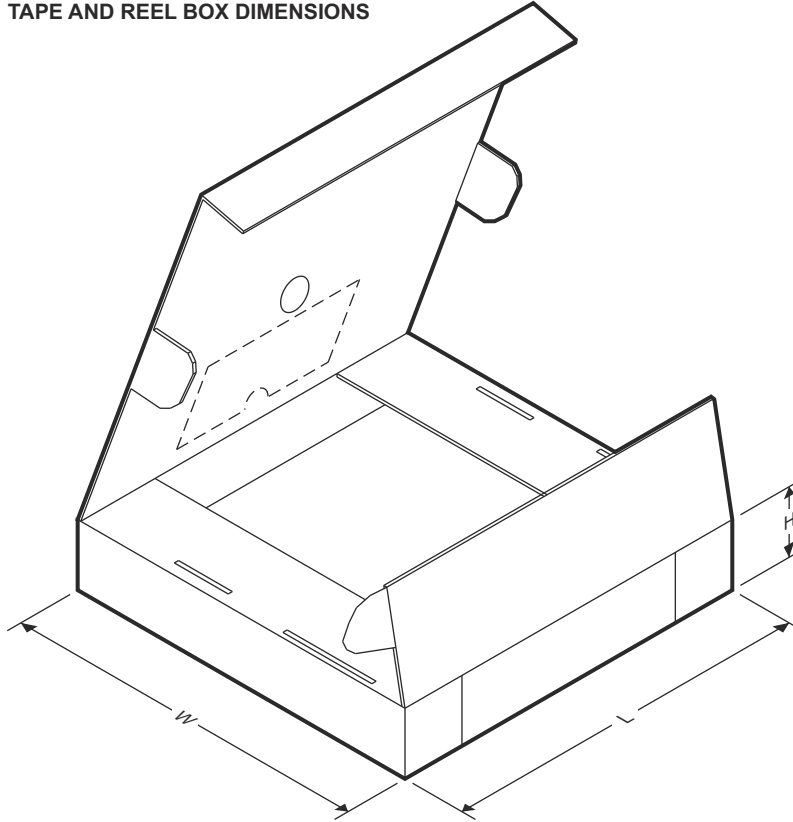


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| IWRL6432BRQGAMYR | FCCSP | AMY | 101 | 1000 | 330 | 24.4 | 7.25 | 11.25 | 1.0 | 12 | 24 | Q2 |
| IWRL6432BRQAAMYR | FCCSP | AMY | 101 | 1000 | 330 | 24.4 | 7.25 | 11.25 | 1.0 | 12 | 24 | Q2 |

TAPE AND REEL BOX DIMENSIONS



| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| IWRL6432BRQGAMYR | FCCSP | AMY | 101 | 1000 | 315 | 135.9 | 7.62 |
| IWRL6432BRQAAMYR | FCCSP | AMY | 101 | 1000 | 315 | 135.9 | 7.62 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|-------------------|------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| IWR6432BRQAAMY | Active | Production | FCCSP (AMY) 101 | 208 JEDEC TRAY (5+1) | Yes | SNAGCUBI | Level-3-260C-168 HR | -40 to 105 | IWR6432 QA |
| IWR6432BRQAAMYR | Active | Production | FCCSP (AMY) 101 | 1000 LARGE T&R | Yes | SNAGCUBI | Level-3-260C-168 HR | -40 to 105 | IWR6432 QA |
| IWR6432BRQGAMYR | Active | Production | FCCSP (AMY) 101 | 1000 LARGE T&R | Yes | SNAGCUBI | Level-3-260C-168 HR | -40 to 105 | IWR6432 QG |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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