LM25576-Q1 42V, 3A Step-Down Switching Regulator

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
- Integrated 42V, 170mΩ N-channel MOSFET
- Ultra-wide input voltage range from 6V to 42V
- Adjustable output voltage as low as 1.225V
- 1.5% feedback reference accuracy
- Operating frequency adjustable between 50kHz and 1MHz with single resistor
- Controller or peripheral frequency synchronization
- Adjustable soft-start
- Emulated current mode control architecture
- Wide bandwidth error amplifier
- Built-in protection
- HTSSOP-20 EP (exposed pad)
- Create a custom design using the LM25576-Q1 with the WEBENCH® Power Designer

2 Applications

- Automotive

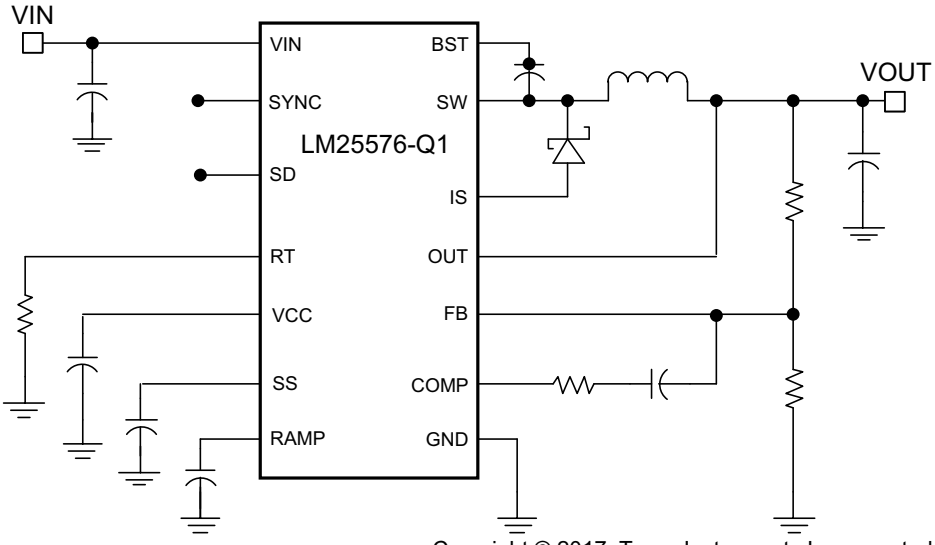
3 Description

The LM25576-Q1 is an easy-to-use buck regulator which allows users to design and optimize a robust power supply using a minimum set of components. Operating with an input voltage range of 6V to 42V, the LM25576-Q1 delivers 3A of continuous output current with an integrated 170mΩ N-Channel MOSFET. The regulator uses an Emulated Current Mode architecture which provides inherent line regulation, tight load transient response, and ease of loop compensation without the usual limitation of low-duty cycles associated with current mode regulators. The operating frequency is adjustable from 50kHz to 1MHz to allow optimization of size and efficiency. To reduce EMI, a frequency synchronization pin allows multiple ICs from the LM(2)557x family to self-synchronize or to synchronize to an external clock. The LM25576-Q1 establishes robustness with a cycle-by-cycle current limit, short-circuit protection, thermal shut-down, and remote shut-down. The device is available in a power enhanced HTSSOP-20 package featuring an exposed die attach pad for thermal dissipation. The LM25576-Q1 is supported by the full suite of WEBENCH® On-Line design tools.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM25576-Q1	PWP (HTSSOP, 20)	6.50mm × 4.40mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Schematic

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4 Pin Configuration and Functions

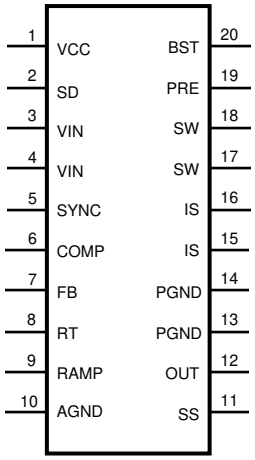


Figure 4-1. LM25576-Q1 PWP 20-HTSSOP (Top View)

Table 4-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	10	Analog ground Internal reference for the regulator control functions
BST	20	Boost input for bootstrap capacitor An external capacitor is required between the BST and the SW pins. A 0.022 µF ceramic capacitor is recommended. The capacitor is charged from V_{CC} via an internal diode during the off-time of the buck switch.
COMP	6	Output of the internal error amplifier The loop compensation network should be connected between this pin and the FB pin.
EP	NA	Exposed Pad Exposed metal pad on the underside of the device. It is recommended to connect this pad to the PWB ground plane, in order to aid in heat dissipation.
FB	7	Feedback signal from the regulated output This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.225V.
IS	15, 16	Current sense Current measurement connection for the re-circulating diode. An internal sense resistor and a sample/hold circuit sense the diode current near the conclusion of the off-time. This current measurement provides the DC level of the emulated current ramp.
OUT	12	Output voltage connection Connect directly to the regulated output voltage.
PGND	13, 14	Power ground Low side reference for the PRE switch and the IS sense resistor.
PRE	19	Pre-charge assist for the bootstrap capacitor This open drain output can be connected to SW pin to aid charging the bootstrap capacitor during very light load conditions or in applications where the output may be pre-charged before the LM25576-Q1 is enabled. An internal pre-charge MOSFET is turned on for 265ns each cycle just prior to the on-time interval of the buck switch.
RAMP	9	Ramp control signal An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control. Recommended capacitor range 50pF to 2000pF.
RT	8	Internal oscillator frequency set input The internal oscillator is set with a single resistor, connected between this pin and the AGND pin.

Table 4-1. Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
SD	2	Shutdown or UVLO input If the SD pin voltage is below 0.7V the regulator will be in a low power state. If the SD pin voltage is between 0.7V and 1.225V the regulator will be in standby mode. If the SD pin voltage is above 1.225V the regulator will be operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the SD pin is left open circuit, a 5 µA pull-up current source configures the regulator fully operational.
SS	11	Soft-start An external capacitor and an internal 10 µA current source set the time constant for the rise of the error amp reference. The SS pin is held low during standby, V_{CC} UVLO and thermal shutdown.
SW	17, 18	Switching node The source terminal of the internal buck switch. The SW pin should be connected to the external Schottky diode and to the buck inductor.
SYNC	5	Oscillator synchronization input or output The internal oscillator can be synchronized to an external clock with an external pull-down device. Multiple LM25576-Q1 devices can be synchronized together by connection of their SYNC pins.
VCC	1	Output of the bias regulator V_{CC} tracks V_{IN} up to 9V. Beyond 9V, V_{CC} is regulated to 7 Volts. A 0.1uF to 1uF ceramic decoupling capacitor is required. An external voltage (7.5V – 14V) can be applied to this pin to reduce internal power dissipation.
VIN	3, 4	Input supply voltage Nominal operating range: 6V to 42V

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
	V_{IN} to GND		45	V
	BST to GND		60	V
	PRE to GND		45	V
	SW to GND (Steady State)		–1.5	V
	BST to V_{CC}		45	V
	SD, V_{CC} to GND		14	V
	BST to SW		14	V
	OUT to GND	Limited	Vin	V
	SYNC, SS, FB, RAMP to GND		7	V
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)	±2	kV
		Charged-device model (CDM), per JEDEC specification JESD22- C101(3)	±500	V

(1) The human-body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

(1)		MIN	NOM	MAX	UNIT
V_{IN}		6		42	V
T_J	Operation junction temperature	–40		125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Section 5.5.

5.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		LM25576-Q1 PWP (HTSSOP) 20 pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W

5.4 Thermal Resistance Characteristics (continued)

THERMAL METRIC[1]		LM25576-Q1 PWP (HTSSOP) 20 pins	UNIT
ψ JB	Junction-to-board characterization parameter	14.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

Typical values correspond to T_J = 25°C, V_{IN} = 24V, R_T = 32.4kΩ. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
V_{CC} Reg	V_{CC} Regulator Output		6.85	7.15	7.45	V
	V_{CC} LDO Mode turn-off			9		V
	V_{CC} Current Limit	V_{CC} = 0V		25		mA
VCC SUPPLY						
	V_{CC} UVLO Threshold	VCC Increasing	5.03	5.35	5.67	V
	V_{CC} Undervoltage Hysteresis			0.25		V
	Bias Current (Iin)	FB = 1.3V.		2	4.5	mA
	Shutdown Current (Iin)	SD = 0V.		48	85	µA
SHUTDOWN THRESHOLDS						
	Shutdown Threshold		0.47	0.7	0.9	V
	Shutdown Hysteresis			0.1		V
	Standby Threshold		1.17	1.225	1.28	V
	Standby Hysteresis			0.1		V
	SD Pull-up Current Source			5		µA
SWITCH CHARACTERISTICS						
	Buck Switch Rds(on)			170	340	mΩ
	BOOST UVLO			3.8		V
	BOOST UVLO Hysteresis			0.8		V
	Pre-charge Switch Rds(on)			70		Ω
	Pre-charge Switch on-time			265		ns
CURRENT LIMIT						
	Cycle by Cycle Current Limit Delay	RAMP = 2.5V.		75		ns
SOFT-START						
	SS Current Source		7	10	14	µA
OSCILLATOR						
	Frequency1		180	200	220	kHz
	Frequency2	R_T = 11kΩ.	425	485	545	kHz
	SYNC Source Impedance			11		kΩ
	SYNC Sink Impedance			110		Ω
	SYNC Threshold (falling)			1.4		V
	SYNC Frequency	R_T = 11kΩ.	550			kHz
	SYNC Pulse Width Minimum		15			ns
RAMP GENERATOR						
	Ramp Current 1	V_{IN} = 36V, V_{OUT} = 10V.	136	160	184	µA
	Ramp Current 2	V_{IN} = 10V, V_{OUT} = 10V.	18	25	32	µA
PWM COMPARATOR						
	Forced Off-time		416	500	575	ns

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C, V_{IN} = 24V, R_T = 32.4kΩ. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Min On-time			80		ns
	COMP to PWM Comparator Offset			0.7		V
ERROR AMPLIFIER						
	Feedback Voltage	Vfb = COMP.	1.207	1.225	1.243	µV
	FB Bias Current			10		nA
	DC Gain			70		dB
	COMP Sink / Source Current		3			mA
	Unity Gain Bandwidth			3		MHz
DIODE SENSE RESISTANCE						
	D_{SENSE}			42		mΩ
THERMAL SHUTDOWN						
Tsd	Thermal Shutdown Threshold (1)			165		°C
Tsd_hys	Thermal Shutdown hysteresis (1)			25		°C

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).

5.6 Typical Characteristics

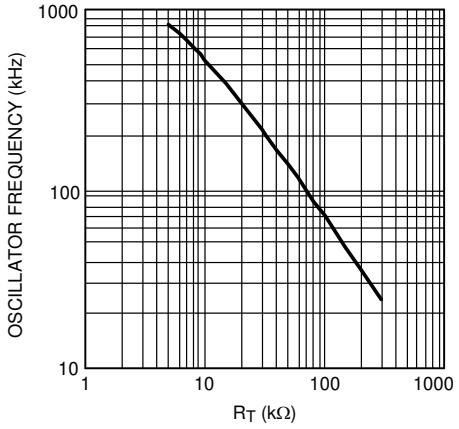
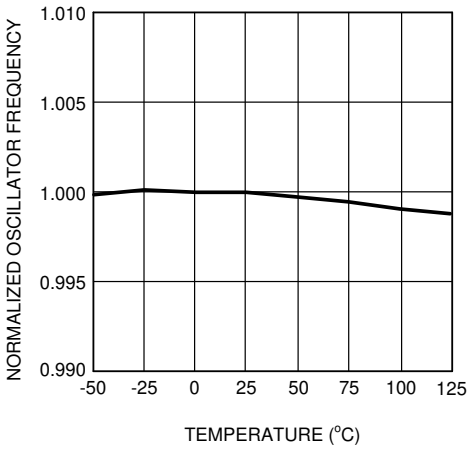


Figure 5-1. Oscillator Frequency vs R_T



F_{OSC} = 200kHz

Figure 5-2. Oscillator Frequency vs Temperature

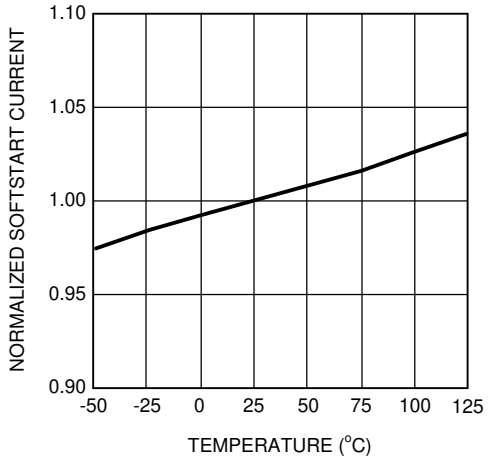
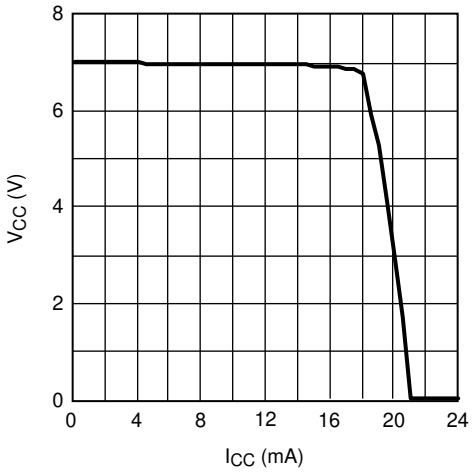
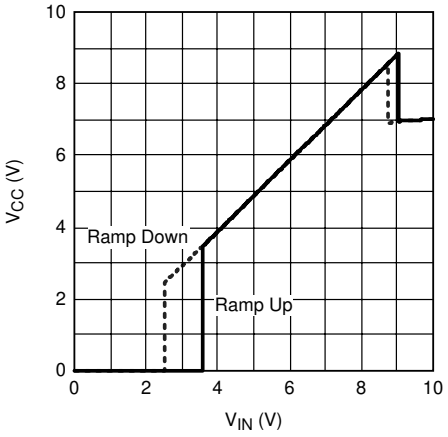


Figure 5-3. Soft Start Current vs Temperature



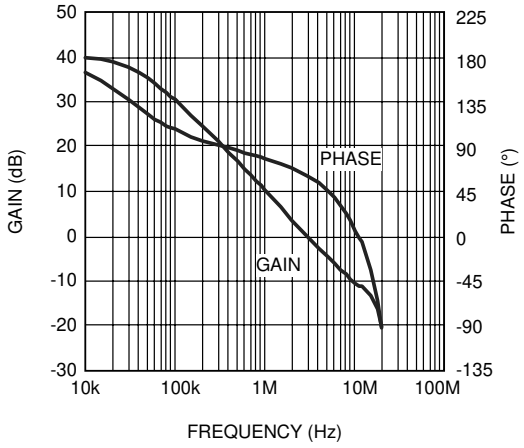
V_{IN} = 12V

Figure 5-4. V_{CC} vs I_{CC}



R_L = 7kΩ

Figure 5-5. V_{CC} vs V_{IN}



A_{VCL} = 101

Figure 5-6. Error Amplifier Gain and Phase

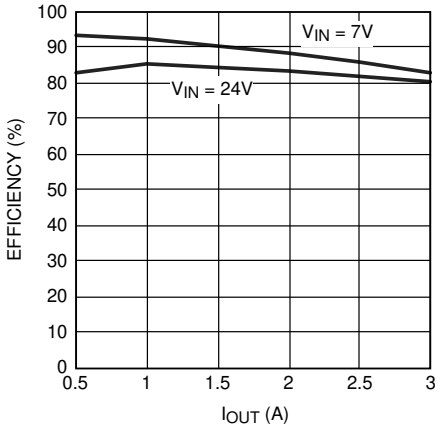


Figure 5-7. Demoboard Efficiency vs I_{OUT} and V_{IN}

6 Detailed Description

6.1 Overview

The LM25576-Q1 switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates a 42V N-Channel buck switch with an output current capability of 3 Amps. The regulator control method is based on current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50kHz to 1MHz. An oscillator synchronization pin allows multiple LM25576-Q1 regulators to self synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225V. Fault protection features include, current limiting, thermal shutdown and remote shutdown capability. The device is available in the HTSSOP-20 package featuring an exposed pad to aid thermal dissipation.

The functional block diagram and typical application of the LM25576-Q1 are shown in *Section 6.2*. The LM25576-Q1 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is well suited for telecom, industrial power bus voltage ranges.

6.2 Functional Block Diagram

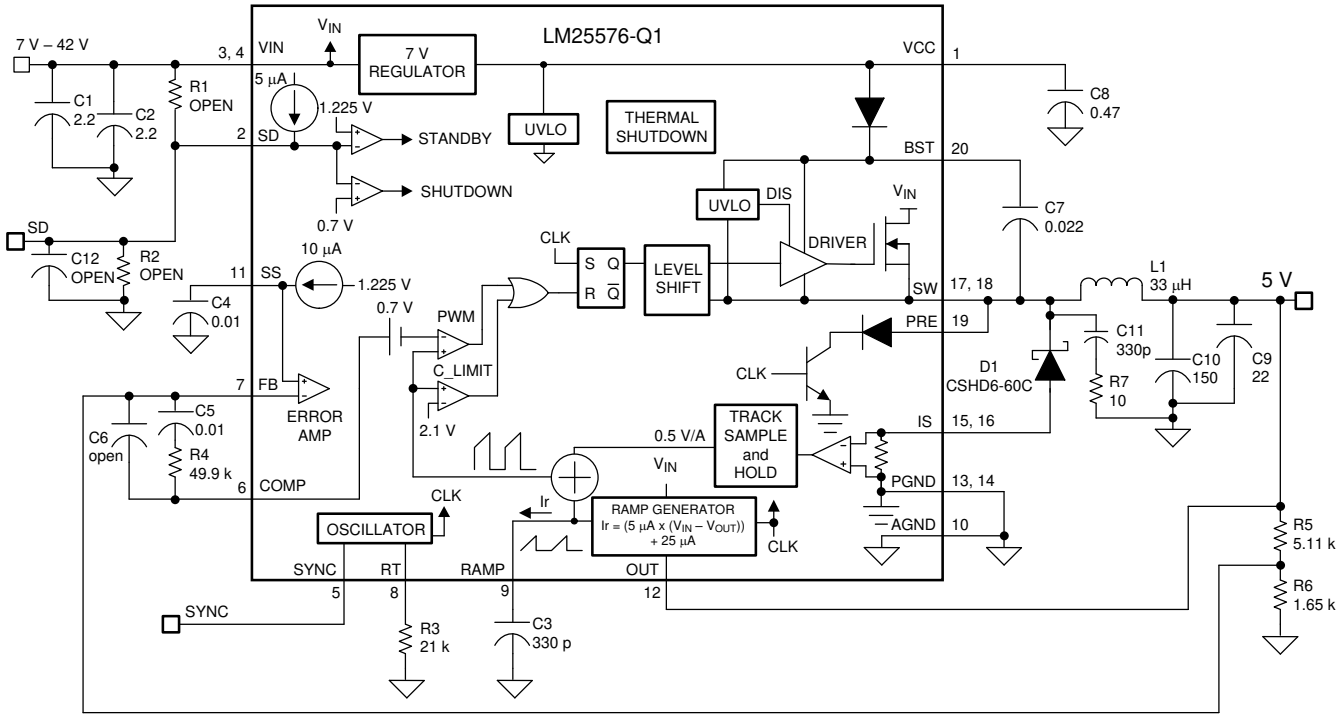


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 High Voltage Start-Up Regulator

The LM25576-Q1 contains a dual-mode internal high voltage start up regulator that provides the V_{CC} bias supply for the PWM controller and boot-strap MOSFET gate driver. The input pin (VIN) directly connects to the input voltage, as high as 42V. For input voltages below 9V, a low dropout switch connects V_{CC} directly to V_{IN}. In this supply range, V_{CC} is approximately equal to V_{IN}. For V_{IN} voltage greater than 9V, the low dropout switch is disabled and the V_{CC} regulator is enabled to maintain V_{CC} at approximately 7V. The wide operating range of 6V to 42V is due to the use of the dual mode regulator.

The output of the V_{CC} regulator is current limited to 25mA. Upon power up, the regulator sources current into the capacitor that connects to the VCC pin. When the voltage at the VCC pin exceeds the V_{CC} UVLO threshold of 5.35V and the SD pin is greater than 1.225V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until V_{CC} falls below 5V or the SD pin falls below 1.125V.

An auxiliary supply voltage applies to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 7.3V, the internal regulator essentially shuts off, reducing the IC power dissipation. The V_{CC} regulator series pass transistor includes a diode between V_{CC} and V_{IN}; do not forward bias the diode in normal operation. Ensure that the auxiliary V_{CC} voltage never exceeds the V_{IN} voltage.

Take extra care in high voltage applications to ensure that the VIN pin does not exceed the absolute maximum voltage rating of 45V. During line or load transients, voltage ringing on the V_{IN} line that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

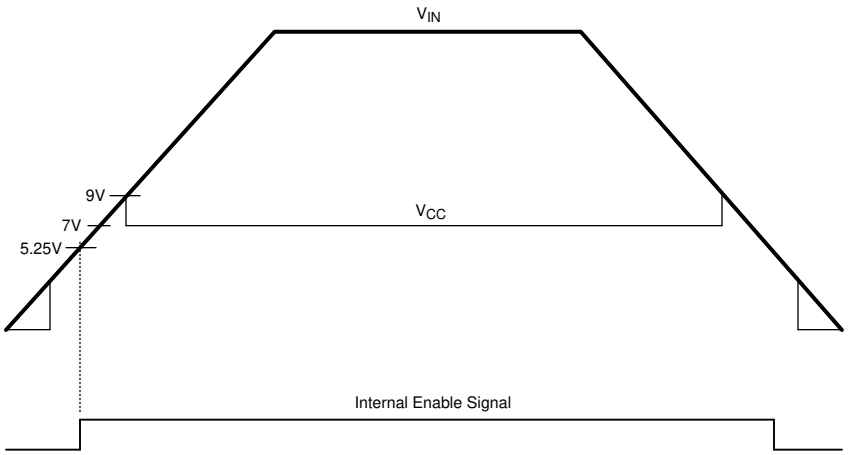


Figure 6-2. V_{IN} and V_{CC} Sequencing

6.4 Device Functional Modes

6.4.1 Shutdown and Stand-by Mode

The LM25576-Q1 contains a dual level Shutdown (SD) circuit. When the SD pin voltage is below 0.7V, the regulator is in a low current shutdown mode. When the SD pin voltage is greater than 0.7V but less than 1.225V, the regulator is in standby mode. In standby mode the V_{CC} regulator is active but the output switch is disabled. When the SD pin voltage exceeds 1.225V, the output switch is enabled and normal operation begins. An internal 5µA pull-up current source configures the regulator to be fully operational if the SD pin is left open.

Use an external set-point voltage divider from VIN to GND to set the operational input range of the regulator. Design the divider so that the voltage at the SD pin is be greater than 1.225V when Vin is in the desired operating range. Include the internal 5µA pull-up current source in calculations of the external set-point divider. Both the shutdown and standby thresholds include hysteresis of 0.1V. The SD pin internally clamps with a 1kΩ resistor and an 8V zener clamp. Ensure that the voltage at the SD pin never exceeds 14V. If the voltage at the SD pin exceeds 8V, the bias current increases at a rate of 1mA/V.

Use the SD pin to implement various remote enable and disable functions. Pulling the SD pin below the 0.7V threshold totally disables the controller. If the SD pin voltage is above 1.225V, the regulator is operational.

6.4.2 Oscillator and Sync Capability

The LM25576-Q1 oscillator frequency is set by a single external resistor connected between the RT pin and the AGND pin. Locate the R_T resistor very close to the device and connected directly to the pins of the IC (RT and AGND). To set a desired oscillator frequency (F), calculate the necessary value for the R_T resistor from the following equation:

$$R_T = \frac{\frac{1}{F} - 580 \times 10^{-9}}{135 \times 10^{-12}} \quad (1)$$

Use the SYNC pin to synchronize the internal oscillator to an external clock. Verify that the external clock is of higher frequency than the free-running frequency set by the R_T resistor. A clock circuit with an open drain output is the recommended interface from the external clock to the SYNC pin. Verify that the clock pulse duration is greater than 15ns.

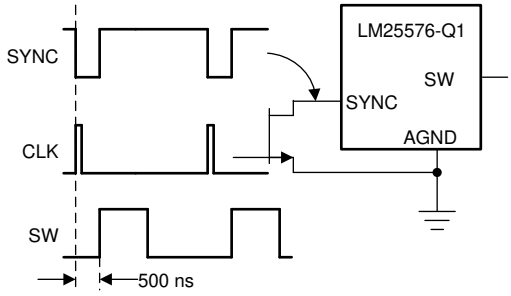


Figure 6-3. Sync from External Clock

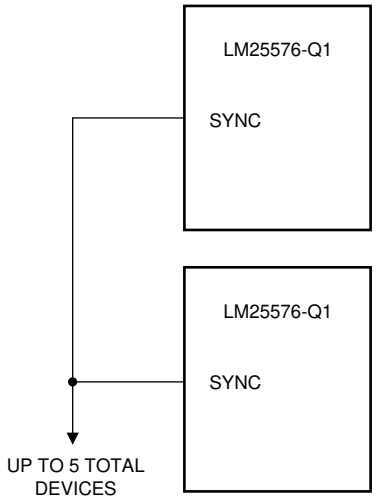


Figure 6-4. Sync from Multiple Devices

Synchronize multiple LM25576-Q1 devices together by connecting the SYNC pins together. In this configuration, all of the devices synchronize to the highest frequency device. The diagram in Figure 6-5 illustrates the SYNC input and output features of the LM25576-Q1. The internal oscillator circuit drives the SYNC pin with a strong pull-down and weak pull-up inverter. When the SYNC pin is pulled low either by the internal oscillator or an external clock, the ramp cycle of the oscillator terminates and a new oscillator cycle begins. Thus, if the SYNC pins of several LM25576-Q1 ICs connect together, the IC with the highest internal clock frequency pulls the connected SYNC pins low first and terminates the oscillator ramp cycles of the other ICs. The LM25576-Q1 with the highest programmed clock frequency serves as the controller and controls the switching frequency of the all the devices with lower oscillator frequency.

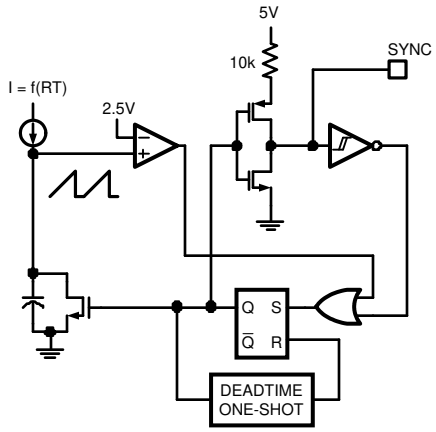


Figure 6-5. Simplified Oscillator Block Diagram and SYNC I/O Circuit

6.4.3 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.225V). The output of the error amplifier connects to the COMP pin, allowing the user to provide loop compensation components, generally a type II network, as illustrated in Figure 6-1. This network creates a pole at DC, a zero and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

6.4.4 RAMP Generator

The ramp signal in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the output inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement can introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulse-width. In applications where the input voltage is relatively large in comparison to the output voltage, controlling small pulse-widths and duty cycles is necessary for regulation. The LM25576-Q1 uses a unique ramp generator, which does not measure the buck switch current but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements: a sample and hold DC level and an emulated current ramp.

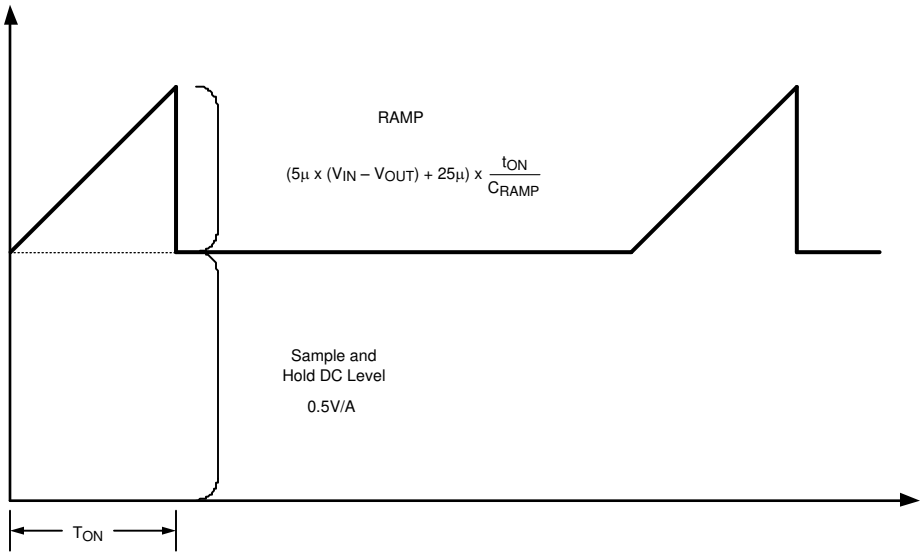


Figure 6-6. Composition of Current Sense Signal

The sample and hold DC level illustrated in Figure 6-6 is derived from a measurement of the re-circulating Schottky diode anode current. Connect the re-circulating diode anode to the IS pin. The diode current flows through an internal current sense resistor between the IS and PGND pins. The voltage level across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample and hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the Vin and Vout voltages per the following equation:

$$I_{RAMP} = [5\mu \times (V_{IN} - V_{OUT})] + 25\mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor. Select the value of C_{RAMP} from the following equation.

$$C_{RAMP} = L \times 10^{-5} \quad (3)$$

- L = value of the output inductor in Henrys

With this value, the scale factor of the emulated current ramp is approximately equal to the scale factor of the DC level sample and hold (0.5V / A). Locate the C_{RAMP} capacitor very close to the device and verify that the capacitor connects directly to the pins of the IC (RAMP and AGND).

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 25µA of offset current provided from the emulated current source adds some fixed slope to the ramp signal. In some high output voltage, high duty cycle applications, additional slope can be required. In these applications, add a pull-up resistor between the V_{CC} and RAMP pins to increase the ramp slope compensation.

For V_{OUT} > 7.5V:

Calculate optimal slope current:

$$I_{OS} = V_{OUT} \times 5\mu A/V \quad (4)$$

For example, at V_{OUT} = 10V, I_{OS} = 50 µA.

Install a resistor from the RAMP pin to V_{CC}:

$$R_{RAMP} = V_{CC} \div [I_{OS} - 25\mu A] \quad (5)$$

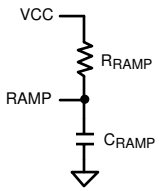


Figure 6-7. R_{RAMP} to V_{CC} for V_{OUT} > 7.5V

6.4.5 Maximum Duty Cycle and Input Drop-Out Voltage

There is a forced off-time of 500ns implemented each cycle to establish sufficient time for the diode current to sample. This forced off-time limits the maximum duty cycle of the buck switch. The maximum duty cycle varies with the operating frequency.

$$D_{MAX} = 1 - Fs \times 500ns \quad (6)$$

- Fs = oscillator frequency

Limiting the maximum duty cycle raises the input dropout voltage. The input dropout voltage is the lowest input voltage required to maintain regulation of the output voltage. An approximation of the input dropout voltage is:

$$Vin_{MIN} = \frac{V_{out} + V_D}{1 - Fs \times 500ns} \quad (7)$$

- V_D = voltage drop across the re-circulatory diode

Operating at high switching frequency raises the minimum input voltage necessary to maintain regulation.

6.4.6 Current Limit

The LM25576-Q1 contains a unique current monitoring scheme for control and over-current protection. When set correctly, the emulated current sense signal provides a signal which is proportional to the buck switch current with a scale factor of 0.5V / A. The emulated ramp signal applies to the current limit comparator. If the emulated ramp signal exceeds 2.1V (4.2A) the present current cycle terminates (cycle-by-cycle current limiting). In applications with small output inductance and high input voltage the switch current can overshoot due to the propagation delay of the current limit comparator. If an overshoot occurs, the diode current sampling circuit detects the excess inductor current during the off-time of the buck switch. If the sample and hold DC level exceeds the 2.1V current limit threshold, the buck switch is disabled and skip pulses until the diode current sampling circuit detects the inductor current decays below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any current overshoot.

6.4.7 Soft-Start

The soft-start feature allows the regulator to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The internal soft-start current source, set to 10µA, gradually increases the voltage of an external soft-start capacitor connected to the SS pin. The soft-start capacitor voltage connects to the reference input of the error amplifier. Implement various sequencing and tracking schemes using external circuits that limit or clamp the voltage level of the SS pin.

In the event a fault is detected (over-temperature, V_{CC} UVLO, SD) the soft-start capacitor discharges. When the fault condition is no longer present, a new soft-start sequence commences.

6.4.8 Boost Pin

The LM25576-Q1 integrates an N-Channel buck switch and associated floating high voltage level shift or gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.022µF ceramic capacitor, connected with short traces between the BST pin and SW pin, is recommended. During the off-time of the buck switch, the SW pin voltage is approximately –0.5V and the bootstrap capacitor is charged from V_{CC} through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch is forced off each cycle for 500ns to confirm that the bootstrap capacitor recharges.

Under very light load conditions or when the output voltage is pre-charged, the SW voltage does not remain low during the off-time of the buck switch. If the inductor current falls to zero and the SW pin rises, the bootstrap capacitor does not receive sufficient voltage to operate the buck switch gate driver. For these applications, connect the PRE pin to the SW pin to pre-charge the bootstrap capacitor. The internal pre-charge MOSFET and diode connected between the PRE pin and PGND turns on each cycle for 265ns just prior to the onset of a new switching cycle. If the SW pin is at a normal negative voltage level (continuous conduction mode), then no current flows through the pre-charge MOSFET or diode.

6.4.9 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Design Requirements

The procedure for calculating the external components is illustrated with the following design example. The Bill of Materials for this design is listed in Table 7-1. The circuit shown in *Section 6.2* is configured for the following specifications:

- V_{OUT} = 5V
- V_{IN} = 7V to 42V
- Fs = 300kHz
- Minimum load current (for CCM) = 250mA
- Maximum load current = 3A

7.1.2 Detailed Design Procedure

Click here to create a custom design using the LM25576-Q1 device with the WEBENCH® Power Designer.

1. Enter the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Use the optimizer dial to optimize the design for key parameters such as efficiency, footprint, and cost.
3. Compare the generated design with other possible designs from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design and share the design with other users

7.1.2.1 R3 (R_T)

R_T sets the oscillator switching frequency. Generally, higher frequency applications are smaller but have higher losses. Operation at 300kHz was selected for this example as a reasonable compromise for both small size and high efficiency. The value of R_T for 300kHz switching frequency can be calculated as follows:

$$R_T = \frac{\left[\left(1 \div 300 \times 10^{-9}\right)\right]}{135 \times 10^{-12}} \quad (8)$$

- R_T = nearest standard value of 21kΩ

7.1.2.2 Inductor (L1)

The inductor value is determined based on:

- Operating frequency
- Load current
- Ripple current
- Minimum input voltage ($V_{IN(min)}$)
- Maximum input voltage ($V_{IN(max)}$)

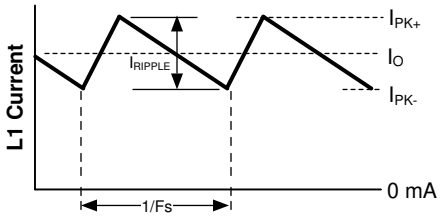


Figure 7-1. Inductor Current Waveform

To keep the circuit in continuous conduction mode (CCM), verify that the maximum ripple current I_{RIPPLE} is less than twice the minimum load current, or 0.5Ap-p. Using this value of ripple current, the value of inductor (L1) is calculated using the following equations:

$$L1 = \frac{V_{OUT} \times \left[V_{IN(max)} - V_{OUT}\right]}{I_{RIPPLE} \times F_S \times V_{IN(max)}} \quad (9)$$

$$L1 = \frac{5V \times [42V - 5V]}{0.5A \times 300kHz \times 42V} = 29\mu H \quad (10)$$

This procedure provides a guide to select the value of L1. Use the nearest standard value (33µH). Verify that L1 is rated for the peak current (I_{PK+}) to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. During an overload condition the peak current is limited to 4.2A nominal (5.1A maximum). The selected inductor (see Table 7-1) has a conservative 6.2 Amp saturation current rating. For this manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30%, at 20°C.

7.1.2.3 C3 (C_{RAMP})

With the inductor value selected, the value of C3 (C_{RAMP}) necessary for the emulation ramp circuit is found in Equation 3

With L1 as 33µH, the recommended value for C3 is 330pF.

7.1.2.4 C9, C10

The output capacitors, C9 and C10, smooth the inductor ripple current and provide a source of charge for transient loading conditions. This design uses a 22µF ceramic capacitor and a 150µF SP organic capacitor. The ceramic capacitor provides ultra low ESR to reduce the output ripple voltage and noise spikes, while the SP capacitor provides a large bulk capacitance in a small volume for transient loading conditions. An approximation for the output ripple voltage is:

$$V_{OUT} = \Delta I_L \times \left[ESR + \frac{1}{8 \times F_S \times C_{OUT}}\right] \quad (11)$$

7.1.2.5 D1

A Schottky type re-circulating diode is required for all LM25576-Q1 applications. Ultra-fast diodes are not recommended and can result in damage to the IC due to reverse recovery current transients. The near-exact reverse recovery characteristics and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications common to the LM25576-Q1. The reverse recovery

characteristic determines how long the current surge lasts each cycle when the buck switch is turned on. The reverse recovery characteristics of Schottky diodes minimize the peak instantaneous power in the buck switch occurring during turn-on each cycle. The resulting switching losses of the buck switch are significantly reduced when using a Schottky diode. Select the reverse breakdown rating for the maximum V_{IN}, plus a safety margin.

The forward voltage drop significantly impacts the conversion efficiency, especially for applications with a low output voltage. *Rated* current for diodes vary widely from various manufacturers. The worst case is to assume a short circuit load condition. In this case the diode carries the output current almost continuously. For the LM25576-Q1 this current can be as high as 4.2A. Assuming a worst case 1V drop across the diode, the maximum diode power dissipation can be as high as 4.2W. Selected in the reference design is a 60V Schottky in a DPAK package.

7.1.2.6 C1, C2

The regulator supply voltage has a large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the VIN pin steps to the lower peak of the inductor current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into VIN during the on-time is the load current. Select the input capacitance for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} \div 2$.

Select quality ceramic capacitors with a low ESR for the input filter. To allow for capacitor tolerances and voltage effects, use two 2.2µF, 100V ceramic capacitors. If expecting step input voltage transients near the maximum rating of the LM25576-Q1, complete a careful evaluation of ringing and possible spikes at the device VIN pin. Use an additional damping network or input voltage clamp in cases with step input voltage transients.

7.1.2.7 C8

The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. The recommended value of C8 id no smaller than 0.1µF. Verify that C8 is a good quality, low ESR, ceramic capacitor. This design uses a value of 0.47µF.

7.1.2.8 C7

The bootstrap capacitor between the BST and the SW pins supplies the gate current to charge the buck switch gate at turn-on. The recommended value of C7 is 0.022µF. Verify that C7 is a good quality, low ESR, ceramic capacitor.

7.1.2.9 C4

The capacitor at the SS pin determines the soft-start time. Soft-start time is the time for the reference voltage and the output voltage to reach the final regulated value. The time is determined from:

$$t_{SS} = \frac{C4 \times 1.225V}{10\mu A} \tag{12}$$

This application uses a C4 value of 0.01µF in correspondence with a soft-start time of 1ms.

7.1.2.10 R5, R6

R5 and R6 set the output voltage level, the ratio of these resistors is calculated from:

$$R5/R6 = \left[\frac{V_{OUT}}{1.225V}\right] - 1 \tag{13}$$

For a 5V output, the R5 and R6 ratio calculates to 3.082. Choose the resistors from standard value resistors, a good starting point is selection in the range from 1kΩ to 0kΩ. The value for R5 is selected as 5.11kΩ. The value of 1.65kΩ is selected for R6.

7.1.2.11 R1, R2, C12

A voltage divider can connect to the SD pin to set a minimum operating voltage $V_{IN(min)}$ for the regulator. If this feature is required, the easiest approach to selecting the divider resistor values is to select a value for R1 (between 10kΩ and 100kΩ recommended) then calculate R2 from:

$$R2 = 1.225 \times \left[\frac{R1}{V_{IN(min)} + \left(5 \times 10^{-6} \times R1\right) - 1.225} \right] \quad (14)$$

Capacitor C12 provides filtering for the divider. Verify that the voltage at the SD pin never exceeds 8V, when using an external set-point divider it may be necessary to clamp the SD pin at high input voltage conditions. The reference design utilizes the full range of the LM25576-Q1 (6V to 42V); therefore these components can be omitted. With the SD pin open circuit the LM25576-Q1 responds once the V_{CC} UVLO threshold is satisfied.

7.1.2.12 R7, C11

A snubber network across the power diode reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. Voltage spikes beyond the rating of the LM25576-Q1 or the re-circulating diode can damage these devices. Selecting the values for the snubber is best accomplished through empirical methods. First, verify that the lead lengths for the snubber connections are very short. For the current levels typical for the LM25576-Q1a resistor value between 5Ω and 20Ω is adequate. Increasing the value of the snubber capacitor results in more damping but higher losses. Select a minimum value of C11 that provides adequate damping of the SW pin waveform at high load.

7.1.2.13 R4, C5, C6

These components configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R4 and C5. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM25576-Q1 is as follows:

$$\text{DC Gain}_{(MOD)} = \text{Gain}_{m(MOD)} \times R_{LOAD} = 2 \times R_{LOAD} \quad (15)$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD}), and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{p(MOD)} = \frac{1}{(2\pi R_{LOAD} C_{OUT})} \quad (16)$$

For R_{LOAD} = 5Ω and C_{OUT} = 177µF then $f_{p(MOD)}$ = 180Hz

$$\text{DC Gain}_{(MOD)} = 2 \times 5 = 10 = 20\text{dB} \quad (17)$$

For the design example of *Section 6.2* the following modulator gain versus frequency characteristic is measured as shown in Figure 7-2.

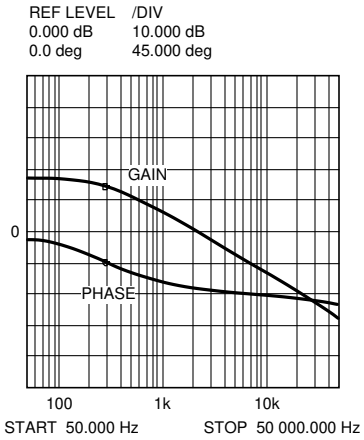


Figure 7-2. Gain and Phase of Modulator R_{LOAD} = 5 Ohms and C_{OUT} = 177 µF

Components R4 and C5 configure the error amplifier as a type II configuration which has a pole at DC and a zero at f_Z = 1 ÷ (2πR4C5). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the loop gain. A single pole response at the crossover frequency yields a stable loop with 90 degrees of phase margin.

This design example uses a target loop bandwidth (crossover frequency) of 20kHz. Select the compensation network zero (f_Z) of at least an order of magnitude less than the target crossover frequency. This constrains the product of R4 and C5 for a desired compensation network zero 1 ÷ (2π R4 C5) as less than 2kHz. Increasing R4, while proportionally decreasing C5, increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C5, decreases the error amp gain. For the design example, C5 is 0.01 µF and R4 is 49.9kΩ. These values configure the compensation network zero at 320Hz. The error amp gain at frequencies greater than f_Z is: R4 / R5, which is approximately 10 (20dB).

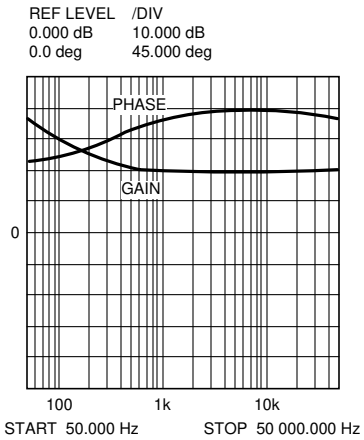


Figure 7-3. Error Amplifier Gain and Phase

The overall loop can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

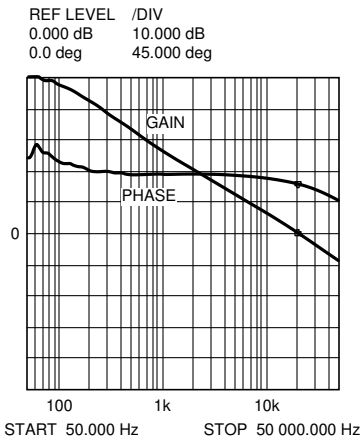


Figure 7-4. Overall Loop Gain and Phase

If a network analyzer is available, measure the modulator gain and configure the error amplifier gain for the desired loop transfer function. If a network analyzer is not available, design the error amplifier compensation components with the guidelines given. Perform step load transient tests to verify acceptable performance. The step load goal is minimum overshoot with a damped response. Add C6 to the compensation network to decrease noise susceptibility of the error amplifier. Verify that the value of C6 is sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. Verify that this pole is well beyond the loop crossover frequency. A good approximation of the location of the pole added by C6 is: f_{p2} = fz × C5 ÷ C6.

7.1.3 Bias Power Dissipation Reduction

Buck regulators operating with high input voltage dissipate an appreciable amount of power for the bias of the IC. The V_{CC} regulator must step-down the input voltage V_{IN} to a nominal V_{CC} level of 7V. The large voltage drop across the V_{CC} regulator translates into a large power dissipation within the V_{cc} regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. Figure 7-5 and Figure 7-6 depict two methods to bias the IC from the output voltage. In each case the internal V_{CC} regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin potential is raised above the nominal 7V regulation level, which effectively disables the internal V_{CC} regulator. Verify that the voltage applied to the VCC pin does not exceed 14V. Establish that the V_{CC} voltage is never larger than the V_{IN} voltage.

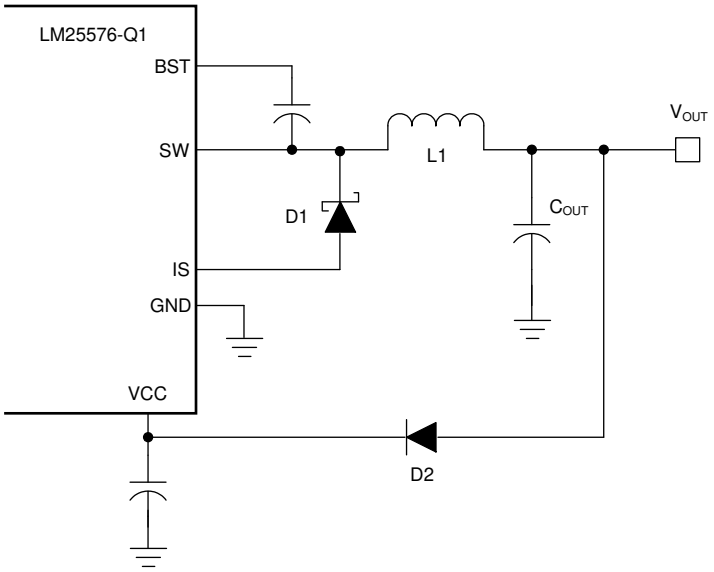


Figure 7-5. VCC Bias from VOUT for 8V < VOUT < 14V

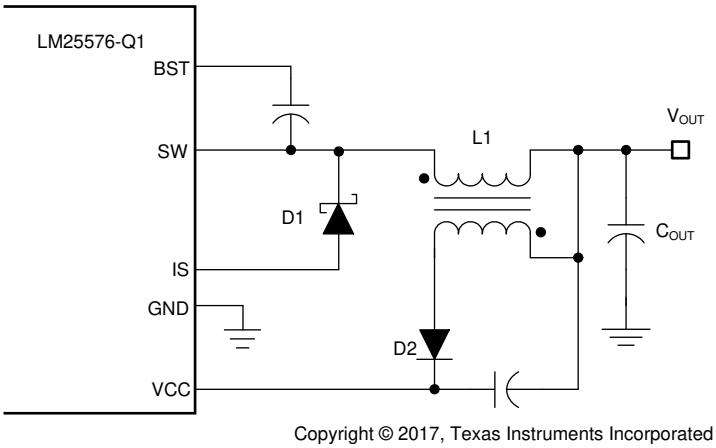


Figure 7-6. VCC Bias with Additional Winding on the Output Inductor

7.2 Typical Application

7.2.1 Typical Schematic for High Frequency (1MHz) Application

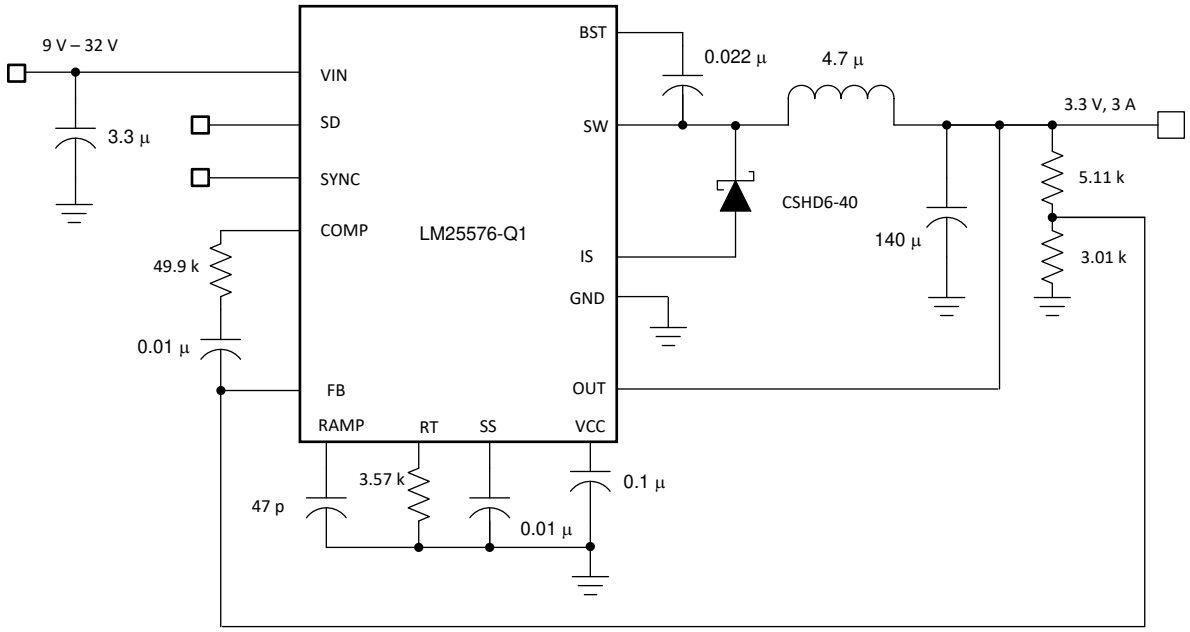
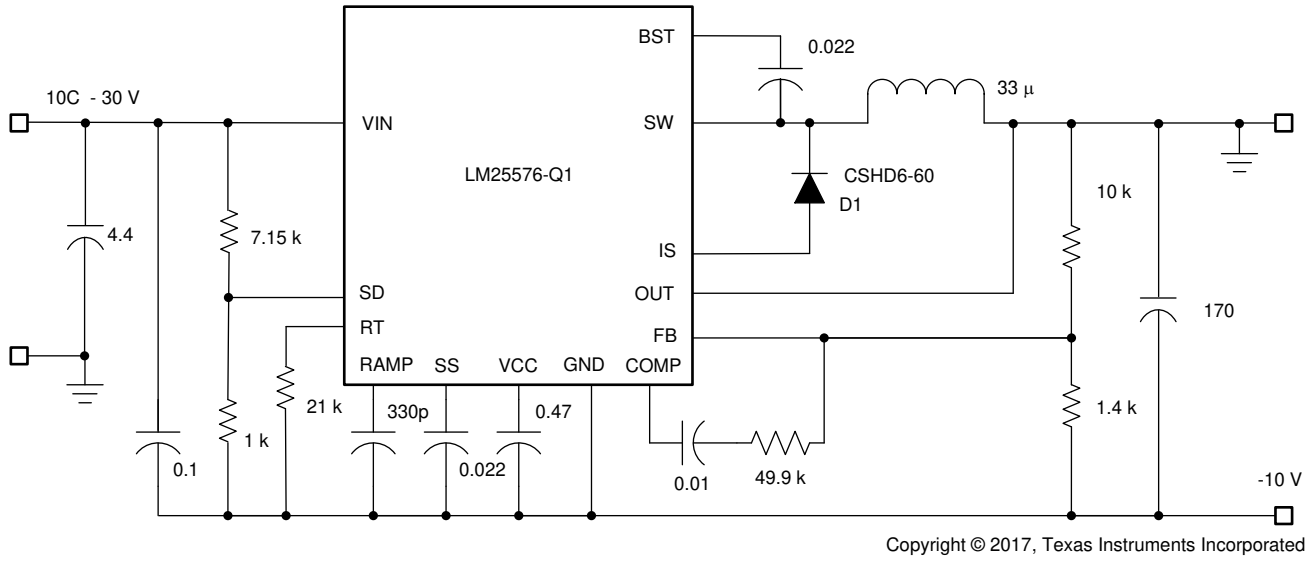


Figure 7-7. Schematic 3.3V, 3A, 1MHz

7.2.2 Typical Schematic for Buck and Boost (Inverting) Application



7.2.3 Application Curves

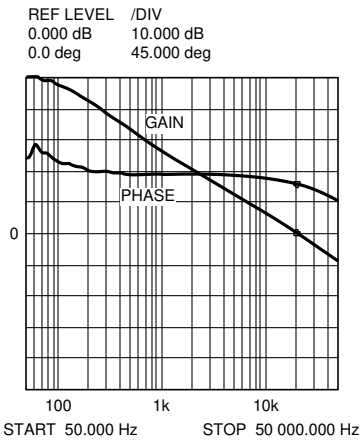


Figure 7-8. Overall Loop Gain and Phase

7.3 Power Supply Recommendations

Verify that the characteristics of the input supply are compatible with the specifications found in this data sheet. In addition, establish that the input supply is capable of delivering the required input current to the loaded regulator. Estimate the average input current using the following equation.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \quad (18)$$

- η = efficiency

If the regulator connects to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20µF to 100µF is typically sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This action can lead to instability, as well as some of the effects mentioned above, unless designed carefully. The AN-2162 Simple Success With Conducted EMI From DC/DC Converters application note provides helpful suggestions when designing an input filter for any switching regulator. In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). TI does not recommend the use of a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 PCB Layout and Thermal Considerations

The circuit in Figure 7-6 serves as both a block diagram of the LM25576-Q1 and a typical application board schematic for the LM25576-Q1. In a buck regulator there are two loops where currents switch very fast. The first loop starts from the input capacitors, to the regulator VIN pin, to the regulator SW pin, to the inductor then

out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the regulator IS pins, to the diode anode, to the inductor and then out to the load. Minimizing the loop area of these two loops reduces the stray inductance and minimizes noise and possible erratic operation. A ground plane in the PC board is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through the topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane.

The two highest power dissipating components are the re-circulating diode and the LM25576-Q1 regulator IC. The easiest method to determine the power dissipated within the LM25576-Q1 is to measure the total conversion losses (Pin – Pout) then subtract the power losses in the Schottky diode, output inductor and snubber resistor. An approximation for the Schottky diode loss is

$$P = [1D] \times I_{out} \times V_{fwd} \tag{19}$$

An approximation for the output inductor power is

$$P = {I_{OUT}}^2 \times F_{sw} \times C_{snub} \tag{20}$$

- R is the DC resistance of the inductor
- 1.1 factor is an approximation for the AC losses

If using a snubber, an approximation for the damping resistor power dissipation is

$$P = {V_{IN}}^2 \times F_{sw} \times C_{snub} \tag{21}$$

where

- F_{sw} is the switching frequency
- C_{snub} is the snubber capacitor

The regulator has an exposed thermal pad to aid power dissipation. Adding several vias under the device to the ground plane greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad aids the power dissipation of the diode.

The most significant variables that affect the power dissipated by the LM25576-Q1 are the output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The operating frequency of the LM25576-Q1 evaluation board has been designed for 300kHz. When operating at 3A output current with a 42V input the power dissipation of the LM25576-Q1 regulator is approximately 1.9W.

The junction-to-ambient thermal resistance of the LM25576-Q1 vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. Referring to the evaluation board artwork, the area under the LM25576-Q1 (component side) is covered with copper and there are 5 connection vias to the solder side ground plane. Additional vias under the IC have diminishing value as more vias are added. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM25576-Q1 mounted in the evaluation board varies from 45°C/W with no airflow to 25°C/W with 900 LFM (Linear Feet per Minute). With a 25°C ambient temperature and no airflow, the predicted junction temperature for the LM25576-Q1 will be 25 + (45 × 1.9) = 110°C. If the evaluation board operates at 3A output current and 42V input voltage for a prolonged period of time the thermal shutdown protection within the IC may activate. The IC turns off, allowing the junction to cool, followed by restart with the soft-start capacitor reset to zero.

Table 7-1. 5V, 3A Demo Board Bill of Materials

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2µ, 100V
C	2	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2µ, 100V
C	3	C0805C331G1GAC	CAPACITOR, CER, KEMET	330p, 100V
C	4	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01µ, 100V
C	5	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01µ, 100V
C	6	OPEN	NOT USED	
C	7	C2012X7R2A223K	CAPACITOR, CER, TDK	0.022µ, 100V
C	8	C2012X7R1C474M	CAPACITOR, CER, TDK	0.47µ, 16V
C	9	C3225X7R1C226M	CAPACITOR, CER, TDK	22µ, 16V
C	10	EEFHE0J151R	CAPACITOR, SP, PANASONIC	150µ, 6.3V
C	11	C0805C331G1GAC	CAPACITOR, CER, KEMET	330p, 100V
C	12	OPEN	NOT USED	
D	1	CSHD6-60C	DIODE, 60V, CENTRAL	
		6CWQ10FN	DIODE, 100V, IR (D1-ALT)	
L	1	DR127-330	INDUCTOR, COOPER	33µH
R	1	OPEN	NOT USED	
R	2	OPEN	NOT USED	
R	3	CRCW08052102F	RESISTOR	21kΩ
R	4	CRCW08054992F	RESISTOR	49.9kΩ
R	5	CRCW08055111F	RESISTOR	5.11kΩ
R	6	CRCW08051651F	RESISTOR	1.65kΩ
R	7	CRCW2512100J	RESISTOR	10, 1W
U	1	LM25576-Q1	REGULATOR, TEXAS INSTRUMENTS	

7.4.2 Layout Example

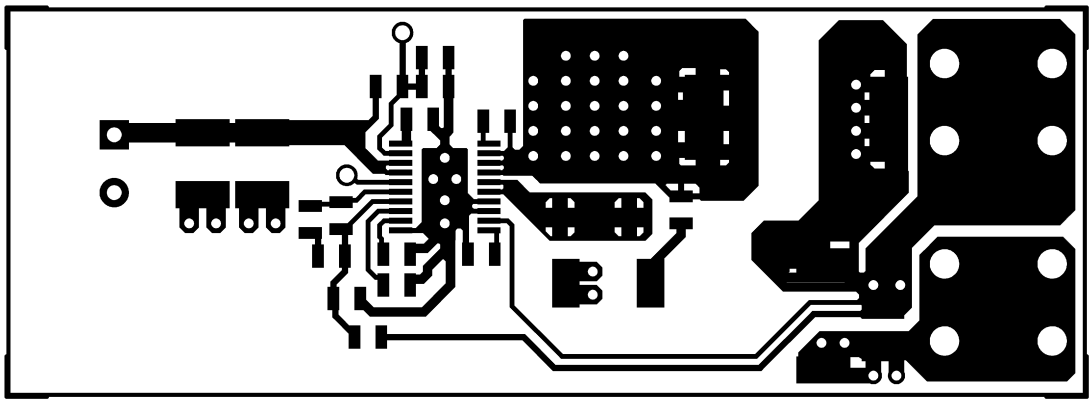


Figure 7-9. Component Side

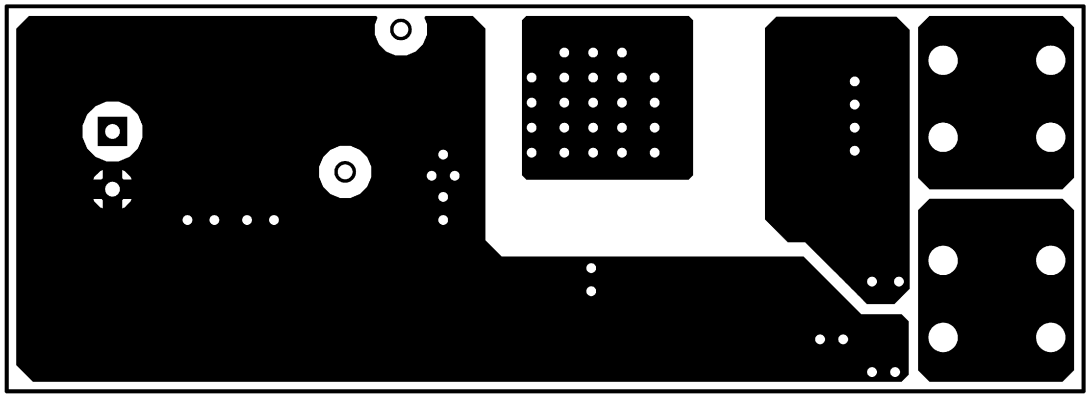


Figure 7-10. Solder Side

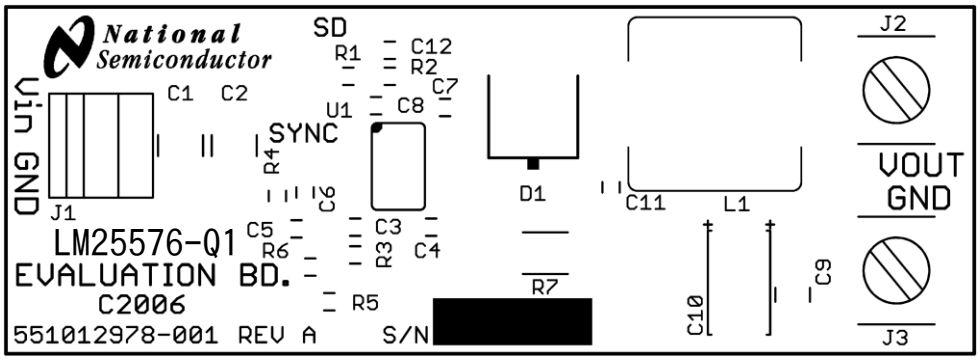


Figure 7-11. Silkscreen

8 Device and Documentation Support

8.1 Device Support

8.1.1 Developmental Support

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25576-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2017) to Revision A (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added charged-device model specification to ESD Ratings section with accompanying table notes	5
• Added Thermal Resistance Characteristics	5
• Updated Bias Current (Iin) from: 3.4mA to: 2mA	6
• Updated Shutdown Current (Iin) from: 57uA to: 48uA	6
• Updated BOOST UVLO Hysteresis from: 0.56V to: 0.8V	6
• Updated FB Bias Current from: 17nA to: 10nA	6
• Updated section title from: External Components to: Design Requirements	16
• Added Detailed Design Procedure section	16
• Added Application Curves section	23
• Added Power Supply Recommendations	24
• Moved Layout to Application and Implementation section	24

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25576QMH/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25576 QMH
LM25576QMH/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25576 QMH
LM25576QMH/NOPB.B	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25576 QMH
LM25576QMHX/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	LM25576 QMH
LM25576QMHX/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	LM25576 QMH
LM25576QMHX/NOPB.B	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	LM25576 QMH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LM25576-Q1 :

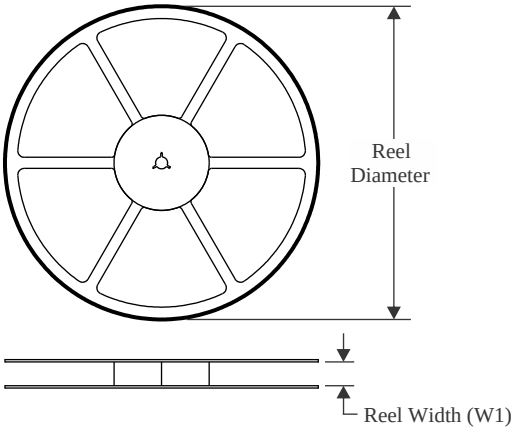
- Catalog : LM25576

NOTE: Qualified Version Definitions:

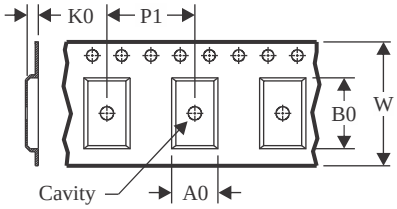
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

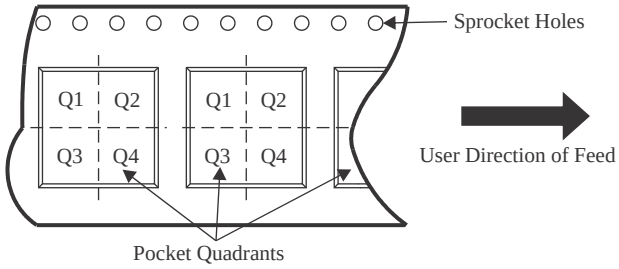


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

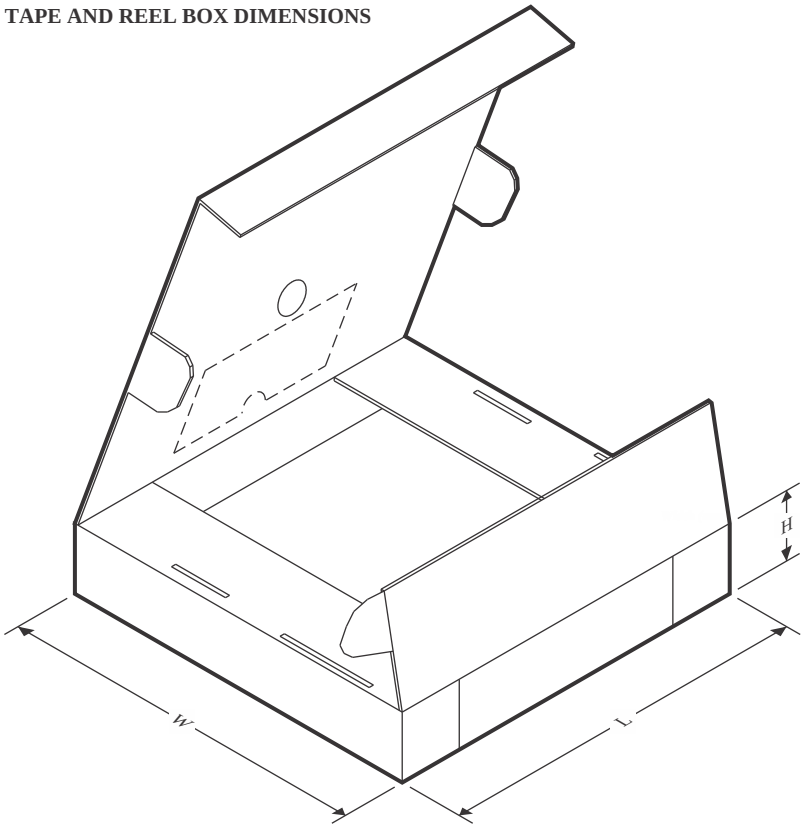
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25576QMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

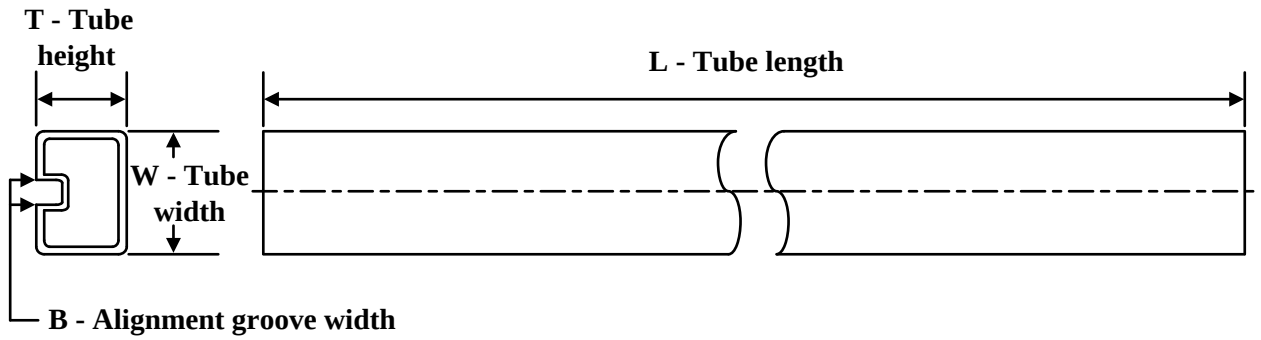
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25576QMHX/NOPB	HTSSOP	PWP	20	2500	356.0	356.0	35.0

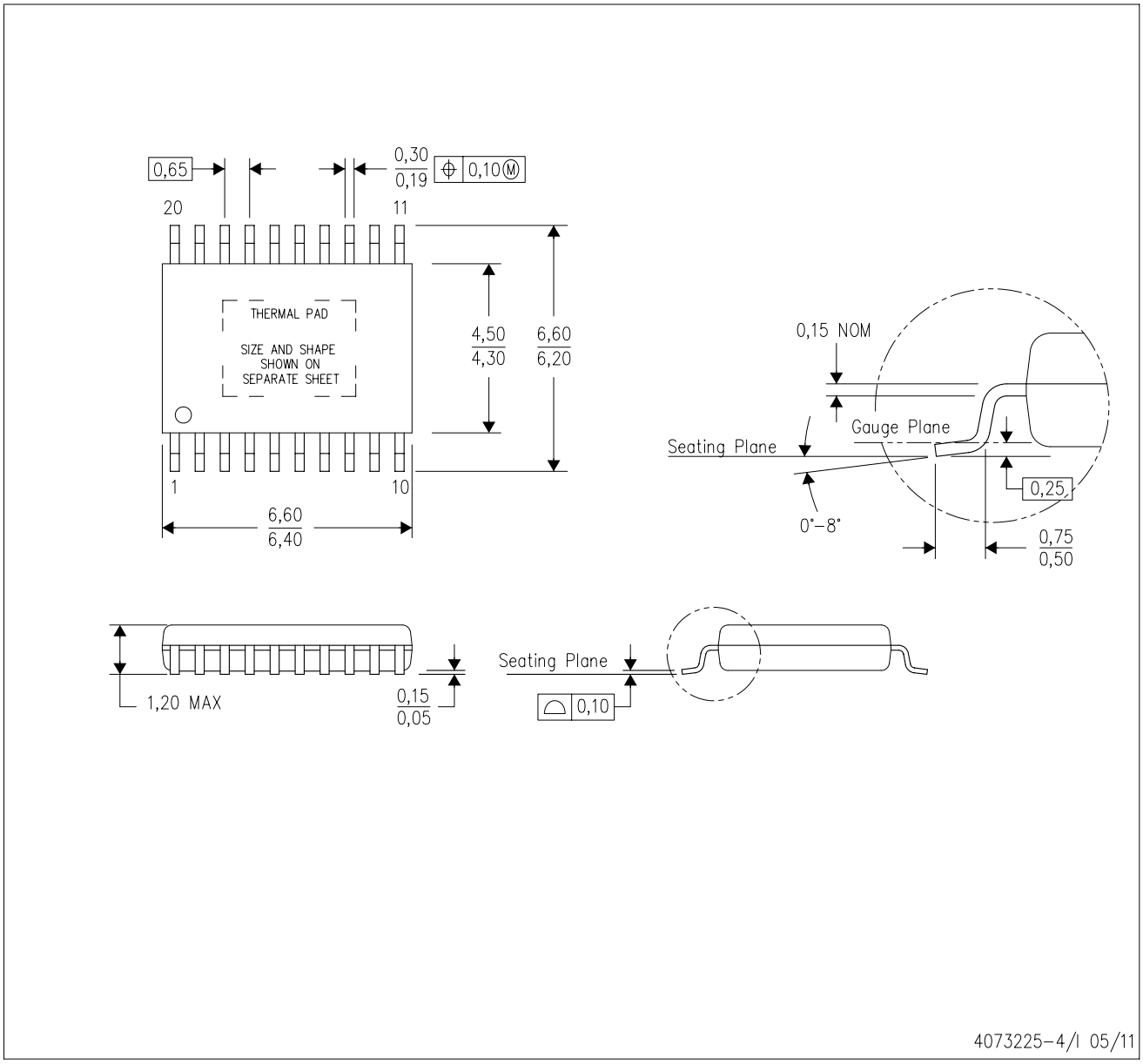
TUBE



*All dimensions are nominal

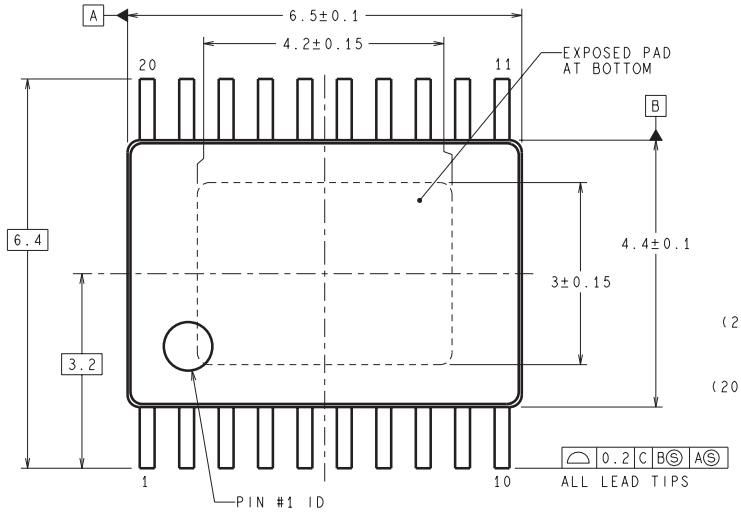
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM25576QMH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM25576QMH/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM25576QMH/NOPB.B	PWP	HTSSOP	20	73	495	8	2514.6	4.06

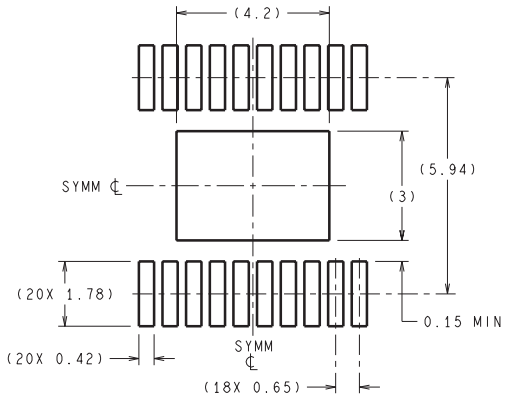
PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



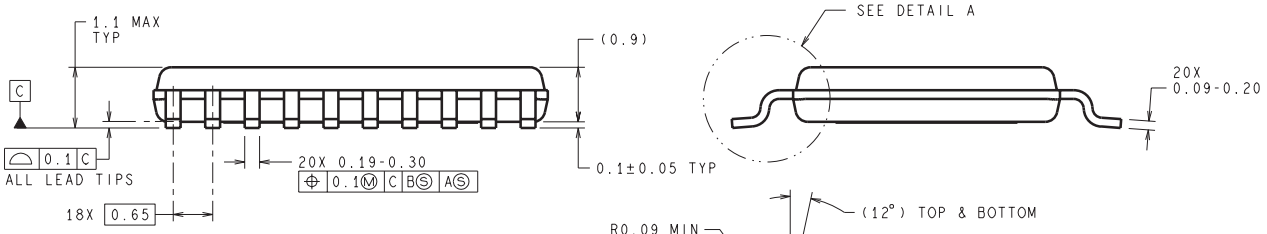
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

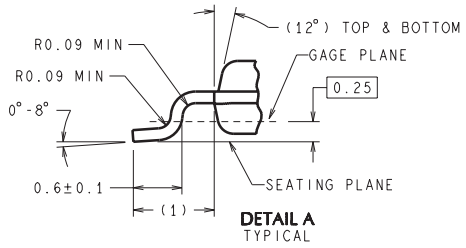
PWP0020A





RECOMMENDED LAND PATTERN





DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MXA20A (Rev C)

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