TL331L-Q1 and LM2903L-Q1 Automotive Open-Drain High Voltage Self-Latching Comparators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Output Latches on High to Low Output Transition
- Level-triggered clear
- Transparent Mode
- Independent latches per channel
- 2.7V to 36V supply range
- Offset Voltage: 2.5mV max at 25°C
- Fault-tolerant inputs
- 300ns typical propagation delay
- Low quiescent current: 350µA per channel
- Open-drain outputs
- CLR input compatable down to 1.2V logic
- Functional Safety-Capable
  - Documentation available to aid functional safety system design

2 Applications

- Telematics eCall
- Automotive head unit
- Instrument Cluster
- On-board (OBC) & wireless chargers

3 Description

The TL331L-Q1 (single) and LM2903L-Q1 (dual) are high voltage self-latching comparators with a open-collector output. The family also offers low input offset voltage and fault-tolerant inputs. These devices have an excellent speed-to-power combination with a propagation delay of 300ns with a quiescent supply current of only 300µA per channel.

The unique feature of the family is the output latching capability. The output latches upon the first high-to-low threshold crossing, allowing capture of an event or error condition without the full attention of a system controller. This allows events to be captured at start up while the system controller is still initializing or busy with other tasks. When the Latch input is held low, the "Transparent" mode is entered and the output continues to reflect the input conditions (latching disabled).

These comparators also feature fault-tolerant inputs that can go up to 36V without damage with no output phase inversion. This makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

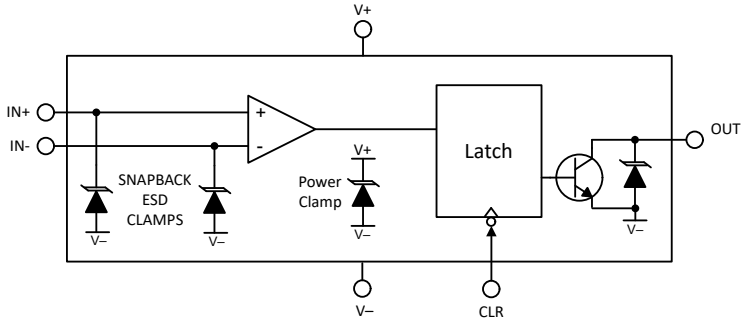
The open-drain outputs can be pulled-up below or beyond the supply voltage for OR'ing multiple outputs or level translation.

The family is specified for the Automotive temperature range of -40°C to +125°C and are available in standard leaded and leadless packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TL331L-Q1 (Single)	DCK (SC-70, 6)(3)	2mm × 2.1mm
	DBV (SOT-23, 6)(3)	2.9mm × 2.8mm
	DSE (WSON, 6)(3)	1.5mm × 1.5mm
LM2903L-Q1 (Dual)	DGS (VSSOP, 10)(3)	3mm × 4.9mm
	RUG (X2QFN, 10)	1.5mm × 2mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product preview (not Production Data).



Simplified Internal Diagram

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4 Pin Configuration and Functions

4.1 Pin Functions: Single TL331L-Q1

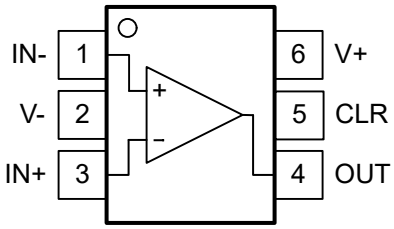

Figure 4-1. DCK and DBV Packages
TL331 Pinout with Clear Pin
6-Pin SC-70 and SOT-23
Top View

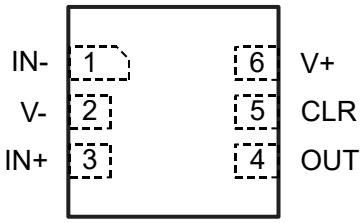

Figure 4-2. DSE Package
6-Pin WSON
Top View

Table 4-1. Pin Configuration: TL331L-Q1

NAME	TL331L-Q1			TYPE(1)	DESCRIPTION
	6 PINS	6 PINS	6 PINS		
	SC-70	SOT-23	WSON		
IN-	1	1	1	I	Inverting (-) input
V-	2	2	2	—	Negative supply voltage
IN+	3	3	3	I	Non-Inverting (+) input
OUT	4	4	4	O	Output
CLR	5	5	5	I	Clear input - clears on falling edge
V+	6	6	6	—	Positive supply voltage

(1) Signal Types: I = Input, O = Output

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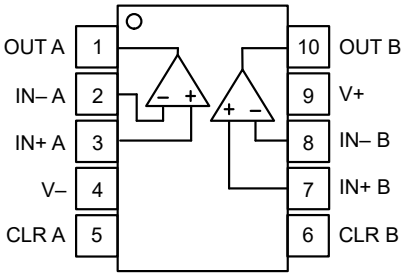
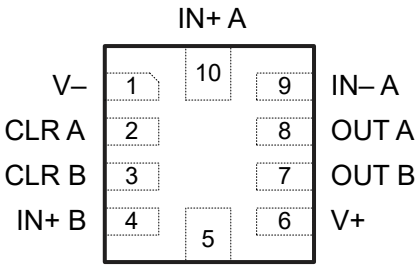
4.2 Pin Configuration: Dual LM2903L-Q1



DGS Package
10-Pin VSSOP
Top View



RUG Package
10-Pin X2QFN
Top View

Table 4-2. Pin Functions: LM2903L-Q1

NAME	LM2903L-Q1		TYPE[1]	DESCRIPTION
	10 PINS VSSOP	10 PINS X2QFN		
OUT A	1	8	O	Output of comparator A
IN– A	2	9	I	Inverting (–) input of comparator A
IN+ A	3	10	I	Non-Inverting (+) input of comparator A
V–	4	1	—	Negative supply voltage
CLR A	5	2	I	Clear input for comparator A - clears on falling edge
CLR B	6	3	I	Clear input for comparator B - clears on falling edge
IN+ B	7	4	I	Non-inverting (+) input of comparator B
IN– B	8	5	I	Inverting (–) input of comparator B
V+	9	6	—	Positive supply voltage
OUT B	10	7	O	Output of comparator B

(1) Signal Types: I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		–0.3	38	V
Input pins (IN+, IN–, CLR) from (V–)(2)	Input pins (IN+, IN–, CLR) from (V–)(2)	–0.3	38	V
Output (OUT) from (V–)(3)	Output (OUT) from (V–)(3)	–0.3	38	V
Output short circuit duration(4)			unlimited	s
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less. Additionally, Inputs (IN+, IN–) can be greater than (V+) and OUT as long as the voltage is within the –0.3V to 36V range
(3) Output (OUT) can be greater than (V+) and inputs (IN+, IN–) as long as the voltage is within the –0.3V to 36V range
(4) Short-circuit to (V–) or (V+).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-0111	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) - (V-)	2.7	36	V
Input voltage range (IN+, IN–, CLR) from (V–)	–0.1	36	V
Input common mode voltage range (IN+, IN–) from (V–)	0	(V+) - 2	V
Output voltage range, from (V-)	0	36	V
Ambient Temperature, T_A	–40	125	°C

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5.4 Thermal Information - Single

THERMAL METRIC (1)		TL331L-Q1			UNIT
		DCK (SC-70)	DBV (SOT-23)	DSE (WSON)	
		6 PINS	6 PINS	6 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	-	-	-	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	-	-	-	°C/W
R_{qJB}	Junction-to-board thermal resistance	-	-	-	°C/W
y_{JT}	Junction-to-top characterization parameter	-	-	-	°C/W
y_{JB}	Junction-to-board characterization parameter	-	-	-	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.5 Thermal Information - Dual

THERMAL METRIC (1)		LM2903L-Q1		UNIT
		DGK (VSSOP)	RUG (X2QFN)	
		10 PINS	10 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	-	150	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	-	58	°C/W
R_{qJB}	Junction-to-board thermal resistance	-	78	°C/W
y_{JT}	Junction-to-top characterization parameter	-	1.3	°C/W
y_{JB}	Junction-to-board characterization parameter	-	78	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	-	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

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5.6 Electrical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V-) = 5V, V_{CM} = (V-) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_T	Input threshold voltage	V_S = 5 to 36V	–2.5	±0.3	2.5	mV
V_T	Input threshold voltage	V_S = 5 to 36V, T_A = –40°C to +125°C	-3		3	
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 5V, No Load, Output Low		250	400	µA
I_Q	Quiescent current per comparator	V_S = 36V, No Load, Output Low, T_A = –40°C to +125°C			600	
INPUT BIAS CURRENT						
I_B	Input bias current			-3.5	-25	nA
I_B	Input bias current	T_A = –40°C to +125°C			-50	nA
I_{OS}	Input offset current		-10	0.5	10	nA
I_{OS}	Input offset current	T_A = –40°C to +125°C	-25		25	nA
INPUT CAPACITANCE						
INPUT VOLTAGE RANGE						
V_{IH_CLR}	Voltage input high threshold of CLR		1.1			V
V_{IL_CLR}	Voltage input low of threshold CLR				0.6	V
$V_{CM\text{-}Range}$	Common-mode voltage range (1)	V_S = 3 to 36V	(V–)		(V+) - 1.5	V
$V_{CM\text{-}Range}$		V_S = 3 to 36V, T_A = –40°C to +125°C	(V–)		(V+) - 2	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; R_L ≥ 15k to (V+)	50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} ≤ 4mA, V_{ID} = -1V		110	400	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} ≤ 4mA, V_{ID} = -1V, T_A = –40°C to +125°C			550	mV
I_{LKG}	Open-drain output leakage current	(V+) = V_O = 5V; V_{ID} = 1V		0.1	20	nA
I_{LKG}	Open-drain output leakage current	(V+) = V_O = 36V; V_{ID} = 1V		0.3	50	nA
I_{OL}	Low Level Output Current	V_{OL} = 1.5V; V_{ID} = -1V; VS = 5V	6	21		mA

(1) The voltage at either input can not be allowed to go negative by more than 0.3V otherwise output can be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by VCC – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum VCC level and the comparator provides a proper output state. Either or both inputs can go to maximum VCC level without damage.

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5.7 Switching Characteristics

V_S = 5V, CLR = 5V_{PP}, V_{O_PULLUP}=5V, V_{CM} = V_S/2, C_L = 15pF, R_L = 5.1k Ohm, T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	TTL input Delay from mid-point of input to mid-point of output, R_P = 5.1kΩ		300		ns
T_{PD-HL}	Propagation delay time, high-to-low	Input overdrive = 5mV, Input step = 100mV from mid-point of input to mid-point of output, R_P = 5.1kΩ		1000		ns
$T_{PD-CLR-F}$	Clear Fall to Latch Reset propagation delay time	CLR = 1.8V to 5V, V_{ID} = 100mV, R_P = 5.1kΩ Delay from CLR falling edge signal to normal output HIGH condition (R_P to Vpull-up)			650	ns
CLR_Min_Pulse_Width	Minimum Clear Hold Pulse time to register latch disable and transition output state	CLR = 1.8V to 5V, V_{ID}= +100 mV Minimum CLR pulse size required to register a change of state (latch reset) upon CLR falling edge		70		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100mV		20		ns
POWER ON TIME						

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5.8 Typical Characteristics

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

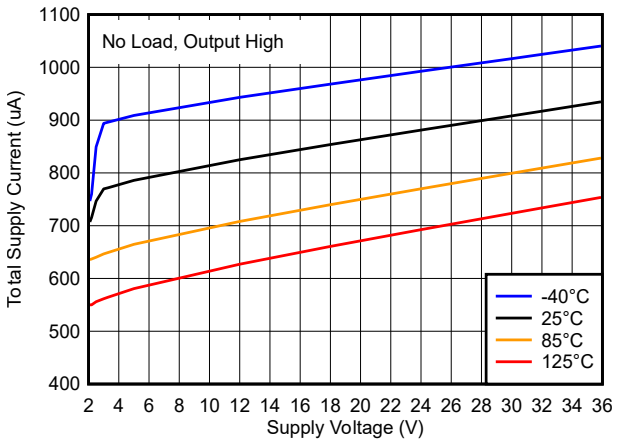

Figure 5-1. Total Supply Current vs Supply Voltage

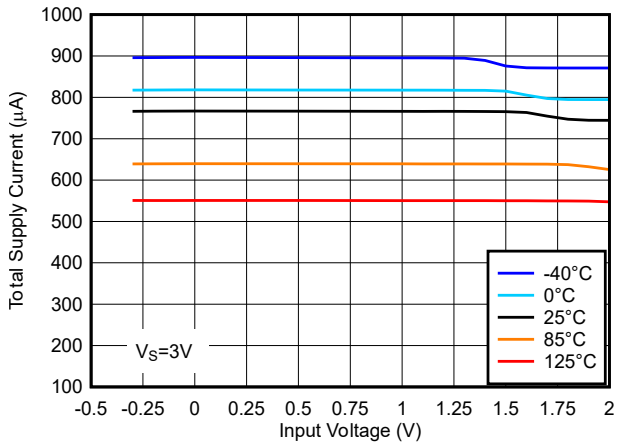

Figure 5-2. Total Supply Current vs Input Voltage at 3V

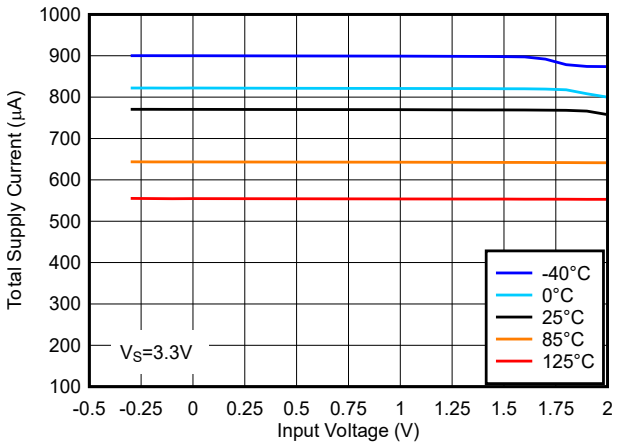

Figure 5-3. Total Supply Current vs Input Voltage at 3.3V

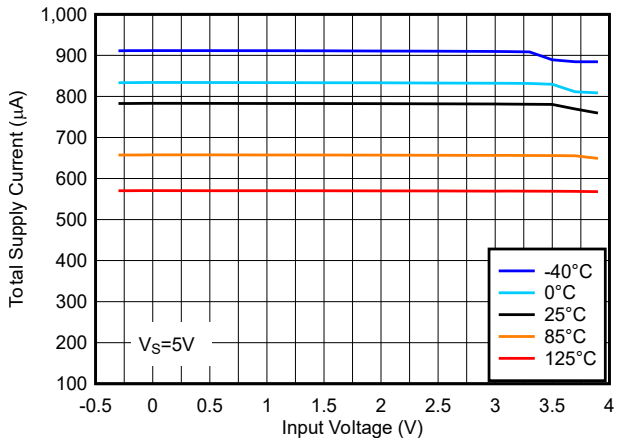

Figure 5-4. Total Supply Current vs Input Voltage at 5V

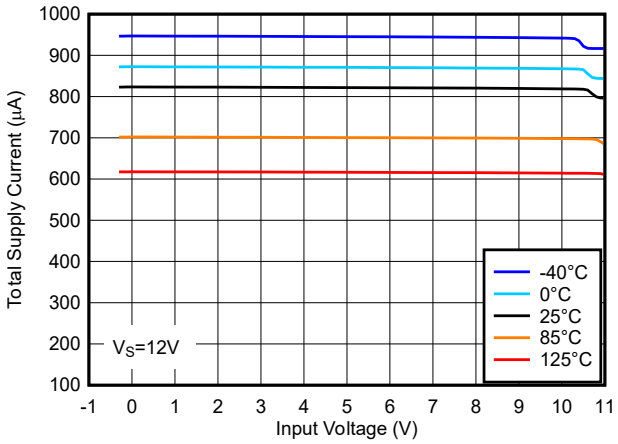

Figure 5-5. Total Supply Current vs Input Voltage at 12V

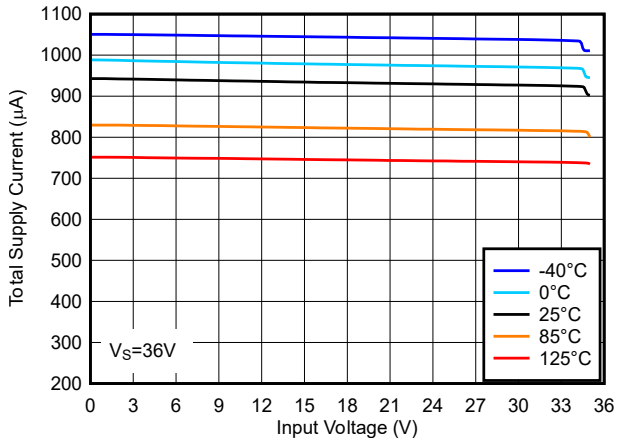

Figure 5-6. Total Supply Current vs Input Voltage at 36V

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5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

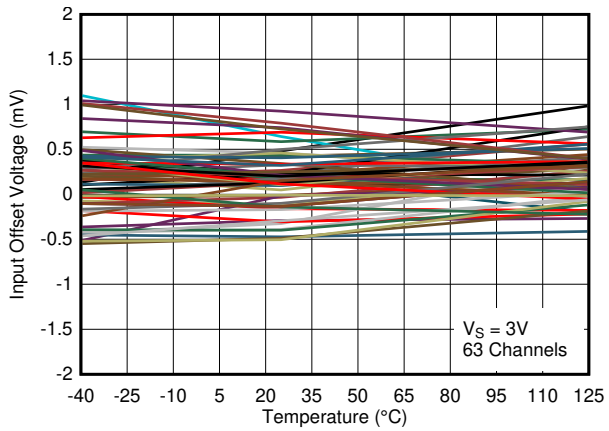

Figure 5-7. Input Offset Voltage vs Temperature at 3V

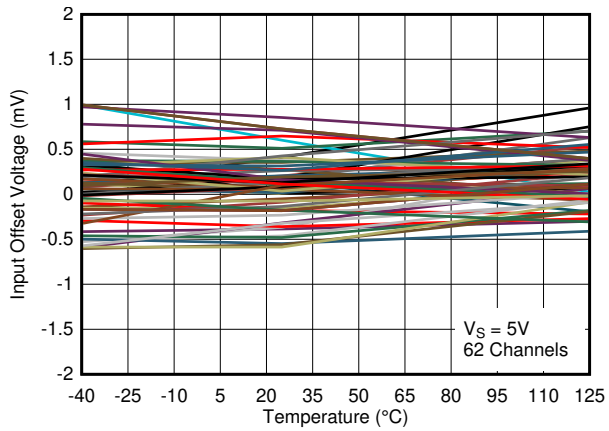

Figure 5-8. Input Offset Voltage vs Temperature at 5V

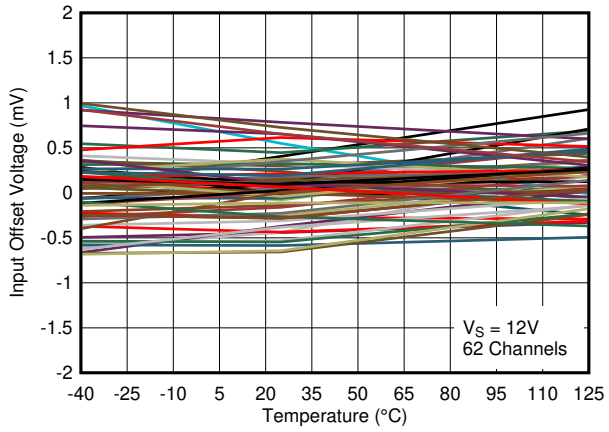

Figure 5-9. Input Offset Voltage vs Temperature at 12V

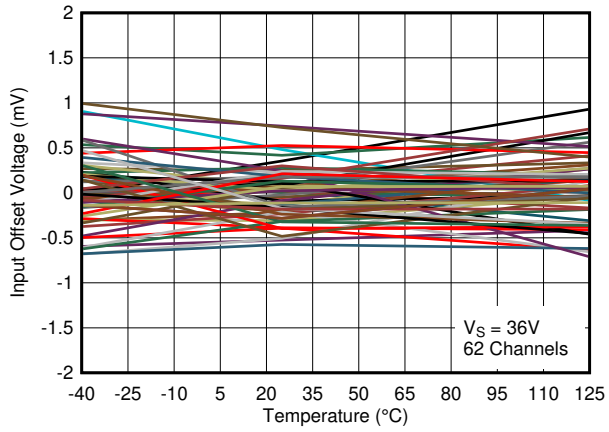

Figure 5-10. Input Offset Voltage vs Temperature at 36V

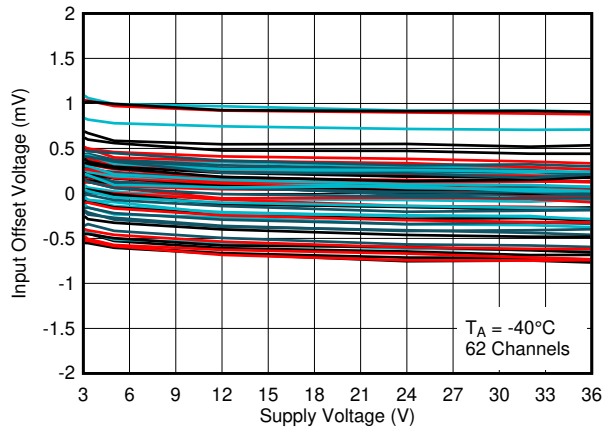

Figure 5-11. Input Offset Voltage vs Supply Voltage at -40°C

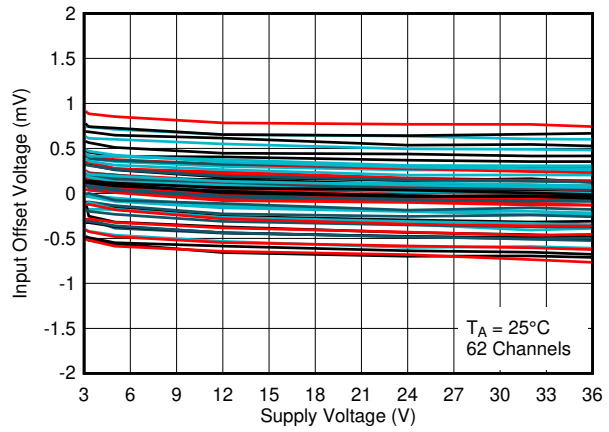

Figure 5-12. Input Offset Voltage vs Supply Voltage at 25°C

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

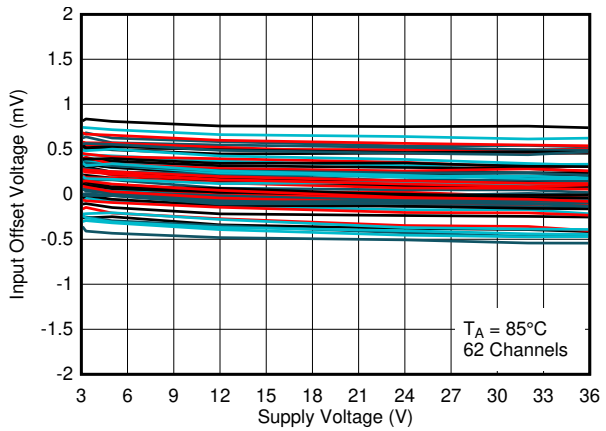

Figure 5-13. Input Offset Voltage vs Supply Voltage at 85°C

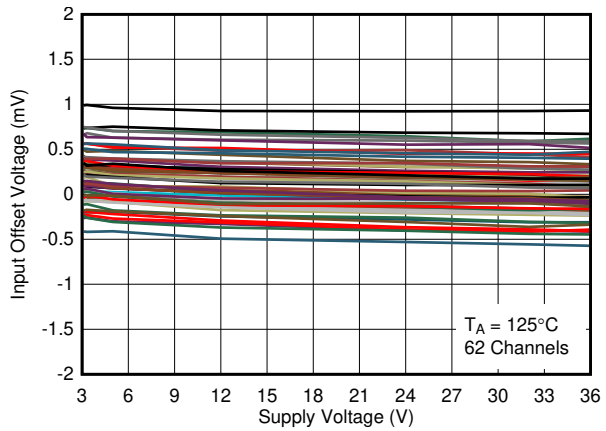

Figure 5-14. Input Offset Voltage vs Supply Voltage at 125°C

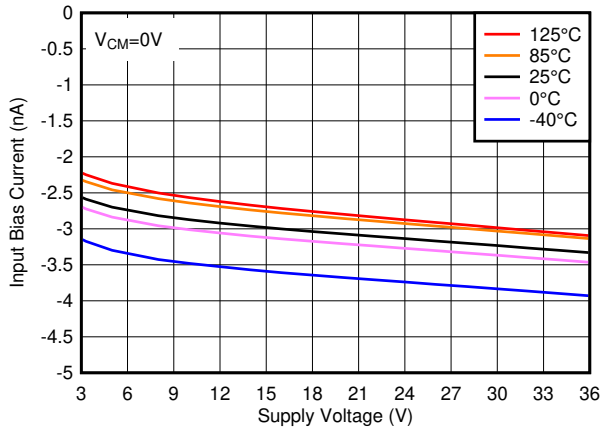

Figure 5-15. Input Bias Current vs Supply Voltage

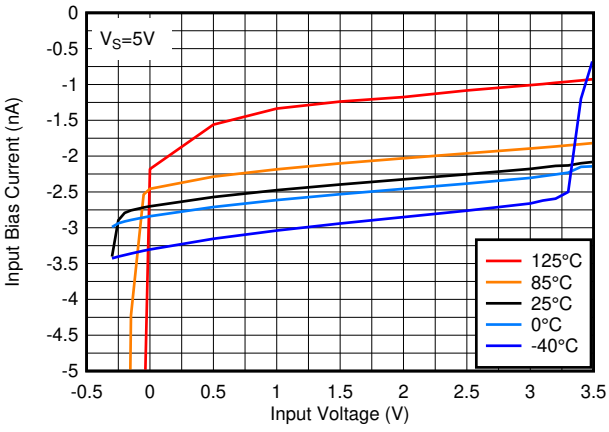

Figure 5-16. Input Bias Current vs Input Voltage at 5V

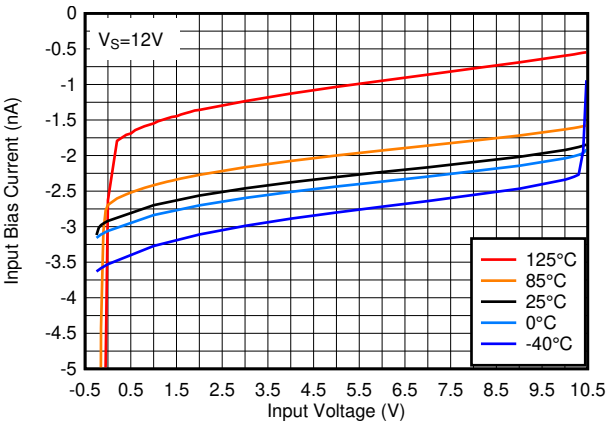

Figure 5-17. Input Bias Current vs Input Voltage at 12V

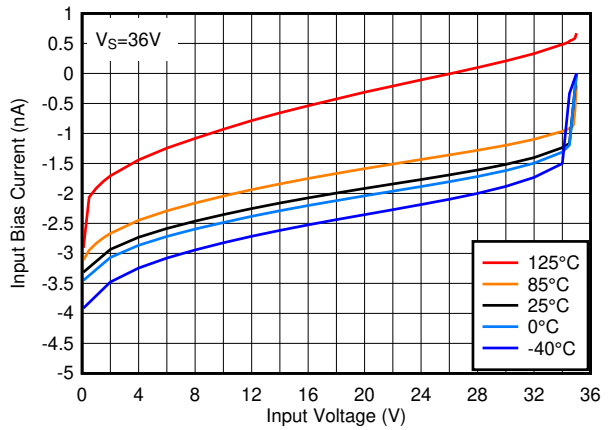

Figure 5-18. Input Bias Current vs Input Voltage at 36V

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5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

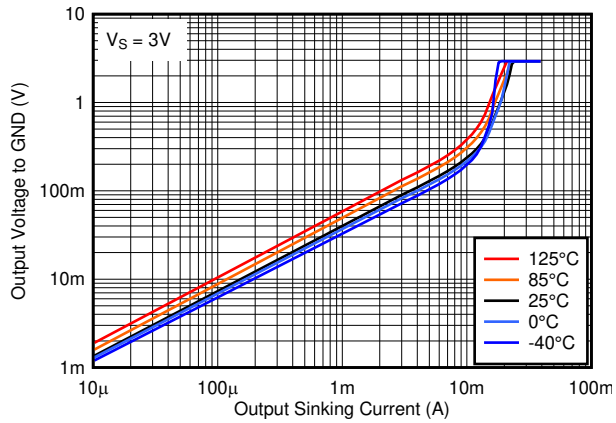

Figure 5-19. Output Low Voltage vs Output Sinking Current at 3V

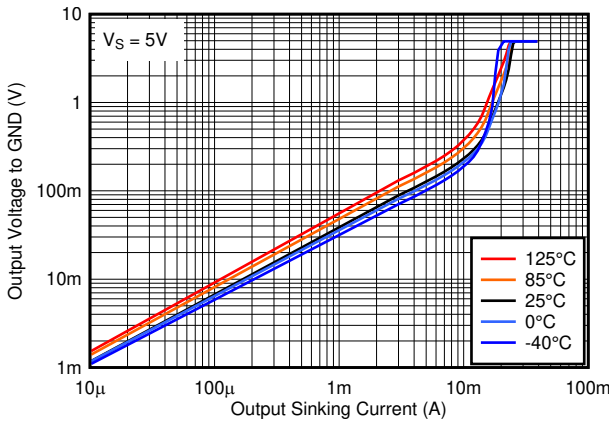

Figure 5-20. Output Low Voltage vs Output Sinking Current at 5V

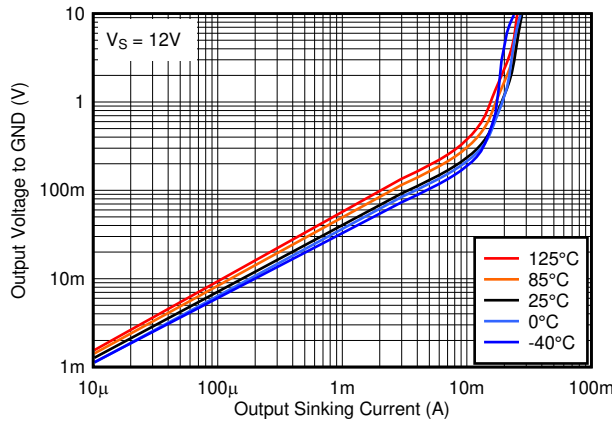

Figure 5-21. Output Low Voltage vs Output Sinking Current at 12V

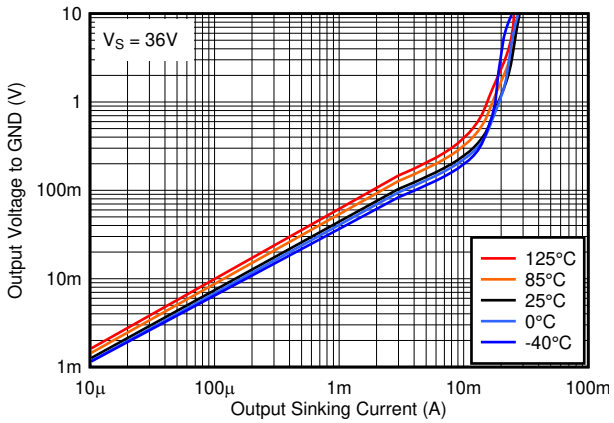

Figure 5-22. Output Low Voltage vs Output Sinking Current at 36V

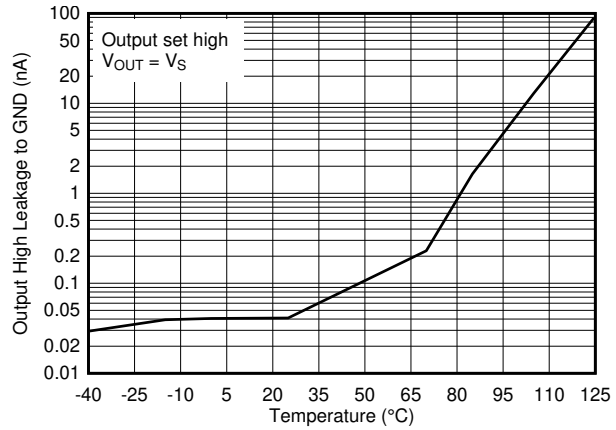

Figure 5-23. Output High Leakage Current vs Temperature at 5V

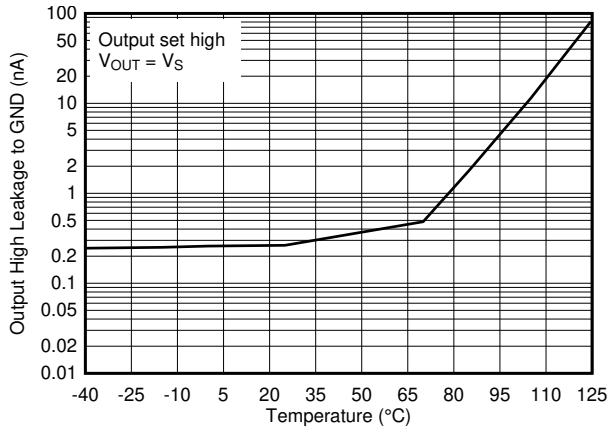

Figure 5-24. Output High Leakage Current vs Temperature at 36V

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

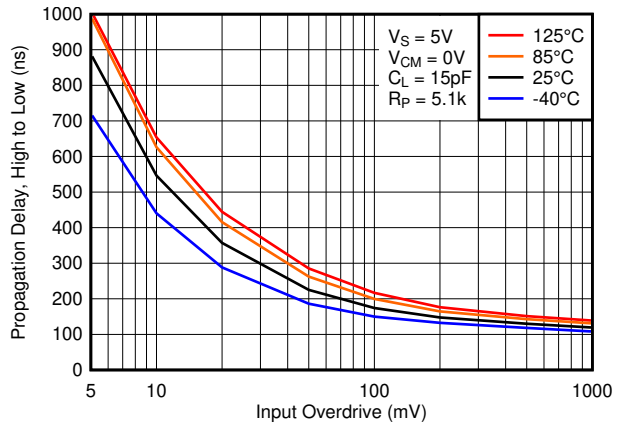

Figure 5-25. High to Low Propagation Delay vs Input Overdrive Voltage, 5V

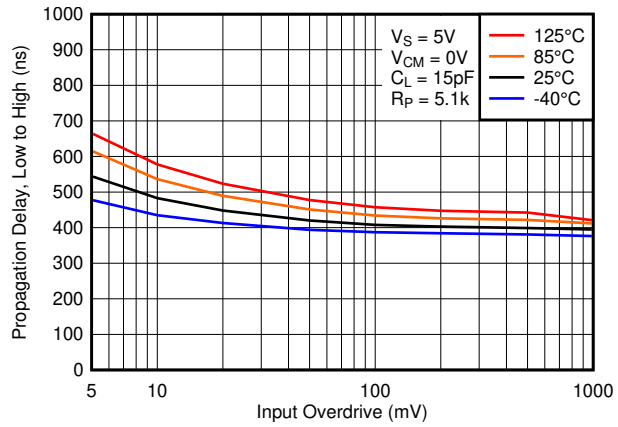

Figure 5-26. Low to High Propagation Delay vs Input Overdrive Voltage, 5V

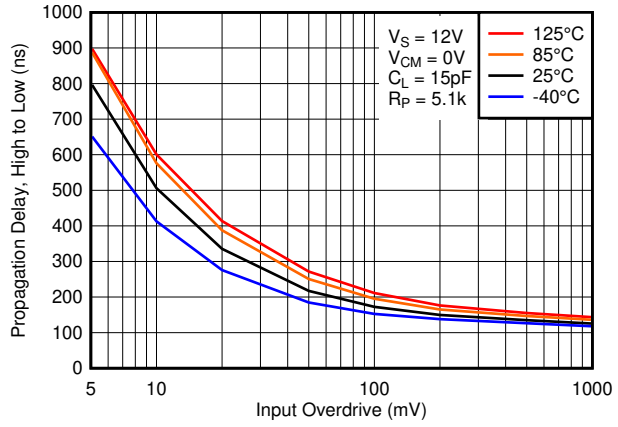

Figure 5-27. High to Low Propagation Delay vs Input Overdrive Voltage, 12V

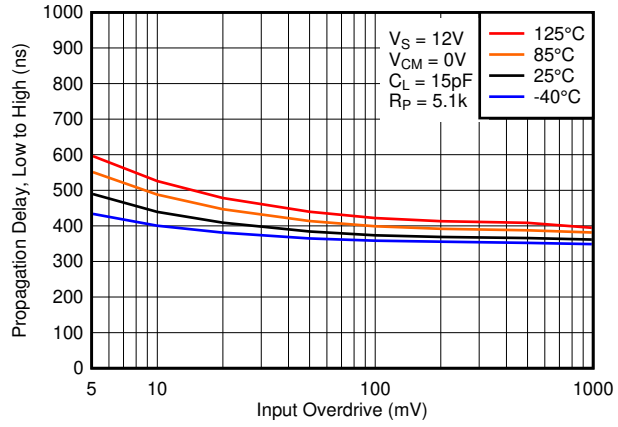

Figure 5-28. Low to High Propagation Delay vs Input Overdrive Voltage, 12V

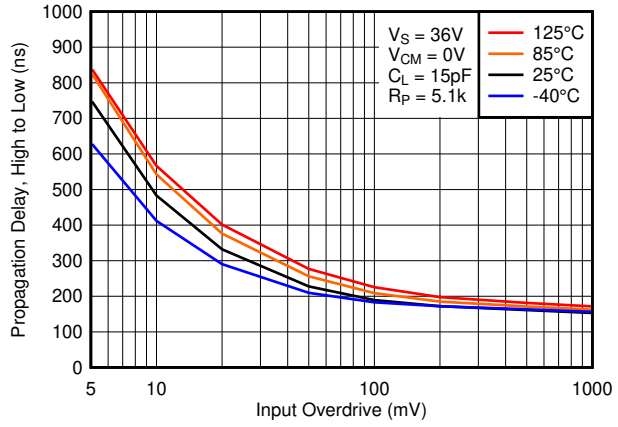

Figure 5-29. High to Low Propagation Delay vs Input Overdrive Voltage, 36V

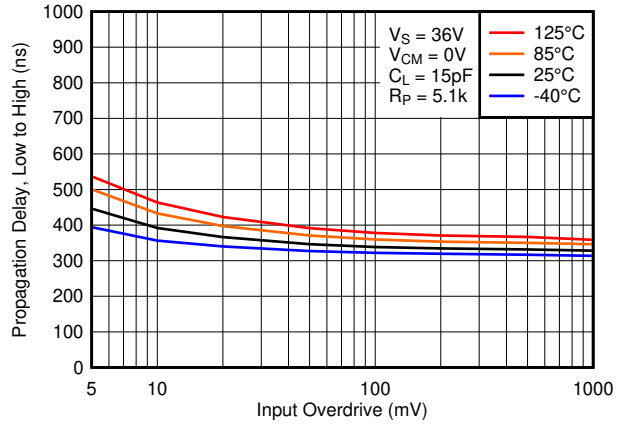

Figure 5-30. Low to High Propagation Delay vs Input Overdrive Voltage, 36V

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5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

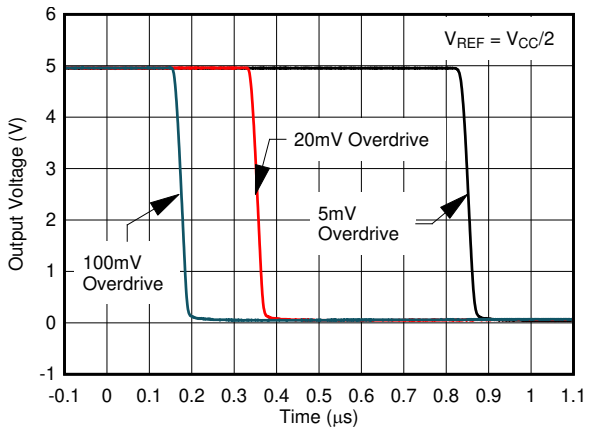


Figure 5-31. Response Time for Various Overdrives, High-to-Low Transition

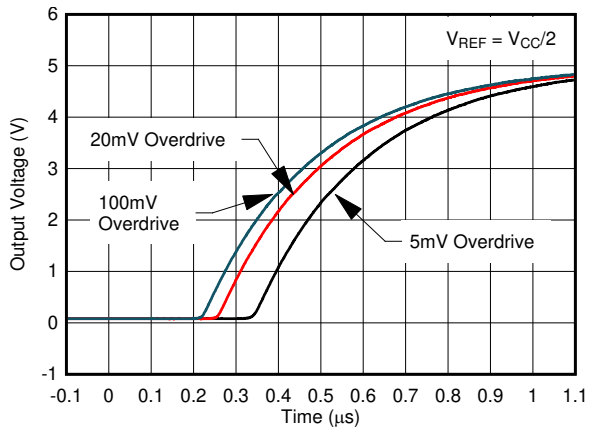


Figure 5-32. Response Time for Various Overdrives, Low-to-High Transition

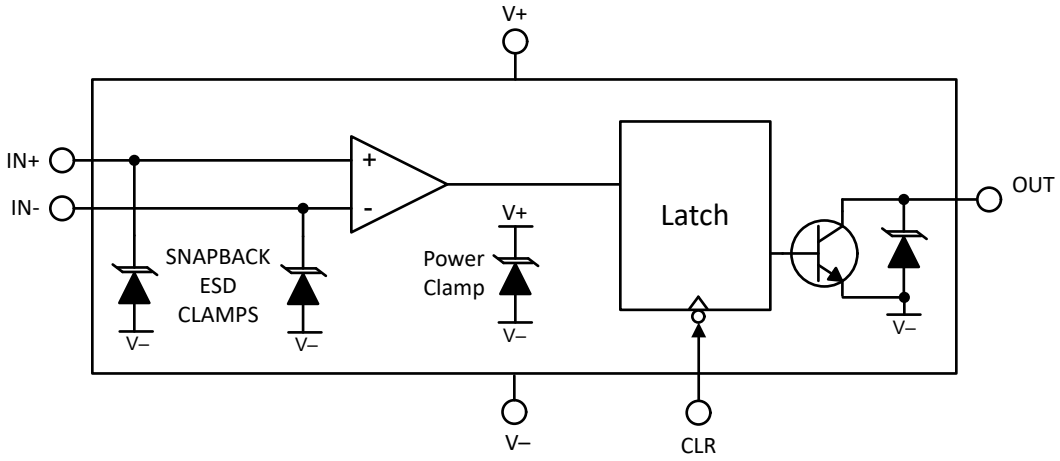
ADVANCE INFORMATION

6 Detailed Description

6.1 Overview

The LM2903L-Q1 and TI331-Q1 are a single and dual channel latching comparator with a open-drain output. The device offers low input offset voltage, fault-tolerant inputs and an excellent speed-to-power combination with a propagation delay of 300ns with a quiescent supply current of 300µA per channel.

6.2 Functional Block Diagram



6.3 Feature Description

The unique feature of the TL331L-Q1 and LM2903L-Q1 is the output latching capability. The output latches upon the first negative threshold crossing to allow capturing of an event or error condition without the full attention of a system controller. This allows events to be captured at start up while the system controller is still initializing. The system controller can reset the latch after performing any needed tasks.

These comparators also feature fault-tolerant inputs that can go up to 36V without damage. This makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

6.4 Device Functional Modes

6.4.1 Outputs

6.4.1.1 Comparator Output

The TL331L-Q1 and LM2903L-Q1 features an open-collector (also commonly called open-drain) sinking-only output stage enabling the output logic levels to be pulled up to any voltage up to 36V, independent of the comparator supply voltage (V_S). The open-collector output also allows logical OR'ing of multiple open-collector outputs and logic level translation.

Unused open-collector outputs can be left floating, or can be tied to the V- pin if floating pins are not allowed.

The open-collector output protection consists of a ESD clamp between the output and V- to allow the output to be pulled to any voltage up to a maximum of 36V, even if the pull-up voltage exceeds V+.

6.4.2 Output Latching

The device has an output that latches upon the first output high-to-low transition after being armed. The output stays latched until the falling edge of the CLR pin.

6.4.2.1 Clear (CLR) Input

When CLR is high, and the output is not in a latched condition, the comparator is armed and ready to respond to next high-to-low output condition to latch.

The CLR input clears the output latch on the high-to-low (falling) edge of the CLR input.

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If CLR is held low, the comparator is in "Transparent" mode and the output continues to respond to input conditions. See Section 6.4.2.2.

The latch is armed when the CLR input returns to high and awaits the next high-to-low output transition.

During the short CLR pulse to clear the latch, there is a possibility that the output transitions during the time the latch is being reset if the inputs are crossing. The CLR reset pulse must be as short as possible for the system to prevent false pulses. The recommended minimum CLR pulse is 200ns.

There can be a setup-time contention if the CLR pin is transitioning (falling) at the same time as the comparator output transitions. The output state is indeterminate during the CLR falling edge time. The recommendation is to make the CLR falling-edge as fast as possible to avoid this contention (<100ns fall time).

The CLR pin is a Failsafe input, accepting logic high levels up to 36V, independent of the comparator supply voltage. The 0.6V maximum threshold accepts digital logic level inputs from 15V CMOS, to low voltage TTL, to 1.2V CMOS logic.

Floating the CLR input is not recommended. If "normal", "unlatched" mode is desired, tie that channels CLR input to V-.

Thought must be taken as to if an external pull-up or pull-down resistor is required on the CLR pin to make sure the CLR pin is in the proper state during start-up when the controller output is Hi-Z during controller initialization. The controller must initialize the GPIO pin as soon as possible after start-up.

6.4.2.2 Transparent Mode

When the CLR pin is held low, the comparator is in "Transparent" mode. In transparent mode, latching is disabled and the output continues to respond to the input conditions, similar to a "normal", non-latching comparator.

If both latched and unlatched comparator paths are desired, the dual LM2903L can be used with one channel in latching mode and the other channel operating in the transparent mode by tying the non-latching channel CLR pin to V-.

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6.4.2.3 Latch Behavior

After power-on, TI recommends that the CLR pin be toggeled low to reset the latch. With the CLR pin high, the latch is armed and **latches low** upon the first **high-to-low** output transition. The following is a summary of the latch operation.

When the CLR pin is held low, the output is in continuous "Transparent" mode (output follows inputs continuously with no latching).

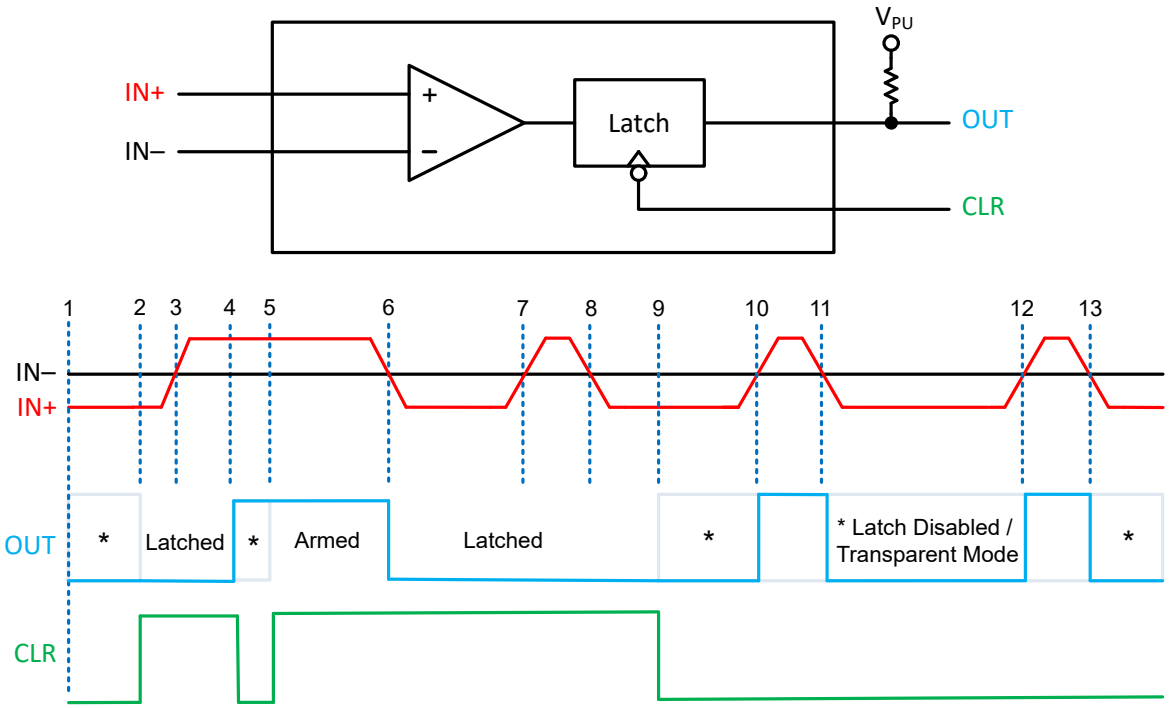

Figure 6-1. Latch Timing Example

* Latch disabled in "Transparent mode"

1. IN- > IN+, CLR is low, output is low in transparent mode.
2. CLR brought high and arms latch, IN– still greater than IN+, output remains low and immediately latches low.
3. IN+ > IN–, but output remains low due to latch condition.
4. CLR is brought low to clear latched output. During the time the CLR pin is low, the output is in transparent mode. IN+ > IN–, so output goes high in transparent mode
5. CLR is brought high, disabling transparent mode and arming the latch. IN+ > IN–, output remains high.
6. +IN crosses -IN, output goes low and latches low.
7. IN+ > IN–, output remains latched low.
8. IN- >IN+, output remains latched low.
9. CLR brought low, clearing latch and enabling transparent mode.
10. IN+ > IN–, output immediately goes high in transparent mode.
11. IN– > IN+, output immediately goes low in transparent mode.
12. IN+ > IN–, output immediately goes high in transparent mode.
13. IN– > IN+, output immediately goes low in transparent mode.

6.4.3 Inputs

6.4.3.1 Fail-Safe Inputs and Input Voltage Range

The inputs are fault tolerant up to 36V independent of V+. Fault tolerant is defined as maintaining the same high input impedance when V+ is un-powered or within the recommended operating ranges.

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The specified input voltage range is from V- to 2V below V+, per input, across temperature.

The fault tolerant inputs can be any value between 0V and 36V, even while V_S is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the maximum specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains high impedance even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid, the output state is correct.

The following is a summary of input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both above and outside the specified input voltage range, the output is low.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain data sheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

6.4.3.2 Input Protection

The device incorporates internal ESD protection circuits on all pins. The inputs use a proprietary "snapback" type ESD clamp from each pin to V-. There is no "upper" ESD clamp to V+, which allows the input pins to exceed the supply voltage (V+). During an ESD event, the snapback diodes "short" and go low impedance to V- (like an SCR crowbar).

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct due to transients. The current must be limited 10mA or less (<1mA is recommended). This series resistance can also be part of any resistive input dividers or networks.

The ESD diodes can not clamp on the upper voltages. The ESD clamps do not "hold" at a fixed maximum voltage like a Zener diode. If the inputs are connected to a source that can exceed 36V, then external clamping is required to prevent exceeding the maximum input voltage.

6.4.3.3 Internal Hysteresis

This device does NOT have internal hysteresis. The latching function negates the need for hysteresis as the output latches upon the first output transition. The reference level must be set to the desired threshold level, and the input signals filtered to remove any noise or transients that can cause early triggering. External hysteresis is only needed in transparent mode.

6.4.3.4 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+) through a current limiting resistor (10kΩ typical).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 7-1. Output Conditions

INPUTS CONDITION	OUTPUT
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (can chatter)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output.

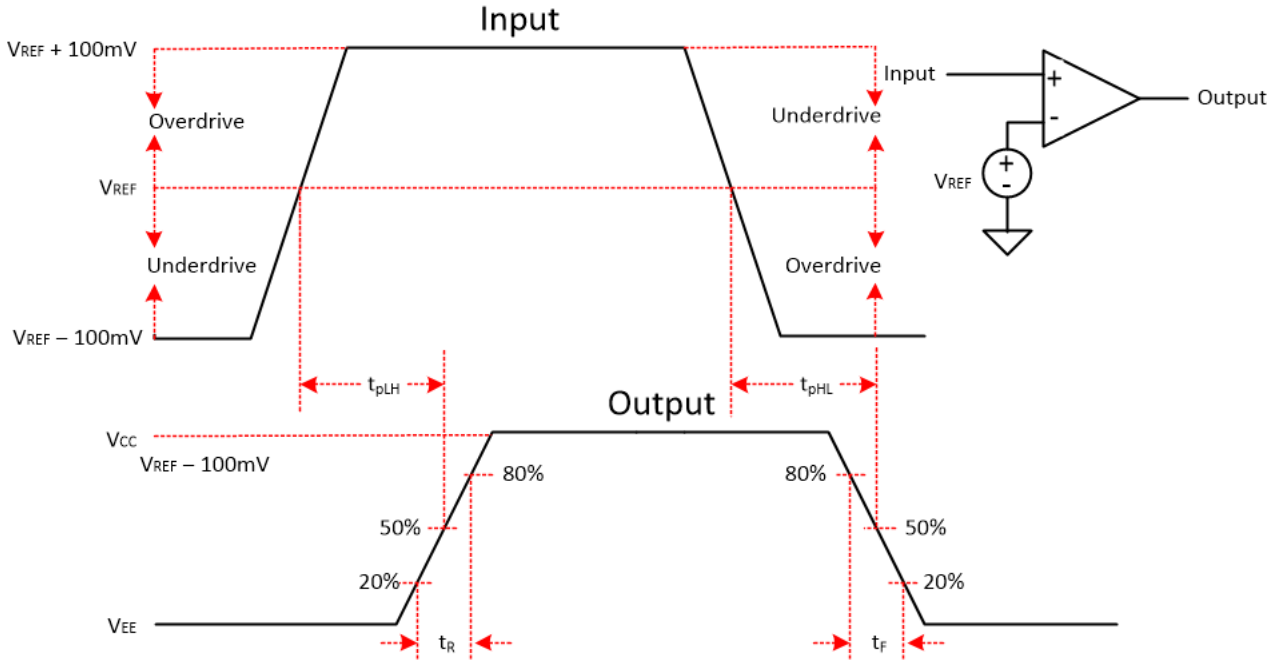

Figure 7-1. Comparator Timing Diagram

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7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 7-2 shows a simple latching window comparator circuit.

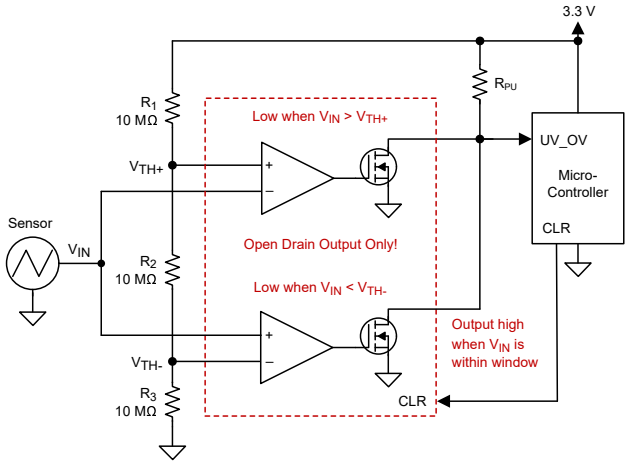

Figure 7-2. Window Comparator using LM2903L-Q1

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Latch (logic low output) when an input signal is less than 1.1V
- Latch (logic low output) when an input signal is greater than 2.2V
- Operate from a 5V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 7-2. Make R1, R2 and R3 each 100kΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 100kΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and non-inverting inputs of the two comparators. The two comparator outputs are Wire-OR'ed together.

The respective comparator outputs latches low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in Figure 7-3.

The CLR pin must be toggled high to low to high to reset the output and arm the window comparator.

7.2.1.3 Application Curve

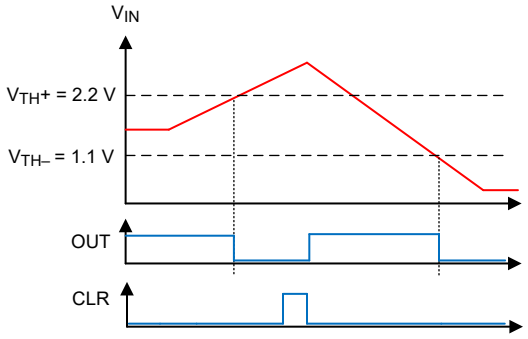

Figure 7-3. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.3 Power Supply Recommendations

Due to the fast output edges, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) and (V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications, maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V+ and V- pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V+ or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

7.4.2 Layout Example

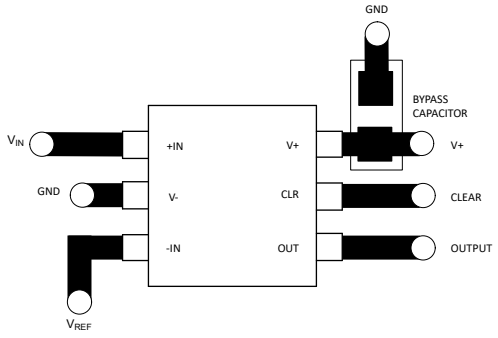

Figure 7-4. Single Layout Example

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLM2903LWRUGRQ1	Active	Preproduction	X2QFN (RUG) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

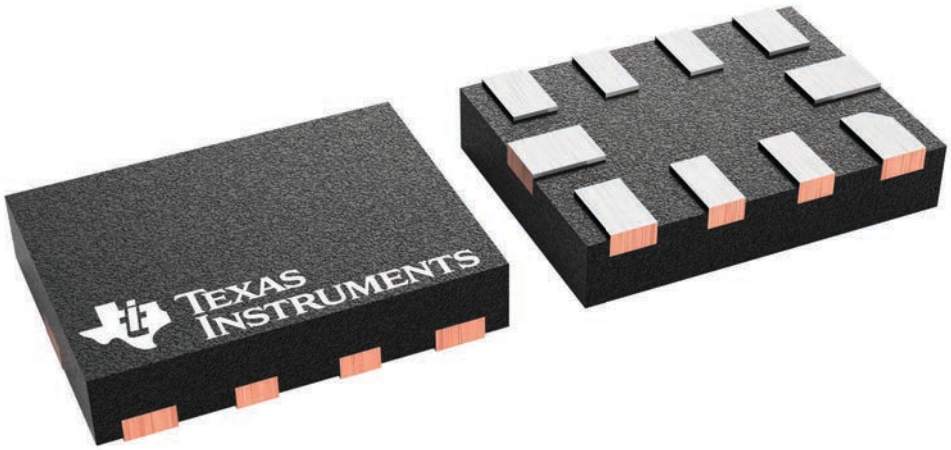
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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Last updated 10/2025