LM393-MIL Dual Differential Comparators

1 Features

- Single-Supply or Dual Supplies
- Wide Range of Supply Voltage
  - Maximum Rating: 2 V to 36 V
  - Tested to 30 V
- Low Supply-Current Drain Independent of Supply Voltage: 0.4 mA (Typical) Per Comparator
- Low Input Bias Current: 25 nA (Typical)
- Low Input Offset Voltage: 2 mV (Typical)
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS
- On Products Compliant to MIL-PRF-38535, All Parameters are Tested Unless Otherwise Noted. On All Other Products, Production Processing does not Necessarily Include Testing of All Parameters.

2 Applications

- Chemical or Gas Sensor
- Desktop PC
- Motor Control: AC Induction
- Weigh Scale

3 Description

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is 2 V to 36 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

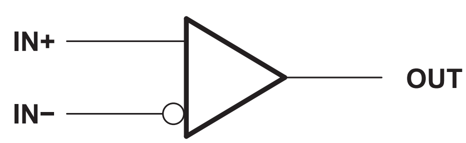
The LM393-MIL device is characterized for operation from 0°C to 70°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM393-MILD	SOIC (8)	4.90 mm × 6.00 mm
LM393-MILDGK	VSSOP (8)	3.00 mm x 5.00 mm
LM393-MILP	PDIP (8)	9.50 mm × 6.30 mm
LM393-MILPS	SO (8)	6.20 mm x 7.90 mm
LM393-MILPW	TSSOP (8)	6.40 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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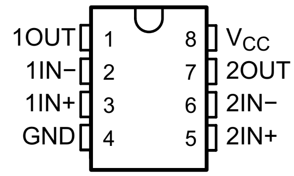
4 Revision History

DATE	REVISION	NOTES
June 2017	*	Initial release.

5 Pin Configuration and Functions

D, DGK, P, PS, or PW
8-Pin SOIC, VSSOP, PDIP, SO, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOIC, VSSOP, PDIP, SO, and TSSOP		
1OUT	1	Output	Output pin of comparator 1
1IN–	2	Input	Negative input pin of comparator 1
1IN+	3	Input	Positive input pin of comparator 1
GND	4	—	Ground
2IN+	5	Input	Positive input pin of comparator 2
2IN-	6	Input	Negative input pin of comparator 2
2OUT	7	Output	Output pin of comparator 2
V_{CC}	8	—	Supply Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		36	V
V_{ID}	Differential input voltage(3)		±36	V
V_I	Input voltage (either input)	–0.3	36	V
V_O	Output voltage		36	V
I_O	Output current		20	mA
	Duration of output short circuit to ground(4)	Unlimited		
T_J	Operating virtual-junction temperature		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}		2	30	V
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM393-MIL					UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	172	85	95	149	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		T_A = 25°C		2	5	mV
				T_A = 0°C to 70°C			9	
I_{IO}	Input offset current	V_O = 1.4 V		T_A = 25°C		5	50	nA
				T_A = 0°C to 70°C			250	
I_{IB}	Input bias current	V_O = 1.4 V		T_A = 25°C		–25	–250	nA
				T_A = 0°C to 70°C			–400	
V_{ICR}	Common-mode input-voltage range(1)			T_A = 25°C	0 to V_{CC} – 1.5			V
				T_A = 0°C to 70°C	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		T_A = 25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V	V_{ID} = 1 V	T_A = 25°C		0.1	50	nA
		V_{OH} = 30 V	V_{ID} = 1 V	T_A = 0°C to 70°C			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = –1 V	T_A = 25°C		150	400	mV
				T_A = 0°C to 70°C			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = –1 V	T_A = 25°C	6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5 V	T_A = 25°C		0.8	1	mA
			V_{CC} = 30 V	T_A = 0°C to 70°C			2.5	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V V_{IC} = $V_{ICR(min)}$		T_A = 25°C		1	2	mV
				T_A = 0°C to 70°C			4	
I_{IO}	Input offset current	V_O = 1.4 V		T_A = 25°C		5	50	nA
				T_A = 0°C to 70°C			150	
I_{IB}	Input bias current	V_O = 1.4 V		T_A = 25°C		–25	–250	nA
				T_A = 0°C to 70°C			–400	
V_{ICR}	Common-mode input-voltage range(1)			T_A = 25°C	0 to V_{CC} – 1.5			V
				T_A = 0°C to 70°C	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		T_A = 25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V	T_A = 25°C		0.1	50	nA
		V_{OH} = 30 V,	V_{ID} = 1 V	T_A = 0°C to 70°C			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = –1 V	T_A = 25°C		150	400	mV
				T_A = 0°C to 70°C			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = –1 V,	T_A = 25°C	6			mA
I_{CC}	Supply current (four comparators)	R_L = ∞	V_{CC} = 5 V	T_A = 25°C		0.8	1	mA
			V_{CC} = 30 V	T_A = 0°C to 70°C			2.5	

(1) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC}+ – 1.5 V, but either or both inputs can go to 30 V without damage.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF(1)(2)	100-mV input step with 5-mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.7 Typical Characteristics

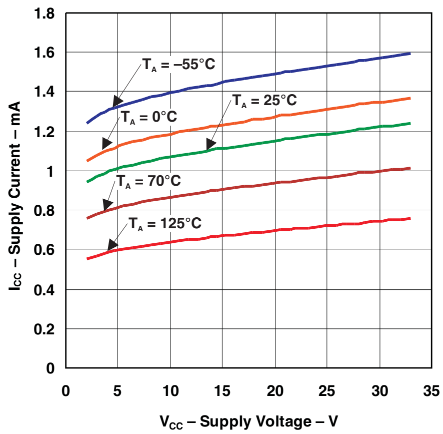


Figure 1. Supply Current vs Supply Voltage

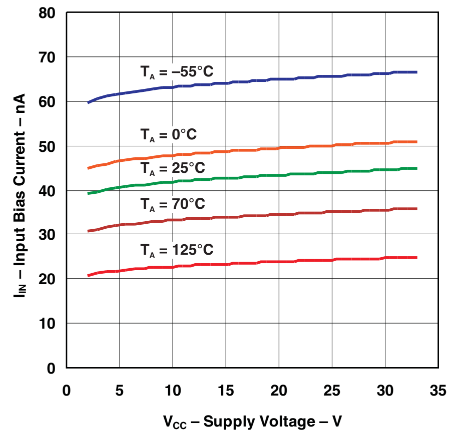


Figure 2. Input Bias Current vs Supply Voltage

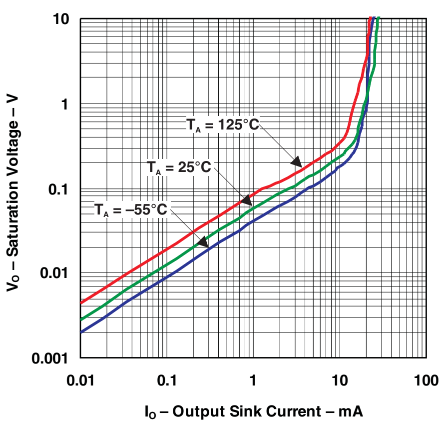


Figure 3. Output Saturation Voltage

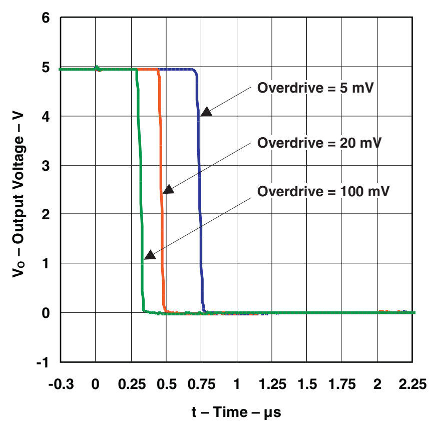


Figure 4. Response Time for Various Overdrives Negative Transition

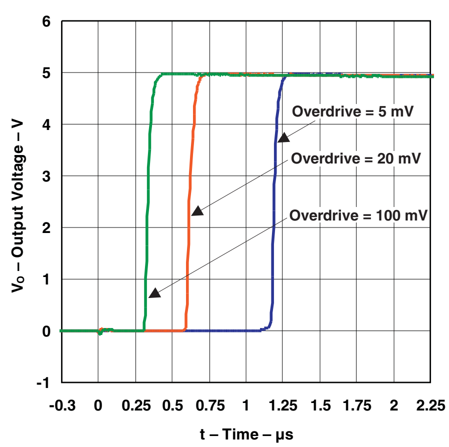


Figure 5. Response Time for Various Overdrives Positive Transition

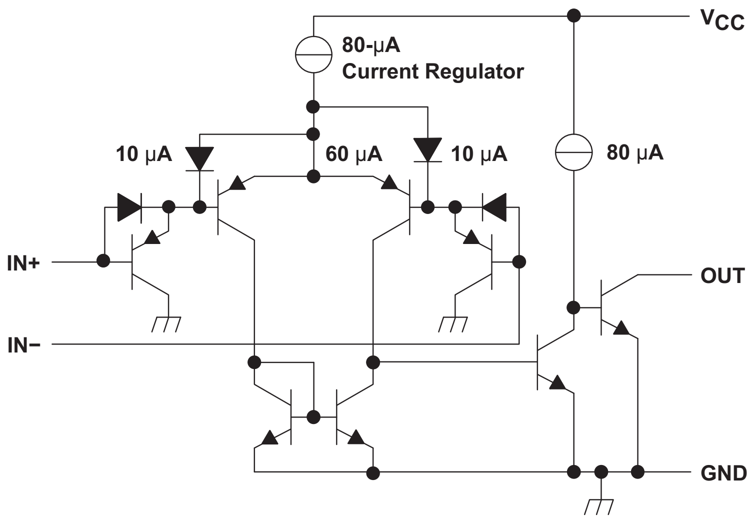
7 Detailed Description

7.1 Overview

The LM393-MIL is a dual comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V to 36 V), low Iq and fast response of the devices.

The open-drain output allows the user to configure the output logic low voltage (V_{OL}) and can be used to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	2
Transistors	30

Figure 6. Schematic (Each Comparator)

7.3 Feature Description

LM393-MIL consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing LM393-MIL to accurately function from ground to V_{CC}–1.5V differential input. This enables much head room for modern day supplies of 3.3 V and 5 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the positive input voltage is higher than the negative input voltage and the offset voltage. The VOL is resistive and will scale with the output current. See Figure 3 for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The LM393-MIL operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LM393-MIL will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM393-MIL optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

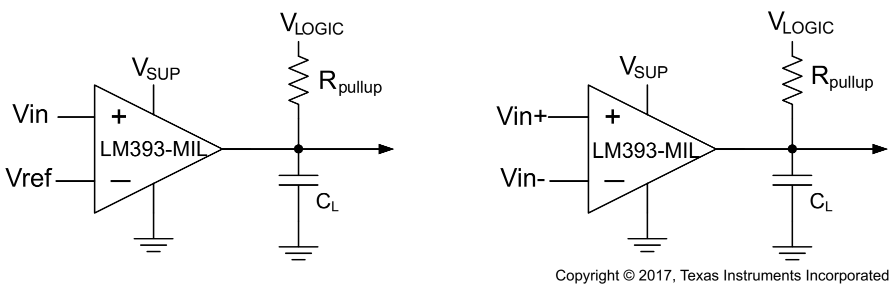


Figure 7. Single-Ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-1.5 V
Supply Voltage	2 V to 36 V
Logic Supply Voltage	2 V to 36 V
Output Current (R_{PULLUP})	1 µA to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using LM393-MIL in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC}– 2.0 V. This limits the input voltage range to as high as V_{CC}– 2.0 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common-mode range:
   (a) If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   (b) If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common-mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 8 and Figure 9 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pullup voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use *Typical Characteristics* to determine V_{OL} based on the output current.

The output current can also effect the transient response. See *Response Time* for more information.

8.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE})..

- The positive response time (τ_P) is approximately $\tau_P \sim R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N \sim R_{CE} \times C_L$
  – R_{CE} can be determine by taking the slope of *Typical Characteristics* in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

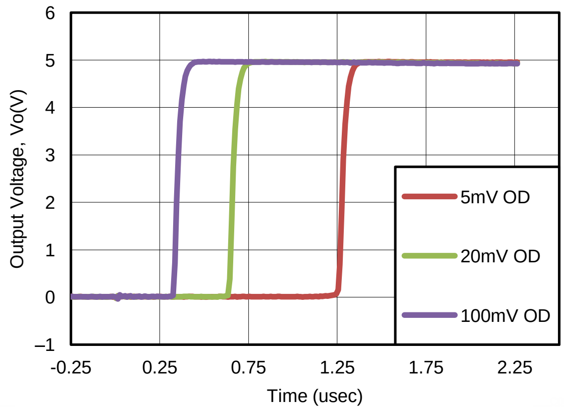


Figure 8. Response Time for Various Overdrives (Positive Transition)

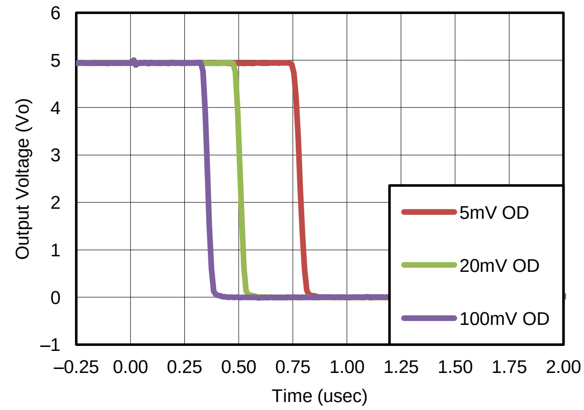


Figure 9. Response Time for Various Overdrives (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the input common-mode range of the comparator and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. To achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC GND pin and system ground.

10.2 Layout Example

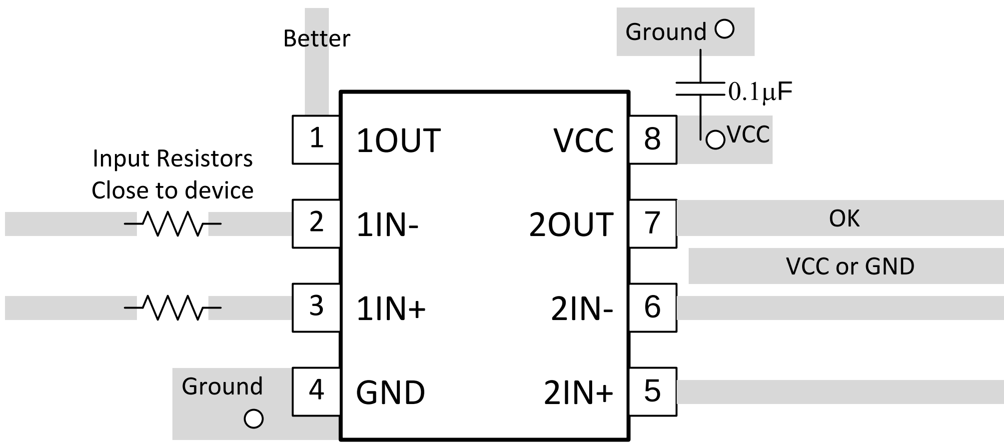


Figure 10. LM393-MIL Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393 MDC	ACTIVE	DIESALE	Y	0	400	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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