LM654xx-Q1 Pin-Compatible 20A (25A Peak), 15A, 12A, 10A, Stackable Automotive Buck Converters With Mitigated Interference and Noise Technology (MINT)

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Built in clocking for stacking of converters
- Internal or external compensation
- Pin selectable output voltage 3.3V and 5V fixed or adjustable from 0.8V to 0.9 × V_{IN}
- Wide input voltage range: 3V to 36V
- Mitigated interference and noise technology – architecture 1 (MINT 1)
  - Optimized for low EMI requirements
  - Facilitates CISPR 25 Class 5 compliance
  - Mode pin configurable +8.5% or +17% dual-random spread spectrum reducing peak emissions
  - Enhanced HotRod™ QFN package with symmetrical pinout
- Switching frequency from 300kHz to 2.2MHz
  - Pin-configurable AUTO or FPWM operation
  - Can be synchronized to external clock
- Low minimum on time: 32ns (typical)
  - Enables 36V to 3.3V conversion at 2.2MHz
- High-efficiency and high power density
  - > 94% efficiency at $12V_{IN}$ to $5V_{OUT}$, I_{OUT} = 15A, 400kHz
  - 8µA PFM no-load input current with bias pin at V_{OUT}
  - 4.5mm × 4.5mm eQFN-26 with wettable flanks

2 Applications

- Advanced driver assistance systems (ADAS)
- Automotive infotainment and cluster
- Hybrid, electric, and powertrain systems

3 Description

The LM654xx-Q1 is a buck converter family designed for high efficiency, high-power density, and low EMI performance with mitigated interference and noise technology (MINT 1) switcher technology for automotive applications. The converter operates over a wide input voltage range of 3V to 36V with pin selectable fixed output voltages of 3.3V and 5V or an adjustable output.

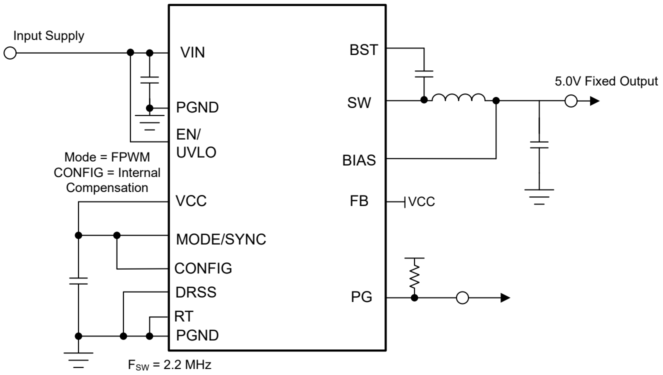
The low EMI operation is enabled with minimized loop inductance, optimized SW node slew-rate, and pin-selectable +8.5% or +17% dual-random spread spectrum (DRSS). The DRSS significantly reduces peak emissions through a combination of triangular and pseudo-random modulation while keeping output voltage ripple very low.

The current-mode control architecture with 32ns typical minimum on-time allows high conversion ratios at high frequencies, fast transient response, and excellent load and line regulation.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM654B0-Q1	VDA (WQFN-FCRLF, 26)	4.5mm × 4.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	ENGINEERING PART NUMBER	OUTPUT CURRENT	TOP-SIDE EXPOSED THERMAL PAD	BOTTOM EXPOSED THERMAL PAD	PACKAGE	JUNCTION TEMPERATURE RANGE
LM654B0-Q1	LM654B0VDARQ1	PLM654B0VDARQ1	20	YES	YES	VDA (26)	–40°C to 150°C
LM654A5-Q1 (1)	LM654A5VDARQ1	PLM654A5VDARQ1	15	YES	YES	VDA (26)	–40°C to 150°C
LM654A2-Q1 (1)	LM654A2VDARQ1	PLM654A2VDARQ1	12	YES	YES	VDA (26)	–40°C to 150°C
LM654A0-Q1 (1)	LM654A0VDARQ1	PLM654A0VDARQ1	10	YES	YES	VDA (26)	–40°C to 150°C

(1) Preview information (not Production Data)

5 Pin Configuration and Functions

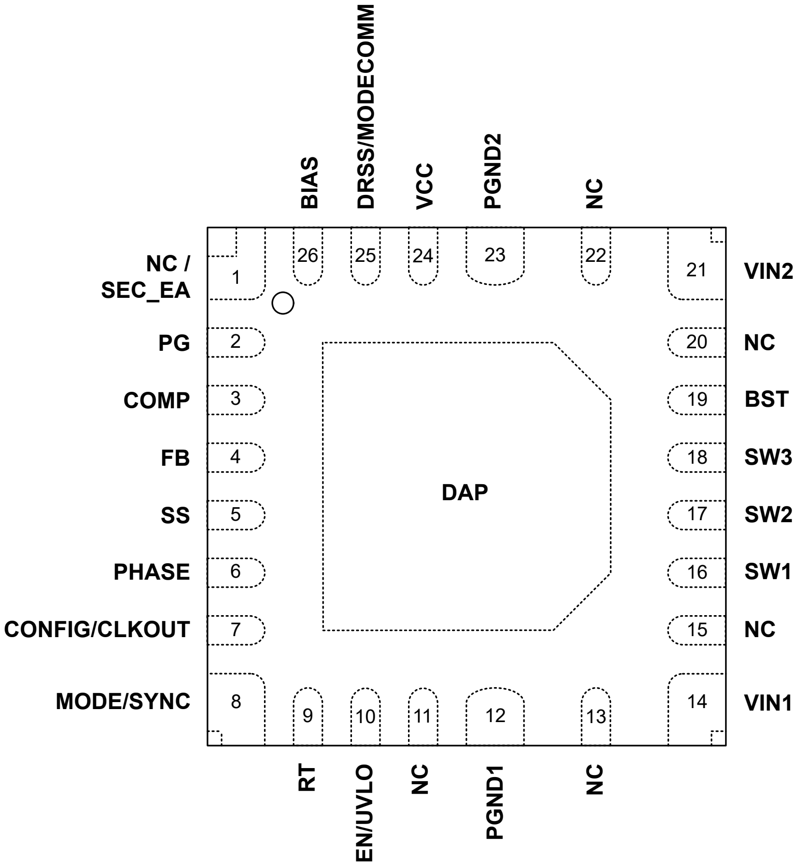


Figure 5-1. VDA 26-Pin WQFN-FCRLF Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC / SEC_EA	1	—	**For the primary device:** Leave floating or tie to ground. **For secondary devices**: tie to VCC to enable secondary error amplifier. This action increases the loop gain of the multiphase design. Tie to GND to disable secondary error amplifier. Enabling the error amplifier requires the FB pin of the secondary to be configured with either a resistor divider or configured for fixed 3.3 or 5V.
PG / NC	2	O	**For the primary device**: Power-Good output pin. This pin is an open-collector output that goes low if VOUT is outside of the specified regulation window. During power up, PG pulls low after VIN is above 1.25V and remain low until the part is enabled and soft start is complete. **For secondary devices**: This pin is grounded internally and must be left floating or tied to ground
COMP	3	A	**For the primary device**: External compensation pin. This pin is the output of the transconductance amplifier. If used, connect the compensation network from the COMP pin to GND. If unused, the pin can be tied to ground. **For secondary devices**: Tie to the COMP pin of the PRIMARY device to all secondary COMP pins. When secondary error amplifier is used (SEC_EA = VCC), the values of Rcomp and Ccomp must be scaled based on the number of devices with the error amplifier enabled.

Table 5-1. Pin Functions (continued)

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
FB	4	A	**For the primary device**: Feedback pin. Connect this pin to a feedback divider tap point for adjustable output options. The regulation threshold is 0.8V. Connect to GND to configure 3.3V fixed output voltage. Connect to VCC to configure 5V fixed output voltage. When using fixed output voltage settings the BIAS pin must be connected to VOUT and provides the feedback path for the error amplifier. **For secondary devices**: Enable the secondary error amplifier with (SEC_EA = VCC) or disable with (SEC_EA = GND). When the secondary error amplifier is disabled, the FB can be left floating. When enabling the secondary error amplifier the FB must be configured as for the primary. Enabling the error amplifier decreases the routing sensitivity of the COMP trace by doubling the effective transconductance of the design.
SS	5	A	Soft-start delay programming pin. If the SS pin is left open, the internal soft-start circuit ramps the FB reference from zero to full value in 2.6ms (typical). If a capacitor is connected from the SS pin to GND, the soft-start time can be set to a higher value. See Equation 5. For multiphase designs, tie the SS pins of all the devices together.
PHASE	6	I	**For the primary device**: Grounding this pin sets the output clock from CONFIG to 180 degrees out of phase from the primary and is useful for one or two phase designs. Connecting this pin to VCC sets the output clock from CONFIG in phase with the primary and is useful for three or more phases where the phase shift of each secondary can be set individually with the phase pin voltage of the secondary. **For secondary devices**: A voltage between 0 and 1V on this pin corresponds to a phase shift of 0 to 360 degrees of the clock frequency on secondary devices. To easily configure the phase shift on the secondary devices set frequency on RT pin with two resistors whose sum sets the frequency. The resistor pair is used to divide the 1V reference generated on RT. The center tap of the voltage divider is connected to the phase pin to set phase shift of the secondary device. Do not float.
CONFIG / CLKOUT	7	I/O	Configuration pin. **For the primary device**: A 49.9kΩ resistor to ground configures the device with external compensation and allows multiphase operation. The CONFIG pin becomes an output CLKOUT after self-test and provides a clock that can be connected to MODE/SYNC on a secondary device. When external compensation and multiphase operation are not required, this pin must be tied to VCC. **For the secondary devices**: Connect this pin to ground to set the device as a secondary. In secondary operation, clocking is provided by the primary with appropriate phase shift set on the phase pin of the secondary device.
MODE / SYNC	8	I	Mode and synchronization input pin. Tie this pin to GND or drive this pin low to operate in AUTO mode. Tie this pin to VCC or drive this pin high, to operate in FPWM. Apply synchronization clock signal to this pin to operate in FPWM mode at the synchronizing frequency. When synchronized to an external clock, use the RT pin to set the internal frequency close to the synchronized frequency to avoid disturbances if the external clock is turned on and off.
RT	9	I/O	Switching frequency programming pin. Connect this pin to ground through a resistor with a value between 6.81kΩ and 54.2kΩ to set the switching frequency between 2200kHz and 300kHz, respectively. Connect to VCC for 400kHz operation. Connect to GND for 2.1MHz operation. Do not float.
EN / UVLO	10	P	Precision enable pin. Drive this pin high / low to enable / disable the device. This pin can be directly connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Do not float.
NC	11	—	No connect pin. Leave floating.
PGND1	12	G	Power ground to the internal low-side MOSFET. Connect this pin to the system ground. Low-impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
NC	13	—	No connect pin. Leave floating to maintain 1mm clearance between PGND1 and VIN1 pins. This pin can be shorted to PGND1 provided the 0.5mm clearance between PGND1 and VIN1 pins meets system pin clearance requirements.
VIN1	14[(2)]	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Make sure a 100nF bypass capacitor is placed within 1mm of both the VIN1 and PGND1 pins. Provide a low-impedance connection to VIN2.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	15	—	No connect pin. Leave floating to maintain 0.5mm clearance between VIN1 and SW1.
SW1	16	P	Device switch pins and the switch node of the regulator. Connect to the output inductor.
SW2	17	P	
SW3	18	P	
BST	19	P	High-side driver upper supply rail. Connect a high quality 100nF capacitor between the SW node and BST. An internal diode charges the capacitor while SW node is low.
NC	20	—	No connect pin. Leave floating to maintain 0.5mm clearance between VIN2 and BST.
VIN2	21[2]	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Make sure a 100nF bypass capacitor is placed within 1mm of both the VIN2 and PGND2 pins. Provide a low-impedance connection to VIN1.
NC	22	—	No connect pin. Leave floating to maintain 1mm clearance between PGND2 and VIN2 pins. This pin can be shorted to PGND2 provided the 0.5mm clearance between PGND2 and VIN2 pins meets system pin clearance requirements.
PGND2	23	G	Power ground to internal low-side MOSFET. Connect to system ground. Low-impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VCC	24	P	Internal regulator output. Used as supply to internal control circuits. Do not connect this pin to any external loads. Connect a high-quality 1µF capacitor from this pin to GND.
DRSS / MODECOMM	25	I/O	Dual Random Spread-Spectrum (DRSS) select pin. See the Section 7.3.6 section for available DRSS options. For multiphase operation, this pin becomes a spread spectrum timing pin between the primary and the secondary devices and all DRSS pins must be connected together.
BIAS	26	P	Input to internal voltage regulator. If configured for fixed VOUT, connect this pin to the VOUT node to close the control loop. If configured for an adjustable VOUT, connect the pin to the VOUT node or an external bias supply from 3.3V to 30V. If output voltage is above 30V or no external supply is used, tie the pin to GND. This pin can also be grounded in adjustable VOUT mode.
DAP	—	G	Exposed die attach pad (DAP). Connect to system GND on a PCB. This pin is a major heat dissipation path for the die. The pad must be used for heat sinking by soldering the pin to the GND copper on a PCB. The pad must also have a low impedance connection to the PGND connection of the input bypass capacitors. Implementing as many thermal vias as suggested in the example board layout makes sure of the lowest package thermal resistance and best possible thermal performance.

(1) I = input, O = output, P = power, G = ground

(2) Input capacitor placement outside the recommended range can result in device performance degradation including, but not limited to, increased input voltage and switch-node ringing outside the absolute maximum rating, and instability. See Section 8.4.2 for a recommended layout example.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	42	V
Input voltage	EN/UVLO TO PGND	–0.3	42	V
Input voltage	RT to PGND	–0.3	42	V
Input voltage	DRSS/MODECOMM to PGND	–0.3	42	V
Input voltage	SEC_EA to PGND	–0.3	20	V
Input voltage	BIAS TO PGND	–0.3	42	V
Input voltage	MODE/SYNC to PGND	–0.3	5.5	V
Input voltage	CONFIG/CLKOUT to PGND	–0.3	5.5	V
Input voltage	COMP, FB to PGND	–0.3	5.5	V
Input voltage	SS to PGND	–0.3	V_{CC} + 0.3	V
Output voltage	SW to PGND	–0.6	V_{IN} + 0.3	V
Output voltage	PG to PGND	–0.3	42	V
Output voltage	BST to SW	–0.3	5.5	V
Output voltage	VCC to PGND	–0.3	5.5	V
Operating junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	3	36	V
Input voltage	EN	0	36	V
Input voltage	BIAS, PG	0	30	V
Input voltage	FB, SEC_EA	0	5.5	V
Input voltage	MODE/SYNC, RT	0	5.5	V
Pullup resistance	$R_{PU(PG)}$	4		kΩ
Pullup reference voltage	$V_{PU(PG)}$	0.8	36	V
Output voltage	VOUT	0.8	0.9 × VIN	V
Output current	IOUT, LM654B0-Q1	0	20	A
Output current	IOUT, LM654A5-Q1	0	15	A
Output current	IOUT, LM654A2-Q1	0	12	A

6.3 Recommended Operating Conditions (continued)

Over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Output current	IOUT, LM654A0-Q1	0	10	A

6.4 Thermal Information

THERMAL METRIC [1]		DEVICE		UNIT
		VDA (WFQN-FCRLF) JESD 51-7	LM654B0EVM	
		26 PINS	26 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.3	16 (no heat-sink)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.32	-	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	-	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.1	5.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	- [2]	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2.2 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN PIN)						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising (Needed to start up)	3.2	3.4	3.6	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling (Once operating)		2.5	2.6	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.92	1.35	V
I_{VIN}	VIN pin input current, internal COMP, no switching	V_{BIAS} = 3.3V + 2%, CONFIG short to V_{CC}, T_J = 25°C		1	1.64	µA
$I_{BIAS(FIX\text{-}3.3V)}$	BIAS pin input current, fixed 3.3-V output, internal COMP, no switching	V_{BIAS} = 3.3V + 2%, CONFIG short to V_{CC}, T_J = 25℃, auto mode enabled		20	25	µA
$I_{Q(FIX\text{-}3.3V)}$	Total V_{IN} quiescent current, fixed 3.3-V output, internal COMP, no switching	V_{IN} = 24V, V_{BIAS} = 3.3V + 2%, CONFIG short to V_{CC}, T_J = 25℃, auto mode enabled		3.8	5	µA
		All temperatures		3.8	53	µA
$I_{BIAS(ADJ\text{-}3.3V)}$	BIAS pin input current, adjustable 3.3-V output, internal COMP, no switching	V_{FB} = 0.8V + 2%, CONFIG short to V_{CC}, auto mode enabled, T_J = 25℃		8	22	µA
$I_{Q(ADJ\text{-}3.3V)}$	Total V_{IN} quiescent current, adjustable 3.3-V output, internal COMP, no switching	V_{IN} = 24.0V, V_{FB} = 0.8V + 2%, CONFIG short to V_{CC}, auto mode enabled, T_J = 25℃		2.1	4.6	µA
$I_{BIAS(ADJ\text{-}3.3V\text{-}EXT)}$	BIAS pin input current, adjustable 3.3-V output, external COMP, no switching	V_{FB} = 0.8V + 2%, R_{CFG} = 49.9kΩ, auto mode enabled, T_J = 25℃		53	64	µA
$I_{Q(ADJ\text{-}3.3V\text{-}EXT)}$	Total V_{IN} quiescent current, adjustable 3.3-V output, external COMP, no switching	V_{IN} = 24.0V, V_{FB}=0.8V + 2%, R_{CFG} = 49.9kΩ, auto mode enabled, T_J = 25℃		8	11.1	µA
$I_{Q\text{-}SD}$	V_{IN} Shutdown supply current	V_{EN} = 0V, T_J = 25℃		1	2	µA
ENABLE (EN PIN)						
$V_{EN\text{-}TH(R)}$	Enable voltage rising threshold	V_{EN} rising	1.15	1.25	1.35	V
$V_{EN\text{-}TH(F)}$	Enable input low threshold	V_{EN} falling	0.9	1	1.1	V
$V_{EN\text{-}HYS}$	Enable voltage hysteresis			250		mV
$I_{EN\text{-}LKG}$	Enable input leakage current	V_{EN} = V_{IN}		0.35	6.28	µA
INTERNAL LDO (VCC PIN)						

6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2.2 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCC}	Internal LDO output voltage	3.4V ≤ V_{IN} ≤ 36V, V_{BIAS} = 0V		3.3		V
		3.4V ≤ V_{BIAS} ≤ 30V		3.2		V
$V_{VCC-OVLO(R)}$	VCC OVLO rising threshold	VCC over-voltage rising threshold, I_{VCC} = 0A		4.38		V
$V_{VCC-OVLO(F)}$	VCC OVLO falling threshold	VCC over-voltage falling threshold, I_{VCC} = 0A		3.63		V
$t_{VCC-OVLO\_DEGLITCH(R)}$	VCC OVLO rising edge comparator delay			20.5		us
$V_{VCC-UVLO(H)}$	VCC UVLO hysteresis			0.9		V
VOLTAGE REFERENCE (FB PIN)						
V_{FB1}	Internal feedback reference voltage, internal compensation	FPWM Mode, CONFIG shorted to V_{CC}	0.792	0.8	0.808	V
V_{FB2}	Internal feedback reference voltage, external compensation	FPWM Mode, R_{CONFIG} = 49.9kΩ	0.792	0.8	0.808	V
I_{FB-LKG}	Feedback pin input leakage current	V_{FB} = 0.8V, adjustable Version			90	nA
$R_{FB-SEL-ADJ}$	Adjustable output voltage setting resistance (thevenin equivalent)	Resistor ladder between VOUT and GND, center tap connected to FB	4		100	kΩ
FIXED OUTPUT VOLTAGE (BIAS PIN)						
$V_{OUT1(3.3V)}$	3.3V fixed output voltage, internal COMP	FB shorted to GND, CONFIG shorted to V_{CC}	3.255	3.3		V
$V_{OUT2(3.3V)}$	3.3V fixed output voltage, external COMP	FB shorted to GND, R_{CONFIG} = 49.9kΩ	3.255	3.3	3.333	V
$V_{OUT1(5V)}$	5.0V fixed output voltage, internal COMP	FB shorted to V_{CC}, CONFIG shorted to V_{CC}	4.92	5	5.065	V
$V_{OUT2(5V)}$	5.0V fixed output voltage, external COMP	FB shorted to V_{CC}, R_{CONFIG} = 49.9kΩ	4.92	5	5.065	V
STARTUP (SS PIN)						
t_{EN_HIGH}	Enable HIGH to start of switching delay	V_{FB} = V_{RT} = V_{MODE} = GND, V_{BIAS} = V_{OUT}		1.3		ms
t_{SS}	Internal fixed soft-start time	Time from first SW pulse to V_{REF} at 90% of set point	1.6	2.65	4.2	ms
I_{SS}	Soft-start charge current	V_{SS} = 0V		22		µA
R_{SS}	Soft-start discharge resistor	EN = 0V		7		Ω
ERROR AMPLIFIER (COMP PIN)						
$g_{m(EXTERNAL)}$	EA transconductance – external COMP	V_{COMP} = 0.8V, V_{FB} = +5%, and V_{FB} = -5%		1		mS
$V_{COMP-EXT(h-clamp)}$	External COMP- high clamp voltage	V_{FB} = 0V, Adjustable output voltage		1.2		V
CURRENT LIMITS AND HICCUP						
I_{HS-LIM}	High-side peak current limit, LM654B0-Q1	Duty-cycle approaches 0%.	31.5	36	39	A
I_{LS-LIM}	Low-side valley current limit, LM654B0-Q1			27.5		A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty-cycle, LM654B0-Q1	V_{VCC} = 3.3V, tpulse ≤ 100ns, auto mode		5.5		A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty-cycle, LM654B0-Q1	V_{VCC} = 3.3V, t_{pulse} ≥ 1µs, auto mode		0.55		A
$I_{LS-NEG-LIM}$	Low-side negative current limit	Sinking current limit, FPWM mode		–13.4		A
I_{HS-LIM}	High-side peak current limit, LM654A5-Q1	Duty-cycle approaches 0%.	20.6	23.6	25.6	A
I_{LS-LIM}	Low-side valley current limit, LM654A5-Q1			18.4		A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty-cycle, LM654A5-Q1	V_{VCC} = 3.3V, tpulse ≤ 100ns, auto mode		5		A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty-cycle, LM654A5-Q1	V_{VCC} = 3.3V, t_{pulse} ≥ 1µs, auto mode		1.7		A
$I_{LS-NEG-LIM}$	Low-side negative current limit	Sinking current limit, FPWM mode		–8		A
I_{HS-LIM}	High-side peak current limit, LM654A2-Q1	Duty-cycle approaches 0%.	16.5	18.9	20.5	A
I_{LS-LIM}	Low-side valley current limit, LM654A2-Q1			14.7		A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty-cycle, LM654A2-Q1	V_{VCC} = 3.3V, tpulse ≤ 100ns, auto mode		4		A

6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2.2 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{L\text{-}PEAK\text{-}MAX}$	Minimum peak inductor current at maximum duty-cycle, LM654A2-Q1	V_{VCC} = 3.3V, tpulse ≥ 1µs, auto mode		1.25		A
$I_{LS\text{-}NEG\text{-}LIM}$	Low-side negative current limit	Sinking current limit, FPWM mode		–6.4		A
$I_{HS\text{-}LIM}$	High-side peak current limit, LM654A0-Q1	Duty-cycle approaches 0%.	13.8	15.8	17.1	A
$I_{LS\text{-}LIM}$	Low-side valley current limit, LM654A0-Q1			12		A
$I_{L\text{-}PEAK\text{-}MIN}$	Minimum peak inductor current at minimum duty-cycle, LM654A0-Q1	V_{VCC} = 3.3V, tpulse ≤ 100ns, auto mode		3.35		A
$I_{L\text{-}PEAK\text{-}MAX}$	Minimum peak inductor current at maximum duty-cycle, LM654A0-Q1	V_{VCC} = 3.3 V, tpulse ≥ 1 µs, auto mode		1		A
$I_{LS\text{-}NEG\text{-}LIM}$	Low-side negative current limit	Sinking current limit, FPWM mode		–5		A
$I_{L\text{-}ZC\text{-}LIM}$	Zero-cross current limit	V_{VCC} = 3.3V, auto mode		140		mA
V_{HIC}	Overcurrent hiccup threshold on FB pin	Low-side FET ON-time > 165ns, after soft-start		0.32		V
t_{HIC_DLY}	Hiccup mode activation delay			128		cycles
t_{HIC}	Hiccup mode duration time			52		ms
POWER GOOD MONITOR (PG PIN)						
$V_{PG\text{-}OVP(R)}$	PG overvoltage rising threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	103	105	107	%
$V_{PG\text{-}OVP(F)}$	PG overvoltage falling threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	102	104	106	%
$V_{PG\text{-}UVP(R)}$	PG undervoltage rising threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	94	96	98	%
$V_{PG\text{-}UVP(F)}$	PG undervoltage falling threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	93	95	97	%
$t_{PG\text{-}DEGLITCH(F)}$	Deglitch filter delay on PG falling edge		55	114	175	µs
$t_{PG\text{-}DEGLITCH(R)}$	Deglitch filter delay on PG rising edge		1.2	2	3	ms
$V_{IN(PG\text{-}VALID)}$	Minimum V_{IN} for valid PG output	$V_{OL(PG)}$ < 0.4V, R_{PU} = 50kΩ, V_{PU} = 5V			1.25	V
$V_{OL(PG)}$	Output low voltage	I_{OL} = 1mA, V_{IN} = 1.25V			0.4	V
$R_{ON(PG)}$	PG FET ON resistance	I_{PG} = 1mA		35	110	Ω
SWITCHING FREQUENCY AND PHASE SHIFT						
$f_{SW1(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = GND	1.89	2.1	2.31	MHz
$f_{SW2(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = 15.8kΩ, 1%	900	1000	1100	kHz
$f_{SW3(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = VCC	360	400	440	kHz
SYNCHRONIZATION (MODE/SYNC PIN)						
$V_{IH(SYNC)}$	SYNC input high level threshold				1.3	V
$V_{IL(SYNC)}$	SYNC input low level threshold		0.45			V
$V_{OH(CLKOUT)}$	CLKOUT output high level threshold	I_{OH} = -2mA	2.4			V
$V_{OL(CLKOUT)}$	CLKOUT output low level threshold	I_{OL} = 2mA			0.4	V
$f_{SYNC\text{-}RANGE(FPWM)}$	Synchronization frequency range for set 2.2 MHz f_{SW}	R_{RT} = 6.81kΩ, 1%	1.76		2.64	MHz
$f_{SYNC\text{-}RANGE(FPWM)}$	Synchronization frequency range for set 300 kHz f_{SW}	R_{RT} = 54.2kΩ, 1%	240		360	kHz
$t_{SYNC(TON\text{-}MIN)}$	Minimum positive pulse width of external sync signal				80	ns
$t_{SYNC(TOFF\text{-}MIN)}$	Minimum negative pulse width of external sync signal				80	ns
$t_{SYNC\text{-}SW\text{-}DLY}$	SYNC to SW delay time			42	75	ns
DUAL RANDOM SPREAD SPECTRUM						
$\Delta f_{SS1\text{-}LF}$	Low-frequency triangular spread spectrum modulation range - standard	DRSS pin floating.		8.5		%

6.5 Electrical Characteristics (continued)

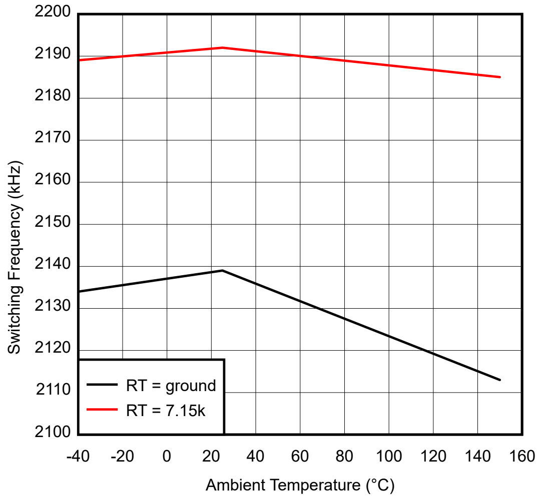
Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2.2 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta f_{SS2\text{-}LF}$	Low-frequency triangular spread spectrum modulation range - extended	R_{DRSS} = 150kΩ, 1%.		17		%
$f_{m1\text{-}LF}$	Triangular modulation frequency - standard	DRSS pin floating	7.2	12.3	17.5	kHz
$f_{m2\text{-}LF}$	Triangular modulation frequency - extended	R_{DRSS} = 150kΩ, 1%	3.6	6.6	9.5	kHz
$\Delta f_{SS\text{-}HF}$	High-frequency pseudo-random spread spectrum modulation range	R_{DRSS} = 150kΩ, 1% OR DRSS pin floating.		2.5		%
POWER STAGE						
$R_{DS\text{-}ON\text{-}HS}$	High-side FET ON resistance	I_{SW} = 500mA, $V_{BOOT\text{-}SW}$ = 3.3V		11		mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low-side FET ON resistance			6.5		mΩ
$t_{ON\text{-}MIN(FPWM)}$	Minimum on-time(1)	FPWM: I_{OUT} = 0A, R_{RT} = 6.81kΩ		32		ns
$t_{ON\text{-}MIN(AUTO)}$	Minimum on-time(1)	AUTO: I_{OUT} = 2A, R_{RT} = 6.81kΩ		32		ns
$t_{OFF\text{-}MIN}$	Minimum off-time	V_{IN} = 4V, Fsw = 2.2 MHz, R_{RT} = 6.81kΩ		110	155	ns
$t_{ON\text{-}MAX}$	Maximum on-time	Fsw = 300kHz, R_{RT}= 54.2kΩ		12		µs
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown(1)	Shutdown threshold	155	165	177	ºC
		Recovery threshold		156		ºC

(1) Specified by design.

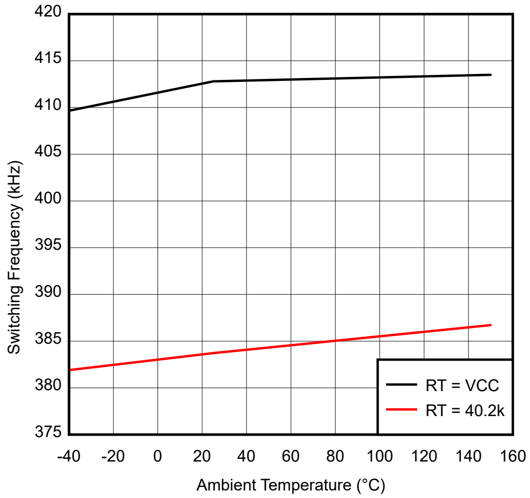
6.6 Typical Characteristics

V_{IN} = 12V, unless otherwise specified.



V_{IN} = 12V

Figure 6-1. Switching Frequency



V_{IN} = 12V

Figure 6-2. Switching Frequency

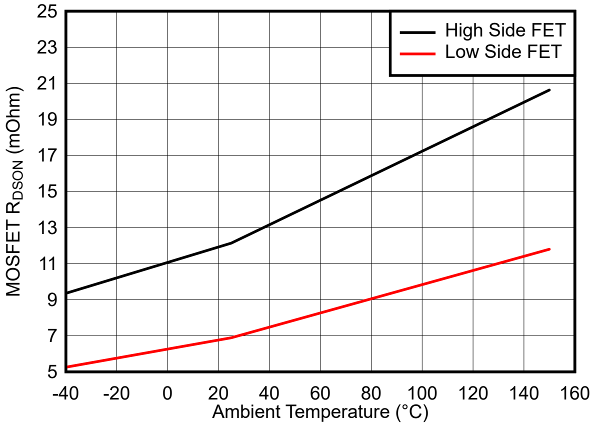


Figure 6-3. MOSFET R_{DSON}

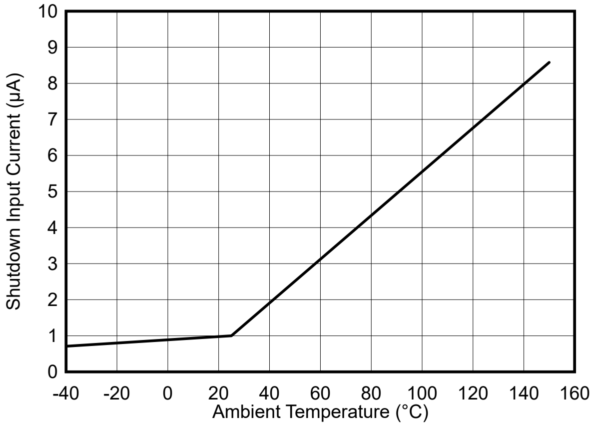


Figure 6-4. Shutdown Current

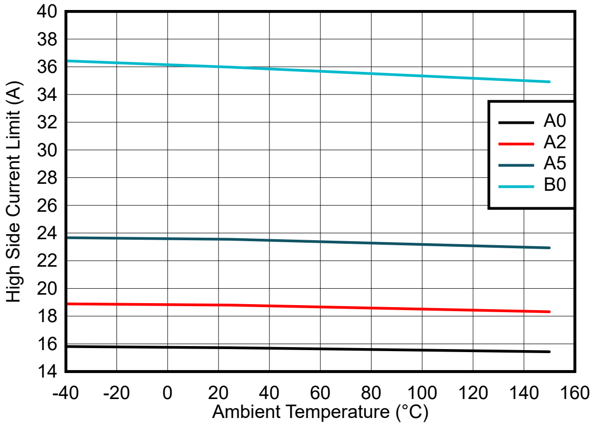


Figure 6-5. High Side Current Limit

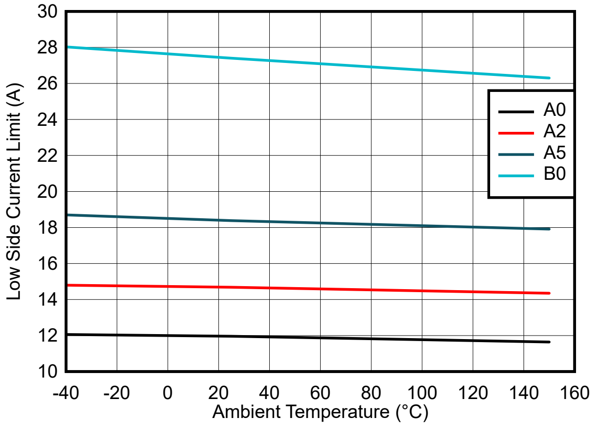


Figure 6-6. Low Side Current Limit

6.6 Typical Characteristics (continued)

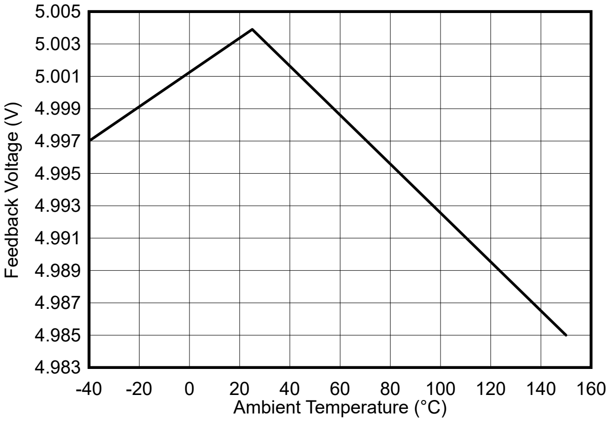


Figure 6-7. 5V Feedback Voltage

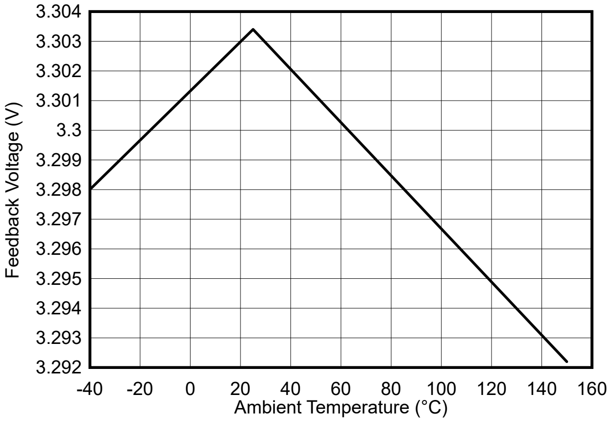


Figure 6-8. 3.3V Feedback Voltage

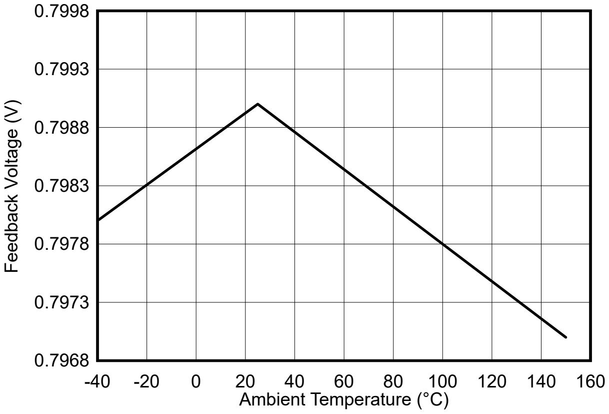
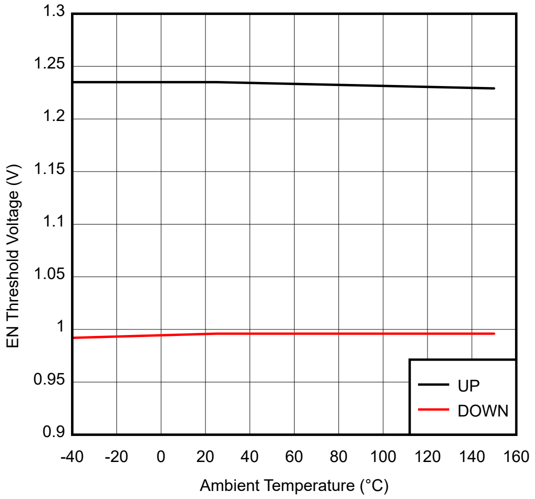


Figure 6-9. ADJ Feedback Voltage



V_{IN} = 12V

Figure 6-10. Enable Thresholds

7 Detailed Description

7.1 Overview

The LM654xx-Q1 is a family of high-efficiency, high-power density, stackable, ultra low-EMI buck converters. These converters operate over a wide input voltage range of 3V to 36V with pin selectable fixed output voltages of 3.3V, 5V, or an adjustable output configuration.

The current-mode control architecture, with 32ns minimum on-time, allows high conversion ratios at high frequencies, fast transient response, and excellent load and line regulation. Automatic frequency foldback occurs if the minimum on-time, or off-time, is violated. This feature allows regulation to be maintained during load dump events and cold cranking situations.

This device is designed to minimize end-product cost and size while operating in demanding automotive and high-performance industrial environments. The LM654xx-Q1 can be set to operate at fixed 400kHz, fixed 2.2MHz, or any frequency in the range of 300kHz to 2.2MHz using the RT pin. Internal compensation and an accurate current limit scheme minimizes BOM cost and component count.

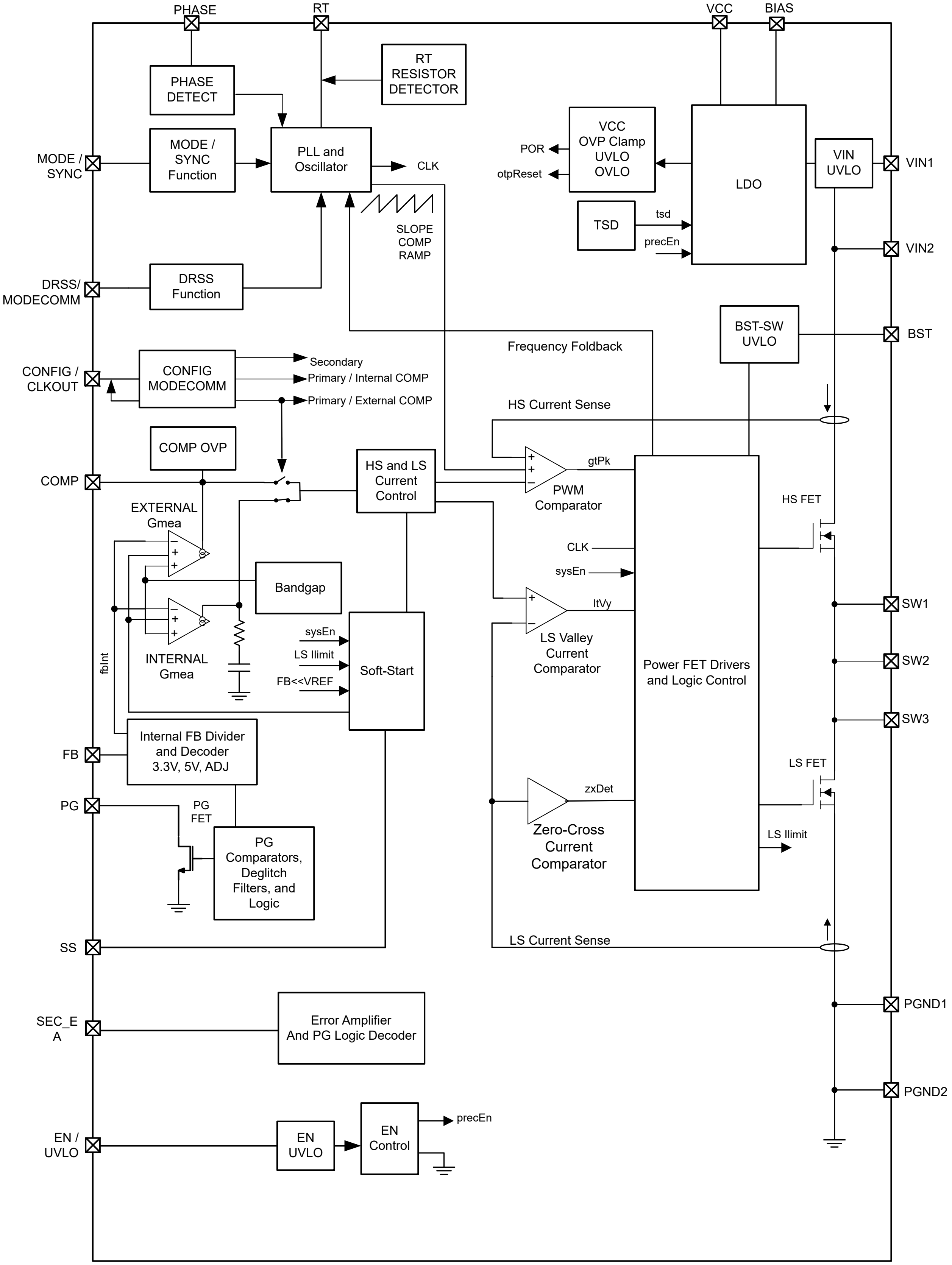
The LM654xx-Q1 has been designed for low EMI, incorporating the following features:

- Pin-configurable +8.5% or +17% dual random spread spectrum (DRSS) frequency hopping.
- Symmetrical pin out, low inductance package
- Operation over a frequency range above or below AM radio band
- Pin-configurable for AUTO or FPWM mode along with external clock synchronization capabilities

Together, these features can reduce or eliminate the need for shielding and other expensive EMI mitigation measures.

To use the device in reliability-conscious environments, the LM654xx-Q1 features a package with enlarged corner terminals for improved board level reliability and wettable flanks, allowing optical inspection.

7.2 Functional Block Diagram



7.3 Feature Descriptions

7.3.1 Output Voltage Selection

The LM654xx-Q1 features pin-selectable fixed output voltage or adjustable output voltage mode. In fixed output voltage mode, the output voltage is selected by the FB pin. Connect the FB pin to GND to select a 3.3V output, or connect to VCC for a 5V output. When the fixed output voltage mode is selected, the BIAS pin must be connected directly to the output of the regulator. In this mode the BIAS pin closes the feedback loop of the regulator and provides input power to the internal VCC regulator.

Table 7-1. Output Voltage Selection

FB	VOUT
Short to GND	3.3V
Short to VCC	5V
Connect to a feedback resistor divider tap point (Figure 7-1)	ADJ

In the adjustable output voltage mode, a voltage divider is connected between the regulator output voltage and the FB pin. The resistor values are calculated based on the desired output voltage and the 0.8V reference of the regulator. See Figure 7-1 for detailed connections.

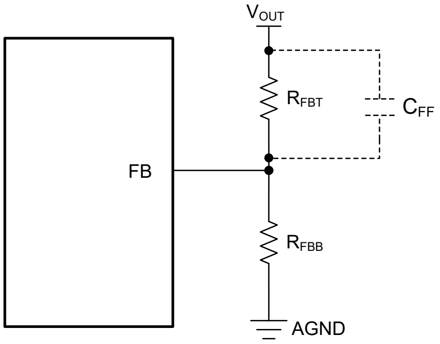


Figure 7-1. Setting Output Voltage of Adjustable Versions

Use Equation 1 to select a value for R_{FBB}, based on a desired value of R_{FBT}. Limiting the value of R_{FBT} to 100kΩ or less is best practice. Larger values of resistance are susceptible to leakage currents on the PCB, caused by environmental contamination, that can shift the desired output voltage. Values up to about 1MΩ can be used to reduce the no-load supply current, in those cases where excessive PCB leakage currents are not present.

$$R_{FBB} = R_{FBT} \times \frac{0.8}{V_{OUT} - 0.8} \tag{1}$$

In some cases, when using the adjustable mode, a feedforward capacitor can be used to improve the loop phase margin and load transient response. The exact value of C_{FF} is best selected empirically during the initial bench evaluation of the design. In any event, leaving a placeholder for this capacitor in the PCB layout is best practice if needed at some point during the development of the application.

7.3.2 EN Pin and Use as V_{IN} UVLO

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input undervoltage lockout (UVLO). Applying a voltage greater than about 0.9V causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to $V_{EN\_TH\_R}$ fully enables the device, allowing the device to enter start-up mode and begin the soft-start period. When the EN input is brought below $V_{EN\_TH\_F}$, the regulator stops switching and enters standby mode. Further decrease in the EN voltage to below 0.9V completely shuts down the device, providing a shutdown current of less than 1.4μA (typical). The EN input can be connected directly to VIN if this feature is not needed. The enable must not float as floating the pin forces the device off. The values for the various EN thresholds can be found in the *Electrical Characteristics* table. Keep in mind that the internal VIN UVLO overrides the EN input. The device does not start-up unless the input voltage is above $VIN_{UVLO(R)}$. Conversely, the device shuts down when the input voltage falls below $VIN_{UVLO(F)}$.

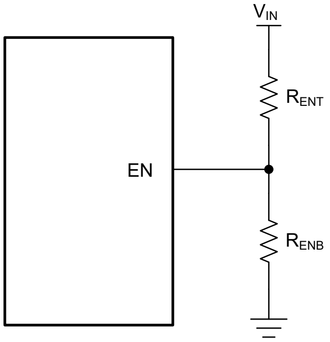


Figure 7-2. VIN UVLO Using the EN Pin

In some cases, an input UVLO level different than that provided internal to the device is needed. This feature can be used for special sequencing or to prevent input voltage oscillations caused by excessively long power cables. External UVLO can be accomplished by using the circuit shown in Figure 7-2. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. The current in the divider must be greater than the current into the EN input (I_{EN_LKG}), to preserve accuracy. Values for R_{ENB} between 10kΩ and 50kΩ are reasonable. Then, Equation 2 is used to calculate R_{ENT} and Equation 3 is used to calculate V_{OFF}.

$$R_{ENT} = R_{ENB} \times \left(\frac{V_{ON}}{V_{EN\_TH\_R}} - 1\right) \tag{2}$$

$$V_{OFF} = V_{ON} \times \left(\frac{V_{EN\_TH\_F}}{V_{EN\_TH\_R}}\right) \tag{3}$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

7.3.3 Device Configuration

The device configuration is implemented with the CONFIG pin.

The CONFIG pin selects either internal compensation (1-phase operation) or external compensation (1-phase or multiphase operation), and affects the DRSS / MODECOMM pin functionality as shown in the following table.

Table 7-2. Device Configuration

CONFIG PIN	CONFIGURATION	DRSS / MODECOMM PIN FUNCTIONALITY
Short to GND	Secondary device, CLKOUT disabled	MODECOMM input
49.9kΩ to GND	Primary device, external COMP, CLKOUT enabled	DRSS control / MODECOMM output
Short to VCC	Primary device, internal COMP, CLKOUT disabled	DRSS control

7.3.4 Mode Selection

The MODE / SYNC pin is a multifunction pin that configures the mode of operation, and serves as an input for an external synchronization signal. If the pin is grounded or driven to logic low, the converter operates in AUTO mode. If the pin is tied to VCC or driven to logic high, or synchronized to an external clock source, the converter operates in FPWM mode.

Transitioning the device from AUTO to FPWM mode requires driving the pin from low to high or sending a synchronization signal. Transitioning the device from FPWM to auto mode requires driving the pin from high to low or stop sending the synchronization signal.

7.3.4.1 MODE/SYNC Pin Uses for Synchronization

The LM654xx-Q1 MODE/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by coupling a positive edge into the pin. The coupled edge voltage at the pin must exceed the SYNC amplitude threshold of $V_{IH(SYNC)}$ to trip the internal synchronization pulse detector. The minimum SYNC ON pulse and OFF pulse durations must be longer than $t_{SYNC(TON\text{-}MIN)}$ and $t_{SYNC(TOFF\text{-}MIN)}$ respectively. The LM654xx-Q1 switching action can be synchronized to an external clock from 300kHz to 2.2MHz.

Note, an external SYNC signal is only recognized by the device before or after pin detection. That is, before the device has been enabled or 2ms (t_{EN_HIGH}) after enabled. If applied during the pin detection, the SYNC signal cannot be detected.

The synchronization frequency must be within +/– 20% of the frequency set on the RT pin for the internal slope compensation ramp to function correctly.

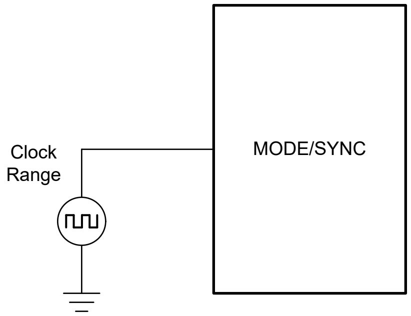
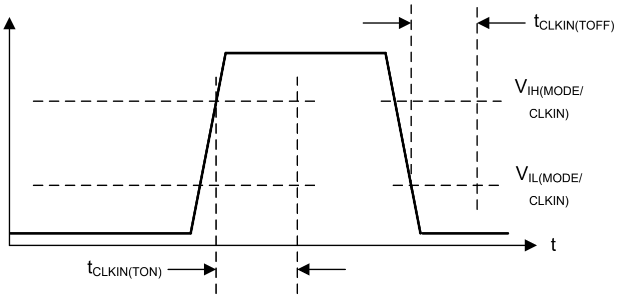


Figure 7-3. Typical Implementation Allowing Synchronization Using the MODE/SYNC Pin

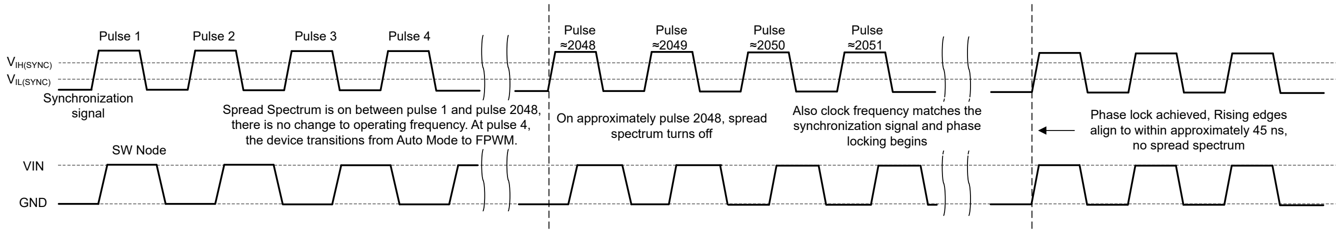


This figure shows the conditions needed for detection of a synchronization signal.

Figure 7-4. Typical SYNC Waveform

7.3.4.2 Clock Locking

After a valid synchronization signal is detected, a clock locking procedure is initiated. After approximately 2048 pulses, the clock frequency abruptly changes to the frequency of the synchronization signal. While the frequency adjusts suddenly, phase is maintained so that the clock cycle lying between operation at the default and synchronization frequencies is of intermediate length. There are no very long or very short pulses. After frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising the SW node pulses. See Figure 7-5.



At pulse 4, the synchronization signal is detected. After approximately pulse 2048, the synchronization signal is ready to synchronize and the frequency is adjusted using a glitch-free technique, then the phase is locked.

Figure 7-5. Synchronization Process

7.3.5 Adjustable Switching Frequency and Phase Shift

The RT pin is configurable. This pin can be tied to VCC for 400kHz operation, grounded for 2.2MHz operation, or a resistor to GND can be used to set an intermediate operating frequency. Note that if a resistor value falls outside of the range of 6.81kΩ to 54.2kΩ, the device can revert to 400kHz or 2.2MHz. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, see the SYNC/MODE pin in Section 7.3.4.1.

Use Equation 4 to select RT for the desired switching frequency.

$$R_T(k\Omega) = \frac{14972}{f_{SW}(kHz) - 8.5} \tag{4}$$

For example, for f_{SW} = 380kHz, R_T = 40.3kΩ so a 40.2kΩ resistor can be selected as the closest value.

Phase shifts between the primary and secondaries is controlled by the status of the PHASE pin. For a dual phase (or single phase) design, connect the PHASE pin of the primary, and the secondary, to ground. The secondary is clocked 180º out of phase from the primary. Connect the CONFIG/CLKOUT pin of the primary to the SYNC/MODE pin on the secondary. See Figure 8-5 for details.

For designs with more than two phases, connect the PHASE pin of the primary to VCC. The PHASE pin of the secondaries are connected to a tap on the split RT resistors. In this case, each secondary has a voltage divider between the RT pin and PHASE pin. The sum of the two resistors in the divider must equal the value of the RT resistor on the primary. The phase shift from the primary of a particular secondary is proportional to the voltage on the PHASE pin, with respect to a reference voltage of one volt. As an example, 0.5V on the PHASE pin provides a 180º phase shift. See Table 7-3 through Table 7-6 for examples. Also, the LM654xx quick start tool automatically calculates the correct resistor values. The CONFIG/CLKOUT pin of the primary is connected to the SYNC/MODE pin of the secondaries. See Figure 8-6.

The following tables provides the recommended phase delays for various configurations and frequencies.

Table 7-3. Recommended Secondary Phase Shift for Number of Phases

	45º	60º	90º	120º	135º	180º	225º	240º	270º	300º	315º
2 Phase						X					
3 Phase				X				X			
4 Phase			X			X			X		
6 Phase		X		X		X		X		X	
8 Phase	X		X		X	X	X		X		X

Table 7-4. RT Resistors for 380kHz

RT	0º Primary	45º	60º	90º	120º	135º	180º	225º	240º	270º	300º	315º
RT_{top}	40.2kΩ	34.8kΩ	33.2kΩ	30.1kΩ	26.7kΩ	24.9kΩ	20kΩ	15kΩ	13.3kΩ	10kΩ	6.65kΩ	4.99kΩ
RT_{bott}	N/A	4.99kΩ	6.65kΩ	10kΩ	13.3kΩ	15kΩ	20kΩ	24.9kΩ	26.7kΩ	30.1kΩ	33.2kΩ	34.8kΩ

Table 7-5. RT Resistors for 1000kHz

RT	0º Primary	45º	60º	90º	120º	135º	180º	225º	240º	270º	300º	315º
RT_{top}	15.8kΩ	13.7kΩ	13.3kΩ	11.8kΩ	10.5kΩ	10kΩ	7.87kΩ	5.9kΩ	5.23kΩ	3.92kΩ	2.61kΩ	2kΩ
RT_{bott}	N/A	2kΩ	2.61kΩ	3.92kΩ	5.23kΩ	5.9kΩ	7.87kΩ	10kΩ	10.5kΩ	11.8kΩ	13.3kΩ	13.7kΩ

Table 7-6. RT Resistors for 2100kHz

RT	0º Primary	45º	60º	90º	120º	135º	180º	225º	240º	270º	300º	315º
RT_{top}	7.15kΩ	6.34kΩ	5.9kΩ	5.36kΩ	4.75kΩ	4.53kΩ	3.57kΩ	2.67kΩ	2.37kΩ	1.78kΩ	1.11kΩ	0.886kΩ
RT_{bott}	N/A	0.886kΩ	1.18kΩ	1.78kΩ	2.37kΩ	2.67kΩ	3.57kΩ	4.53kΩ	4.75kΩ	5.36kΩ	5.9kΩ	6.34kΩ

7.3.6 Dual Random Spread Spectrum (DRSS)

The LM654xx-Q1 provides a Dual Random Spread Spectrum (DRSS) function that reduces the EMI of the power supply over a wide-frequency range; see Figure 7-6. The DRSS function combines a low-frequency triangular modulation profile (standard or wide) with a high-frequency cycle-by-cycle pseudo-random modulation profile. The low frequency triangular modulation improves performance in the lower radio frequency bands, while the high frequency random modulation improves performance in the higher radio frequency bands.

The low frequency triangular modulation profiles are pin-selectable. The standard low-frequency modulation profile spreads the switching frequency by 8.5% while the wide low frequency modulation profile spreads the switching frequency by 17%.

Table 7-7. DRSS Settings for External Error Amplifier Designs

MODECOM/DRSS PIN PRIMARY DEVICE	DRSS PROFILE
Tie to MODECOM/DRSS of secondary devices	17% frequency spread
Tie to secondary devices and connect 149.9kΩ to GND	8.5% frequency spread
Tie to secondary devices and connect 49.9kΩ to GND	Spread spectrum disabled
GND	Spread spectrum disabled
VCC	Spread spectrum disabled

Table 7-8. DRSS Settings for Single-phase Internal Error Amplifier Designs

MODECOM/DRSS PIN	DRSS PROFILE
FLOAT	17% frequency spread
149.9kΩ to GND	8.5% frequency spread
49.9kΩ to GND	Spread spectrum disabled
Short to GND	Spread spectrum disabled
Short to VCC	17% frequency spread

Spread spectrum works by converting a narrow band signal into a wide band signal which spreads the energy over multiple frequencies. Industry standards require different spectrum analyzer resolution bandwidth (RBW) settings for different frequency bands. The RBW has an impact on the spread spectrum performance. For example, CISPR-25 requires 9kHz RBW for the 150kHz to 30MHz frequency band. For frequencies greater than 30MHz, the required RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance when using either high or low RBWs with the low frequency triangular modulation and high-frequency cycle-by-cycle pseudo-random modulation. In the low-frequency band (150kHz – 30MHz), the DRSS function can reduce the conducted emissions by as much as 15dBµV, and in the high-frequency band (30MHz – 108MHz) by as much as 5dBµV. The DRSS function is disabled when an external clock is applied to the MODE / SYNC pin.

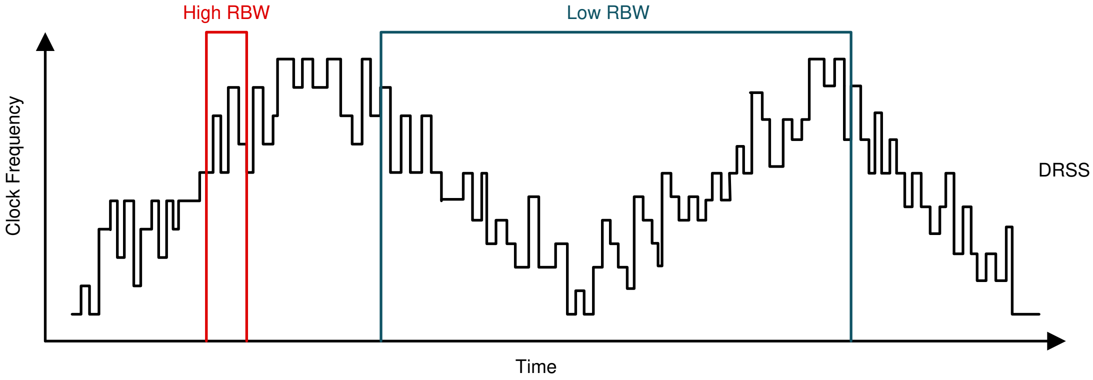


Figure 7-6. Dual Random Spread Spectrum Implementation

7.3.7 Internal LDO, VCC UVLO, and BIAS Input

The BIAS pin of the LM654xx-Q1 is the input voltage supply for the internal VCC regulator. This regulator powers most of the internal circuits including the MOSFET drivers and charging the BST capacitor. The BIAS pin must be connected to VOUT for fixed VOUT applications because the pin also closes the feedback loop. In this case, the VCC LDO is powered from VOUT and helps improve efficiency under some operating conditions. For adjustable output voltage applications, the BIAS pin can be grounded, connected to VOUT, or to an external supply. With the BIAS pin grounded, the VCC LDO receives power from the input supply of the regulator. With the other connections, the BIAS pin voltage must be within the range of 3.2V to 30V; lower voltages providing improved efficiency.

The VCC pin is the output of the internal LDO and requires a high quality 1µF ceramic capacitor rated for at least 10V with X7R or better dielectric from VCC to PGND. The VCC voltage is typically between 3.2V and 3.3V, assuming a valid input voltage to the regulator is present. This pin can be used for logic pullups but must not be loaded by external circuits. To prevent unsafe operation, VCC has a UVLO that prevents switching if the VCC voltage is too low. See $V_{CC\text{-}UVLO\_R}$ and $V_{CC\text{-}UVLO\_HYST}$ in Section 6.5. During start-up, VCC momentarily exceeds the normal operating voltage until $V_{CC\text{-}UVLO\_R}$ is exceeded, then drops to the normal operating voltage.

7.3.8 Bootstrap Voltage (BST Pin)

A boot capacitor is required to be connected between the BST pin and one of the SW pins of the regulator. This capacitor provides the gate drive supply to the high-side power MOSFET. This capacitor must be a high quality 100nF ceramic capacitor rated for 10V with X7R or better dielectric.

7.3.9 Soft Start and Recovery From Dropout

The soft-start features brings the output voltage up from zero volts to the programmed output voltage in a controlled manner helping to prevent inrush current and overshoots in the output voltage of the regulator. Soft start is triggered by any of the following conditions:

- EN is used to turn on the device.
- Recovery from a hiccup waiting period; see Section 7.3.10.3.
- Recovery from shutdown due to over-temperature protection.
- Power is applied to the VIN of the IC or the VCC UVLO is released.

After soft start is initiated, the IC takes the following actions:

- The reference used by the IC to regulate the output voltage is slowly ramped up from zero. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of the regulation value.
- Operating mode is set to AUTO, activating diode emulation. This action allows start-up without pulling the output voltage low if there is a voltage already present on the output.
- Hiccup is disabled for the duration of soft start; see Section 7.3.10.3.

All of these actions together provide start-up with limited inrush currents. These actions also allow the use of output capacitors and loading conditions that can cause current limit during start-up without triggering hiccup. In addition, if the output voltage is already present, the output voltage does not discharge.

With the SS pin open, the default soft-start time, to 90% of the regulation point, is about 2.6ms (typical). This time can be increased by placing a high quality ceramic capacitor on the SS pin to ground. Use Equation 5 to select an appropriate capacitor value.

$$C_{SS}[\mu F] = 0.031 \times T_{SS}[ms] \tag{5}$$

If the output voltage goes below the regulation point by several percent for any reason, the output voltage ramps back up slowly after the condition has been removed. This action is the recovery from dropout condition which differs from soft start in three important ways:

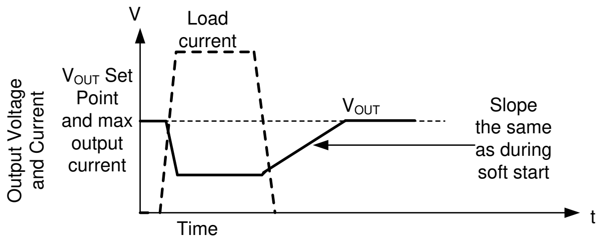
- Hiccup is allowed only if output voltage is less than 0.4 times the regulation point. Note that during dropout regulation, hiccup is inhibited. See Section 7.3.10.3.
- FPWM mode is allowed during recovery from dropout. If the output voltage suddenly pulled up by an external supply, the LM654xx-Q1 can pull down on the output. Note that all the protections that are present during normal operation are in place, protecting the device if output is shorted to a high voltage or ground.
- The reference voltage is set to approximately 1% above the regulation point; the reference voltage is not started from zero.

Despite the name, recovery from dropout is active whenever the output voltage is several percent below the regulation point for the following conditions:

- Duty cycle is controlled by minimum on-time
- When the device is operating in current limit.

This action primarily occurs under the following conditions:

- Dropout: when there is insufficient input voltage for the desired output voltage to be regulated.
- Current limit that is not severe enough to trigger hiccup or if the duration is too short to trigger hiccup. See Section 7.3.10.3.



Whether the output voltage falls due to high load or low input voltage, after the condition that causes the output of regulation event is removed, the output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, hiccup can, in principle, be triggered during recovery if output voltage is below 0.4 times output the set-point for more than 128 clock cycles during recovery.

Figure 7-7. Recovery From Dropout

7.3.10 Safety Features

The LM654xx-Q1 includes the following set of safety features:

- Power-Good monitor with output undervoltage (UV) and overvoltage (OV) protection
- Overcurrent and short-circuit protection with HICCUP mode
- Thermal shutdown (TSD)

7.3.10.1 Power-Good Monitor

The LM654xx-Q1 includes a power-good function to simplify supply sequencing and supervision in a system. The power-good function can be used to enable downstream circuits that are supplied by the LM654xx-Q1, control downstream protection circuits such as load switches, or to turn on sequenced supplies. The function monitors the output voltage with a window comparator through the FB pin for adjustable V_{OUT} configurations and the BIAS pin for fixed V_{OUT} configurations. The power-good output (PG) switches to a high impedance open-drain state when the output voltage is in regulation. When the output voltage is outside of the ±5% range from the set voltage, the PG pin is driven low ($< V_{OL(PG)}$) warning the system of an output over-voltage or undervoltage condition. A 114µs deglitch filter on the PG falling edge prevents false tripping of the power good signals during transients. When the output voltage returns within the regulation window, a 2ms filter on the PG rising edge allows extra processing time for the downstream components.

TI recommends a 100kΩ pullup resistor from the PG pin to the relevant logic rail not greater than 30V. PG is asserted low during soft start and when the LM654xx-Q1 is disabled but VIN is greater than $V_{IN(PG\text{-}VALID)}$. On secondary devices, output voltage monitoring is disabled and the power good is pulled low.

7.3.10.2 Overcurrent and Short-Circuit Protection

The LM654xx-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side switch current is sensed when the high-side FET is turned on after a short blanking time. The high-side switch current is compared to the minimum of a fixed current set-point, or the output of the voltage regulation loop minus slope compensation, every switching cycle. Because of this, the high-side peak current limit drops slightly with increasing switch duty cycle. See Figure 7-8 for typical variations of the high side current limit with duty cycle.

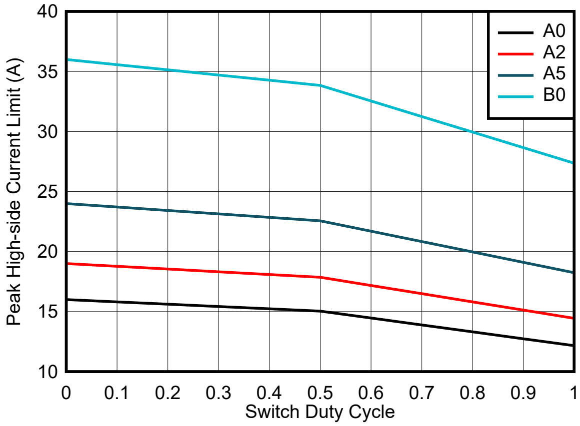


Figure 7-8. High Side Current Limit vs Duty Cycle

When the low-side switch is turned on, the current is also sensed. Like the high-side MOSFET, the low-side MOSFET turn-off is commanded by the voltage control loop. For the low-side FET, turn-off is prevented if the low-side current limit is exceeded, even if the oscillator normally starts a new switching cycle; see the *Electrical Characteristics* for values. If the low-side current limit is exceeded, the low-side MOSFET stays on and the high-side switch is not turned on. The low-side switch is turned off after the low-side current falls below the limit. The high-side switch is turned on again as long as at least one clock period has passed since the last time the high-side device has turned on.

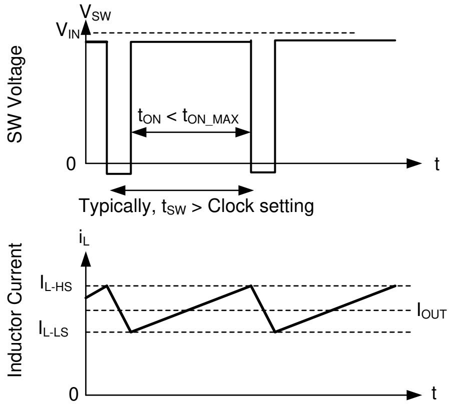


Figure 7-9. Current Limit Waveforms

The maximum output current is therefore controlled by both the high-side and low-side peak current limit. Use Equation 6 to provide an approximate value of maximum load current. With severe overloads or short circuit on the output, the device goes into hiccup current limit mode. In this case, the output current "folds-back" and falls to a very low level to prevent excessive device temperature. See also Section 7.3.10.3.

$$I_{OUT-MAX} \cong \frac{I_{HS-LIM} + I_{LS-LIM}}{2} \tag{6}$$

The above considers the effect of the current limits on the maximum available output current. However, the maximum output current can be limited by thermal considerations. This possibility can be checked by referring to Section 8.2.2.8. In any case, paralleling two or more LM654xx regulators can mitigate issues with current limit and thermal constraints.

After the overload condition is removed, the device recovers as though in soft start; see *Electrical Characteristics*. Note that hiccup can be triggered if output voltage drops below approximately 0.4 times the intended output voltage.

7.3.10.3 Hiccup

The LM654xx-Q1 employs hiccup over-current protection when all of the following conditions are met for 128 consecutive switching cycles:

- A time greater than t_{SS} has passed since soft start has started; see Section 7.3.9.
- Output voltage is below approximately 40% of the regulation point.
- The device is not operating in dropout defined as having minimum off-time controlled by duty factor.

In hiccup mode, the device shuts down and attempts to soft start after t_{HIC}. Hiccup mode helps reduce the device power dissipation under severe over-current conditions and short circuits. See the Section 8.2.3 for typical waveforms.

In hiccup mode, the average output current is reduced to approximately 25% of the device high-side current limit value.

7.3.10.4 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 165°C (typical), no earlier than 155°C (minimum). Recovery occurs at approximately 156°C (typical). This hysteresis, after thermal shutdown occurs, prevents the device from immediately restarting. When the junction temperature falls below 156°C, the LM654xx-Q1 attempts to soft start.

While the LM654xx-Q1 is in shutdown due to high junction temperature, power continues to be provided to VCC. To prevent overheating from a short circuit applied to VCC, the LDO providing power to VCC has reduced current limit while the device is disabled due to high junction temperature.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on and off control of the device. When the EN pin voltage is below 0.9V, both the regulator and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to about 1µA.

7.4.2 Active Mode

The LM654xx-Q1 is in active mode when the following occurs:

- The EN pin is above V_{EN}.
- V_{IN} is above $V_{IN\_UVLO\_R}$.
- V_{IN} is high enough to satisfy the V_{IN} minimum operating input voltage.
- No other fault conditions are present.

See Section 7.3 for protection features. The simplest way to enable the operation is to connect EN to VIN, allowing self-start-up when the applied input voltage exceeds the minimum $V_{IN\_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the LM654xx-Q1 is in one of six sub-modes:

- Continuous conduction mode (CCM) with fixed switching frequency and peak current mode operation.
- Discontinuous conduction mode (DCM) while in auto mode when the load current is lower than half of the inductor current ripple. If current continues to reduce, the device enters Pulse Frequency Modulation (PFM) which reduces the switch frequency to maintain regulation while reducing switching losses to achieve higher efficiency at light load.
- Minimum on-time operation while the on-time of the device needed for full-frequency operation at the requested low-duty cycle is not supported by T_{ON_MIN}
- Forced pulse width modulation (FPWM) similar to CCM with fixed-switching frequency, but extends the fixed frequency range of operation from full to no load.
- A current limiting condition where the output voltage remains above 0.4 times the output setpoint.
- Dropout mode when switching frequency is reduced to minimize dropout.
- Recovery from dropout similar to other modes of operation except the output voltage setpoint is gradually moved up until the programmed setpoint is reached.

7.4.2.1 Peak Current Mode Operation

The following operating description of the LM654xx-Q1 refers to Section 7.2 and the waveforms in Figure 7-10. Both supply a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW terminal voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, forcing V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period: $D = T_{ON} / (T_{ON} + T_{OFF})$.

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

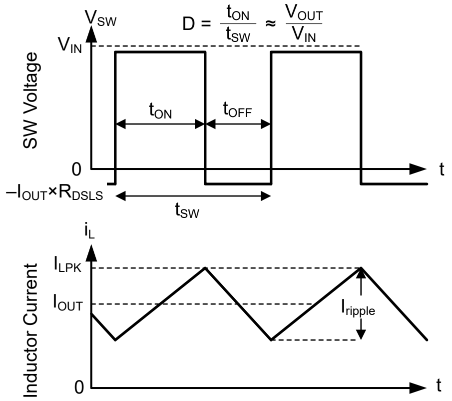


Figure 7-10. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

To get accurate DC load regulation, a voltage feedback loop is used. Peak and valley inductor currents are sensed for peak current mode control and current protection. The regulator operates with continuous conduction mode with constant switching frequency when load level is above one half of the minimum peak inductor current. The internally-compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.4.2.2 Auto Mode Operation

The LM654xx-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows a seamless transition between normal current mode operation while heavily loaded and in highly-efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LM654xx-Q1 operates in depends on the SYNC/MODE pin. When SYNC/MODE is high, the device is in FPWM. When SYNC/MODE is low, the device is in PFM.

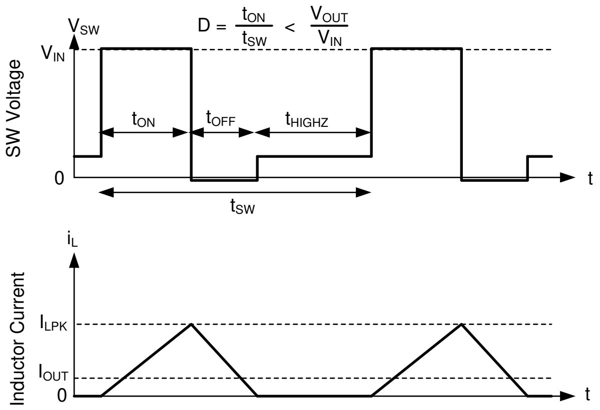
In auto mode, light-load operation is employed in the LM654xx-Q1 at load lower than approximately 1/10th of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation
- Frequency reduction

Note that while these two features operate together to create excellent light load behavior, these features operate independently of each other.

7.4.2.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. Frequency reduces when the peak inductor current goes below $I_{PEAK\text{-}MIN}$. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



In auto mode, the low-side device is turned off after inductor current is near zero. As a result, after output current is less than half of inductor ripple in CCM, the device operates in DCM. This is equivalent to saying that diode emulation is active.

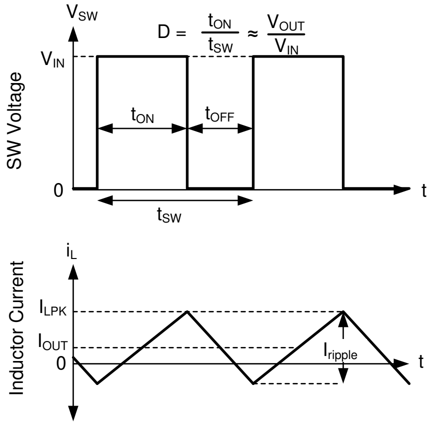
Figure 7-11. PFM Operation

The LM654xx-Q1 has a minimum peak inductor current setting in auto mode. That being said, when current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.2.3 FPWM Mode Operation

Like auto mode operation, FPWM mode operation during light-load operation is selected using the SYNC/MODE pin.

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See the *Electrical Characteristics* for reverse current limit values.



FPWM mode Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of Iripple.

Figure 7-12. FPWM Mode Operation

In FPWM mode, frequency reduction is still available if the input voltage is high enough to command minimum on-time. This frequency reduction allows good behavior during line faults to avoid the output voltage being pulled up.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM654xx-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage while supplying an output current of less than or equal to 20A, depending on operating conditions. See Section 7.3.10.2 and Section 8.2.2.2 for details regarding the maximum available output current.

The following design procedure can be used to select components for the LM654xx-Q1 family of regulators.

8.2 Typical Application

Figure 8-1 to Figure 8-6 show typical application circuits for a wide variety of applications. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation for single phase operation is designed for a certain range of external inductance and output capacitance. As a quick-start guide, Table 8-1 through Table 8-2 provide typical component values for a range of application parameters. The component values in these table represent stable designs and are not necessarily optimized. Note that the designs in these tables are based on a typical input voltage of 12V. For a complete design, use the quick start calculator tool associated with this family of devices and consult Section 8.2.1.

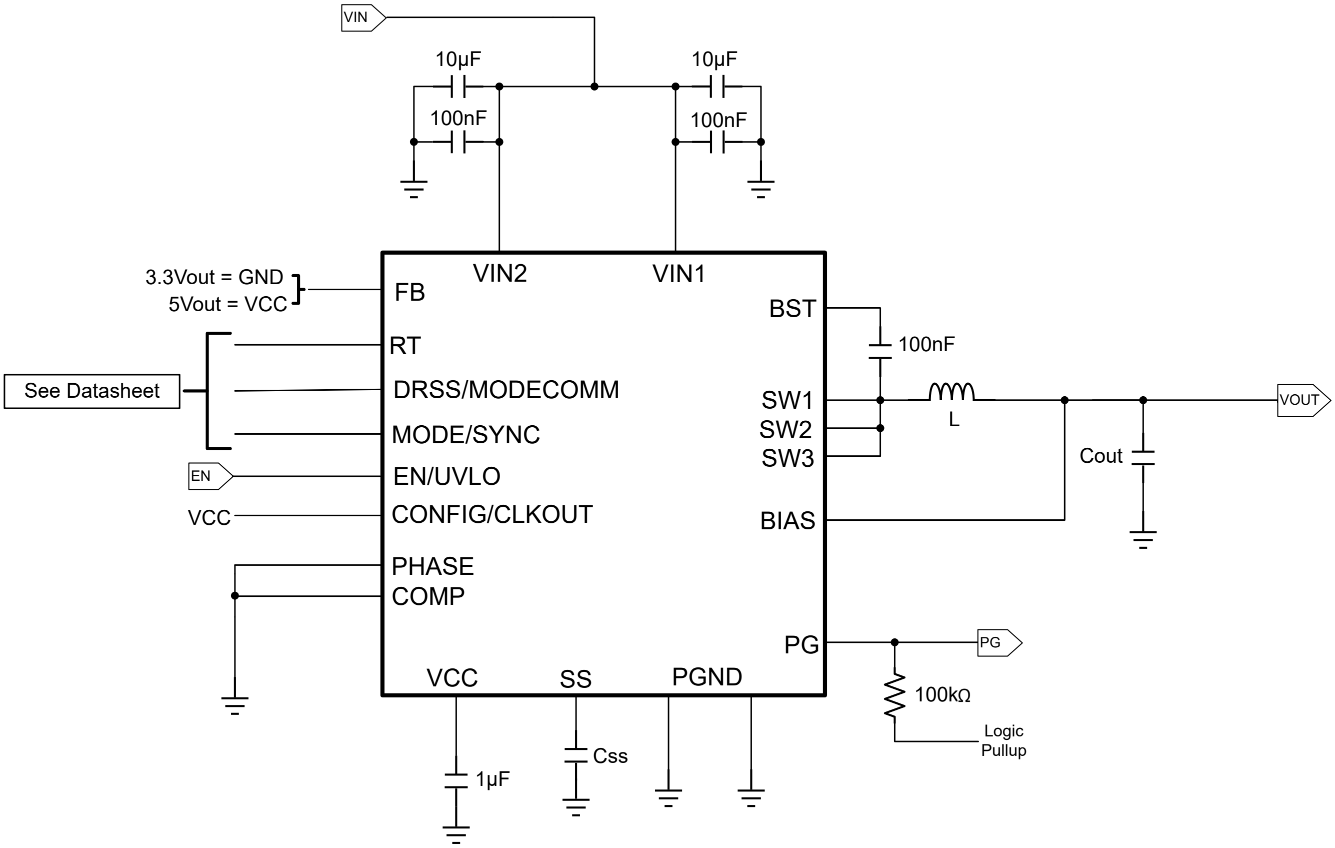


Figure 8-1. Example Single Phase Application Using Fixed Output Voltage and Internal Compensation

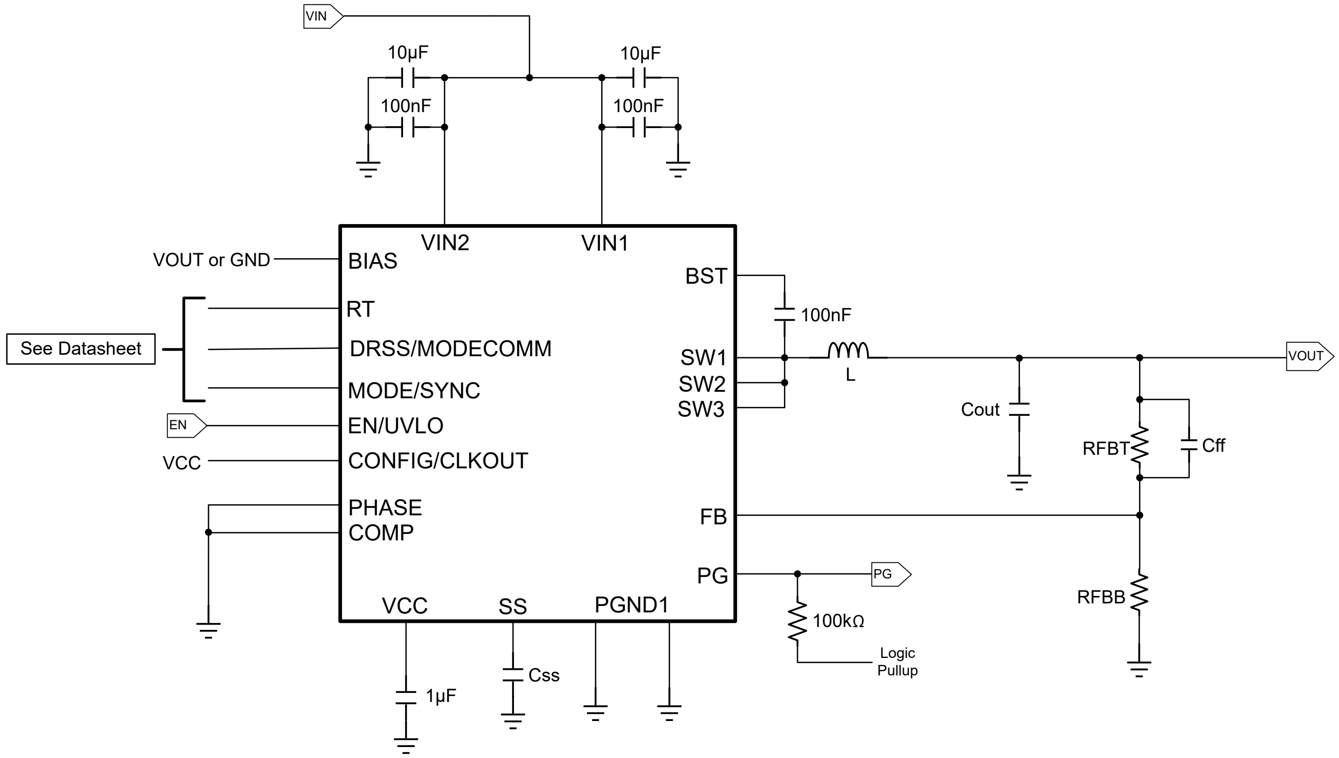


Figure 8-2. Example Single Phase Application Using Adjustable Output Voltage and Internal Compensation

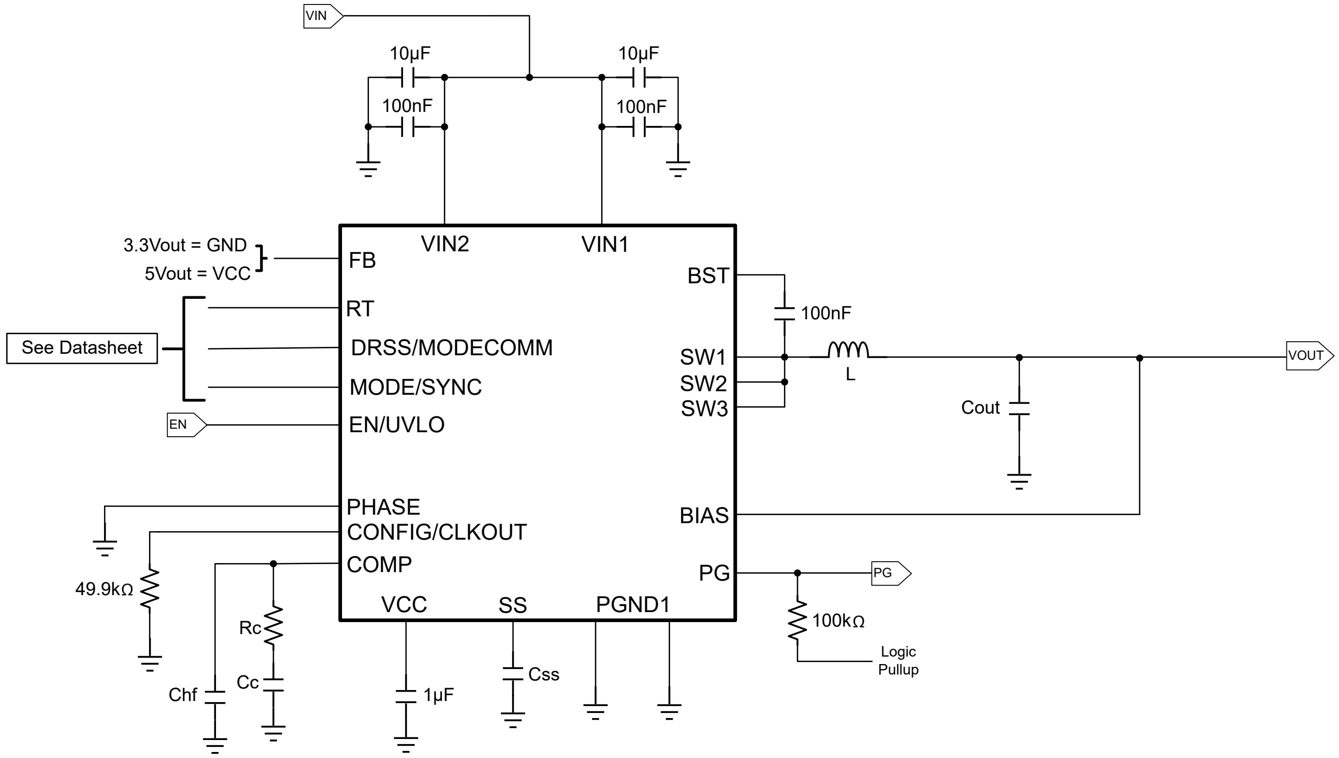


Figure 8-3. Example Single Phase Application Using Fixed Output Voltage and External Compensation

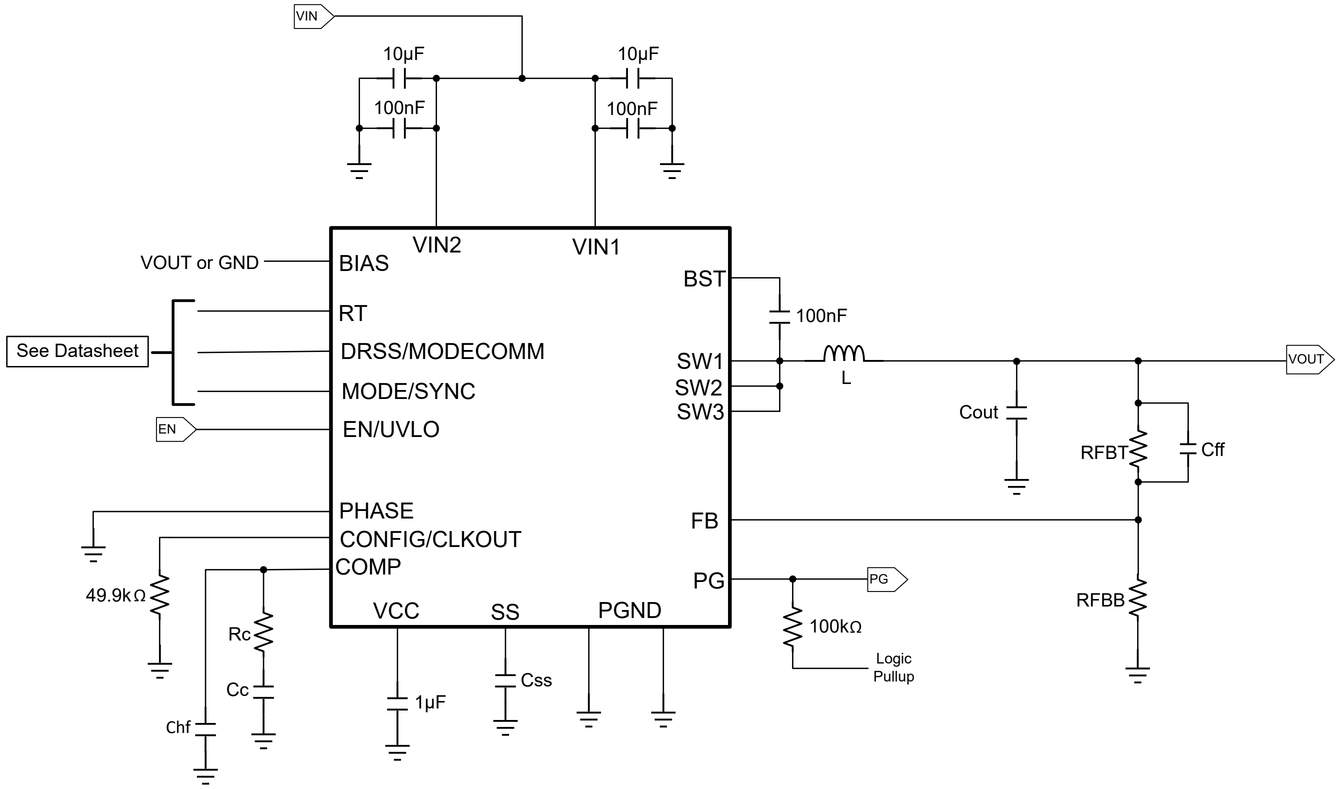


Figure 8-4. Example Single Phase Application Using Adjustable Output Voltage and External Compensation

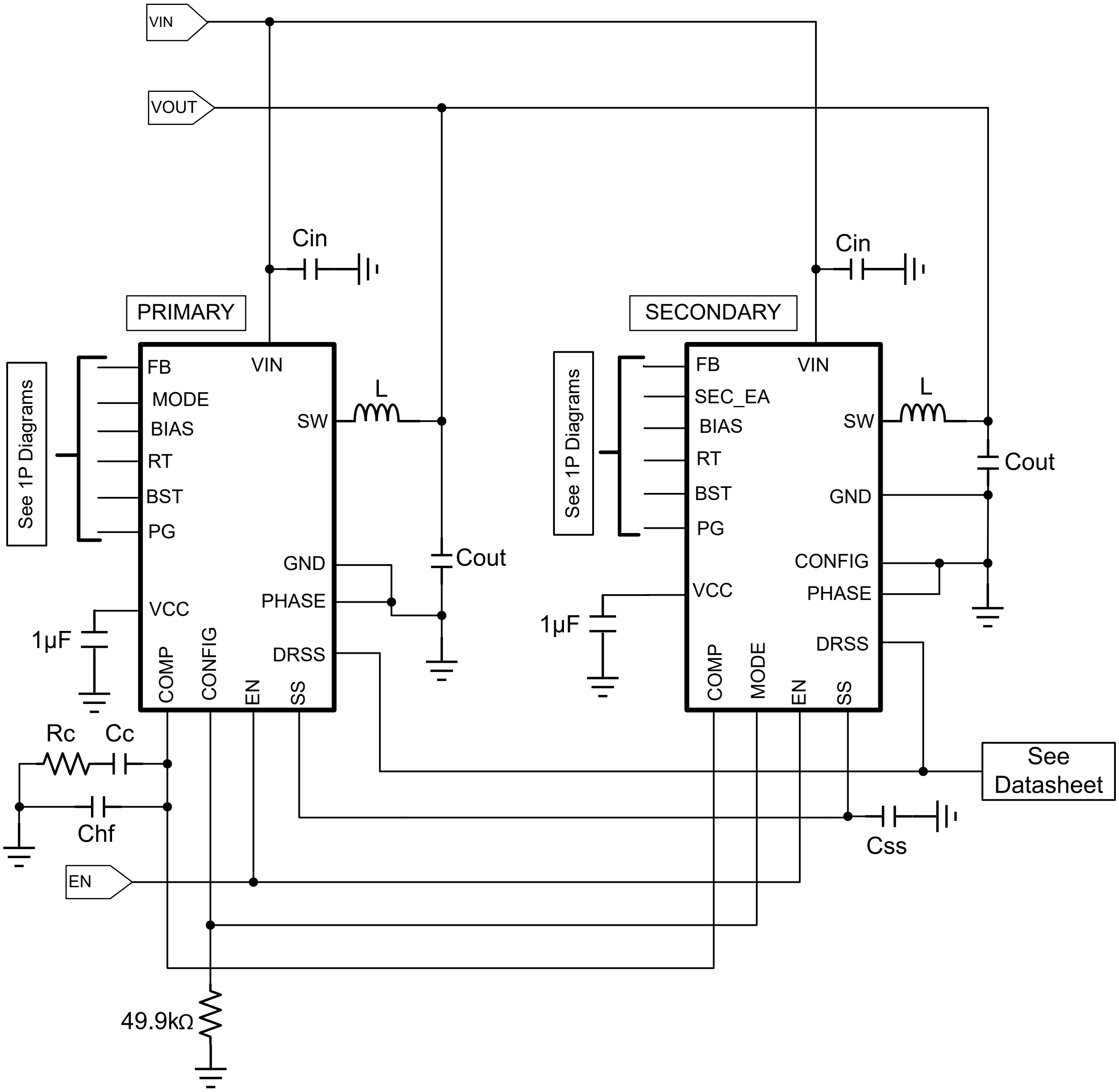


Figure 8-5. Simplified Two-Phase Application Circuit Example

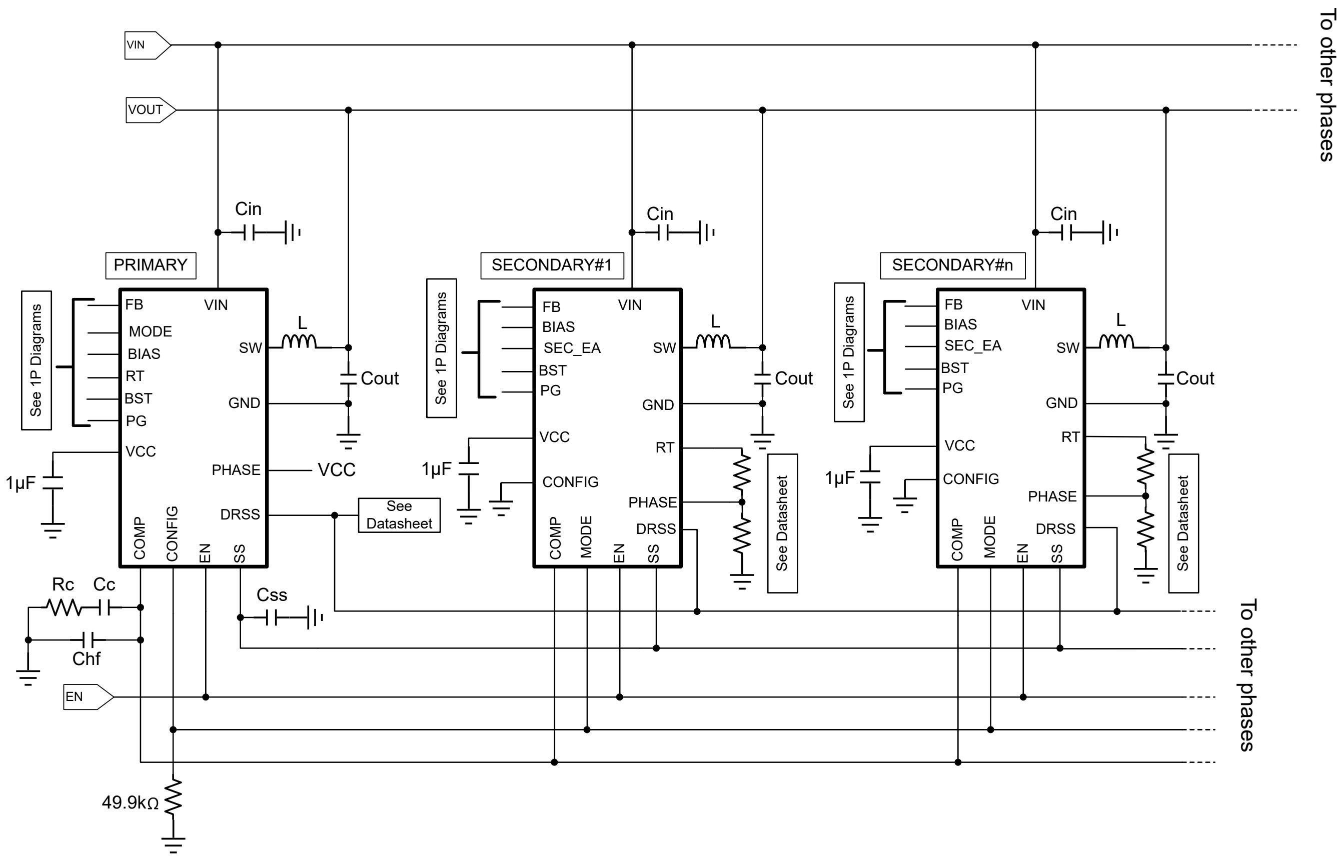


Figure 8-6. Simplified Multi-Phase Application Circuit Example

Table 8-1. Typical External Components for Fixed Output Voltage Mode

OUTPUT VOLTAGE	FREQUENCY	FB	LM6xxB0		LM6xxA5		LM6xxA2		LM6xxA0	
			L	COUT	L	COUT [(1)]	L	COUT [(1)]	L	COUT [(1)]
3.3V	400kHz	GND	1µH	245µF	1.5µH	245µF	1.8µH	196µF	2.2µH	161µF
5V	400kHz	VCC	1.5µH	175µF	1.8µH	175µF	2.2µH	140µF	2.7µH	115µF
3.3V	2200kHz	GND	0.22µH	105µF	0.27µH	105µF	0.33µH	85µF	0.47µH	70µF
5V	2200kHz	VCC	0.33µH	70µF	0.38µH	70µF	0.47µH	53µF	0.68µH	46µF

(1) All COUT values shown in these tables, and in this datasheet, represent the capacitance under the indicated D.C. bias and all other applicable derating.

Table 8-2. Typical External Components for LM6x4B0 in Adjustable Output Voltage Mode

OUTPUT VOLTAGE	FREQUENCY	L	COUT PER PHASE(1)	R_{FBT}	R_{FBB}	C_{FF}	R_{COMP} (2)	C_{COMP} (2)
3.3V	400kHz	1µH	245µF	100kΩ	31.6kΩ	20pF	7.5kΩ/Ne	10nF × Ne
4.5V	400kHz	1.2µH	175µF	100kΩ	21.5kΩ	20pF	7.5kΩ/Ne	10nF × Ne
5V	400kHz	1.5µH	175µF	100kΩ	19.1kΩ	20pF	7.5kΩ/Ne	10nF × Ne
3.3V	2200kHz	0.22µH	105µF	100kΩ	31.6kΩ	10pF	7.5kΩ/Ne	2.2nF × Ne
4.5V	2200kHz	0.27µH	70µF	100kΩ	21.5kΩ	10pF	7.5kΩ/Ne	2.2nF × Ne
5V	2200kHz	0.33µH	70µF	100kΩ	19.1kΩ	10pF	7.5kΩ/Ne	2.2nF × Ne

(1) All COUT values shown in these tables, and in this datasheet, represent the capacitance under the indicated D.C. bias and all other applicable derating.
(2) Ne equals the number of secondary error amplifiers enabled in the application.

8.2.1 Design Example Requirements

The following example provides a detailed design procedure based on the specifications found in Table 8-3. Figure 8-7 shows the complete detailed design schematic.

Table 8-3. Detailed Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	8V to 18V
Minimum transient input voltage (warm crank)	6V
Maximum transient input voltage (load dump)	36V
Output voltage	5V
Steady state output current	12A
Transient load current	20A
Switching frequency	2100kHz
Output voltage regulation	±1%
Active current, no load	23µA
DRSS	8.5%

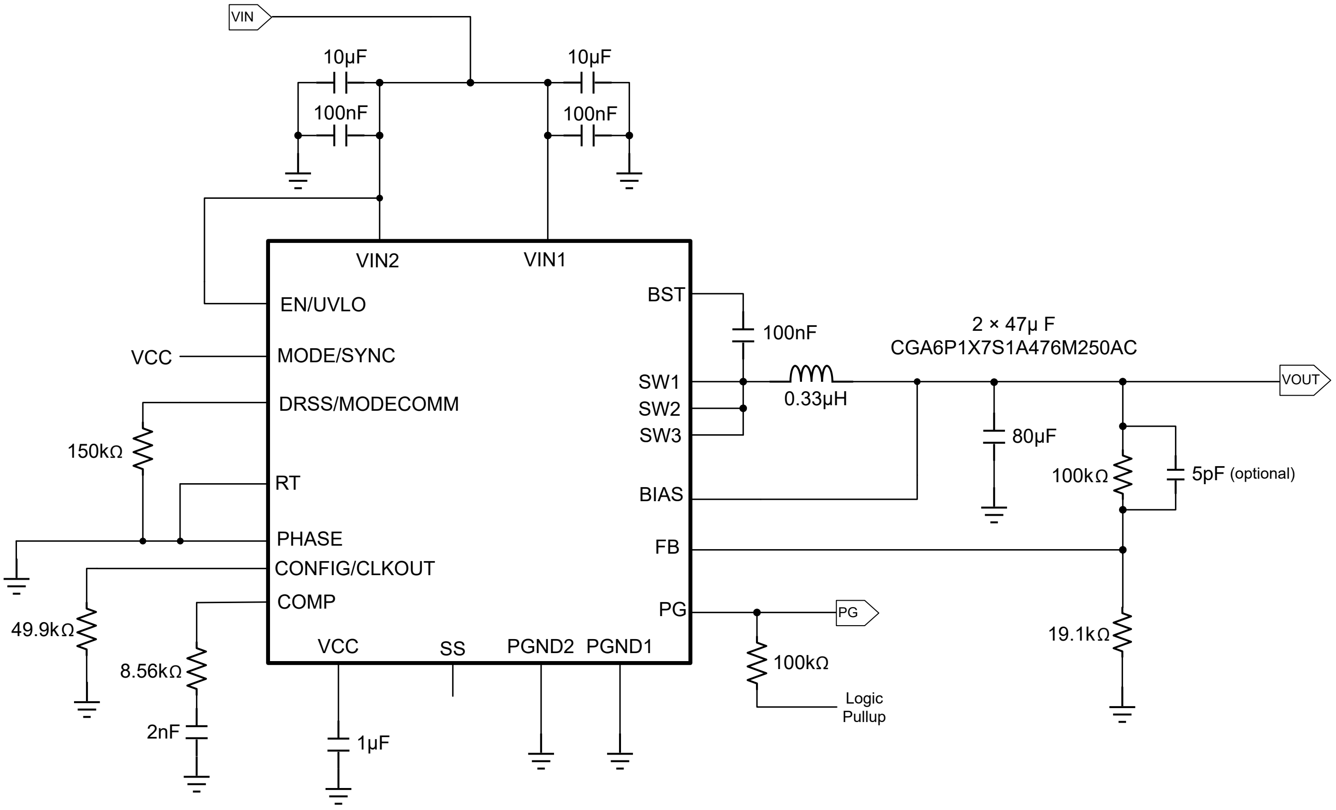


Figure 8-7. Design Example Schematic

8.2.2 Detailed Design Procedure

The following design procedure applies to Table 8-3. Based on the transient load current requirement of 20A, select the LM654B0 in a single phase design. The 12A steady state load requirement must be easy to achieve with a proper PCB design. See Section 8.2.2.8 for details on thermal design. To demonstrate the design procedure, select the adjustable output voltage mode and external loop compensation.

8.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and typically results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this application example, a compact design is selected with a frequency of 2100kHz. In this case, the RT pin can be connected to ground or to a resistor of 7.15kΩ. See also Section 7.3.5.

8.2.2.2 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 50% of the maximum output current *rating* of the device.

Larger values of ripple current can restrict the maximum output current, before current limit is reached. Smaller values of ripple current reduce the SNR of the current mode controller and can lead to increased jitter in the duty cycle. Both the inductor and switching frequency tolerance have an impact on the selection of ripple current, and, therefore, inductor value. Use the maximum device current rating when calculating the ripple current for applications with much smaller maximum load than the maximum available from the device. The ratio of inductor ripple current over maximum output current is designated as K. Use Equation 7 to determine the value of inductance:

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times K \times f_{SW} \times I_{OUT-RATED}} \quad (7)$$

The typical input voltage for the application is typically used in Equation 7. However, if the application requires very wide range of input voltages, then some voltage near the upper end of the range can be used. In any case, after the inductor has been selected, the ripple current must be checked at the maximum input voltage. Too large a ripple current can limit the maximum output current, as mentioned above. Use Equation 8 to check for these concerns.

$$I_{OUT-MAX} = I_{HS} - \frac{1}{2} \times \frac{(V_{IN-MAX} - V_{OUT}) \times V_{OUT}}{V_{IN-MAX} \times f_{SW} \times L} \quad (8)$$

During inductor selection, the saturation current rating of the inductor needs to be as large as the high-side switch current limit, $I_{HS\text{-}LIM}$. This size makes sure that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This rise can lead to component damage. Inductors with a ferrite core material have very hard saturation characteristics, but typically have lower core losses than powdered iron cores. Powdered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, powdered iron cores have more core losses at frequencies above about 1MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

To avoid subharmonic oscillation, the inductance value must not be less than that given in Equation 9. This limit applies to applications where the switch duty cycle becomes greater than or equal to 50%, under any operating condition.

$$L_{min} \geq M \times \frac{V_{OUT}}{F_{SW}} \quad (9)$$

where

- M = 0.072: LM654B0
- M = 0.1: LM654A5
- M = 0.12: LM654A2
- M = 0.15: LM654A0

The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

For this example, using the LM654B0 and assuming an 18V input, 5V output, a K = 0.3, Iout-rated = 20A and a switching frequency of 2100kHz Equation 7 gives an inductor value of 0.28µH. Use the closest standard value of 0.33µH. Equation 9 gives a minimum value of 0.17µH.

8.2.2.3 Output Capacitors

1. Use Equation 10 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 3.5% (170mV for a 5V output).

$$C_{OUT} = \frac{(\Delta I_{OUT})^2 \times L_O}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} = \frac{(20A)^2 \times 0.33\mu H}{(5V + 0.170V)^2 - 5V^2} = 76\mu F \quad (10)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select two 47µF, 10V, X7S, 1210 ceramic output capacitors. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory. For this example, choosing two TDK 47µF CGA6P1X7S1A476M250AC gives an effective capacitance of 80µF for a 5V output.

3. Use Equation 11 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{out} = \sqrt{\left(\frac{\Delta I_{LO}}{8 \times C_{OUT} \times F_{SW}}\right)^2 + \left(R_{ESR} \times \Delta I_{LO}\right)^2} = \sqrt{\left(\frac{5.2\text{A}}{8 \times 80\mu\text{F} \times 2100\text{kHz}}\right)^2 + \left(1\text{m}\Omega \times 5.2\text{A}\right)^2} = 6.4\text{mV} \quad (11)$$

$$\Delta I_{LO} = \frac{(V_{IN-MAX} - V_{OUT}) \times V_{OUT}}{V_{IN-MAX} \times f_{SW} \times L} \quad (12)$$

where

- ΔI_{LO} is the desired peak-to-peak ripple inductor current. For this example, a 20A rated device with K = 0.3 yields an inductor ripple current of 5.2A.
- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 80µF is the total effective (derated) ceramic output capacitance at 5V.

4. Use Equation 13 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO(rms)} \cong 0.29 \times \Delta I_{LO} = 1.5\text{A} \quad (13)$$

8.2.2.4 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 2 × 4.7µF is required on the input of the regulator. Place one capacitor on each side of the package and connected directly to the VIN and GND pins of the device. This capacitance must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. The value can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, high frequency bypass capacitors of 2 × 100nF ceramic capacitor must be used at the input. Place one capacitor on each side of the package and connected directly to the VIN and GND pins of the device. The 100nF high frequency input capacitors must be placed with 1mm of the VIN and PGND pins of the regulator. This requirement provides a high frequency bypass for the control circuits internal to the device.

For this example, 2 × 10µF, 50V, X5R (or better) ceramic capacitors are chosen. The 100nF capacitors must also be rated at 50V with an X7R (or better) dielectric.

Using an electrolytic capacitor on the input in parallel with the ceramics is often desirable. This statement is especially true if long leads or traces are used to connect the input supply to the regulator, or an input EMI filter is used. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by any inductance on the input. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from Equation 14 and must be checked against the manufacturers maximum ratings. For this example, the input capacitor RMS current is about 6A.

$$I_{CIN(rms)} \cong \frac{I_{OUT}}{2} \quad (14)$$

8.2.2.5 Setting the Output Voltage

The adjustable output voltage version of the LM654xx-Q1 uses a feedback divider network to set the output voltage. The divider network comprises top and bottom feedback resistors designated as R_{FBT} and R_{FBB}, respectively. The resistances of the feedback divider are a compromise between excessive noise pickup and quiescent current consumption. Lower resistance values reduce noise sensitivity but also impact light-load efficiency. The recommended value for R_{FBT} is 100kΩ with a maximum value of 1000kΩ. Use Equation 15 to calculate the value of R_{FBB} after R_{FBT} is selected.

$$R_{FBB} = R_{FBT} \times \frac{0.8}{V_{OUT} - 0.8} \quad (15)$$

Note that Equation 16 states that the parallel combination of R_{FBB} and R_{FBT} must be greater than 4kΩ and less than 100kΩ. This limit is required because the regulator must reliably detect the state of the FB pin during the start-up sequence to set the output voltage configuration (fixed or adjustable output voltage setting) correctly.

$$100\text{k}\Omega \geq R_{FBB} || R_{FBT} \geq 4\text{k}\Omega \tag{16}$$

For this example, select R_{FBT} and R_{FBB} values of 100kΩ and 19.1kΩ, respectively. This selection sets the output voltage to 5V and satisfy both Equation 15 and Equation 16.

8.2.2.6 Compensation Components

Select compensation components for a stable control loop using the procedure outlined as follows.

1. For this example, select a loop crossover frequency of about 130kHz (f_C). This value is less than 1/10 of the switching frequency and provides good loop bandwidth. From Equation 17 with an effective output capacitance of 80µF (2 × 47µF TDK CGA6P1X7S1A476M250AC capacitors) calculate the value of R_{comp} to be about 8.51kΩ; use a standard value of 8.56kΩ.

   $$R_{comp} = 2 \times \pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{C_{OUT}}{g_{me} \times G} \tag{17}$$

   Where:

   - $g_{me} = 0.001$
   - $V_{REF} = 0.8$
   - G = 48A/V for LM654B0
   - G = 35A/V for LM654A5
   - G = 28.5A/V for LM654A2
   - G = 23.5A/V for LM654A0
2. To provide adequate phase boost at crossover while also allowing a fast settling time during a load or line transient, select C_{COMP} to place a zero at: (a) one eighth of the crossover frequency, or (b) the load pole. Select the lower of these two values for C_{COMP}. Use Equation 18 for the first requirement and Equation 19 and Equation 20 for the second. Based on this method, C_{COMPa} = 1.1nF and C_{COMPb} = 4nF. We select C_{COMP} = 2nF for this application.

   $$C_{COMPa} = \frac{8}{2 \times \pi \times f_C \times R_{comp}} \tag{18}$$

   $$f_{load} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{Load}} \tag{19}$$

   $$C_{COMPb} = \frac{1}{2 \times \pi \times f_{load} \times R_{comp}} \tag{20}$$

   A low capacitance for C_{COMP} also helps to avoid output voltage overshoot when recovering from dropout (when the input voltage is less than the output voltage set point and V_{COMP} is railed high).
3. For multiphase designs only small changes are needed in the compensation. As an example, for a three phase design, the gain of the loop is three times higher. However, if the output capacitance calculated for one phase is replicated for each phase, for a total of 3 × 80µF, the extra gain is canceled by the increased output capacitance keeping the R_{COMP} and C_{COMP} unchanged.

   Multiple error amplifiers can be enabled to help mitigate the effects of a parasitic pole created from R_{COMP} and the trace routing capacitance of COMP. This allows the bandwidth to be increased to higher frequencies for even faster transient response. For example, if two error amplifiers are enabled, Ne = 2, then R_{COMP} is reduced by 2, and C_{COMP} is increased by 2.

   A high frequency loop capacitor can be placed on the COMP pin to ground to help roll off the frequency response near the switching frequency or mitigate the effect of output capacitor ESR. The value of this capacitor is best determined experimentally in the final design, if needed. A place on the PCB must be reserved for this capacitor (C_{HF}).

Note

Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

Note

Use the quick start calculator tool associated with this family of devices to provide optimum loop compensation.

8.2.2.7 Feed-forward Capacitor (C_{FF})

The value of the C_{FF} capacitor is calculated so that the resulting phase margin of the overall system is improved. The addition of the C_{FF} capacitor does not change the response of the system at the DC level or at lower frequencies. At higher frequencies, the capacitor helps reduce the impedance from V_{OUT} to FB. This action helps propagate any high frequency change due to a fast load transient at the output to the feedback, and allows the error amplifier to correct for this.

In the frequency domain, the addition of the C_{FF} capacitor creates one zero and one pole. The zero helps increase the gain by 20dB/decade and gives a phase boost at the loop crossover frequency, that increases the phase margin of the loop. This extra phase boost is most effective when there is a wide ratio between the output voltage and the reference voltage values. Adding a C_{FF} to a low VOUT application does not provide much help to the phase margin of the loop. The pole from C_{FF} helps to roll off the frequency response and improve the loop gain margin.

Phase boost values at the loop crossover frequency in the range of 5º to 20º are reasonable. The loop crossover frequency is generally increased slightly by the use of a CFF, so only moderate values of phase boost must be used. Use Equation 21 to help select a starting point value for C_{FF} for a desired phase boost, θ_B, in the above range, in degrees.

$$C_{FF} \cong \frac{\theta_B}{360 \times R_{FBT} \times f_C \times \left(1 - \frac{0.8}{V_{OUT}}\right)} \tag{21}$$

Where:

- C_{FF} = Feed forward capacitor value (F)
- R_{FBT} = Upper feedback resistor value (Ω)
- θ_B = Desired phase boost (º)
- f_C = Loop crossover frequency (Hz)
- V_{OUT} = Output voltage (V)

For the conditions of this example and assuming a desired phase boost of 10º, we get a value of 2.5pF. In this case a 5pFcapacitor can be used and the results evaluated on the bench.

This method of selecting a C_{FF} gives only an estimate. In addition, a C_{FF} can not be needed in every case. The best way to select C_{FF}, if used, is to follow the recommendations in the quick start calculator tool for this family of devices. In any case, a place for a C_{FF} must be provided on the PCB.

8.2.2.8 Maximum Ambient Temperature

As with any power conversion device, the LM654xx-Q1 family of regulators dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum junction temperature for the LM654xx-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 22 shows the relationships between the important parameters. Higher ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* application note, many of the values given in the column labeled "JESD"of the *Thermal Information* table are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that column of the table are measured under a specific set of conditions that are rarely obtained in an actual application. The column labeled "LM654B0EVM" represent measured data on the EVM, and can be helpful when estimating thermal performance. Also, the data given for $R_{\theta JC(bott)}$, $R_{\theta JC(top)}$, and Ψ_{JT} can be useful.

$$I_{OUT_{MAX}} = \left(\frac{T_J - T_A}{R_{\theta JA}}\right) \times \left(\frac{\eta}{1-\eta}\right) \times \left(\frac{1}{V_{OUT}}\right) \tag{22}$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature, flow
- PCB area
- Copper heat-sink area
- External heat-sink
- Number of thermal vias under the package
- Adjacent component placement

The advanced package used for this regulator features a die attach paddle, or "thermal pad" (DAP), to provide a place to solder down to the PCB heat-sinking copper. This feature provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. A typical curve of $R_{\theta JA}$ versus copper board area can be found in Figure 8-8. The copper area given in the graph is for each of six layers. The top and bottom layers are 2oz copper each, while the inner layers are 1oz. Remember that the data given in this graph is for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors. As one data point, the EVM exhibits an approximate $R_{\theta JA}$ of about 16ºC/W for a copper area of about $100cm^2$, using a six layer design.

In addition, the package for this device family features an exposed top side. This allows the use of an external heat-sink to further reduce the effective $R_{\theta JA}$ when required.

The data in Figure 8-9 and Figure 8-10 provide an example of the allowable output current for a given ambient temperature. This data is valid only under the specific conditions given in the figures. The data is taken on the LM654B0EVM, with no external heat-sink and no air-flow.

The major advantage to the 'stackability" of the LM654xx family is that several regulators can be paralleled to share the total load current. Not only does advantage bring the total load current within the capability of a single regulator, but this advantage also reduces the individual power dissipation, thus reducing the regulator junction temperature.

The *PCB Thermal Design Tips for Automotive DC/DC Converters* application note is a good place to start when designing the thermal system for any DC/DC converter.

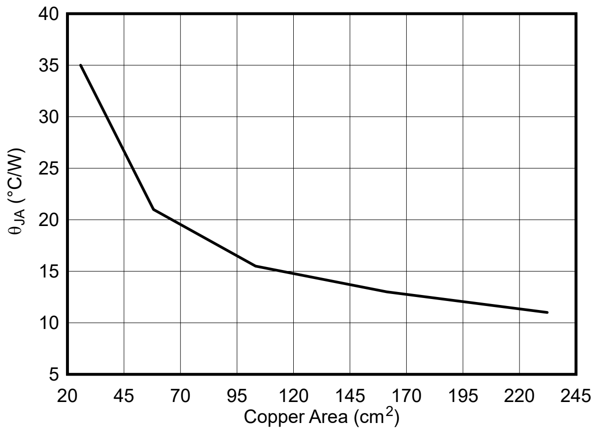
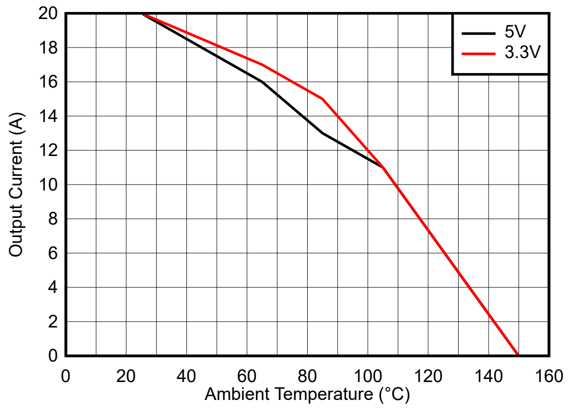
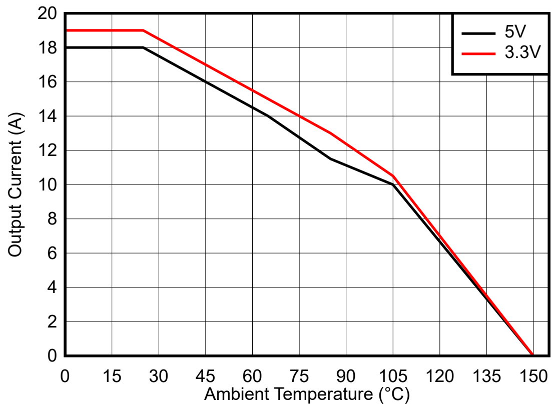


Figure 8-8. Thermal Resistance vs Copper Area



V_{IN} = 12V 400kHz TJ = 150ºC
1.2µH, 3.4mΩ

Figure 8-9. Maximum Output Current vs. Ambient Temperature



V_{IN} = 12V 2100kHz T_J = 150ºC
0.35µH, 2.2mΩ

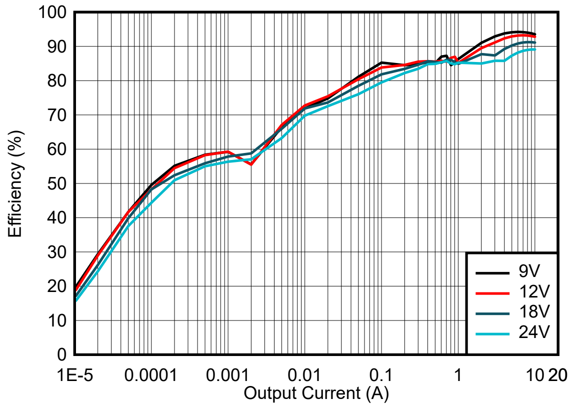
Figure 8-10. Maximum Output Current vs. Ambient Temperature

Use the following resources as guides to excellent thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight* application note
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- *How to Properly Evaluate Junction Temperature with Thermal Metrics* application note

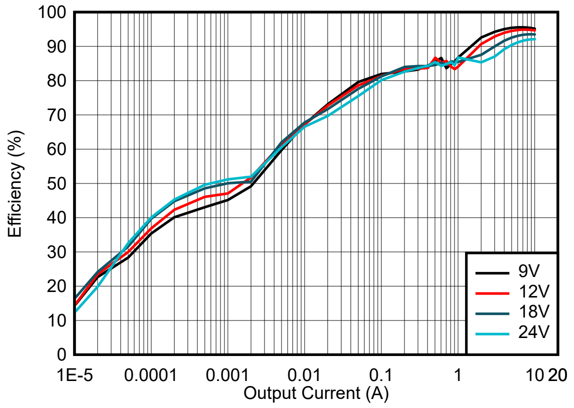
8.2.3 Application Curves

Unless otherwise specified the following condition apply: T_A = 25ºC, V_{IN} = 12V, No heat-sink. The component values for these curves can be found in Table 8-4 unless otherwise noted.



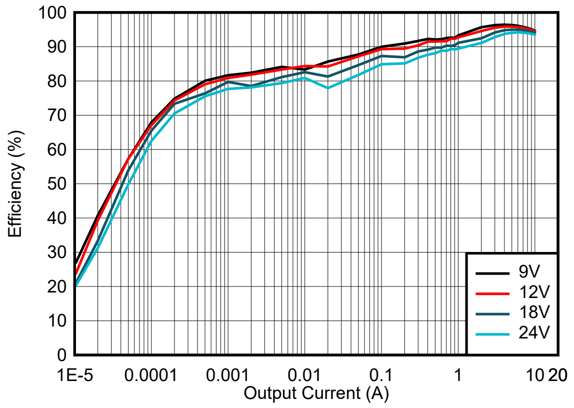
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-11. LM654A0 Efficiency



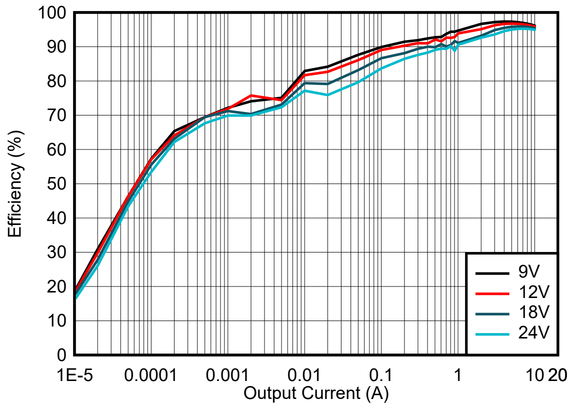
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-12. LM654A0 Efficiency



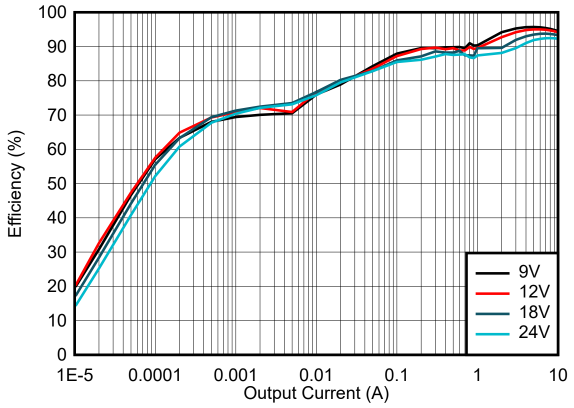
V_{OUT} = 3.3V 400kHz AUTO mode

Figure 8-13. LM654A0 Efficiency



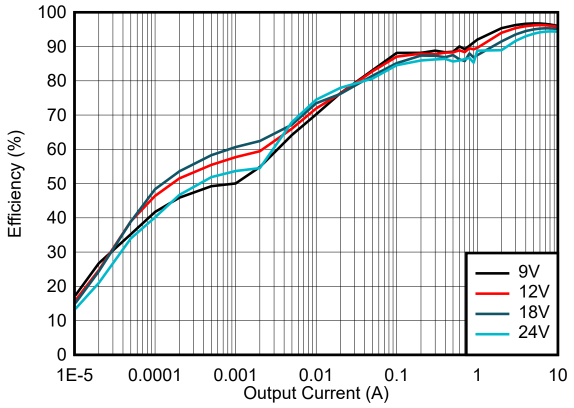
V_{OUT} = 5V 400kHz AUTO mode

Figure 8-14. LM654A0 Efficiency



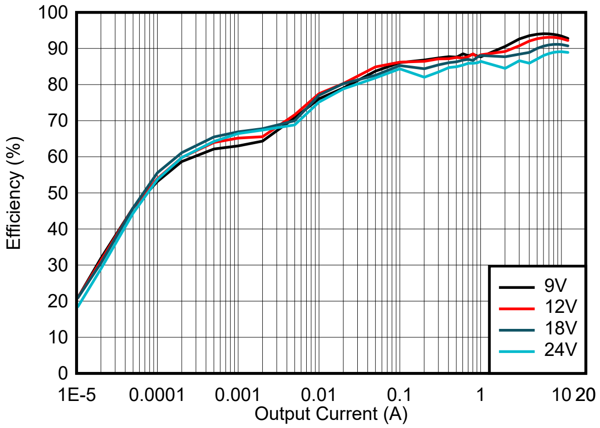
V_{OUT} = 3.3V 1000kHz AUTO mode

Figure 8-15. LM654A0 Efficiency



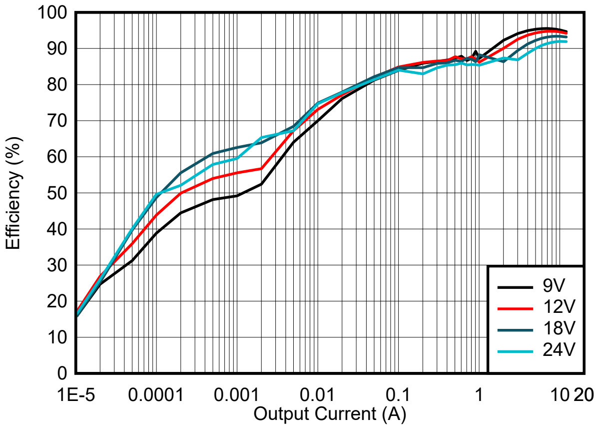
V_{OUT} = 5V 1000kHz AUTO mode

Figure 8-16. LM654A0 Efficiency



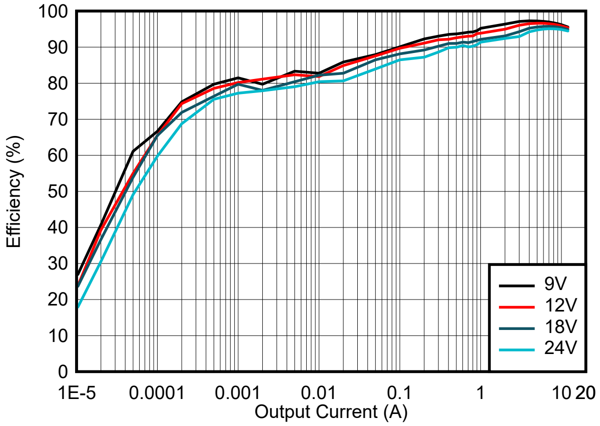
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-17. LM654A2 Efficiency



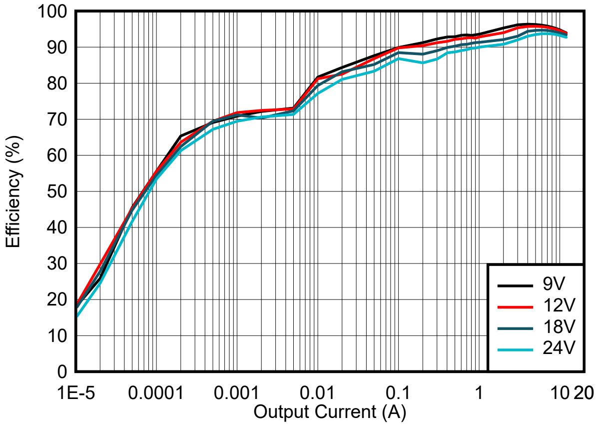
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-18. LM654A2 Efficiency



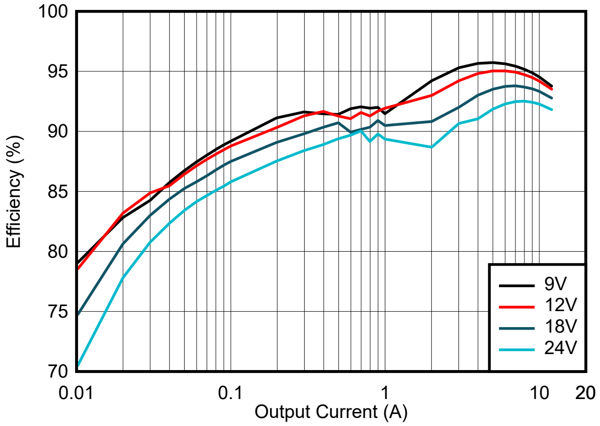
V_{OUT} = 3.3V 400kHz AUTO mode

Figure 8-19. LM654A2 Efficiency



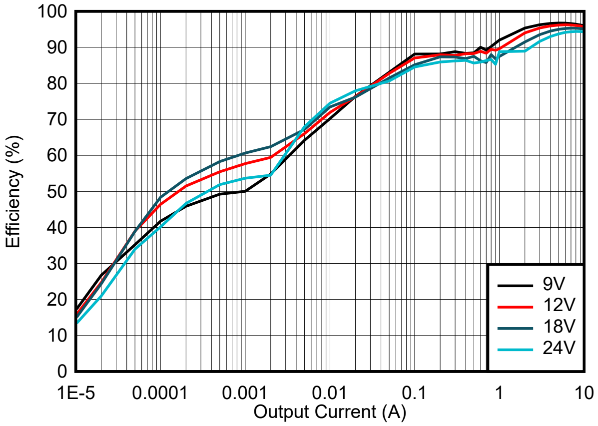
V_{OUT} = 5V 400kHz AUTO mode

Figure 8-20. LM654A2 Efficiency



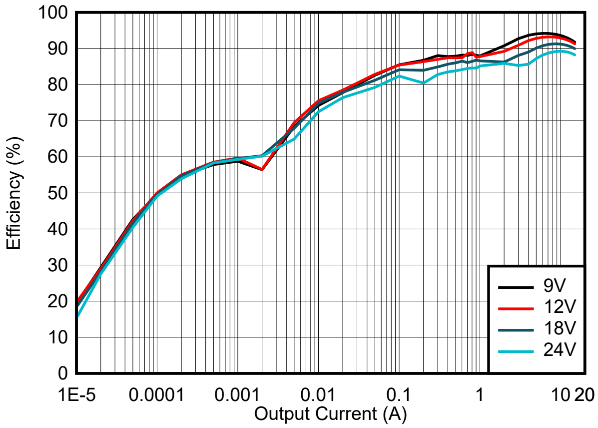
V_{OUT} = 3.3V 1000kHz AUTO mode

Figure 8-21. LM654A2 Efficiency



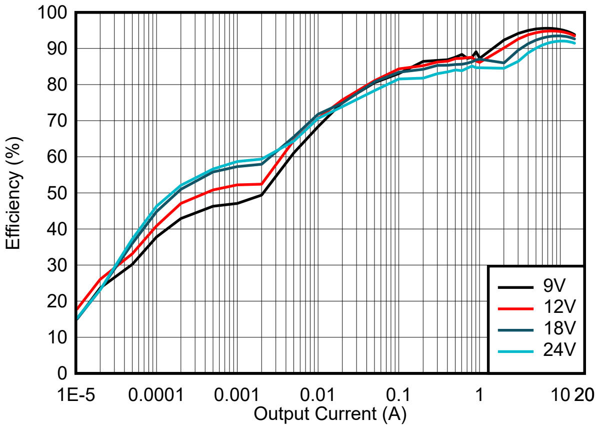
V_{OUT} = 5V 1000kHz AUTO mode

Figure 8-22. LM654A2 Efficiency



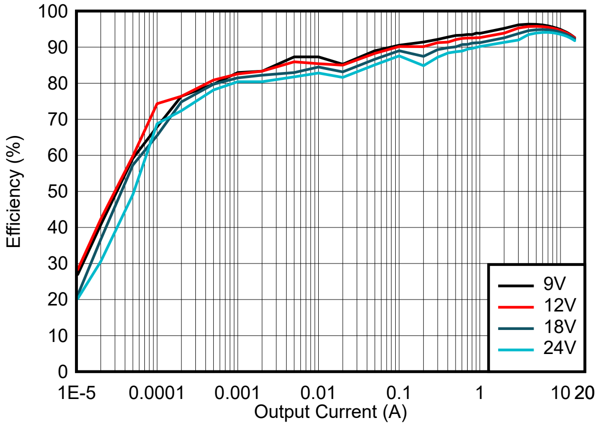
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-23. LM654A5 Efficiency



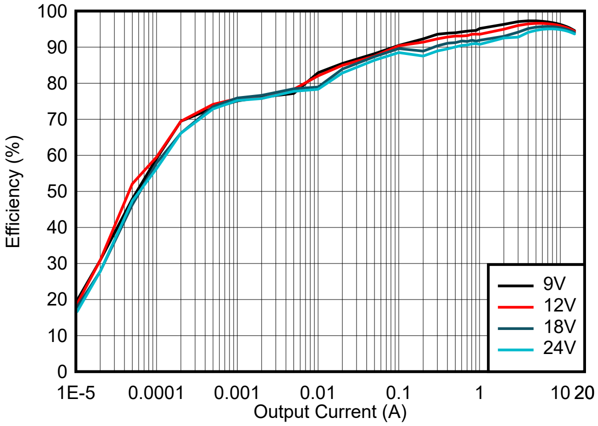
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-24. LM654A5 Efficiency



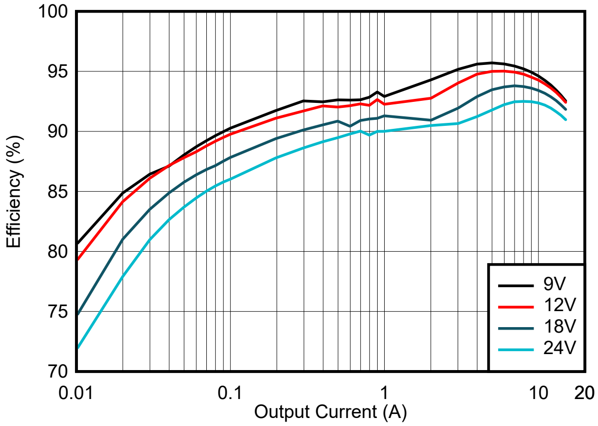
V_{OUT} = 3.3V 400kHz AUTO mode

Figure 8-25. LM654A5 Efficiency



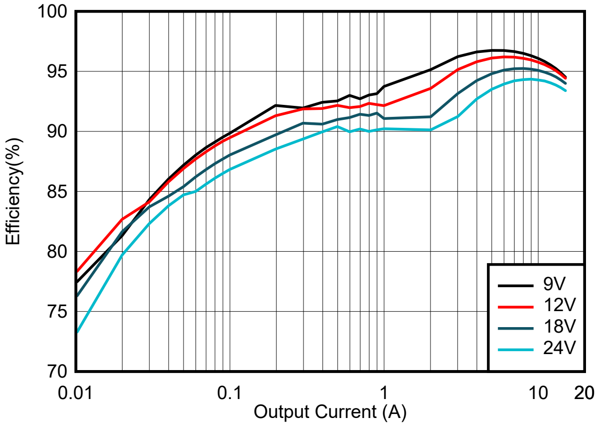
V_{OUT} = 5V 400kHz AUTO mode

Figure 8-26. LM654A5 Efficiency



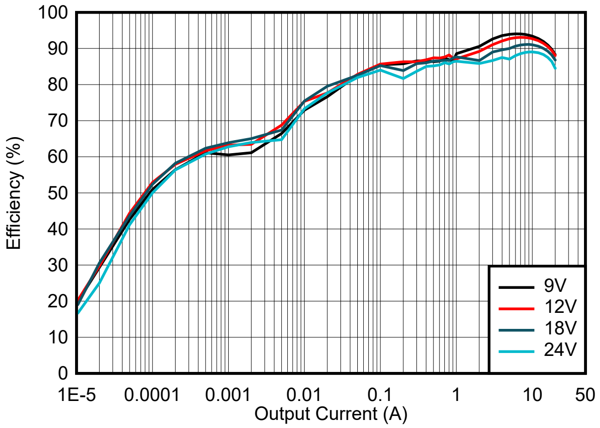
V_{OUT} = 3.3V 1000kHz AUTO mode

Figure 8-27. LM654A5 Efficiency



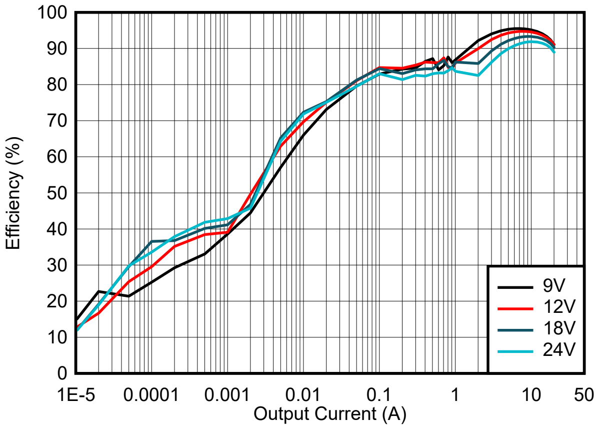
V_{OUT} = 5V 1000kHz AUTO mode

Figure 8-28. LM654A5 Efficiency



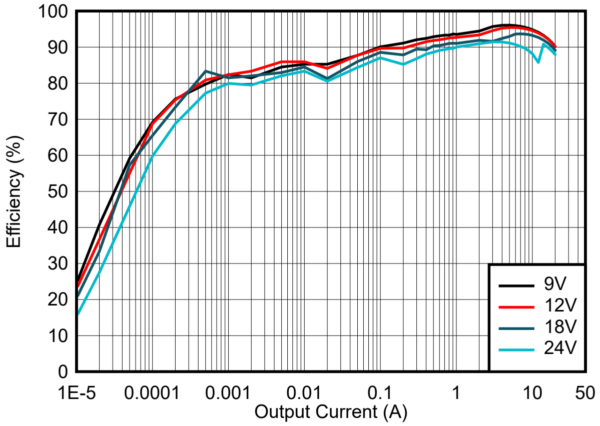
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-29. LM654B0 Efficiency



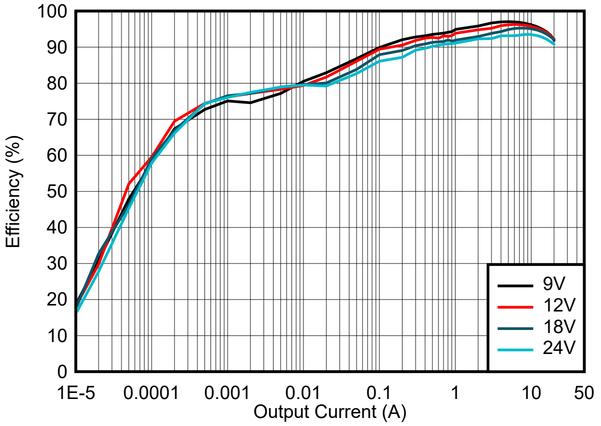
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-30. LM654B0 Efficiency



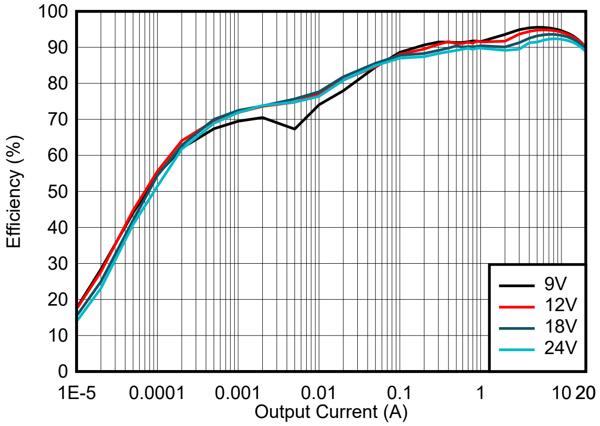
V_{OUT} = 3.3V 400kHz AUTO mode

Figure 8-31. LM654B0 Efficiency



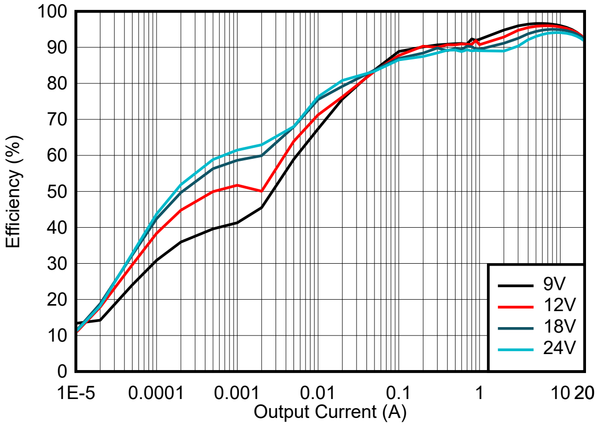
V_{OUT} = 5V 400kHz AUTO mode

Figure 8-32. LM654B0 Efficiency



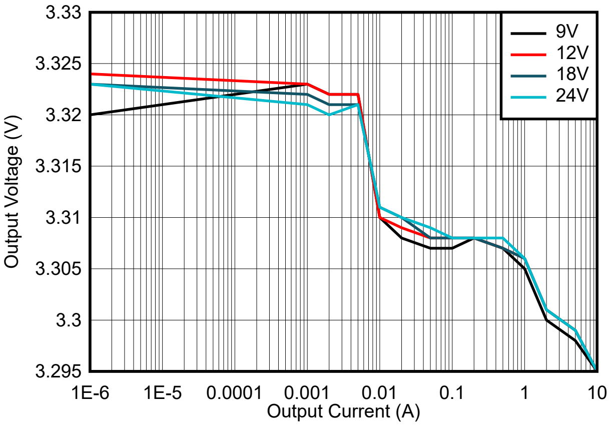
V_{OUT} = 3.3V 1000kHz AUTO mode

Figure 8-33. LM654B0 Efficiency



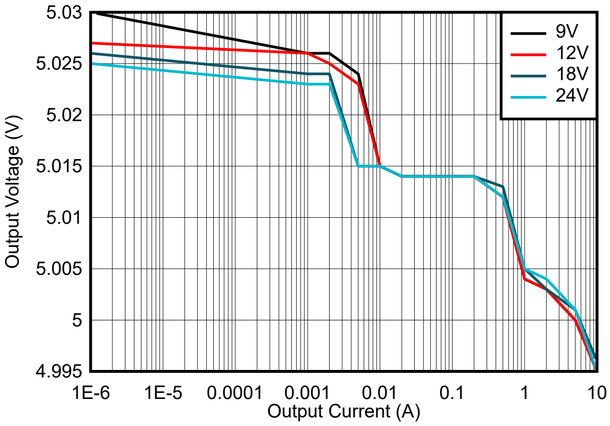
V_{OUT} = 5V 1000kHz AUTO mode

Figure 8-34. LM654B0 Efficiency



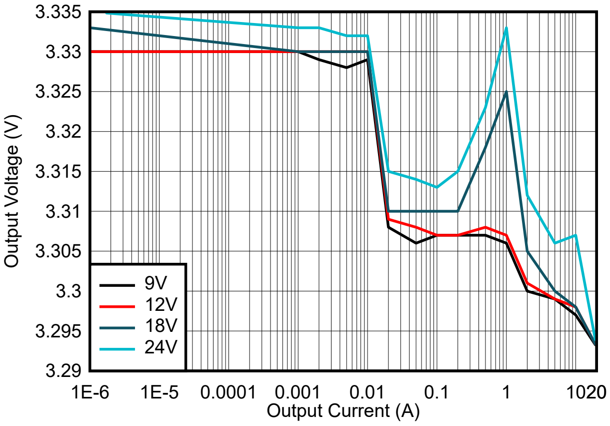
V_{OUT} = 3.3V 400kHz AUTO mode

Figure 8-35. LM654A0 Line and Load Regulation



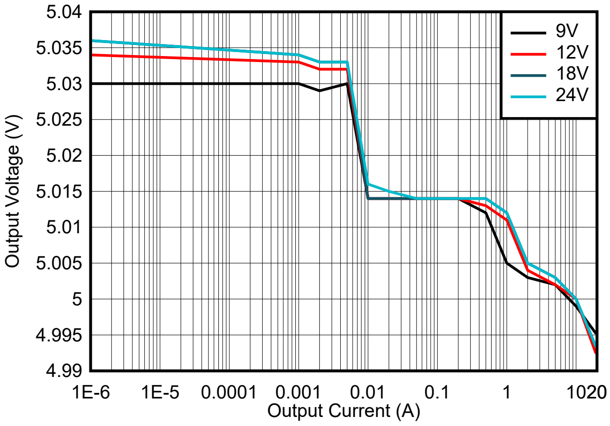
V_{OUT} = 5V 400kHz AUTO mode

Figure 8-36. LM654A0 Line and Load Regulation



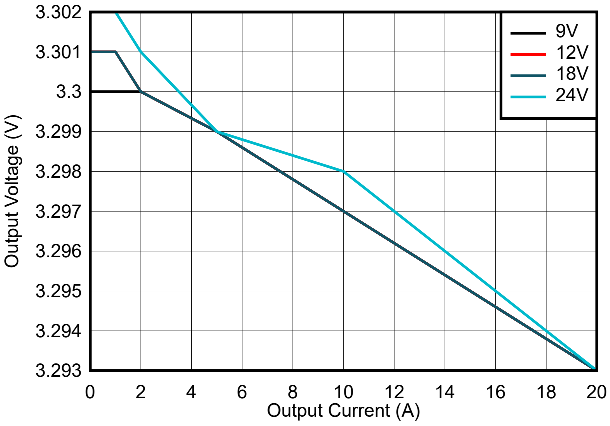
V_{OUT} = 3.3V 400kHz AUTO mode

Figure 8-37. LM654B0 Line and Load Regulation



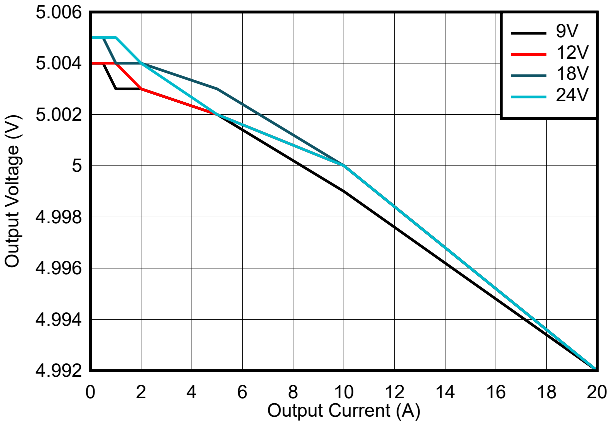
V_{OUT} = 5V 400kHz AUTO mode

Figure 8-38. LM654B0 Line and Load Regulation



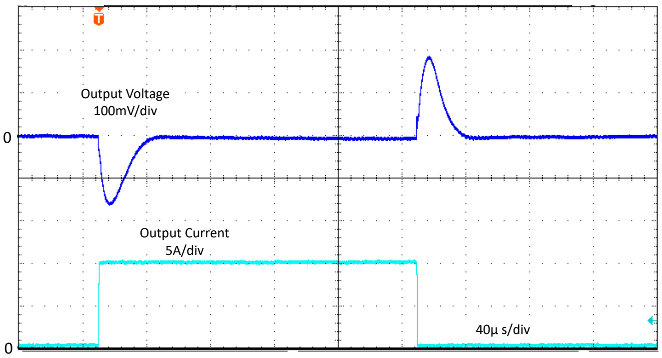
V_{OUT} = 3.3V 400kHz FPWM mode

Figure 8-39. LM654B0 Line and Load Regulation



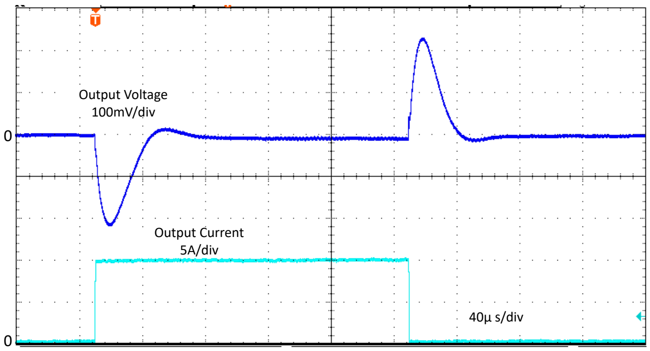
V_{OUT} = 5V 400kHz FPWM mode

Figure 8-40. LM654B0 Line and Load Regulation



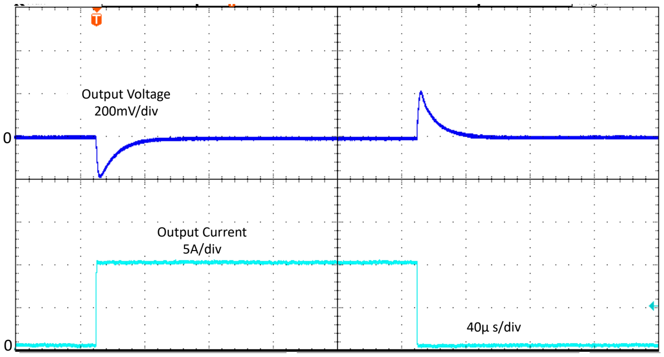
V_{OUT} = 3.3V 400kHz FPWM mode
I_{OUT} = 0A to 10A (1µs)

Figure 8-41. LM654A0 Load Transient



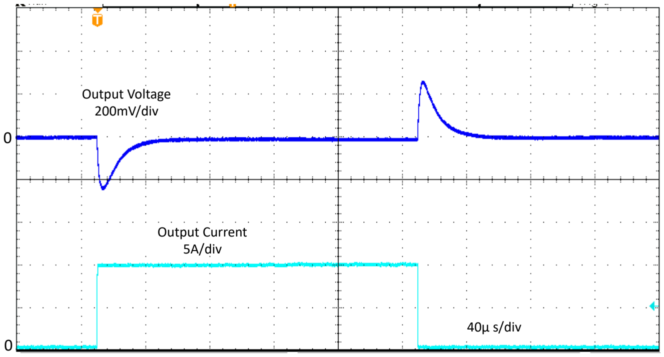
V_{OUT} = 5V 400kHz FPWM mode
I_{OUT} = 0A to 10A (1µs)

Figure 8-42. LM654A0 Load Transient



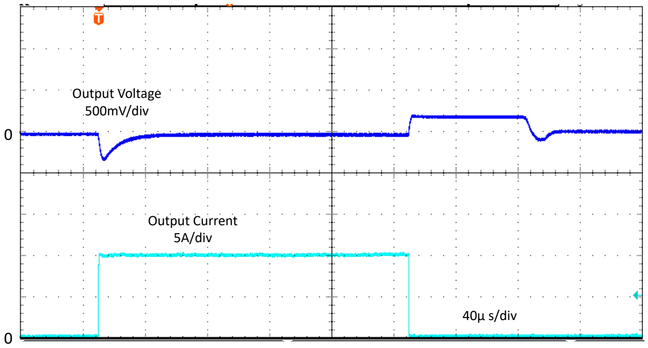
V_{OUT} = 3.3V 2100kHz FPWM mode
I_{OUT} = 0A to 10A (1µs)

Figure 8-43. LM654A0 Load Transient



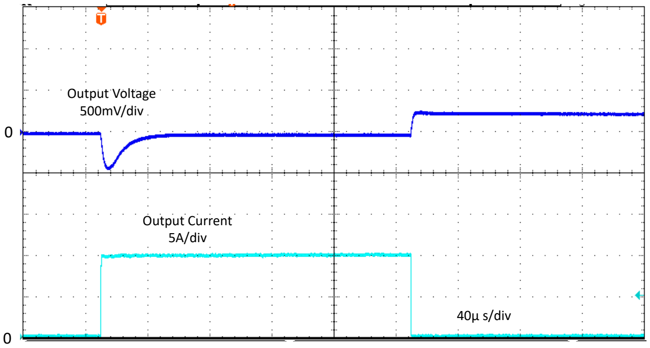
V_{OUT} = 5V 2100kHz FPWM mode
I_{OUT} = 0A to 10A (1µs)

Figure 8-44. LM654A0 Load Transient



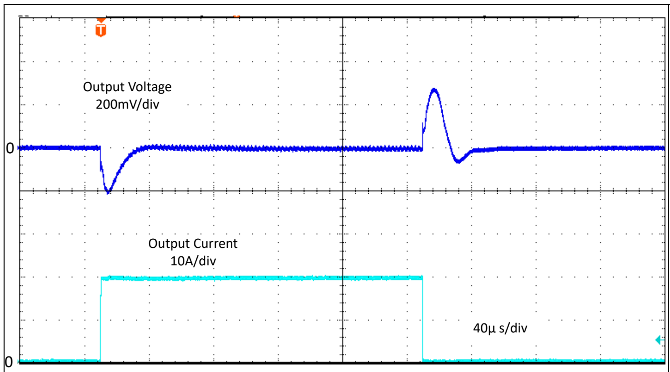
V_{OUT} = 3.3V 2100kHz AUTO mode
I_{OUT} = 0A to 10A (1µs)

Figure 8-45. LM654A0 Load Transient



V_{OUT} = 5V 2100kHz AUTO mode
I_{OUT} = 0A to 10A (1µs)

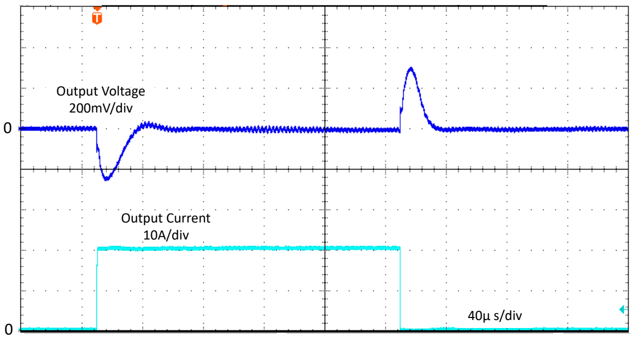
Figure 8-46. LM654A0 Load Transient



V_{OUT} = 3.3V 400kHz FPWM mode

I_{OUT} = 0A to 20A (1µs)

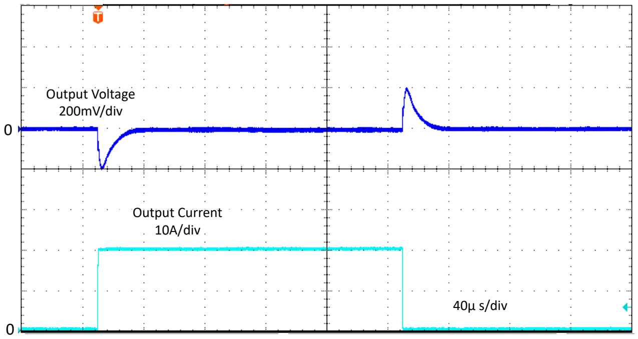
Figure 8-47. LM654B0 Load Transient



V_{OUT} = 5V 400kHz FPWM mode

I_{OUT} = 0A to 20A (1µs)

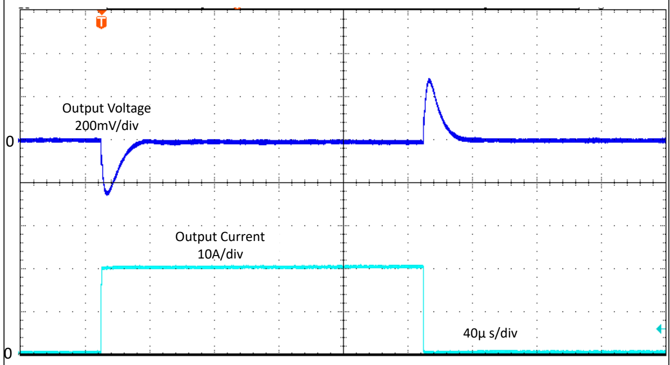
Figure 8-48. LM654B0 Load Transient



V_{OUT} = 3.3V 2100kHz FPWM mode

I_{OUT} = 0A to 20A (1µs)

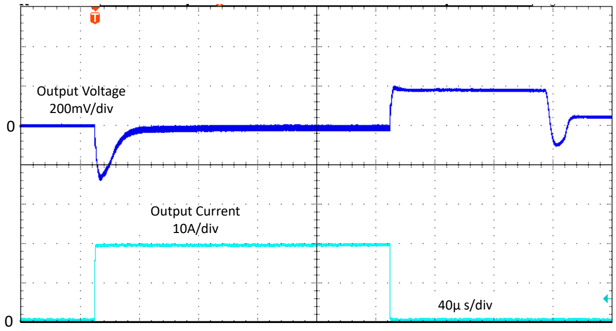
Figure 8-49. LM654B0 Load Transient



V_{OUT} = 5V 2100kHz FPWM mode

I_{OUT} = 0A to 20A (1µs)

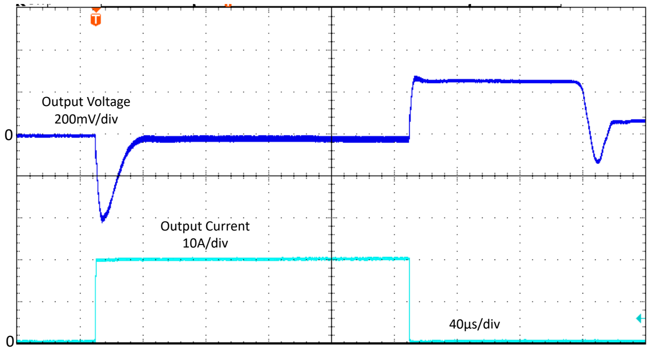
Figure 8-50. LM654B0 Load Transient



V_{OUT} = 3.3V 2100kHz AUTO mode

I_{OUT} = 0A to 20A (1µs)

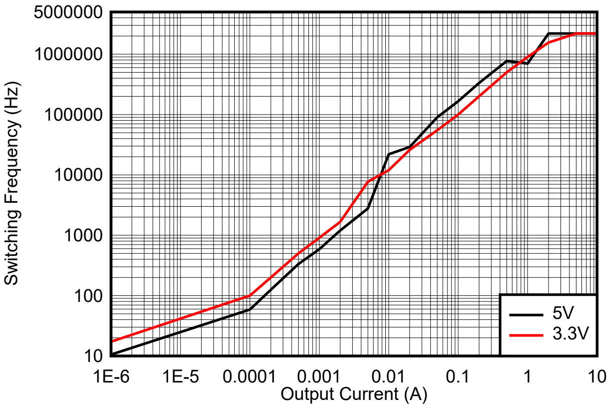
Figure 8-51. LM654B0 Load Transient



V_{OUT} = 5V 2100kHz AUTO mode

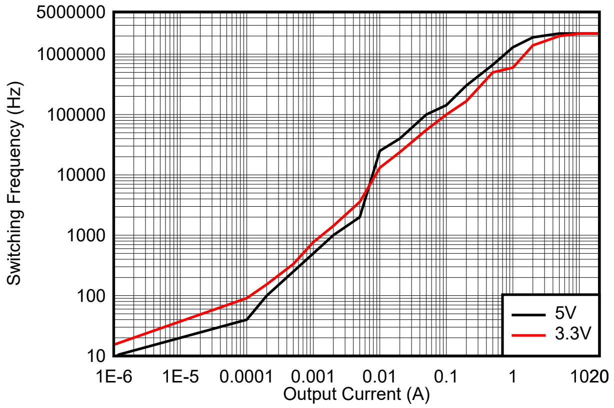
I_{OUT} = 0A to 20A (1µs)

Figure 8-52. LM654B0 Load Transient



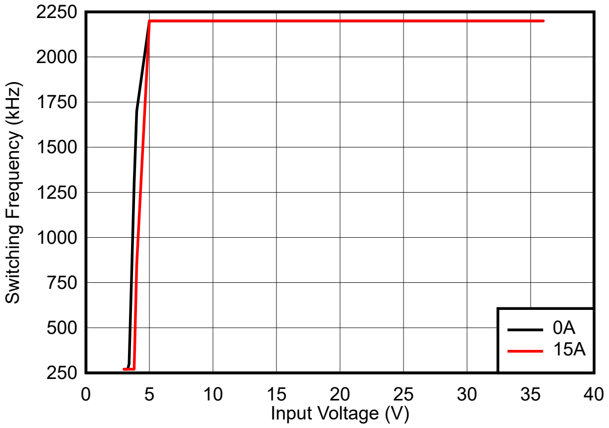
V_{IN} = 12V 2100kHz AUTO mode

Figure 8-53. LM654A0 Switching Frequency vs Output Current



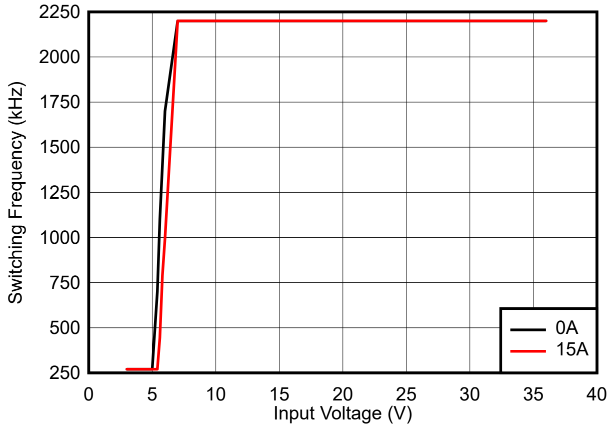
V_{IN} = 12V 2100kHz AUTO mode

Figure 8-54. LM654B0 Switching Frequency vs Output Current



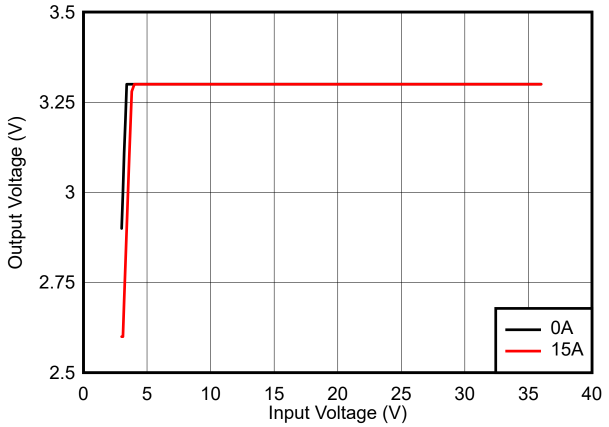
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-55. LM654B0 Switching Frequency vs Input Voltage



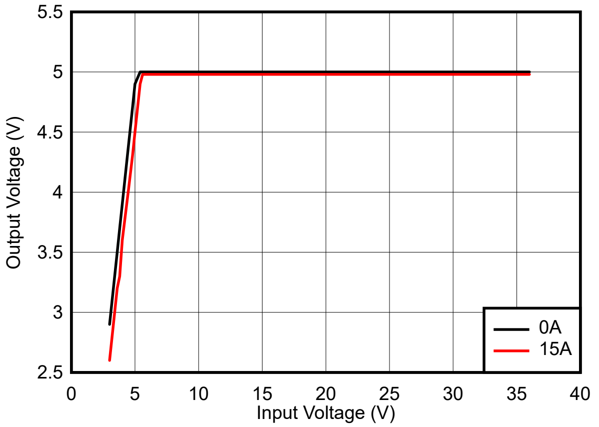
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-56. LM654B0 Switching Frequency vs Input Voltage



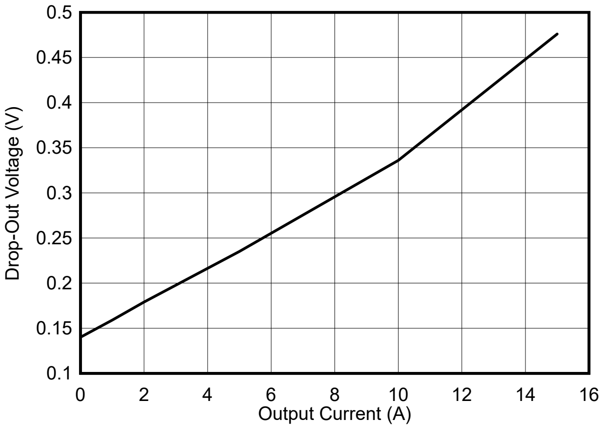
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-57. LM654B0 Output Voltage vs Input Voltage



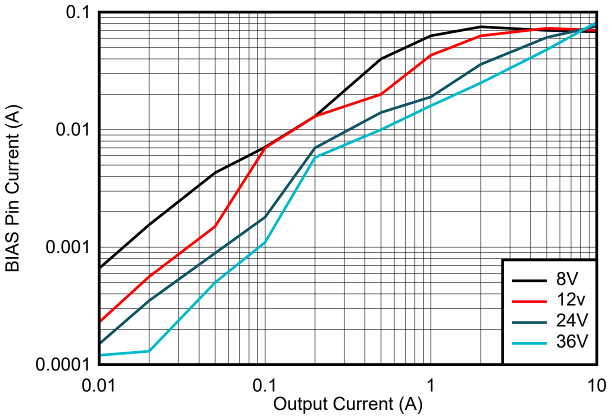
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-58. LM654B0 Output Voltage vs Input Voltage



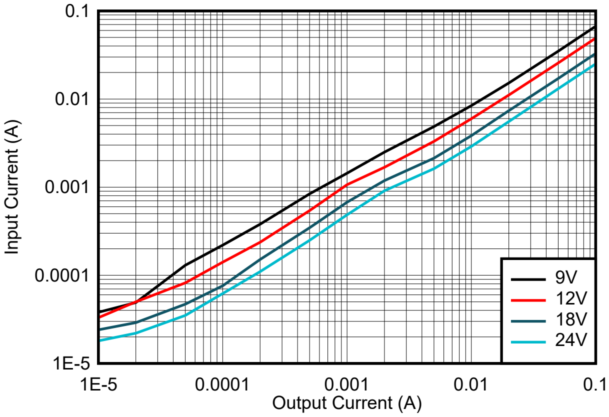
V_{OUT} = 5V-1% 2100kHz Rinductor = 1.8mΩ

Figure 8-59. LM654B0 Drop-Out Voltage



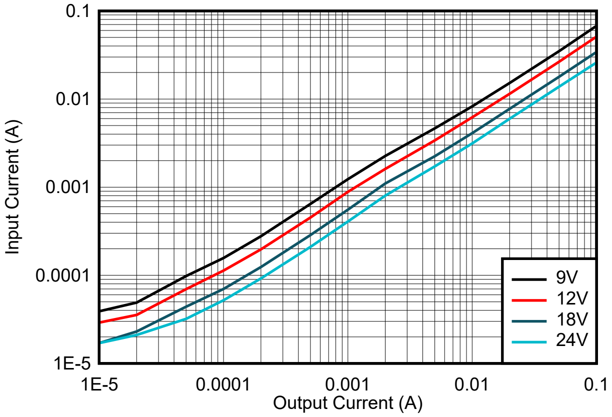
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-60. LM654B0 BIAS Pin Input Current



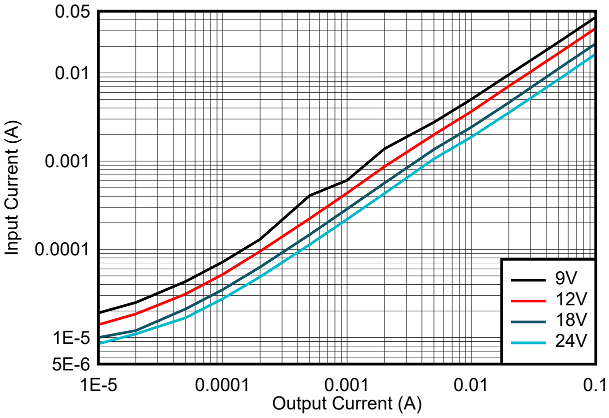
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-61. LM654B0 Input Current



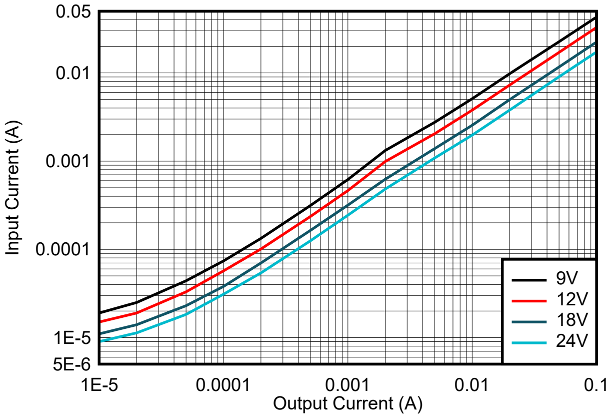
V_{OUT} = 5V 2100kHz AUTO mode

Figure 8-62. LM654A0 Input Current



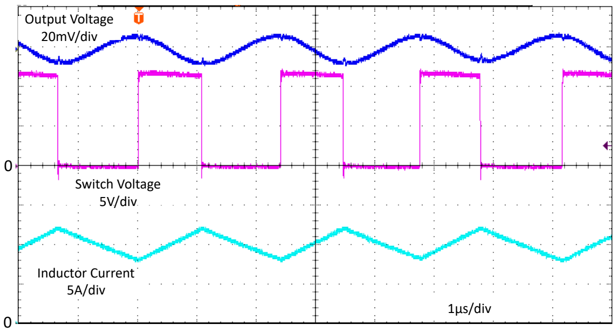
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-63. LM654B0 Input Current



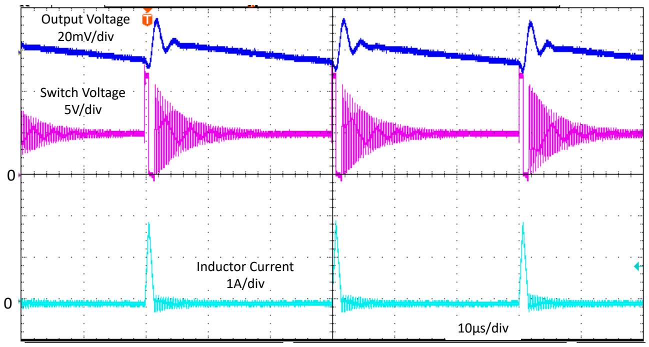
V_{OUT} = 3.3V 2100kHz AUTO mode

Figure 8-64. LM654A0 Input Current



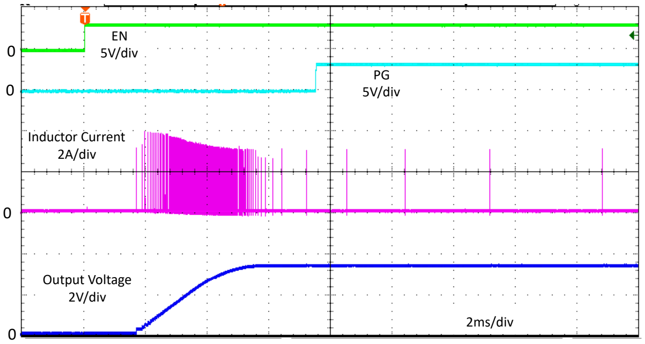
LM654A0 V_{IN} = 12V V_{OUT} = 5V
I_{OUT} = 10A 400kHz

Figure 8-65. Typical Switching Waveforms - PWM



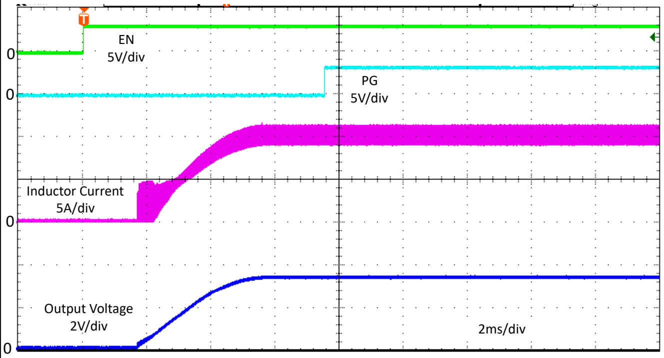
LM654A0 V_{IN} = 12V V_{OUT} = 5V
I_{OUT} = 50mA 400kHz AUTO mode

Figure 8-66. Typical Switching Waveforms - PWM



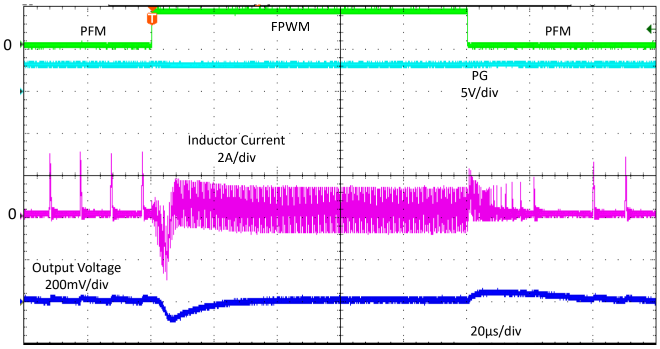
LM654A2 V_{IN} = 12V V_{OUT} = 3.3V
I_{OUT} = 0A 400kHz AUTO mode

Figure 8-67. Start-up from Enable



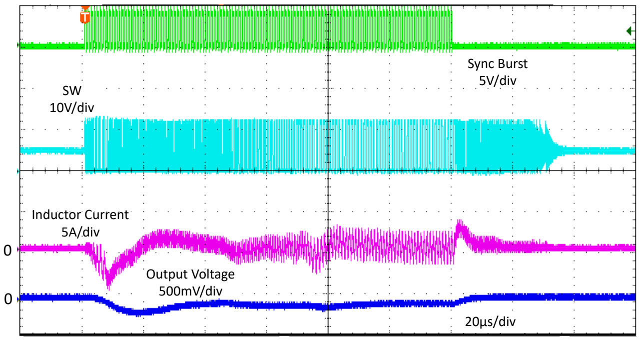
LM654A2 V_{IN} = 12V V_{OUT} = 3.3V
I_{OUT} = 10A 400kHz AUTO mode

Figure 8-68. Start-up from Enable



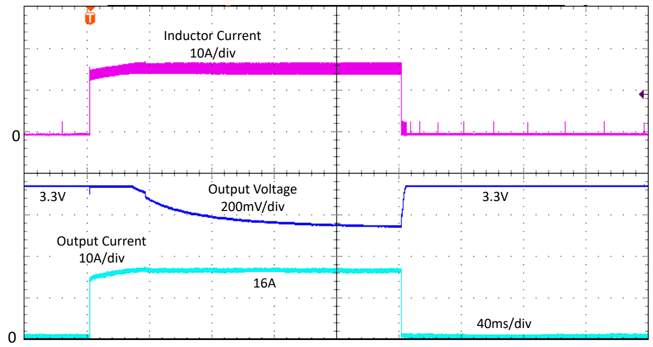
LM654A2 V_{IN} = 12V V_{OUT} = 3.3V
I_{OUT} = 100mA 2100kHz

Figure 8-69. Mode Change Transient



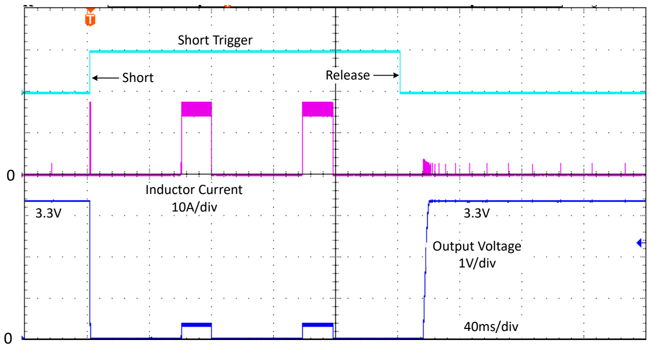
LM654A0 V_{IN} = 12V V_{OUT} = 5V
I_{OUT} = 0A AUTO Burst = 120
cycles of 1MHz

Figure 8-70. Sync Burst Transient



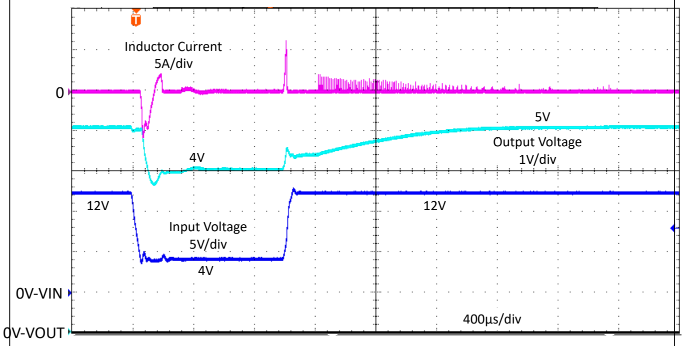
LM654A2 V_{IN} = 12V V_{OUT} = 3.3V
2100kHz

Figure 8-71. Current Limit



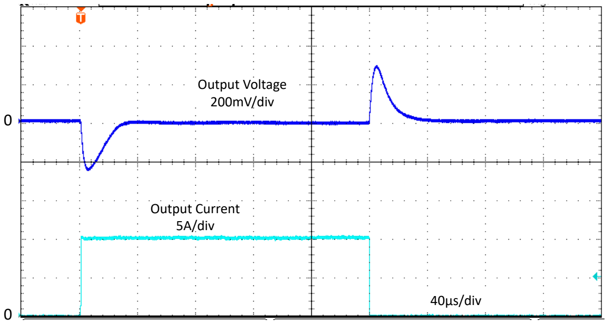
LM654A2 V_{IN} = 12V V_{OUT} = 3.3V
2100kHz

Figure 8-72. Short Circuit-Hiccup



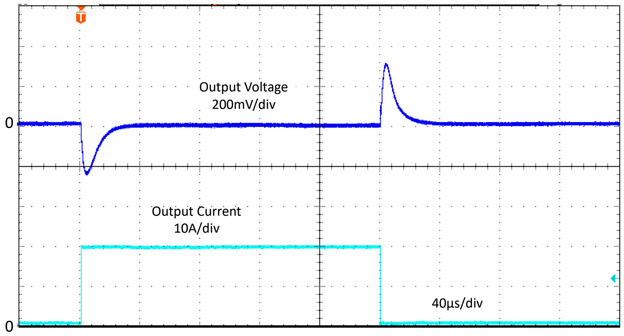
LM654A0 400kHz V_{OUT} = 5V
I_{OUT} = 0A

Figure 8-73. Drop Out Transient



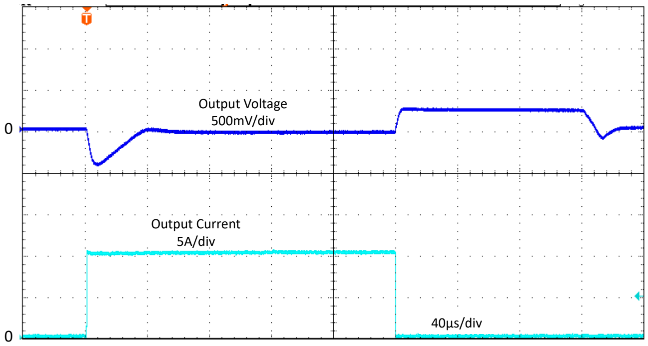
LM654A0 1000kHz V_{OUT} = 5V
FPWM 0A to 10A (1µs) V_{IN} = 24V

Figure 8-74. Load Transient - 1MHz



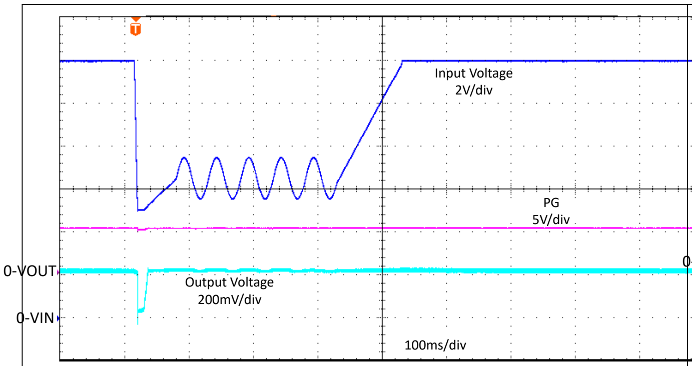
LM654B0 1000kHz V_{OUT} = 5V
FPWM 0A to 20A (1µs) V_{IN} = 24V

Figure 8-75. Load Transient - 1MHz



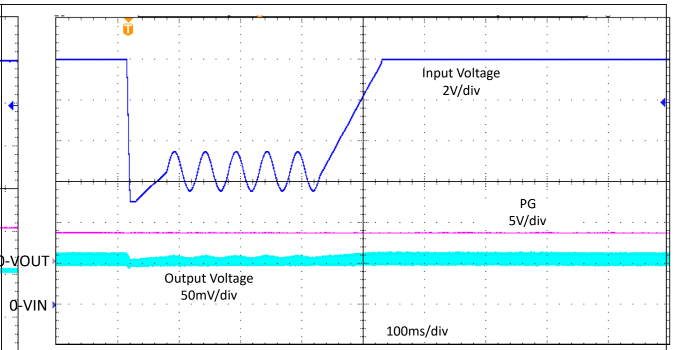
LM654A0 1000kHz V_{OUT} = 5V
AUTO 0A to 10A (1µs) V_{IN} = 24V

Figure 8-76. Load Transient - 1MHz



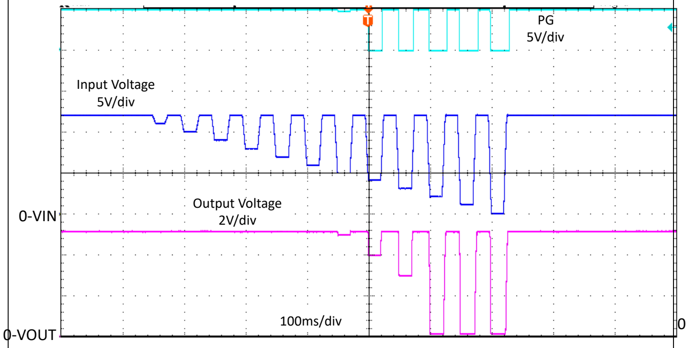
LM654A2 2100kHz V_{OUT} = 5V
FPWM I_{OUT} = 1A

Figure 8-77. Cold Crank Simulation



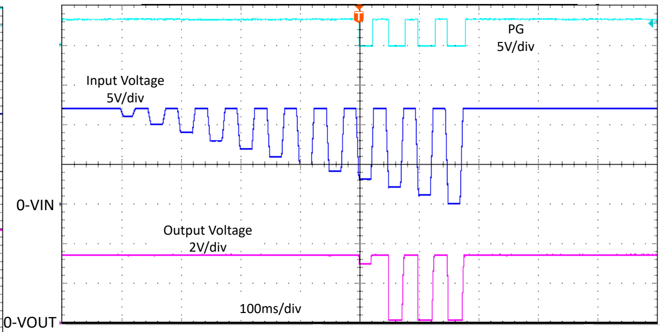
LM654A2 2100kHz V_{OUT} = 3.3V
FPWM I_{OUT} = 1A

Figure 8-78. Cold Crank Simulation



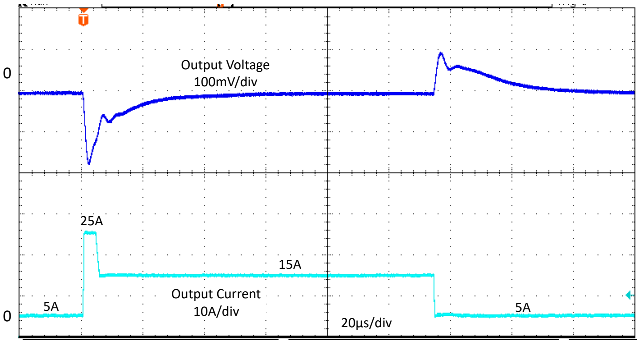
LM654A2 2100kHz V_{OUT} = 5V
FPWM I_{OUT} = 1A

Figure 8-79. Power Reset Simulation



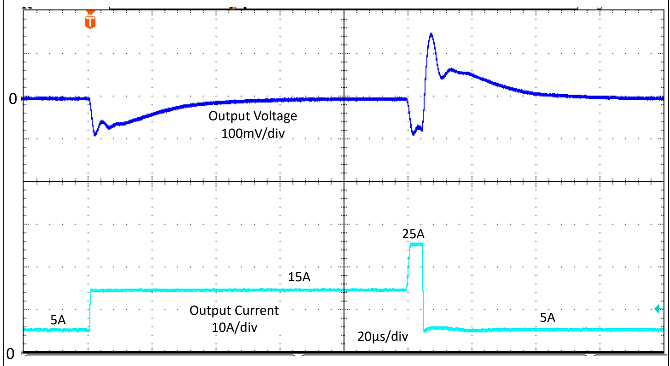
LM654A2 2100kHz V_{OUT} = 3.3V
I_{OUT} = 1A

Figure 8-80. Power Reset Simulation



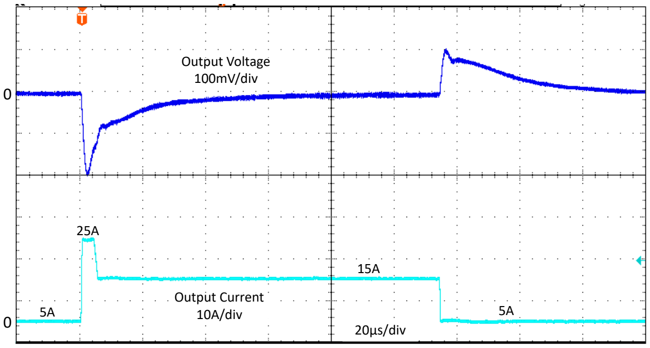
LM654B0 2100kHz V_{OUT} = 3.3V
See Figure 8-91 V_{IN} = 12V

Figure 8-81. Load Transient Profile #1



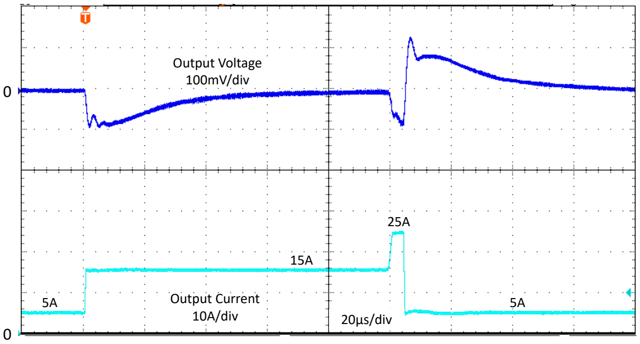
LM654B0 2100kHz V_{OUT} = 3.3V
See Figure 8-91 V_{IN} = 12V

Figure 8-82. Load Transient Profile #2



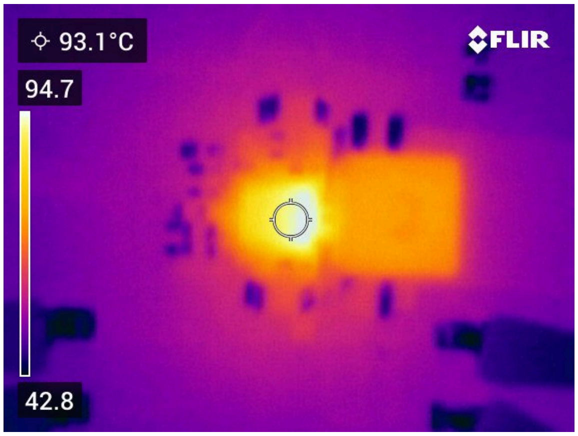
LM654B0 2100kHz V_{OUT} = 5V
See Figure 8-92 V_{IN} = 12V

Figure 8-83. Load Transient Profile #1



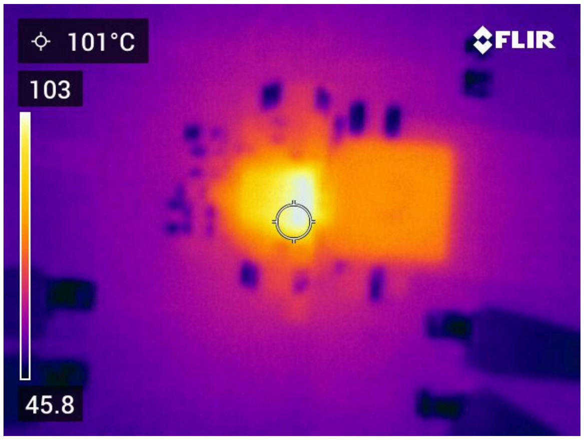
LM654B0 2100kHz V_{OUT} = 5V
See Figure 8-92 V_{IN} = 12V

Figure 8-84. Load Transient Profile #2



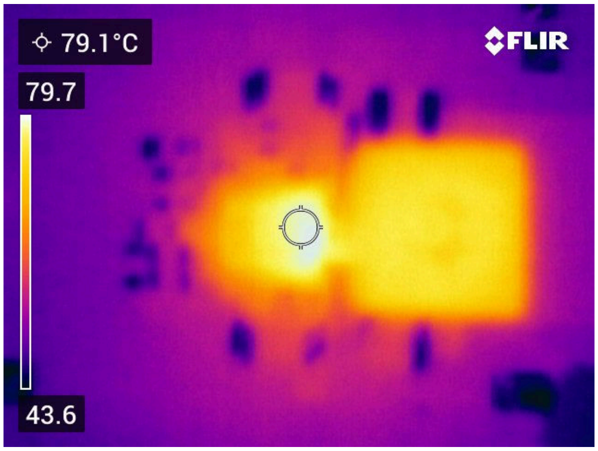
LM654B0 2100kHz V_{OUT} = 3.3V
Θ_{JA} = 16ºC/W 1.2µH, 3mΩ I_{OUT} = 15A

Figure 8-85. Thermal Image



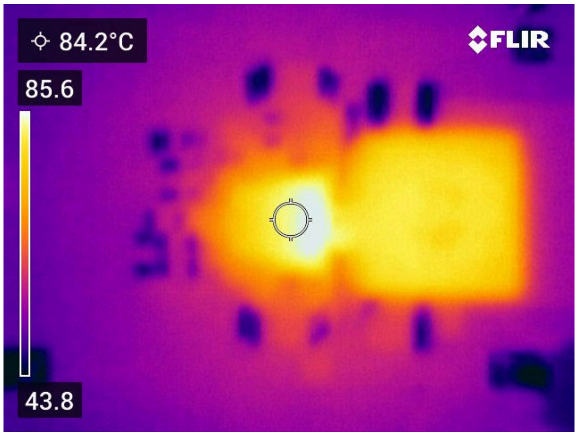
LM654B0 2100kHz V_{OUT} = 5V
Θ_{JA} = 16ºC/W 1.2µH, 3mΩ I_{OUT} = 15A

Figure 8-86. Thermal Image



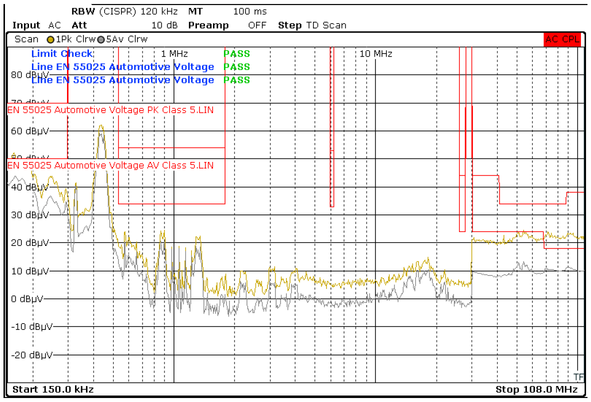
LM654B0 400kHz V_{OUT} = 3.3V
Θ_{JA} = 16ºC/W 1.2µH, 3mΩ I_{OUT} = 15A

Figure 8-87. Thermal Image



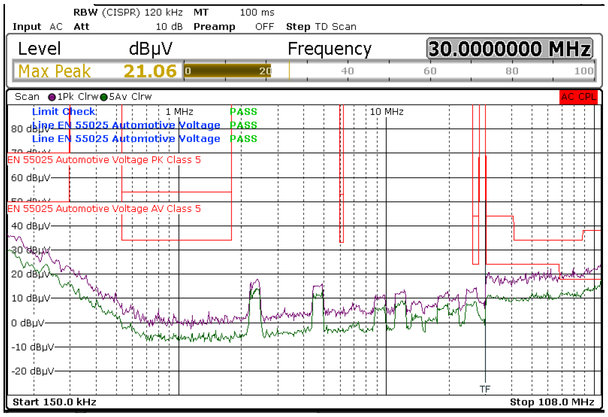
LM654B0 400kHz V_{OUT} = 5V
Θ_{JA} = 16ºC/W 1.2µH, 3mΩ I_{OUT} = 15A

Figure 8-88. Thermal Image



LM654B0 400kHz V_{OUT} = 5V
V_{IN} = 12V See Figure 8-93 I_{OUT} = 20A

Figure 8-89. CISPR25 CE Scan



LM654B0 2200kHz V_{OUT} = 3.3V
V_{IN} = 12V See Figure 8-93 I_{OUT} = 13A

Figure 8-90. CISPR25 CE Scan

Table 8-4. BOM for Typical Curve Data

DEVICE	FREQUENCY	INDUCTOR[1]	OUTPUT CAPACITANCE[2]	FB/COMP
LM654A0	2.2MHz	0.68µH, 2.3mΩ	59µF at 3.3V, 51µF at 5V	Fixed/Int.
LM654A0	400kHz	2.2µH, 4.8mΩ	215µF at 3.3V, 180µF at 5V	Fixed/Int.
LM654A2	2.2MHz	0.47µH, 1.8mΩ	63µF at 3.3V, 53µF at 5V	Fixed/Int.
LM654A2	400kHz	1.8µH, 4.3mΩ	63µF at 3.3V, 53µF at 5V	Fixed/Int.
LM654A5	2.2MHz	0.47µH, 1.8mΩ	63µF at 3.3V, 53µF at 5V	Fixed/Int.
LM654A5	400kHz	1.8µH, 4.3mΩ	63µF at 3.3V, 53µF at 5V	Fixed/Int.
LM654B0	2.2MHz	0.47µH, 1.8mΩ	140µF at 3.3V, 120µF at 5V	Fixed/Int.
LM654B0	400kHz	1.2µH, 3.4mΩ	280µF at 3.3V, 240µF at 5V	Fixed/Int.
LM654A0	1000kHz	1.2µH, 3.4mΩ	102µF at 3.3V, 85µF at 5V	Fixed/Int.
LM654B0	1000kHz	0.68µH, 2.3mΩ	140µF at 3.3V, 115µF at 5V	Fixed/Int.

(1) Applies to both 3.3V and 5V output
(2) Measured on EVM under indicated D.C. bias.

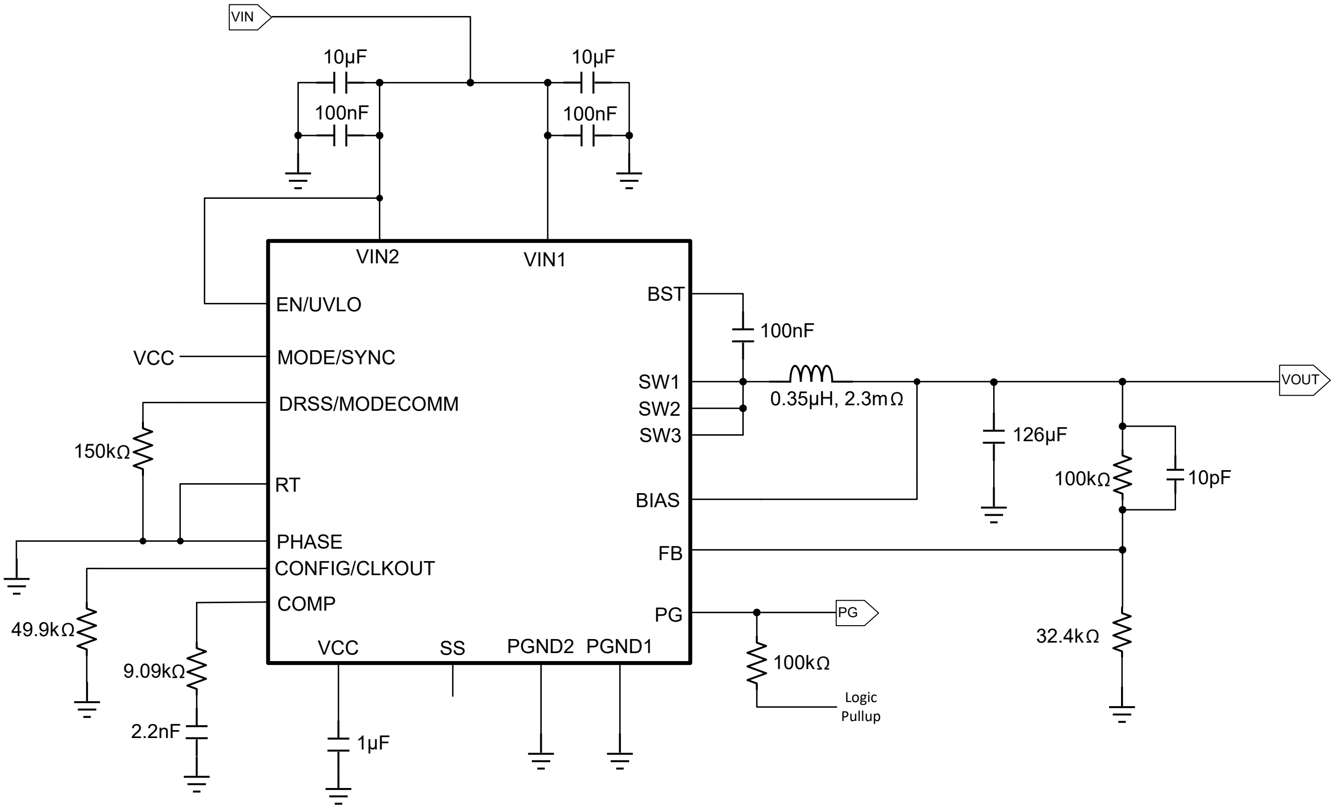


Figure 8-91. Schematic for 3.3V Special Load Profiles

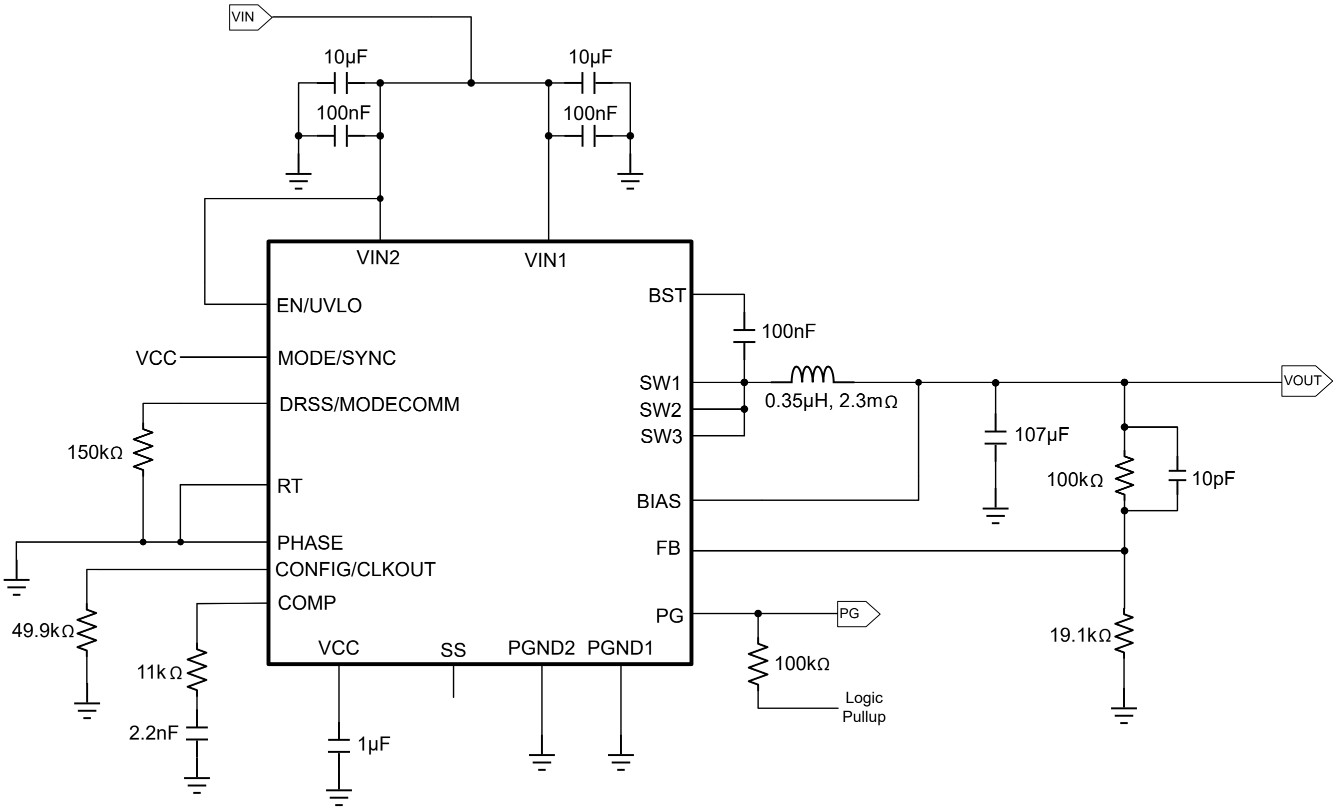


Figure 8-92. Schematic for 5V Special Load Profiles

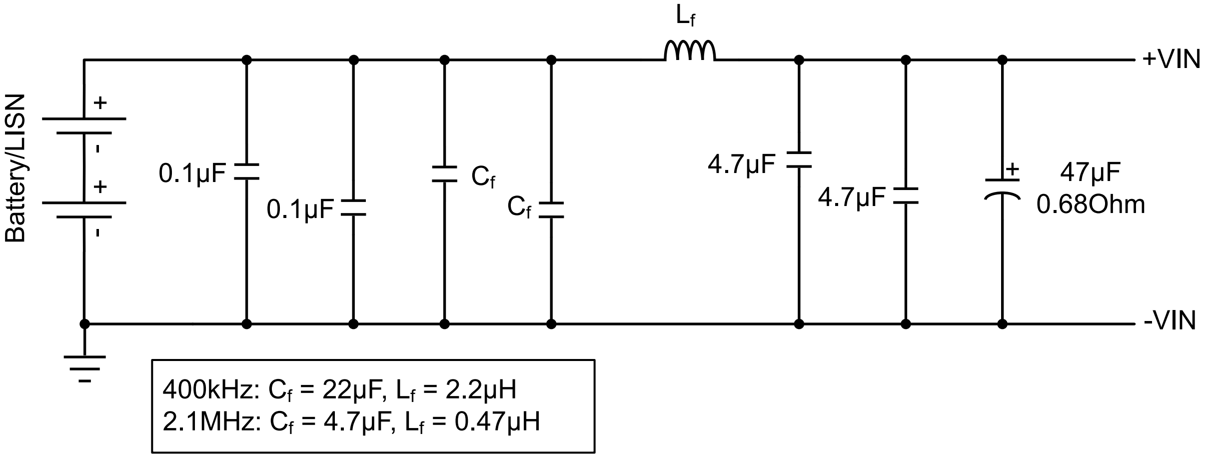


Figure 8-93. Typical EMI Filter Schematic

8.3 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 23.

$$I_{IN} \cong \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{23}$$

where

η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an under damped resonant circuit. This can result in over-voltage transients at the input to the regulator or outright oscillation of the power supply. This is especially true when an EMI input filter is used. Consider that the supply voltage can dip when a load transient is applied to the output depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients. The use of an electrolytic input capacitor is usually required when an input EMI filter is used.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). TI does not recommend to use a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output.

8.4 Layout

8.4.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most EMI-critical PCB feature is the loop formed by the input capacitor or capacitors and power ground. This action is shown in Figure 8-94. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. Excessive transient voltages can disrupt the proper operation of the converter. Because of this possible disruption, the traces in this loop must be wide and short while keeping the loop area as small as possible to reduce the parasitic inductance.

- *Place the input capacitor or capacitors as close as possible to the input pin pairs*: VIN1 to PGND1 and VIN2 to PGND2. Place the small capacitors closest. Each pair of pins are adjacent, simplifying the input capacitor placement. With this package, there are two VIN/PGND pairs on either side of the package. This provides a symmetrical layout and helps minimize switching noise and EMI generation. Use a wide VIN plane on a mid-layer to connect both of the VIN pairs together to the input supply. Route symmetrically from the supply to each VIN pin to best use the benefits of the symmetric layout. The 100nF high frequency input capacitors must be placed with 1mm of the VIN and PGND pins of the regulator. [1]
- *Place the bypass capacitor for VCC close to the VCC pin and PGND pin:* This capacitor must be routed with short, wide traces to the VCC and PGND pins.
- *Place the BST capacitor as close as possible to the device with short, wide traces to the BST and SW pins:*
- *Place the feedback divider as close as possible to the FB pin of the device*: Place R_{FBB}, R_{FBT}, C_{FF} if used, physically close to the device. The connections to FB and PGND through R_{FBB} must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Place the compensation components as close as possible to the COMP pin*: If external compensation components are used, the components must be placed as close to the COMP pin as possible. This action reduces the parasitic capacitance on the COMP pin and help prevent noise pick-up.
- *Layer 2 of the PCB must be a ground plane*: This plane acts as a noise shield and as a heat dissipation path. Using layer 2 reduces the inclosed area in the input circulating current in the input loop, reducing inductance.
- *Provide wide paths for V_{IN}, V_{OUT}, and PGND*: These paths must be as wide and direct as possible to reduce any voltage drops on the input or output paths of the converter to maximize efficiency.
- *Provide enough PCB area for proper heat sinking or use an external heat sink*: Enough copper area must be used to make sure of a low $R_{\theta JA}$, considering maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces can be used for all pins except where noise considerations dictate minimization of area. Consider the use of an external heat sink and the mounting requirements.
- *Use generous ground vias*: Multiple ground vias must be used (stitching). This action provides both a low impedance ground connection and low impedance heat path for the regulator. This is especially important around the input capacitor grounds. Thermal ground vias are also required under the DAP of the regulator, extending to both side of the PCB. Use the LM654B0EVM as an example. (Figure 8-95 is for illustrative purposes as regards the number and placement of ground vias)
- *Keep switch area small*: Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

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[1] Input capacitor placement outside of the recommended range can result in device performance degradation including, but not limited to, increased input voltage and switch-node ringing outside of the absolute maximum rating, and system instability.

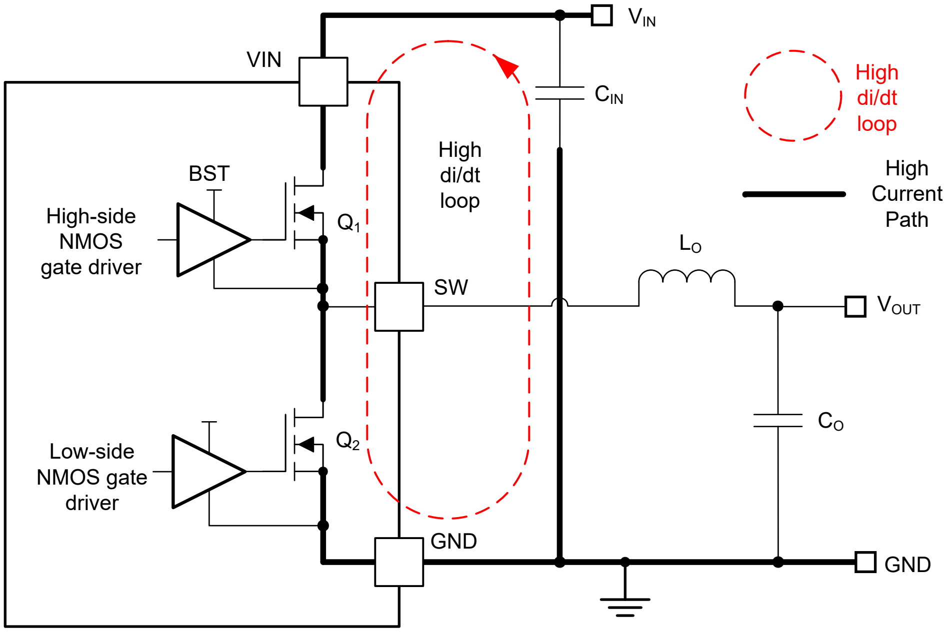

Figure 8-94. Input Current Loop

8.4.2 Layout Example

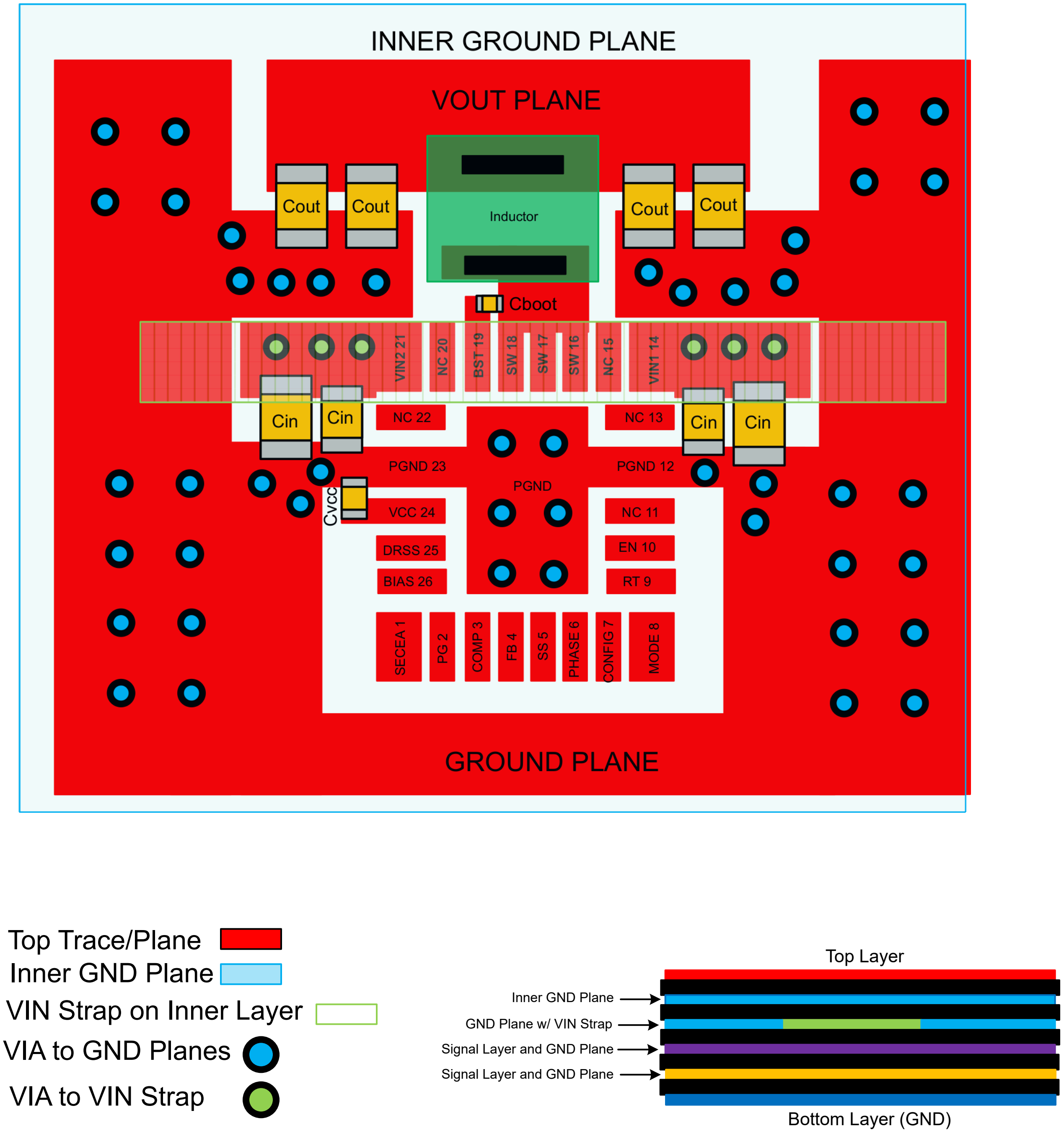

Figure 8-95. PCB Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight* application note
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- Texas Instruments, *How to Properly Evaluate Junction Temperature with Thermal Metrics* application note
- Texas Instruments, *PCB Thermal Design Tips for Automotive DC/DC Converters* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2025) to Revision A (June 2026)	Page
• First public release of the full datasheet.	1
• Changed the document status from Advance Information to Production Mix.	1
• Added MINT description to the document title, *Features* list, and *Description*	1
• Updated *Pin Configuration and Functions* to clarify PHASE pin behavior on primary to allow 0 degree and 180 degree phase shift on output clock.	4
• Added guidelines for high-frequency input capacitor bypass placement in *Pin Configuration and Functions*	4
• Added note on minimum input voltage.	7
• Updated EVM Theta JA to 16.	8
• Updated the Electrical Characteristics table to the production specifications.	8
• Deleted max limit for ton-minimum, not tested in production.	8
• Added the *Typical Characteristics*	12
• Added tables for easier Rt selection in *Adjustable Switching Frequency and Phase Shift*	19
• Changed triangular frequency spread from 17.5% to 17% for DRSS pin short to VCC condition in *Dual Random Spread Spectrum (DRSS)*	20
• Added equation for soft-start capacitor selection in *Soft Start and Recovery From Dropout*	21
• Added additional typical application schematics in *Typical Application*	28
• Added minimum inductance equation for different current limits in *Inductor Selection*	34
• Added typical performance curves.	41

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM654B0VDARQ1	Active	Production	WQFN-FCRLF (VDA) | 26	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	MT654B0Q
PLM654B0VDARQ1	Active	Preproduction	WQFN-FCRLF (VDA) | 26	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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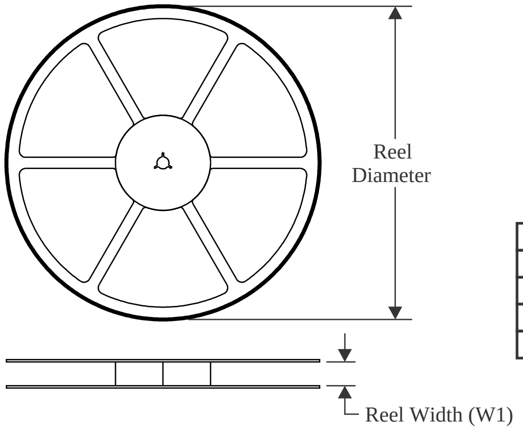
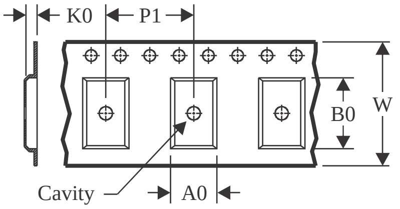
TAPE AND REEL INFORMATION

REEL DIMENSIONS

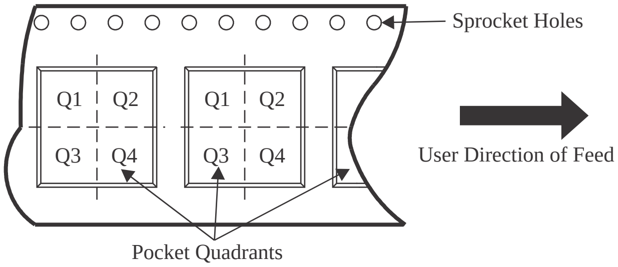


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

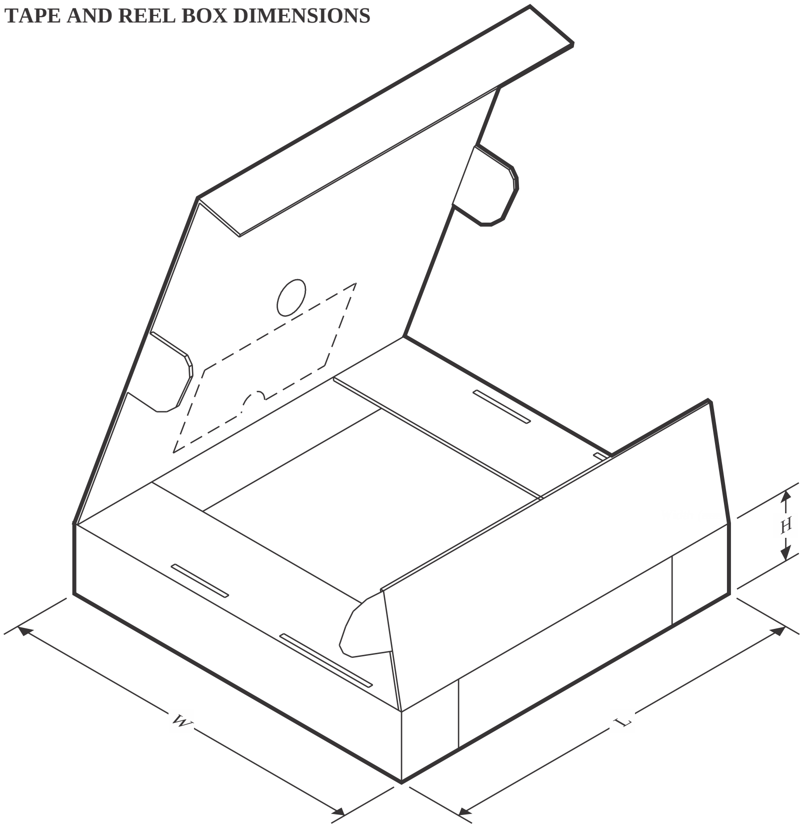
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM654B0VDARQ1	WQFN-FCRLF	VDA	26	3000	330.0	12.4	4.8	4.8	1.4	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

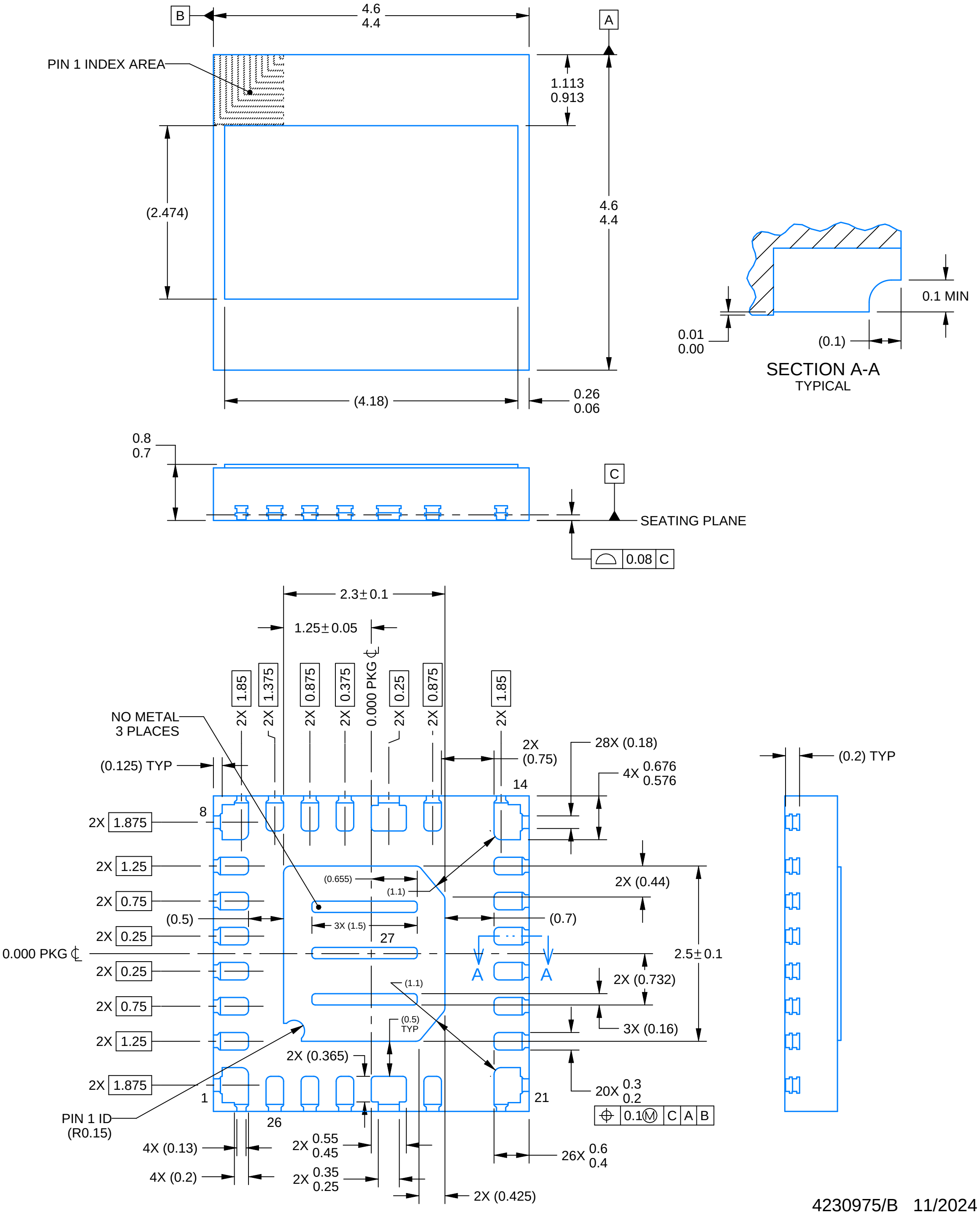
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM654B0VDARQ1	WQFN-FCRLF	VDA	26	3000	346.0	346.0	33.0

PACKAGE OUTLINE

VDA0026A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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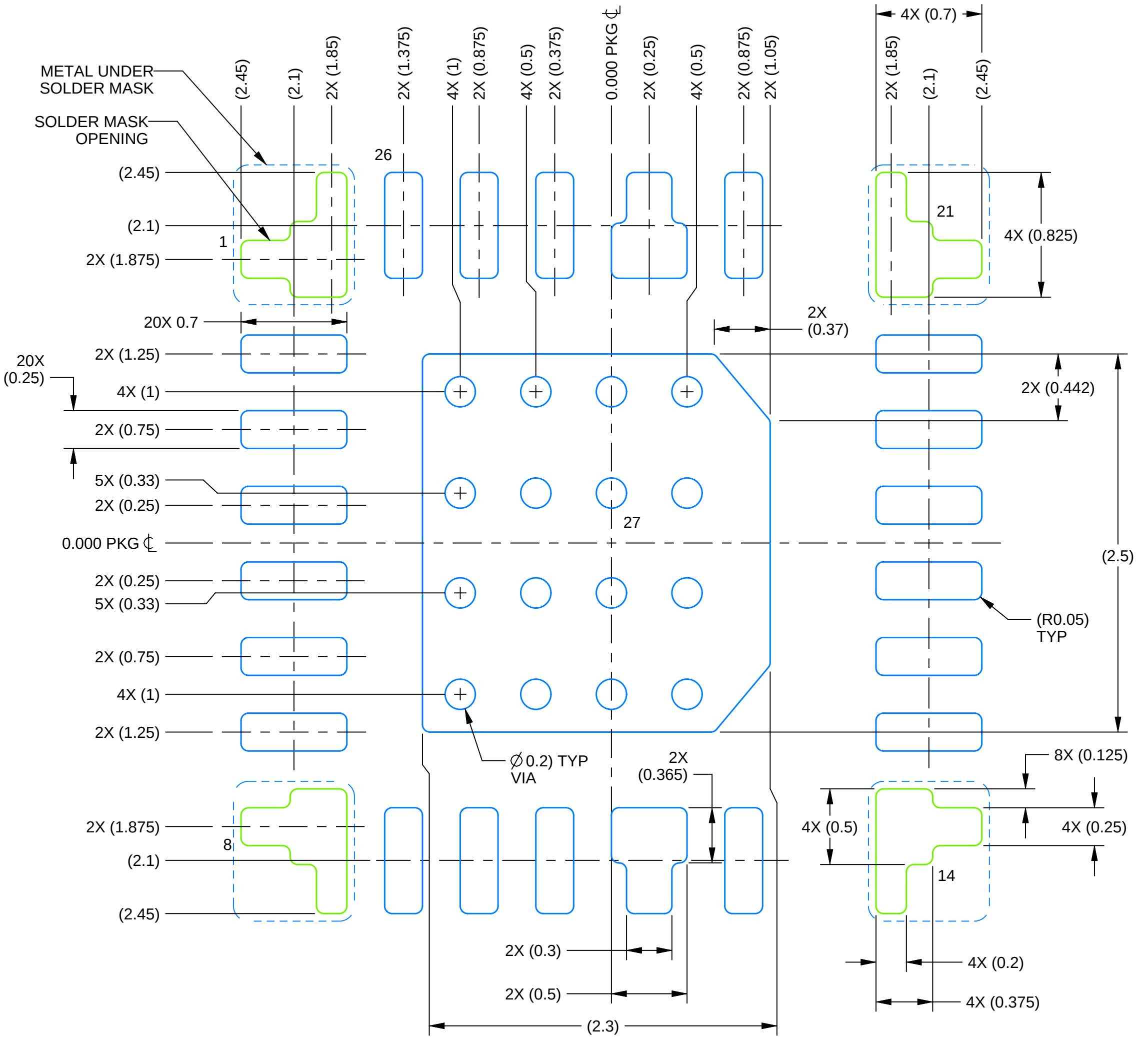
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

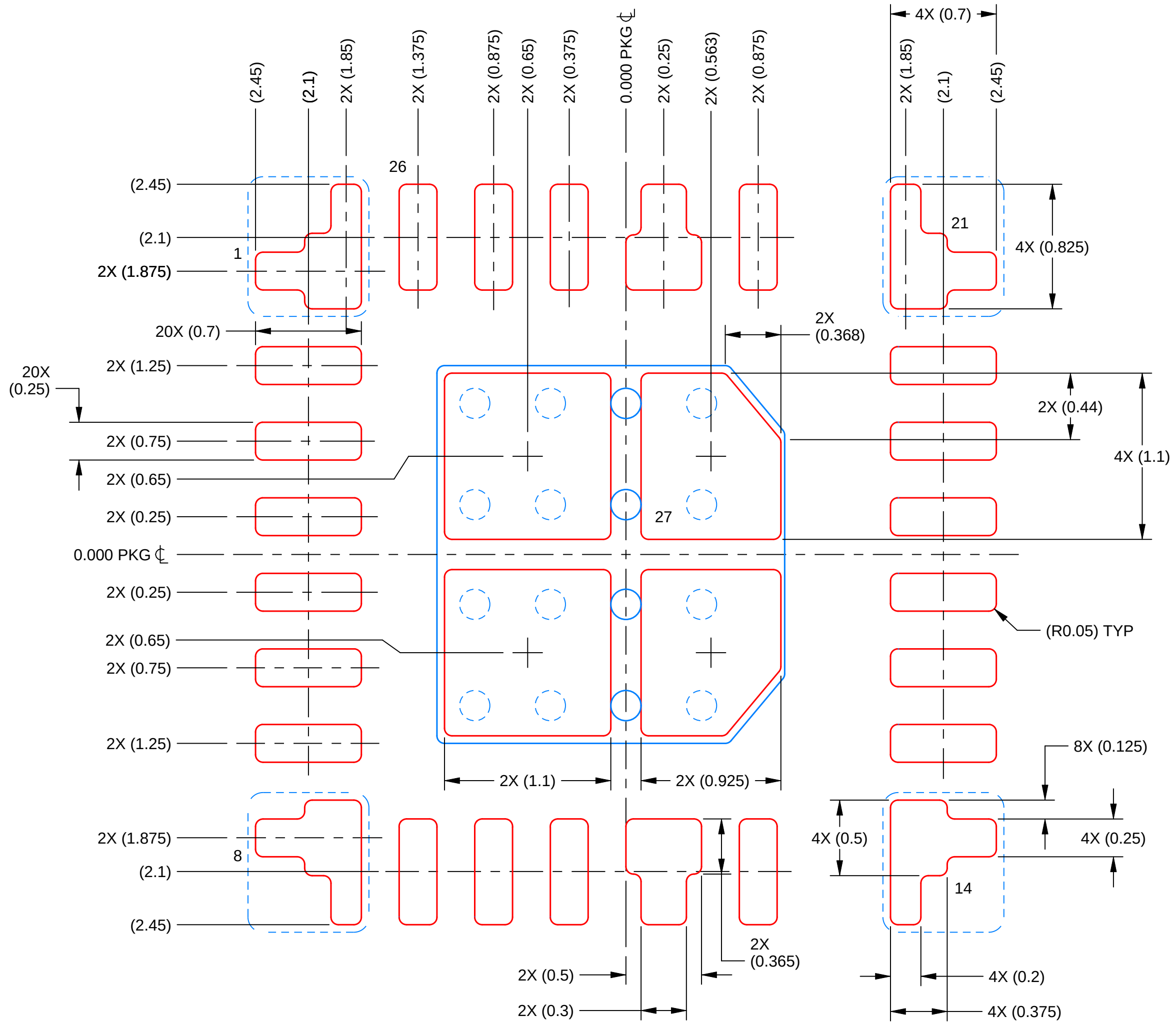
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 27: 84%

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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