LM656x0-Q1 70V, 8A/6A/4A, Automotive Buck Converters Optimized for Low EMI and High Power Density

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Wide input voltage range: 3V to 70V
- 1% accurate, V_{OUT} from 0.8V to 60V
- Optimized for low EMI requirements
  - Facilitates CISPR 25 Class 5 compliance
  - Pin-configurable dual-random spread spectrum and slew-rate control reduce peak emissions
  - Enhanced HotRod™ QFN package with symmetrical pinout
  - Switching frequency from 300kHz to 2.2MHz
  - Pin-configurable AUTO or FPWM operation
- Low minimum on time: 36ns (typical)
  - Enables 36V to 3.3V conversion at 2.1MHz
- High-efficiency power conversion
  - > 95% peak efficiency, $12V_{IN}$ to $5V_{OUT}$, 400kHz
  - No-load input current: 2.1µA
- High power density
  - Internal compensation, OCP, and TSD
  - 4.5mm × 4.5mm eQFN-26 with wettable flanks
  - Θ_{JA} = 18°C/W (LM65680-Q1EVM)
- VIN to PGND pin clearance: 1.1mm

2 Applications

- Advanced Driver Assistance Systems (ADAS)
- Automotive infotainment and cluster
- Hybrid, electric, and powertrain systems

3 Description

The LM656x0-Q1 are a family of stackable, automotive buck converters designed for high efficiency, high power density, and ultra-low electromagnetic interference (EMI). The converters operate over a wide input voltage range of 3V to 70V simplifying input surge protection design.

The low EMI operation is enabled with minimized loop inductance, pin-selectable SW node slew-rate control and dual-random spread spectrum (DRSS). The DRSS significantly reduces peak emissions through a combination of triangular and pseudo-random modulation while keeping output voltage ripple very low.

The current-mode control architecture with 36ns minimum on-time allows high conversion ratios at high frequencies, easy loop compensation, fast transient response, and excellent load and line regulation. Up to two converters can be set up in an interleaved mode (paralleled outputs) with accurate current sharing for supporting output current up to 16A.

Device Information

PART NUMBER(2)	PACKAGE(1)	OUTPUT CURRENT
LM65680-Q1	RZY (WQFN-FCRLF, 26)	8A
LM65660-Q1 (3)		6A
LM65640-Q1 (3)		4A

(1) For more information, see Section 11.
(2) See the *Device Comparison Table*.
(3) Preview information (not Advance Information).

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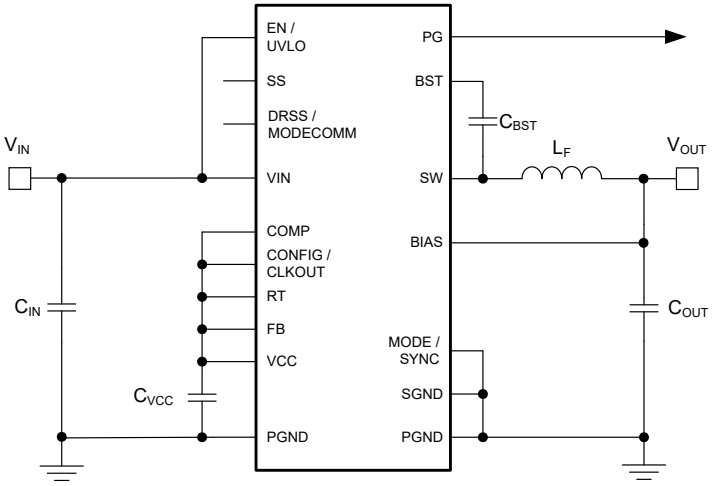
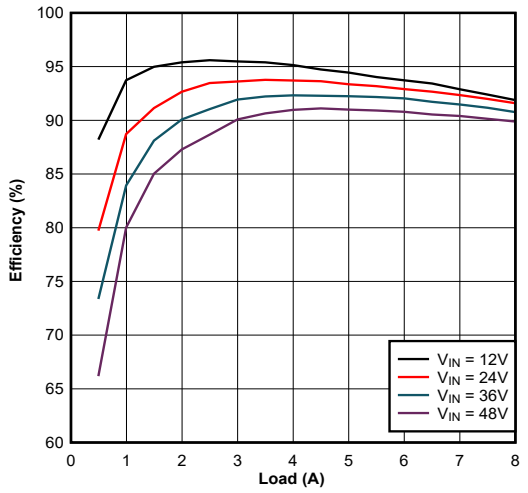


Typical Application Circuit



Typical Efficiency V_{OUT} = 5V, f_{SW} = 400kHz

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4 Device Comparison Table

Orderable Part Number	Input Voltage Rating	Current	Functional Safety	Level-Shifters for Inverting Buck-Boost Topology
LM65680RZYRQ1	70V	8A	Capable	No
LM65660RZYRQ1(1)	70V	6A	Capable	No
LM65640RZYRQ1(1)	70V	4A	Capable	No
LM68680FRZYRQ1(1)	70V	8A	Compliant	No
LM68660FRZYRQ1(1)	70V	6A	Compliant	No
LM68640FRZYRQ1(1)	70V	4A	Compliant	No
LM68580FRZYRQ1(1)	42V	8A	Compliant	No
LM68560FRZYRQ1(1)	42V	6A	Compliant	No
LM67680RZYRQ1(1)	70V	8A	Capable	Yes
LM67660RZYRQ1(1)	70V	6A	Capable	Yes
LM67640RZYRQ1(1)	70V	4A	Capable	Yes

(1) Preview information (not Advance Information). For more information, please contact Texas Instruments.

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5 Pin Configuration and Functions

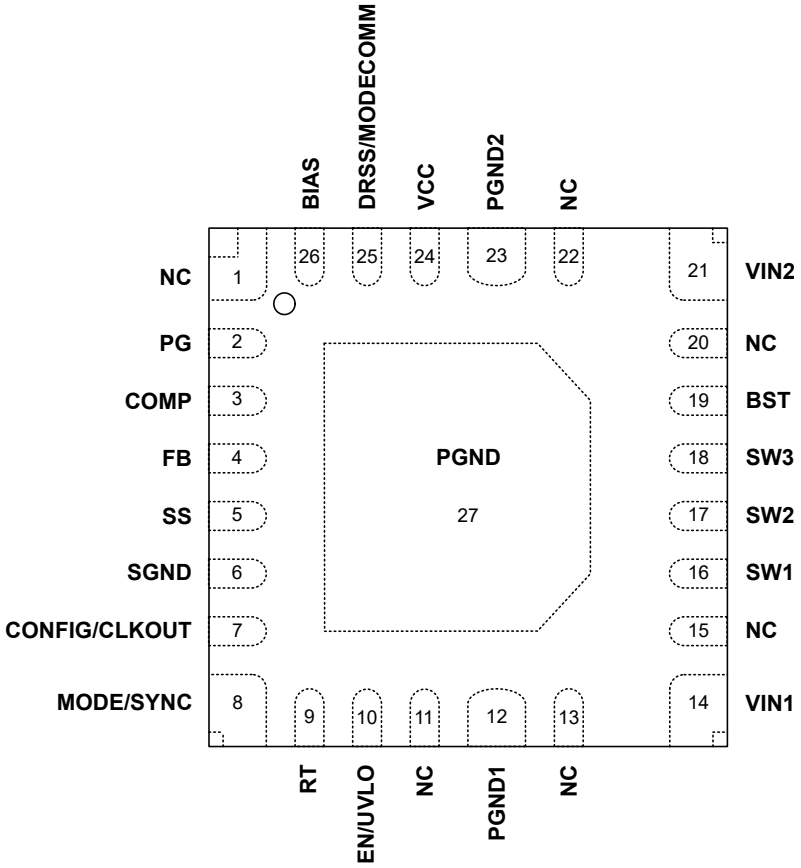

Figure 5-1. RZY 26-Pin WQFN-FCRLF Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	1	A	No connect pin. Leave floating.
PG	2	O	Power-Good output pin. This pin is an open-collector output that goes low if the output voltage is outside of the specified regulation window.
COMP	3	A	External compensation pin. This pin is the output of the transconductance amplifier. If used, connect a compensation network from the COMP pin to PGND. If unused, the pin must be tied to VCC.
FB	4	A	Feedback pin. Connect to GND to configure 3.3V fixed output voltage. Connect to VCC to configure 5V fixed output voltage. Connect this pin to a feedback divider tap point for adjustable output options. The regulation threshold is 0.8V.
SS	5	A	Soft-start delay programming pin. If the SS pin is left open, the internal soft-start circuit ramps the FB reference from zero to full value in 5.3ms. If a capacitor is connected from the SS pin to PGND, the soft-start time can be set to a higher value.
SGND	6	G	Sense GND pin. Connect to the system ground.
CONFIG / CLKOUT	7	I/O	Configuration pin. This pin configures the device as a primary (1-phase or 2-phase operation) or a secondary (2-phase operation) and selects internal (1-phase operation) or external compensation (1-phase or 2-phase operation). If configured as a primary for 2-phase operation, the pin becomes a CLKOUT pin after start-up.
MODE / SYNC	8	I/O	Mode and synchronization input pin. Tie this pin to PGND or drive the pin low to operate in AUTO mode. Tie this pin to VCC or drive the pin high, or send a synchronization clock signal to operate in FPWM mode. When synchronized to an external clock, use the RT pin to set the internal frequency close to the synchronized frequency to avoid disturbances if the external clock is turned on and off.

Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RT	9	I/O	Switching frequency programming pin. Connect this pin to PGND through a resistor with a value between 6.81kΩ and 54.2kΩ to set the switching frequency between 300kHz and 2200kHz. Connect to VCC for 400kHz operation. Connect to PGND for 2.2MHz operation. Do not float.
EN / UVLO	10	P	Precision enable pin. Drive this pin high / low to enable / disable the device. This pin can be directly connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Do not float.
NC	11	O	No connect pin. Leave floating.
PGND1	12	G	Power ground to the internal low-side MOSFET. Connect this pin to the system ground. Low-impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
NC	13	—	No connect pin. Leave floating to maintain 1mm clearance between PGND1 and VIN1 pins. This pin be shorted to PGND1 provided the 0.75mm clearance between PGND1 and VIN1 pins meets system pin clearance requirements.
VIN1	14	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Provide a low-impedance connection to VIN2.
NC	15	—	No connect pin. Leave floating to maintain 0.5mm clearance between VIN1 and SW1.
SW1	16	P	Device switch pins and the switch node of the regulator. Connect to the output inductor.
SW2	17	P	
SW3	18	P	
BST	19	P	High-side driver upper supply rail. Connect a 100nF capacitor between the SW node and BST. An internal diode charges the capacitor while SW node is low.
NC	20	—	No connect pin. Leave floating to maintain 0.5mm clearance between VIN2 and BST.
VIN2	21	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Provide a low-impedance connection to VIN1.
NC	22	—	No connect pin. Leave floating to maintain 1mm clearance between PGND2 and VIN2 pins. This pin be shorted to PGND2 provided the 0.75mm clearance between PGND2 and VIN2 pins meets system pin clearance requirements.
PGND2	23	G	Power ground to internal low-side MOSFET. Connect to system ground. Low-impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VCC	24	P	Internal regulator output. Used as supply to internal control circuits. Do not connect this pin to any external loads. Connect a high-quality 1µF capacitor from this pin to PGND.
DRSS / MODECOMM	25	I/O	Dual Random Spread-Spectrum (DRSS) select pin. See Dual Random Spread Spectrum (DRSS) for available DRSS options. If configured for 2-phase operation, this pin becomes a mode communication pin between a primary and a secondary device. For 2-phase operation, tie together the MODECOMM pins of the primary and secondary devices.
BIAS	26	P	Input to internal voltage regulator. If configured for fixed VOUT, connect the pin to the VOUT node to close the control loop. If configured for an adjustable VOUT, connect the pin to the VOUT node or an external bias supply from 3.3V to 30V. If output voltage is above 30V and no external supply is used, tie the pin to GND.
PGND	27	G	Exposed PGND pad. Connect to system GND on a PCB. This pin is a major heat dissipation path for the die. The pad must be used for heat sinking by soldering to a large copper area on a PCB. Implementing as many thermal vias as suggested in the example board layout makes sure of lowest package thermal resistance and best possible thermal performance.

(1) I = input, O = output, A = analog, G = ground, P = power

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	75	V
Input voltage	EN/UVLO TO PGND	–0.3	75	V
Input voltage	RT to PGND	–0.3	75	V
Input voltage	DRSS/MODECOMM to PGND	–0.3	40	V
Input voltage	BIAS TO PGND	–0.3	40	V
Input voltage	MODE/SYNC to PGND	–0.3	5.5	V
Input voltage	CONFIG/CLKOUT to PGND	–0.3	5.5	V
Input voltage	COMP, FB to PGND	–0.3	5.5	V
Input voltage	SS to PGND	–0.3	V_{CC} + 0.3	V
Output voltage	SW to PGND	–0.6	V_{IN} + 0.3	V
Output voltage	PG to PGND	–0.3	40	V
Output voltage	BST to SW	–0.3	5.5	V
Output voltage	VCC to PGND	–0.3	5.5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN (DC)	3	65	V
Input voltage	VIN (Transient)(1)	3	70	V
Input voltage	EN (DC)	0	65	V
Input voltage	EN (Transient)(1)	0	70	V
Input voltage	BIAS, PG	0	30	V
Input voltage	FB	0	5.5	V
Input voltage	MODE/SYNC, RT	0	5.5	V
Pullup resistance	$R_{PU(PG)}$	4		kΩ
Pullup reference voltage	$V_{PU(PG)}$	0.8	30	V
Output voltage	VOUT	0.8		V
Output current	IOUT, 8A option	0	8	A
Output current	IOUT, 6A option	0	6	A
Output current	IOUT, 4A option	0	4	A

(1) Operation at the maximum transient voltage is limited to < 1% of device operating lifetime.

6.4 Thermal Information

THERMAL METRIC[1]		DEVICE		UNIT
		eQFN (JESD 51-7)	eQFN (EVM)	
		26 PINS	26 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.7[2]	18[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	[4]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	[4]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.9	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. It was calculated in accordance with JESD 51-7, simulated with a 4-layer JEDEC board, and does do not represent the performance obtained in an actual application. For thermal design information please see the *Maximum Ambient Temperature* section.
(3) Refer to the LM65680-Q1EVM user's guide for board layout and additional information. For thermal design information please see the *Maximum Ambient Temperature* section.
(4) Not applicable to an EVM.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2.2MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN PIN)						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising (Needed to start up)	3.3	3.4	3.45	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling (Once operating)		2.5	2.55	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.9		V
I_{VIN}	VIN pin input current, internal COMP, no switching	V_{BIAS} = 3.3V + 2%, CONFIG short to V_{CC},		0.9	1.4	µA
$I_{BIAS(FIX-3.3V)}$	BIAS pin input current, fixed 3.3V output, internal COMP, no switching	V_{BIAS} = 3.3 V + 2%, CONFIG short to V_{CC}, Auto Mode enabled		8.4	10	µA
$I_{Q(FIX-3.3V)}$	Total V_{IN} quiescent current, fixed 3.3V output, internal COMP, no switching	V_{IN} = 24V, V_{BIAS} = 3.3V + 2%, CONFIG short to V_{CC}, T_J = 25°C, auto mode enabled		2.1	2.7	µA
		All temperatures		2.1	6.4	µA
$I_{BIAS(ADJ-3.3V)}$	BIAS pin input current, adjustable 3.3V output, internal COMP, no switching	V_{FB} = 0.8V + 2%, CONFIG short to V_{CC}, auto mode enabled		6.8	8.1	µA
$I_{Q(ADJ-3.3V)}$	Total V_{IN} quiescent current, adjustable 3.3V output, internal COMP, no switching	V_{IN} = 24.0V, V_{FB} = 0.8V + 2%, CONFIG short to V_{CC}, auto mode enabled		1.9	2.5	µA
$I_{BIAS(ADJ-3.3V-EXT)}$	BIAS pin input current, adjustable 3.3V output, external COMP, no switching	V_{FB} = 0.8V + 2%, R_{CFG} = 49.9kΩ, auto mode enabled		37	44	µA
$I_{Q(ADJ-3.3V-EXT)}$	Total V_{IN} quiescent current, adjustable 3.3V output, external COMP, no switching	V_{IN} = 24.0V, V_{FB}=0.8V + 2%, R_{CFG} = 49.9kΩ, auto mode enabled		6	7.4	µA
I_{Q-SD}	V_{IN} Shutdown supply current	V_{EN} = 0V, T_J = 25°C		1.3	1.6	µA
ENABLE (EN PIN)						
$V_{EN-TH(R)}$	Enable voltage rising threshold	V_{EN} rising	1.15	1.25	1.35	V
$V_{EN-TH(F)}$	Enable input low threshold	V_{EN} falling	0.9	1	1.1	V
V_{EN-HYS}	Enable voltage hysteresis			250		mV
I_{EN-LKG}	Enable input leakage current	V_{EN} = V_{IN}		0.22	3.45	µA
INTERNAL LDO (VCC PIN)						
V_{VCC}	Internal LDO output voltage	3.4V ≤ V_{IN} ≤ 65V, V_{BIAS} = 0V		3.3		V
		3.4V ≤ V_{BIAS} ≤ 30V		3.2		V
$V_{VCC-UVLO(R)}$	VCC UVLO rising threshold	VCC undervoltage rising threshold, I_{VCC} = 0A	3.3	3.4	3.5	V
$V_{VCC-UVLO(H)}$	VCC UVLO hysteresis			0.9		V
VOLTAGE REFERENCE (FB PIN)						

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6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2.2MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB1}	Internal feedback reference voltage, internal compensation	FPWM Mode, CONFIG shorted to V_{CC}	0.792	0.8	0.808	V
V_{FB2}	Internal feedback reference voltage, external compensation	FPWM Mode, R_{CONFIG} = 49.9kΩ	0.792	0.8	0.808	V
I_{FB-LKG}	Feedback pin input leakage current	V_{FB} = 0.8V, adjustable V_{OUT} setting		0.025	90	nA
$R_{FB-SEL-ADJ}$	Adjustable output voltage setting resistance (thevenin equivalent)	Resistor ladder between V_{OUT} and GND, center tap connected to FB	4		100	kΩ
FIXED OUTPUT VOLTAGE (BIAS PIN)						
$V_{OUT1(3.3V)}$	3.3V fixed output voltage, internal COMP	FB shorted to GND, CONFIG shorted to V_{CC}	3.267	3.3	3.333	V
$V_{OUT2(3.3V)}$	3.3V fixed output voltage, external COMP	FB shorted to GND, R_{CONFIG} = 49.9kΩ	3.267	3.3	3.333	V
$V_{OUT1(5V)}$	5.0V fixed output voltage, internal COMP	FB shorted to V_{CC}, CONFIG shorted to V_{CC}	4.95	5	5.05	V
$V_{OUT2(5V)}$	5.0V fixed output voltage, external COMP	FB shorted to V_{CC}, R_{CONFIG} = 49.9kΩ	4.95	5	5.05	V
STARTUP (SS PIN)						
t_{EN_HIGH}	Enable HIGH to start of switching delay	V_{FB} = V_{RT} = V_{MODE} = GND, V_{BIAS} = V_{OUT}		2.5		ms
t_{SS}	Internal fixed soft-start time	Time from first SW pulse to V_{REF} at 90% of set point	2.9	5.3	8.1	ms
I_{SS}	Soft-start charge current	V_{SS} = 0V		20		µA
R_{SS}	Soft-start discharge resistor	EN = 0V		7		Ω
$V_{SS(TH)}$	Soft-start multiphase comparator threshold	R_{CONFIG} = 49.9kΩ		60		mV
ERROR AMPLIFIER (COMP PIN)						
$g_{m(EXTERNAL)}$	EA transconductance – external COMP	V_{COMP} = 0.8V, V_{FB} = +5% & V_{FB} = –5%		1		mS
$V_{COMP-EXT(h-clamp)}$	External COMP- high clamp voltage	V_{FB} = 0V, adjustable V_{OUT} setting		1.056		V
CURRENT LIMITS AND HICCUP						
I_{HS-LIM}	High-side peak current limit, 8A option	Duty-cycle approaches 0%.	10.7	12.5	13.7	A
I_{LS-LIM}	Low-side valley current limit, 8A option		8.8	9.9	10.7	A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty-cycle, 8A option	V_{VCC} = 3.3V, tpulse ≤ 100ns, auto mode	2.4	3	3.7	A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty-cycle, 8A option	V_{VCC} = 3.3V, t_{pulse} ≥ 1µs, auto mode		1.1		A
I_{HS-LIM}	High-side peak current limit, 6A option	Duty-cycle approaches 0%.	8.2	9.5	10.6	A
I_{LS-LIM}	Low-side valley current limit, 6A option		6.6	7.4	8	A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty-cycle, 6A option	V_{VCC} = 3.3V, tpulse ≤ 100ns, auto mode	1.8	2.3	2.7	A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty-cycle, 6A option	V_{VCC} = 3.3V, tpulse ≥ 1µs, auto mode		0.95		A
I_{HS-LIM}	High-side peak current limit, 4A option	Duty-cycle approaches 0%.	6.1	7	7.8	A
I_{LS-LIM}	Low-side valley current limit, 4A option		4.8	5.4	5.8	A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty-cycle, 4A option	V_{VCC} = 3.3V, tpulse ≤ 100ns, auto mode	1.3	1.8	2.1	A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty-cycle, 4A option	V_{VCC} = 3.3V, tpulse ≥ 1µs, auto mode		0.65		A
$I_{LS-NEG-LIM}$	Low-side negative current limit	Sinking current limit, FPWM mode	–9.6	–6.9	–4.9	A
$I_{L-ZC-LIM}$	Zero-cross current limit	V_{VCC} = 3.3V, auto mode		100		mA
V_{HIC}	Overcurrent hiccup threshold on FB pin	Low-side FET ON-time > 165ns, after soft start		0.32		V
t_{HIC_DLY}	Hiccup mode activation delay			64		cycles
t_{HIC}	Hiccup mode duration time			40		ms
POWER GOOD MONITOR (PG PIN)						
$V_{PG-OVP(R)}$	PG overvoltage rising threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	103	105	107	%

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6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2.2MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PG-OVP(F)}$	PG overvoltage falling threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	102	104	106	%
$V_{PG-UVP(R)}$	PG undervoltage rising threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	94	96	98	%
$V_{PG-UVP(F)}$	PG undervoltage falling threshold	% of FB voltage (Adj) or BIAS voltage (Fixed)	93	95	97	%
$t_{PG-DEGLITCH(F)}$	Deglitch filter delay on PG falling edge		55	114	175	µs
$t_{PG-DEGLITCH(R)}$	Deglitch filter delay on PG rising edge		1.2	2	3	ms
$V_{IN(PG-VALID)}$	Minimum V_{IN} for valid PG output	$V_{OL(PG)}$ < 0.4V, R_{PU} = 50kΩ, V_{PU} = 5V			1.25	V
$V_{OL(PG)}$	Output low voltage	I_{OL} = 1mA, V_{IN} = 1.25V			0.4	V
$R_{ON(PG)}$	PG FET ON resistance	I_{PG} = 1mA		39	110	Ω
SWITCHING FREQUENCY (RT PIN)						
$f_{SW1(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = GND	1.98	2.2	2.42	MHz
$f_{SW2(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = 15.8kΩ, 1%	900	1000	1100	kHz
$f_{SW3(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = VCC	360	400	440	kHz
SYNCHRONIZATION (MODE/SYNC PIN)						
$V_{IH(SYNC)}$	SYNC input high level threshold				1.3	V
$V_{IL(SYNC)}$	SYNC input low level threshold		0.45			V
$V_{OH(CLKOUT)}$	CLKOUT output high level threshold	I_{OH} = -2mA	2.4			V
$V_{OL(CLKOUT)}$	CLKOUT output low level threshold	I_{OL} = 2mA			0.4	V
$f_{SYNC-RANGE(FPWM)}$	Synchronization frequency range for set 2.2MHz f_{SW}	R_{RT} = 6.81kΩ, 1%	1.76		2.64	MHz
$f_{SYNC-RANGE(FPWM)}$	Synchronization frequency range for set 300kHz f_{SW}	R_{RT} = 54.2kΩ, 1%	240		360	kHz
$t_{SYNC(TON-MIN)}$	Minimum positive pulse width of external sync signal				80	ns
$t_{SYNC(TOFF-MIN)}$	Minimum negative pulse width of external sync signal				80	ns
$t_{SYNC-SW-DLY}$	SYNC to SW delay time		–22		22	ns
DUAL RANDOM SPREAD SPECTRUM						
Δf_{SS-LF}	Low-frequency triangular spread spectrum modulation range	DRSS pin floating		17		%
f_{m-LF}	Triangular modulation frequency	DRSS pin floating	3.6	6	8.4	kHz
Δf_{SS-HF}	High-frequency pseudo-random spread spectrum modulation range	DRSS pin floating		2		%
POWER STAGE						
$R_{DS-ON-HS}$	High-side FET ON resistance	I_{SW} = 500mA, $V_{BOOT-SW}$ = 3.3V		42		mΩ
$R_{DS-ON-LS}$	Low-side FET ON resistance			23		mΩ
$t_{ON-MIN(FPWM)}$	Minimum on-time(1)	FPWM: I_{OUT} = 0A, R_{RT} = 6.81kΩ		36	48	ns
$t_{ON-MIN(AUTO)}$	Minimum on-time(1)	AUTO: I_{OUT} = 2A, R_{RT} = 6.81kΩ		36	48	ns
$t_{OFF-MIN}$	Minimum off-time	V_{IN} = 4V, Fsw = 2.2MHz, R_{RT} = 6.81kΩ		80	111	ns
t_{ON-MAX}	Maximum on-time	Fsw = 300kHz, R_{RT}= 54.2kΩ		13.3		µs
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown(1)	Shutdown threshold	155	165	177	ºC
		Recovery threshold		156		ºC

(1) Specified by design.

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7 Detailed Description

7.1 Overview

The LM656x0-Q1 is a family of high-efficiency, high-power density, ultra low-EMI buck converters. These converters operate over a wide input voltage range of 3V to 70V with an adjustable output from 0.8V to 60V. Up to two converters can be set up in an interleaved mode (paralleled outputs) with accurate current sharing for supporting up to 16A of output current.

The current-mode control architecture, with 36ns minimum on-time, allows high conversion ratios at high frequencies, fast transient response, and excellent load and line regulation. If the minimum on-time or minimum off-time does not support the desired conversion ratio, the switching frequency is automatically reduced. This feature allows regulation to be maintained during load dump events and cold cranking situations.

This device is designed to minimize end-product cost and size while operating in demanding automotive and high-performance industrial environments. The LM656x0-Q1 can be set to operate at switching frequencies from 300kHz to 2.2MHz using the RT pin. Internal compensation and an accurate current limit scheme minimizes BOM cost and component count.

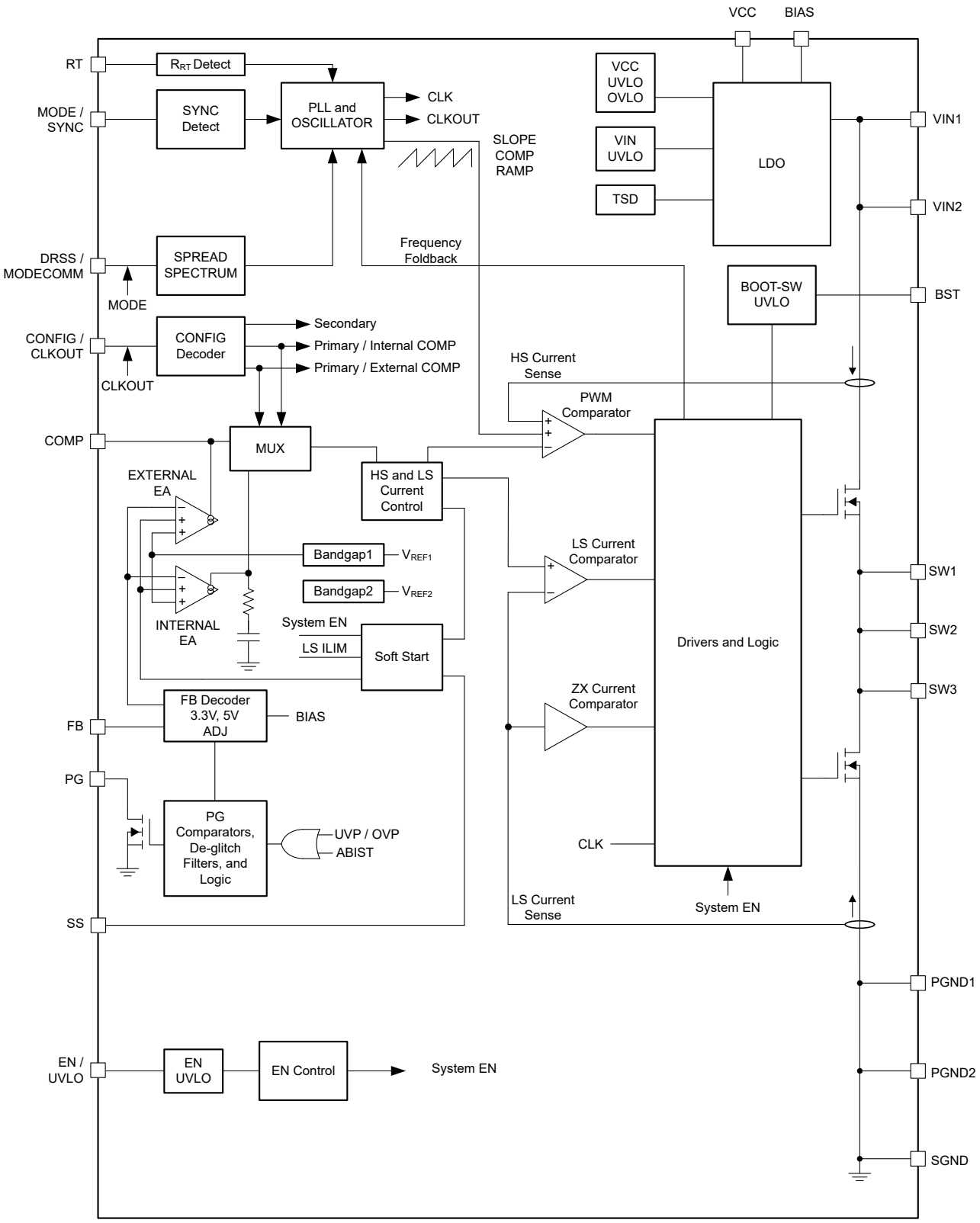
The LM656x0-Q1 has been designed for low EMI. The device includes the following:

- Pin-configurable SW node slew-rate control and dual random spread spectrum (DRSS) frequency hopping
- Symmetrical pinout with low input inductance package
- Operation over a frequency range above and below AM radio band
- Pin-configurable for AUTO or FPWM mode along with external clock synchronization capabilities

Together, these features can eliminate shielding and other expensive EMI mitigation measures.

To use the device in reliability-conscious environments, the LM656x0-Q1 has a package with enlarged corner terminals for improved board level reliability and wettable flanks, allowing optical inspection.

7.2 Functional Block Diagram



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7.3 Feature Descriptions

7.3.1 Output Voltage Selection

The LM656x0-Q1 features pin-selectable fixed output voltage or adjustable output voltage mode. In fixed output voltage mode, the output voltage is selected by the FB pin. Connect the FB pin to GND to select the fixed 3.3V output, or connect to VCC for a fixed 5V output. When the fixed output voltage mode is selected, the BIAS pin is connected directly to the output of the regulator. In this mode, the BIAS pin closes the feedback loop of the regulator and provides input power to the internal bias regulator.

Table 7-1. Output Voltage Selection

FB	VOUT
Short to GND	3.3V
Short to VCC	5V
Connect to a feedback resistor divider tap point (Figure 7-1)	ADJ

In the adjustable output voltage mode, a voltage divider is connected between the regulator output voltage and the FB pin. The resistor values are calculated based on the desired output voltage and the 0.8V reference of the regulator. See Figure 7-1 for detailed connections.

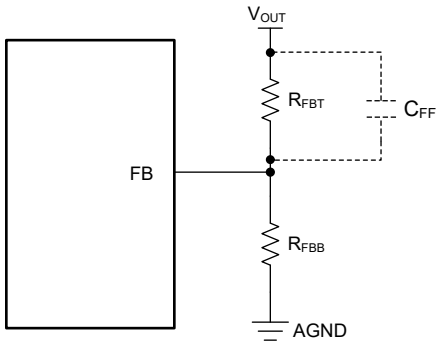

Figure 7-1. Setting Output Voltage of Adjustable Versions

Use Equation 1 to select a value for R_{FBB}, based on a desired value of R_{FBT}. Limiting the value of R_{FBT} to 100kΩ or less is best practice. Larger values of resistance are susceptible to leakage currents on the PCB, caused by environmental contamination, that can shift the desired output voltage. Values up to about 1MΩ can be used to reduce the no-load supply current, in those cases where excessive PCB leakage currents are not present.

$$R_{FBB} = R_{FBT} \times \frac{0.8}{V_{OUT} - 1} \quad (1)$$

In some cases, when using the adjustable mode, a feed-forward capacitor can be used to improve the loop phase margin and load transient response. The exact value of C_{FF} is best selected empirically during the initial bench evaluation of the design. In any event, TI recommends to leave a placeholder for this capacitor in the PCB layout for added design flexibility.

7.3.2 EN Pin and Use as V_{IN} UVLO

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input Undervoltage Lockout (UVLO). Applying a voltage greater than about 0.9V causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to $V_{EN\_TH\_R}$ fully enables the device, allowing the device to enter start-up mode and begin the soft-start period. When the EN input is brought below $V_{EN\_TH\_F}$, the regulator stops switching and enters standby mode. Further decrease in the EN voltage to below 0.9V completely shuts down the device, providing a shutdown current of less than 0.65µA (typical). The EN input can be connected directly to VIN if this feature is not needed. The enable must not float as floating the pin forces the device off. The values

for the various EN thresholds can be found in the *Electrical Characteristics* table. Keep in mind that the internal VIN UVLO overrides the EN input. The device does not start up unless the input voltage is above $VIN_{UVLO(R)}$. Conversely, the device shuts down when the input voltage falls bellow $VIN_{UVLO(F)}$.

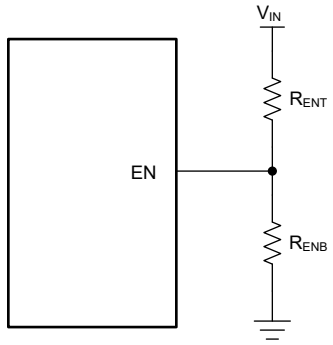

Figure 7-2. VIN UVLO Using the EN Pin

In some cases, an input UVLO level different than that provided internal to the device is needed. This feature can be used for special sequencing or to prevent input voltage oscillations caused by excessively long power cables. External UVLO can be accomplished by using the circuit shown in Figure 7-2. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. The current in the divider must be greater than the current into the EN input (I_{EN_LKG}) to preserve accuracy. Values for R_{ENB} between 10kΩ and 50kΩ are reasonable. Then, Equation 2 is used to calculate R_{ENT} and Equation 3 is used to calculate V_{OFF}.

$$R_{ENT} = R_{ENB} \times \left(\frac{V_{ON}}{V_{EN\_TH\_R}} - 1 \right) \quad (2)$$

$$V_{OFF} = V_{ON} \times \left(\frac{V_{EN\_TH\_F}}{V_{EN\_TH\_R}} \right) \quad (3)$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

7.3.3 Device Configuration

The device configuration is implemented with the CONFIG pin.

The CONFIG pin configures the device as a primary or a secondary device, selects either internal compensation (1-phase operation) or external compensation (1-phase or 2-phase operation), and affects the DRSS / MODECOMM pin functionality as shown in the following table.

Table 7-2. Device Configuration

CONFIG Pin	Configuration	DRSS / MODECOMM Pin Functionality
Short to GND	Secondary device, CLKOUT disabled	MODECOMM input
49.9kΩ to GND	Primary device, external COMP, CLKOUT enabled	DRSS control, MODECOMM output
Short to VCC	Primary device, internal COMP, CLKOUT disabled	DRSS control

7.3.4 Single-Output Dual-Phase Operation

For single-output, dual-phase operation, two LM656x0-Q1 devices are required. Additional phases cannot be added. Configure the first device as a primary device and the second device as a secondary device per Device Configuration. This action disables the feedback error amplifier of the secondary device and places feedback error amplifier into a high-impedance state. As shown in Figure 7-3, connect the FB pin of the secondary device to VCC. Furthermore, connect the COMP pins of the primary and secondary devices together with minimal trace

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length. Add an external compensation network near the primary device. Internal compensation feature is not supported when operating in dual-phase configuration.

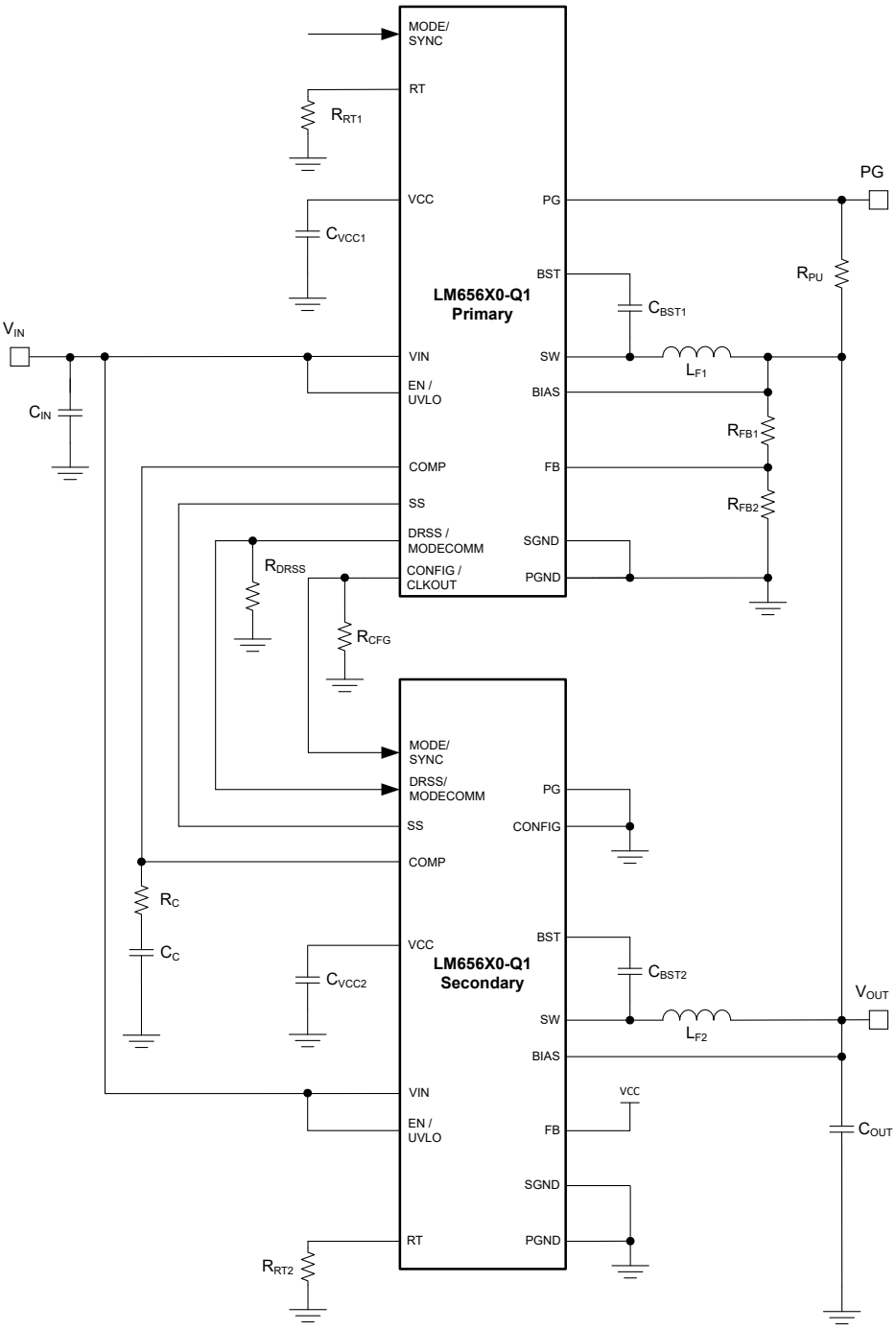

Figure 7-3. Simplified Schematic for Single-Output Dual-Phase Operation

The CONFIG / CLKOUT pin of the primary device must be connected to the MODE / SYNC pin of the secondary device. The CLKOUT signal from the primary device is 180° out-of-phase and facilitates the interleaved operation. When operating in dual-phase configuration, both devices need to be enabled at the exact same time for start-up.

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When configured for dual-phase operation, the DRSS / MODECOMM pin conveys the mode information from the primary device to the secondary device. A MODECOMM high signal from the primary device forces the secondary device to operate in FPWM mode. A MODECOMM low signal from the primary device forces the secondary device to operate in PFM mode. MODECOMM pins of the primary and secondary devices must be tied together. The SS pins of both primary and secondary devices must also be tied together for fault communication.

For more information, see *Benefits of a Multiphase Buck Converter* analog design journal and *Multiphase Buck Design From Start to Finish.* application note.

7.3.5 Mode Selection

The MODE / SYNC pin is a multifunction pin that configures the mode of operation, and serves as an input for an external synchronization signal. If the pin is grounded or driven to a logic low, the converter operates in auto mode. If the pin is tied to VCC (buck only) or driven to a logic high (buck or inverting buck-boost), or synchronized to an external clock source , the converter operates in FPWM mode.

Transitioning the device from AUTO to FPWM mode requires driving the pin from low to high or sending a synchronization signal. Transitioning the device from FPWM to AUTO mode requires driving the pin from high to low or stop sending the synchronization signal.

7.3.5.1 MODE/SYNC Pin Uses for Synchronization

The LM656x0-Q1 MODE/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by coupling a positive edge into the pin. The coupled edge voltage at the pin must exceed the SYNC amplitude threshold of $V_{IH(SYNC)}$ to trip the internal synchronization pulse detector. The minimum SYNC ON pulse and OFF pulse durations must be longer than $t_{SYNC(TON-MIN)}$ and $t_{SYNC(TOFF-MIN)}$ respectively. The LM656x0-Q1 switching action can be synchronized to an external clock from 300kHz to 2.2MHz.

Note, an external SYNC signal can only be applied before or after pin detection. If applied during the pin detection, the SYNC signal can not be detected.

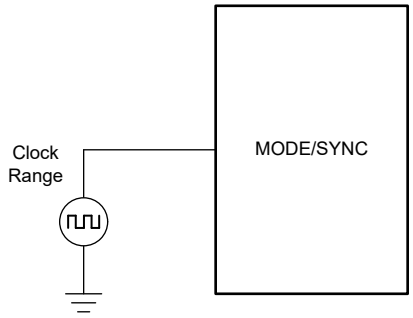
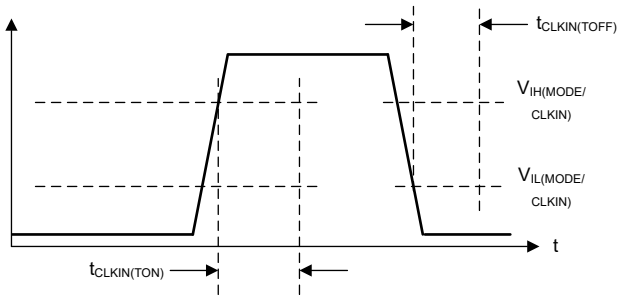


Figure 7-4. Typical Implementation Allowing Synchronization Using the MODE/SYNC Pin



This image shows the conditions needed for detection of a synchronization signal.

Figure 7-5. Typical SYNC Waveform

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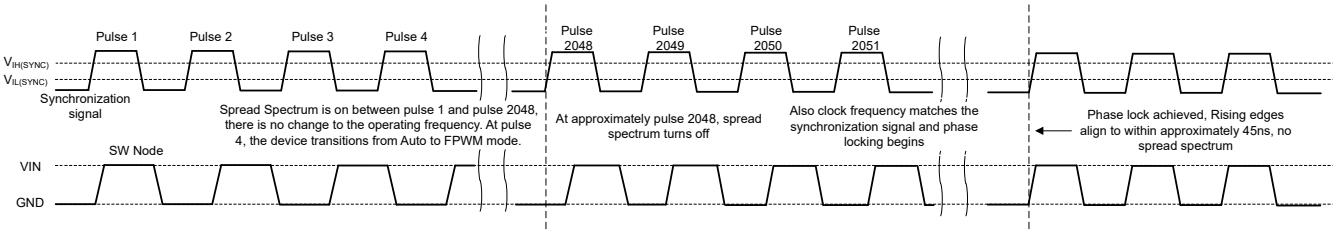
7.3.5.2 Clock Locking

After a valid synchronization signal is detected, a clock locking procedure is initiated. After approximately 2048 pulses, the clock frequency abruptly changes to the frequency of the synchronization signal. While the frequency adjusts suddenly, phase is maintained so the clock cycle lying between operation at the default and synchronization frequencies is of intermediate length. There are no very long or very short pulses. after frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising the SW node pulses. See the following figure.



At pulse 4, the synchronization signal is detected. After approximately pulse 2048, the signal is ready to synchronize and the frequency is adjusted using a glitch-free technique then the phase is locked.

Figure 7-6. Synchronization Process

7.3.6 Adjustable Switching Frequency

The RT pin is configurable. This pin can be tied to VCC for 400kHz operation, grounded (PGND) for 2.2MHz operation, or a resistor to PGND can be used to set an adjustable operating frequency. Note that if a resistor value falls outside of the recommended range, the fall can cause the LM656x0-Q1 to revert to 400kHz or 2.2MHz. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, see the SYNC/MODE pin in Section 7.3.5.1.

$$R_T\ (k\Omega) = (16.4 / f_{SW\ (MHz)}) - 0.633 \quad (4)$$

For example, for f_{SW} = 400kHz, R_T = 40.37kΩ so a 40.2kΩ resistor can be selected as the closest value.

7.3.7 Dual Random Spread Spectrum (DRSS)

Table 7-3. Errata 1

Observation	Root Cause	Recommendation
DRSS pin functionality is different between the prototype device and the final device.	Definition change based on the prototype results. See Table 7-5 and Table 7-4.	If DRSS disabled is a desired setting, connect a 49.9kΩ to GND on the DRSS pin to have the same device behavior when transitioning from the prototype device to the final device.
		If DRSS enabled is a desired setting, tie the DRSS pin to the VCC pin to have a similar device behavior when transitioning from the prototype device to the final device.

The LM656x0-Q1 provides a Dual Random Spread Spectrum (DRSS) function, which reduces EMI of the power supply over a wide-frequency range. The DRSS function combines a low-frequency triangular modulation profile with a high-frequency cycle-by-cycle pseudo-random modulation profile. The low frequency triangular modulation improves performance in the lower radio frequency bands, while the high frequency random modulation improves performance in the higher radio frequency bands.

As shown in Table 7-5, the two low frequency triangular modulation profiles are pin-selectable on the prototype device. The standard low-frequency modulation profile spreads the switching frequency by ±5% with a 12kHz modulation frequency while the wide low frequency modulation profile spreads the switching frequency by ±10% with a 6kHz modulation frequency. The slew rate control is always enabled on the prototype device.

As shown in Table 7-4, the final LM656x0-Q1 device provides a switch-node waveform shaping feature that, when enabled, adjusts the switch-node waveform rising transition for reduced ringing and overshoot. The final device provides the wide low frequency modulation profile which spreads the switching frequency by ±10% with a 6kHz modulation frequency.

Table 7-4. DRSS and Slew-Rate Control - Final Device

DRSS / MODECOMM Pin	DRSS	Slew Rate Control
Short to VCC(1)	Enabled, ±10%, 6kHz	Enabled
Float	Enabled, ±10%, 6kHz	Enabled
150kΩ to GND	Enabled, ±10%, 6kHz	Disabled
49.9kΩ to GND	Disabled	Enabled
Short to GND(1)	Disabled	Disabled

Table 7-5. DRSS and Slew-Rate Control - Prototype Device

DRSS / MODECOMM Pin	DRSS	Slew Rate Control
Short to VCC(1)	Enabled, ±5%, 12kHz	Enabled
Float	Enabled, ±5%, 12kHz	Enabled
150kΩ to GND	Enabled, ±10%, 6kHz	Enabled
49.9kΩ to GND	Disabled	Enabled
Short to GND(1)	Disabled	Enabled

Spread spectrum works by converting a narrowband signal into a wideband signal, which spreads the energy over multiple frequencies. Industry standards require different spectrum analyzer resolution bandwidth (RBW) settings for different frequency bands. The RBW has an impact on the spread spectrum performance. For example, the CISPR-25 requires 9kHz RBW for the 150kHz to 30MHz frequency band. For frequencies greater than 30MHz, the required RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance in the high and low RBWs with the low frequency triangular modulation and high-frequency cycle-by-cycle pseudo-random modulation. In the low-frequency band (150kHz -30MHz), the DRSS function can reduce the conducted emissions by as much as 15dBµV, and in the high-frequency band (30MHz - 108MHz) by as much as 5dBµV. The DRSS function is disabled when an external clock is applied to the MODE/SYNC pin.

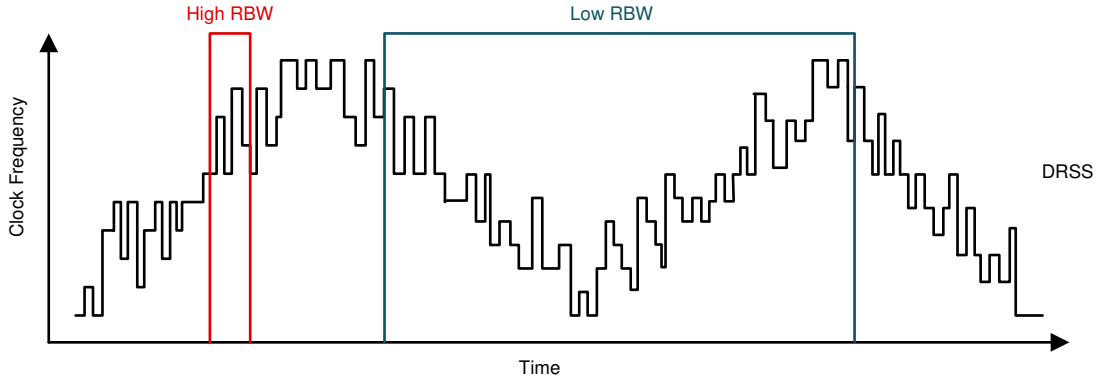


Figure 7-7. Dual Random Spread Spectrum Implementation

7.3.8 Internal LDO, VCC UVLO, and BIAS Input

The LM656x0-Q1 has a dual input for the VCC regulator that is supplied from either VIN or BIAS. After the LM656x0-Q1 is active, power comes from VIN if BIAS is less than approximately 3.1V. However power comes from BIAS if BIAS is more than 3.2V (maximum). VCC is typically 3.2V to 3.3V under most conditions, but can be lower if VIN is very low. To prevent unsafe operation, VCC has a UVLO that prevents switching if the

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internal voltage is too low. See $V_{CC-UVLO\_R}$ and $V_{CC-UVLO\_HYST}$ in *Electrical Characteristics*. During start-up, VCC momentarily exceeds the normal operating voltage until $V_{CC-UVLO\_R}$ is exceeded, then drops to the normal operating voltage. TI recommends a 1µF capacitor rated for 10V with X7R or better dielectric for the VCC capacitor.

7.3.9 Bootstrap Voltage (BST Pin)

The driver of the power switch (HS switch) requires bias higher than VIN when the HS switch is ON. The capacitor connected between BST and SW works as a charge pump to boost voltage on the BST terminal to (SW + VCC). The boot diode is integrated on the LM656x0-Q1 die to minimize the physical design size. TI recommends a 100nF capacitor rated for 10V with X7R or better dielectric for the BST capacitor.

7.3.10 Soft Start and Recovery From Dropout

When designing with the LM656x0-Q1, slower rise in output voltage due to recovery from dropout and soft start must be considered separate phenomena. Soft start is triggered by any of the following conditions:

- EN is used to turn on the device.
- Recovery from a hiccup waiting period; see Section 7.3.11.3.
- Recovery from shutdown due to overtemperature protection.
- Power is applied to the VIN of the IC or the VCC UVLO is released.

After soft start is initiated, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramping up from zero. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of the regulation value.
- Operating mode is set to auto, activating diode emulation. This action allows start-up without pulling output low if there is a voltage already present on the output.
- Hiccup is disabled for the duration of soft start; see Section 7.3.11.3.

All of these actions together provide start-up with limited inrush currents. These actions also allow the use of output capacitors and loading conditions that can cause current limit during start-up without triggering hiccup. In addition, if the output voltage is already present, the output voltage does not discharge.

Any time the output voltage is more than a few percent low for any reason, the output voltage ramps back up slowly. This action is the recovery from dropout condition which differs from soft start in three important ways:

- Hiccup is allowed only if output voltage is less than 0.4 times the set point. Note that during dropout regulation, hiccup is inhibited. See Section 7.3.11.3.
- FPWM mode is allowed during recovery from dropout. If the output voltage were to suddenly be pulled up by an external supply, the LM656x0-Q1can pull down on the output. Note that all the protections that are present during normal operation are in place, protecting the device if output is shorted to a high voltage or ground.
- The reference voltage is set to approximately 1% above that needed to achieve the current output voltage. The reference voltage is not started from zero.

Despite the name, recovery from dropout is active whenever output voltage is more than a few percent lower than the setpoint for long enough that:

- Duty factor is controlled by minimum on-time or
- When the part is operating in current limit.

This primarily occurs under the following conditions:

- Dropout: When there is insufficient input voltage for the desired output voltage to be generated.
- Overcurrent that is not severe enough to trigger hiccup or if the duration is too short to trigger hiccup. See Section 7.3.11.3.

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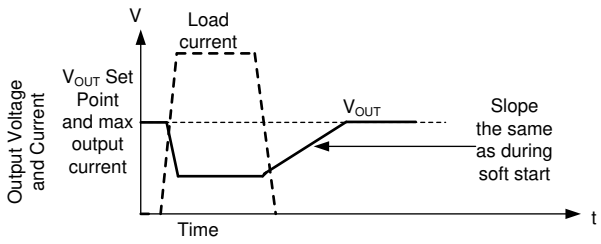

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below the setpoint is removed, output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, hiccup can, in principal, be triggered during recovery if output voltage is below 0.4 times output the setpoint for more than 128 clock cycles during recovery.

Figure 7-8. Recovery From Dropout

7.3.11 Safety Features

The LM656x0-Q1 includes a set of safety features:

- Power-Good monitor with output undervoltage (UV) and overvoltage (OV) protection
- Overcurrent and short-circuit protection with HICCUP mode
- Thermal shutdown (TSD)

7.3.11.1 Power-Good Monitor

The LM656x0-Q1 includes a power-good function to simplify supply sequencing and supervision in a system. The power-good function can be used to enable downstream circuits that are supplied by the LM656x0-Q1, control downstream protection circuits such as load switches, or to turn on sequenced supplies. The function monitors the output voltage with a window comparator through the FB pin for adjustable V_{OUT} configurations and the BIAS pin for fixed V_{OUT} configurations. The power-good output (PG) switches to a high impedance open-drain state when the output voltage is in regulation. When the output voltage is outside of the ±5% range from the set voltage, the PG pin is driven low (< $V_{OL(PG)}$) warning the system of an output overvoltage or undervoltage condition. A 114µs deglitch filter on the PG falling edge prevents false tripping of the power-good signals during transients. When the output voltage returns within the regulation window, a 2ms filter on the PG rising edge allows extra processing time for the downstream components.

TI recommends a100kΩ pullup resistor from the PG pin to the relevant logic rail not greater than 30V. PG is asserted low during soft start and when the LM656x0-Q1 is disabled.

7.3.11.2 Overcurrent and Short-Circuit Protection

The LM656x0-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to the minimum of a fixed current setpoint, or the output of the voltage regulation loop minus slope compensation, every switching cycle. Since the voltage loop has a maximum value and slope compensation increases with duty cycle, the HS current limit decreases with increased duty cycle if duty cycle is above 35%.

When the LS switch is turned on, the current going through the switch is also sensed and monitored. Like the high-side MOSFET, the low-side MOSFET turn-off is commanded by the voltage control loop. For a low-side device, turn-off is prevented if the current limit is exceeded, even if the oscillator normally starts a new switching cycle. Also, like the high-side device, there is a limit on how high the turn-off current is allowed to be. This is called the low-side current limit; see the *Electrical Characteristics* for values. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not turned on. The LS switch is turned off after the LS current

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falls below the limit. The HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

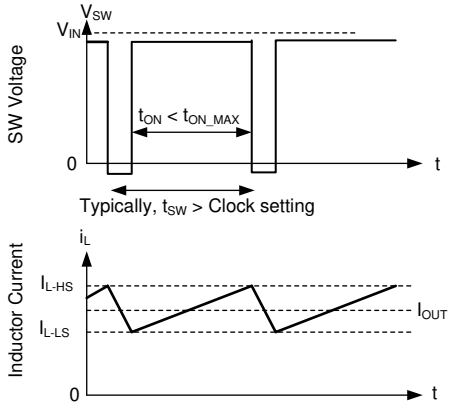

Figure 7-9. Current Limit Waveforms

The net effect of the operation of high-side and low-side current limit is that the IC operates in hysteretic control. Because the current waveform assumes values between I_{L-HS} and I_{L-LS}, output current is close to the average of these two values unless duty cycle is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If the duty cycle is very high, current ripple must be very low to prevent instability. Because the current ripple is low, the part is able to deliver full current. The current delivered is very close to I_{L-LS}.

After the overload condition is removed, the device recovers as though in soft start; see Section 7.3.10. Note that hiccup can be triggered if output voltage drops below approximately 0.4 times the intended output voltage.

7.3.11.3 Hiccup

The LM656x0-Q1 employs hiccup overcurrent protection when all of the following conditions are met for 64 consecutive switching cycles (hiccup mode activation delay, t_{HIC_DLY}):

- A time greater than t_{SS} has passed since soft start has started; see Section 7.3.10.
- Output voltage is below approximately 0.4 times output setpoint.
- The part is not operating in dropout defined as having minimum off-time controlled by duty factor.

In hiccup mode, the device shuts down and attempts to soft start after t_{HIC}. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions and short circuits.

Table 7-6. Errata 2

Observation	Root Cause	Recommendation
Hiccup mode activation delay, t_{HIC_DLY}, is 128 cycles instead of 64 cycles.	Known. Addressed in the final version of the device.	Transition from the prototype version of the device to the final version of the device does not require any special considerations at system level.

7.3.11.4 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 165°C (typical). Thermal shutdown does not trigger below 155°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 156°C. When the junction temperature falls below 156°C (typical), the LM656x0-Q1 attempts to soft start.

While the LM656x0-Q1 is in shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating from a short circuit applied to VCC, the LDO providing power to VCC has

reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on and off control of the device. When the EN pin voltage is below 0.9V, both the regulator and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops below 1µA.

7.4.2 Active Mode

The LM656x0-Q1 is in active mode when the following occurs:

- The EN pin is above V_{EN}.
- V_{IN} is above V_{EN}.
- V_{IN} is high enough to satisfy the V_{IN} minimum operating input voltage.
- No other fault conditions are present.

See Section 7.3 for protection features. The simplest way to enable the operation is to connect EN to VIN, allowing self-start-up when the applied input voltage exceeds the minimum $V_{IN\_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the LM656x0-Q1 is in one of six sub-modes:

- Continuous conduction mode (CCM) with fixed switching frequency and peak current mode operation
- Discontinuous conduction mode (DCM) while in auto mode when the load current is lower than half of the inductor current ripple. If current continues to reduce, the device enters Pulse Frequency Modulation (PFM) which reduces the switch frequency to maintain regulation while reducing switching losses to achieve higher efficiency at light load.
- Minimum on-time operation while the on-time of the device needed for full-frequency operation at the requested low-duty cycle is not supported by T_{ON_MIN}
- Forced pulse width modulation (FPWM) similar to CCM with fixed-switching frequency, but extends the fixed frequency range of operation from full to no load
- A current limiting condition where the output voltage remains above 0.4 times the output setpoint
- Dropout mode when switching frequency is reduced to minimize dropout
- Recovery from dropout similar to other modes of operation except the output voltage setpoint is gradually moved up until the programmed setpoint is reached.

7.4.2.1 Peak Current Mode Operation

The following operating description of the LM656x0-Q1 refers to Section 7.2 and the waveforms in Figure 7-10. Both supply a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW terminal voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, forcing V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period: $D = T_{ON} / (T_{ON} + T_{OFF})$.

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

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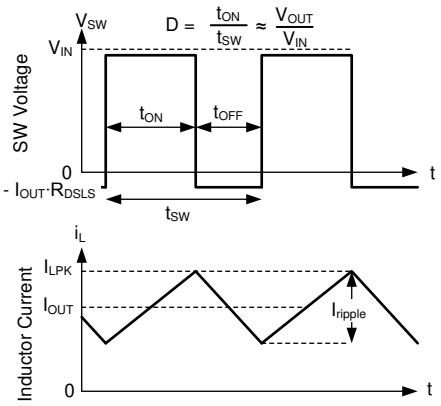


Figure 7-10. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

To get accurate DC load regulation, a voltage feedback loop is used. Peak and valley inductor currents are sensed for peak current mode control and current protection. The regulator operates with continuous conduction mode with constant switching frequency when load level is above one half of the minimum peak inductor current. The internally-compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.4.2.2 Auto Mode Operation

The LM656x0-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows a seamless transition between normal current mode operation while heavily loaded and in highly-efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LM656x0-Q1 operates in depends on the SYNC/MODE pin. When SYNC/MODE is high, the part is in FPWM. When SYNC/MODE is low, the part is in PFM.

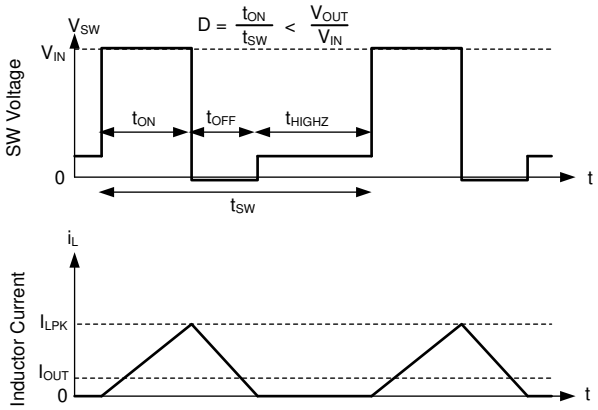
In auto mode, light-load operation is employed in the LM656x0-Q1 at load lower than approximately 1/10th of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation
- Frequency reduction

Note that while these two features operate together to create excellent light load behavior, these features operate independently of each other.

7.4.2.2.1 Diode Emulation

Diode emulation prevents reverse current though the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. Frequency reduces when peak inductor current goes below $I_{PEAK-MIN}$. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



In auto mode, the low-side device is turned off after inductor current is near zero. As a result, after output current is less than half of inductor ripple in CCM, the part operates in DCM. This action is equivalent to saying that diode emulation is active.

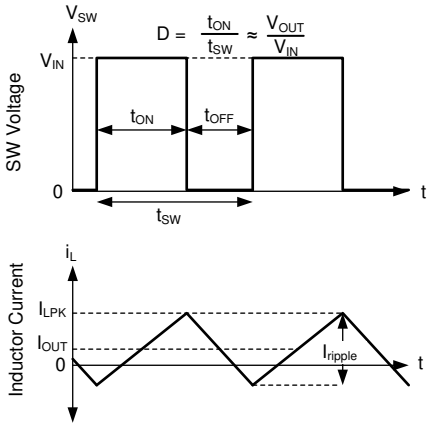
Figure 7-11. PFM Operation

The LM656x0-Q1 has a minimum peak inductor current setting in auto mode. That being said, when current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.2.3 FPWM Mode Operation

Like auto mode operation, FPWM mode operation during light-load operation is selected using the SYNC/MODE pin.

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See the *Electrical Characteristics* for reverse current limit values.



FPWM mode Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of Iripple.

Figure 7-12. FPWM Mode Operation

In FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time, even while lightly loaded. This allows good behavior during faults, which involves the output being pulled up.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following section discuss the output inductor, input and output capacitors, and EMI input filter.

8.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 5 based on a peak inductor current given by Equation 6.

$$L_O = \frac{V_{OUT}}{\Delta I_L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

$$I_{L(PK)} = I_{OUT} + \frac{\Delta I_L}{2} \quad (6)$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This action results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as the core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

8.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by Equation 7.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times F_{SW} \sqrt{\Delta V_{OUT}^2 + \left(R_{ESR} \times \Delta I_L\right)^2}} \quad (7)$$

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Figure 8-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

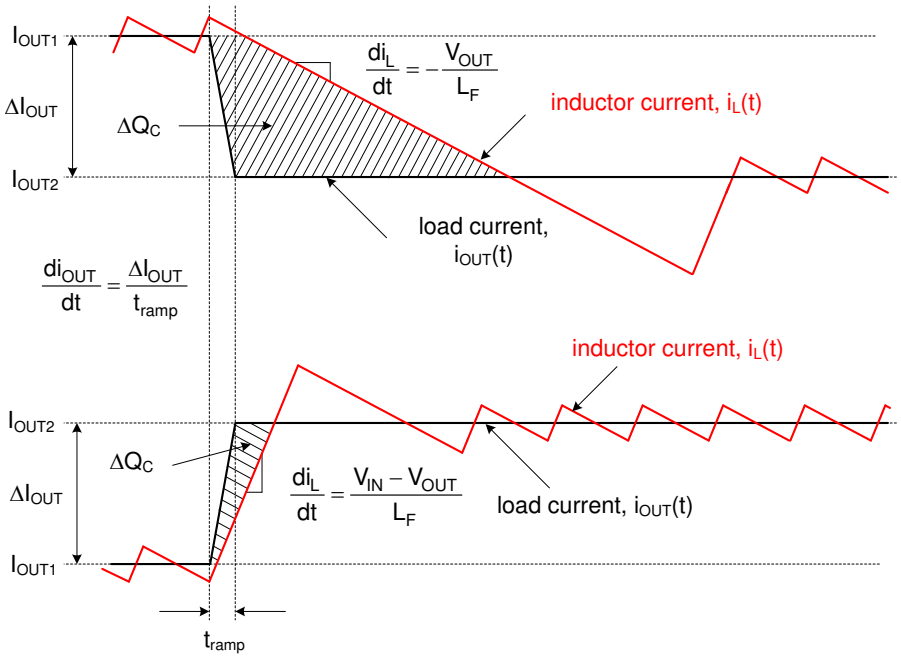

Figure 8-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12V input to low output voltage (for example, 3.3V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below the nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} \quad (8)$$

The ESR of a capacitor is provided in the manufacturer data sheet either explicitly as a specification or implicitly in the impedance vs frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 5mΩ and above, and relatively large ESL, 5nH to 20nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 7 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47µF, 10V, X7R capacitors in 1206 or 1210 footprint is a

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common choice for a 5V output. Use Equation 8 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with the low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with the large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

8.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The input capacitor RMS current for a single-channel buck regulator is given by Equation 9.

$$I_{CIN(rms)} = \sqrt{D \times \left(I_{OUT}^2 \times (1 - D) + \frac{\Delta I_L^2}{12} \right)} \quad (9)$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors must be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The following resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by Equation 10.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \quad (10)$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 11.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \quad (11)$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and two 4.7µF X7R ceramic decoupling capacitors are usually sufficient for most applications. Select the input bulk capacitor based on the ripple current rating and operating temperature range.

Of course, a two-channel buck regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The above equations represent valid calculations when one output is disabled and the other output is fully loaded.

8.1.1.4 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

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$$Z_{IN} = \left| -\frac{V_{IN(min)}^2}{P_{IN}} \right| \quad (12)$$

The EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_{IN} is usually selected between 1µH and 10µH, but can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

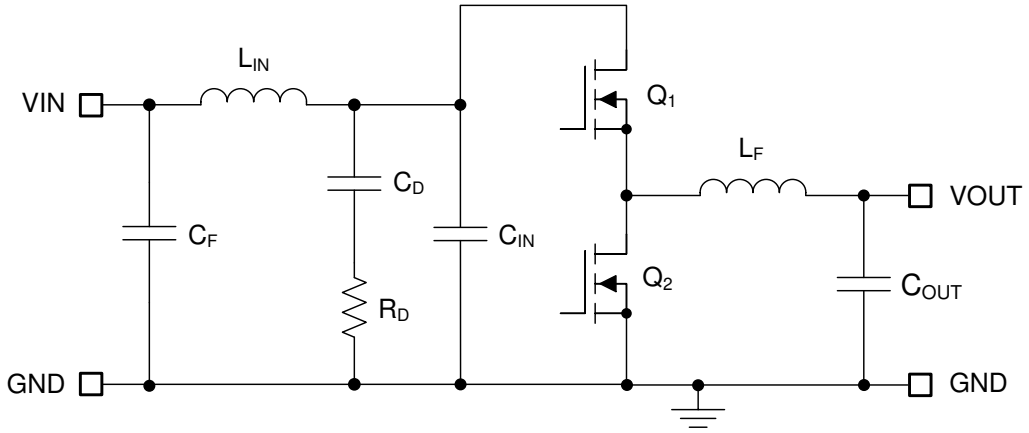

Figure 8-2. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from the fourier series of the input current waveform and multiplying the result by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 13.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \times F_{SW} \times C_{IN}} \times \sin(\pi \times D_{MAX}) \times \frac{1}{1\mu V}\right) - V_{MAX} \quad (13)$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification, for example CISPR 25 Class 5.
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- I_{PEAK} is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from Equation 14.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \times F_{SW}}\right)^2 \quad (14)$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the filter is given by Equation 15.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{IN} \times C_F}} \quad (15)$$

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The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by Equation 16.

$$C_D \geq 4 \times C_{IN} \tag{16}$$

Select the damping resistor R_D using Equation 17.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{17}$$

8.1.2 Error Amplifier and Compensation

A Type-II compensator using a transconductance error amplifier (EA) is shown in Figure 8-3. The dominant pole of the EA open-loop gain is set by the EA output resistance, R_{OEA}, and effective bandwidth-limiting capacitance, C_{BW} as shown by Equation 18.

$$G_{EA(openloop)}(s) = -\frac{g_m \cdot R_{O\text{-}EA}}{1 + s \cdot R_{O\text{-}EA} \cdot C_{BW}} \tag{18}$$

$$G_{EA(openloop)}(s) = -\frac{g_m \times R_{OEA}}{1 + s \times R_{OEA} \times C_{BW}} \tag{19}$$

The EA high-frequency pole is neglected in the above expression. The compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network, is calculated in Equation 20.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \times \frac{g_m \times R_{OEA} \times \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \times \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{20}$$

where

- V_{REF} is the feedback voltage reference of 0.8V
- g_m is the EA gain transconductance of 1000µS
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 500MΩ

$$\omega_{z1} = \frac{1}{R_{COMP} \times C_{COMP}} \tag{21}$$

$$\omega_{p1} = \frac{1}{R_{OEA} \times (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{OEA} \times C_{COMP}} \tag{22}$$

$$\omega_{p2} = \frac{1}{R_{COMP} \times (C_{COMP} \,||\, (C_{HF} + C_{BW}))} \cong \frac{1}{R_{COMP} \times C_{HF}} \tag{23}$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, $R_{COMP} << R_{O\text{-}EA}$ and $C_{COMP} >> C_{BW}$ and C_{HF}, so the approximations are valid. Figure 8-3 circles the poles in red and the zero in blue.

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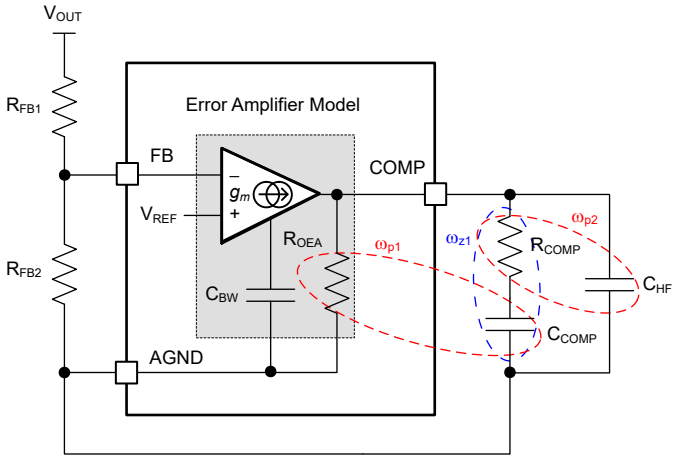

Figure 8-3. Error Amplifier and Compensation Network

8.1.3 Maximum Ambient Temperature

As with any power conversion device, the LM656x0-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient temperature. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$ of the device
- PCB layout

The maximum internal die temperature for the LM656x0-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 24 shows the relationships between the important parameters. Larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in the *Application Curves* section. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* application note, the JESD 51-7 value of $R_{\theta JA}$ given in the *Thermal Information* section is not valid for design purposes and must not be used to estimate the thermal performance of the device in a real application. The JESD 51-7 values reported in the *Thermal Information* table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT(MAX)} = \frac{T_J - T_A}{R_{\theta JA}} \times \frac{\eta}{1-\eta} \times \frac{1}{V_{OUT}} \quad (24)$$

where

- η = efficiency
- T_A = ambient temperature
- T_J = junction temperature
- $R_{\theta JA}$ = the effective thermal resistance of the IC junction to the air, mainly through the PCB

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors. The following are the most critical parameters:

- Power dissipation
- Air temperature
- Airflow
- PCB area

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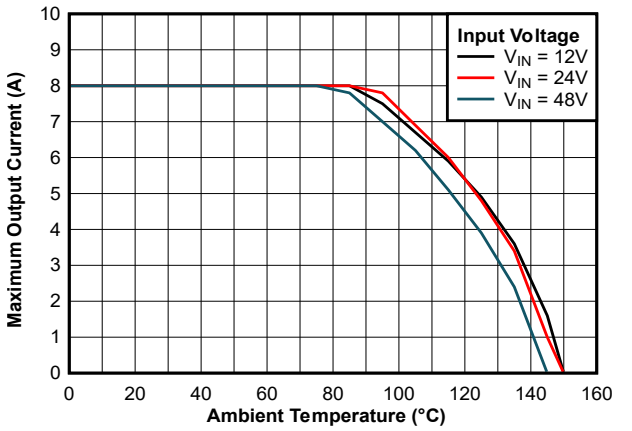
- Copper heat-sink area
- Number of thermal vias under or near the package
- Adjacent component placement

Typical curves of maximum output current versus ambient temperature are shown in *Derating Curves* for a good thermal layout.

Use *Thermal Design Resources* as a guide for thermal PCB design and estimating $R_{\theta JA}$ for a given application environment.

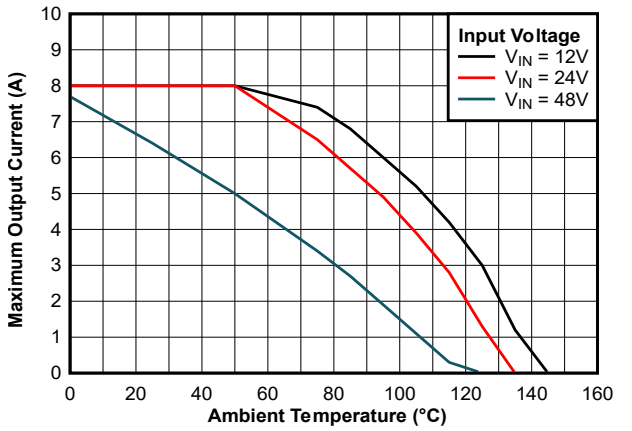
8.1.3.1 Derating Curves

The data in this section was taken on the LM65680-Q1EVM evaluation board with a device and PCB combination, giving an $R_{\theta JA}$ of about 18°C/W. Note that the data given in these graphs are for illustration purposes only and the actual performance in any given application depends on all of the previously mentioned factors.



V_{IN} = 12V, 24V, 48V
V_{OUT} = 5V
f_{SW} = 400kHz
$R_{\theta JA}$ = 18°C/W

Figure 8-4. Maximum Output Current vs Ambient Temperature



V_{IN} = 12V, 24V, 48V
V_{OUT} = 5V
f_{SW} = 2.1MHz
$R_{\theta JA}$ = 18°C/W

Figure 8-5. Maximum Output Current vs Ambient Temperature

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8.2 Typical Application

The LM656x0-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 4A, 6A, or 8A. The following design procedure can be used to select components for the LM656x0-Q1.

Note

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This action can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

Figure 8-6 and Figure 8-7 show typical application circuits for the LM656x0-Q1, when using the adjustable output mode or the fixed output mode, respectively. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is designed for a certain range of external inductance and output capacitance. As a quick-start guide, Table 8-1 through Table 8-4 provide typical component values for a range of application parameters. The component values in these table represent stable designs and are not necessarily optimized. Note that the designs in these tables are based on a typical input voltage of 12V to 48V.

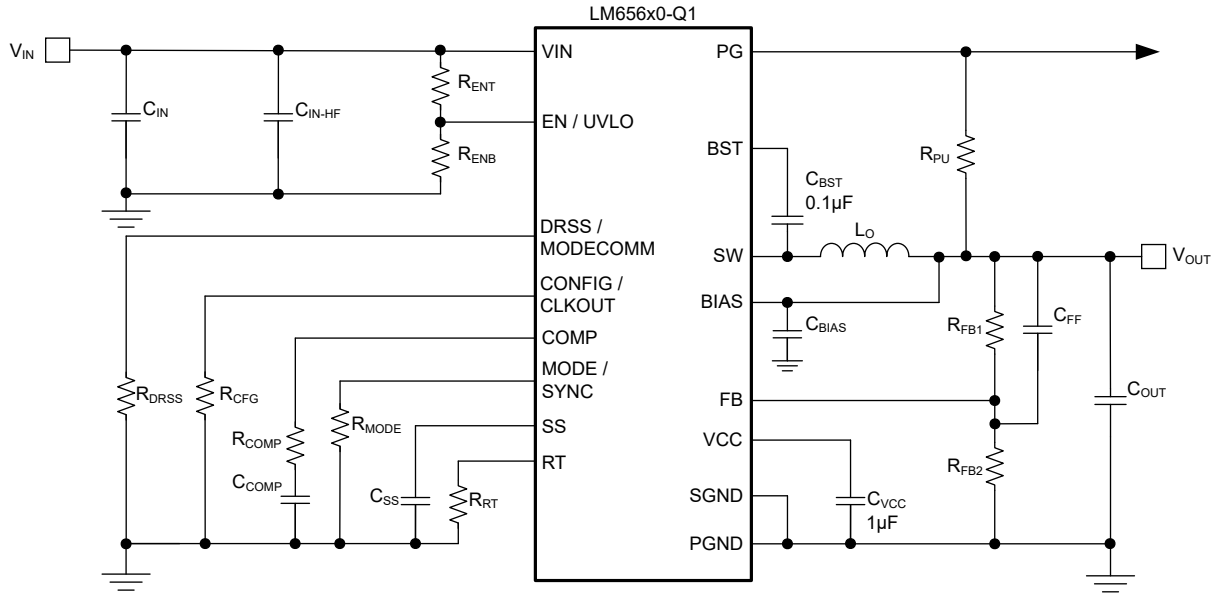

Figure 8-6. Example Application Circuit for Adjustable Output Voltage With LM656x0-Q1

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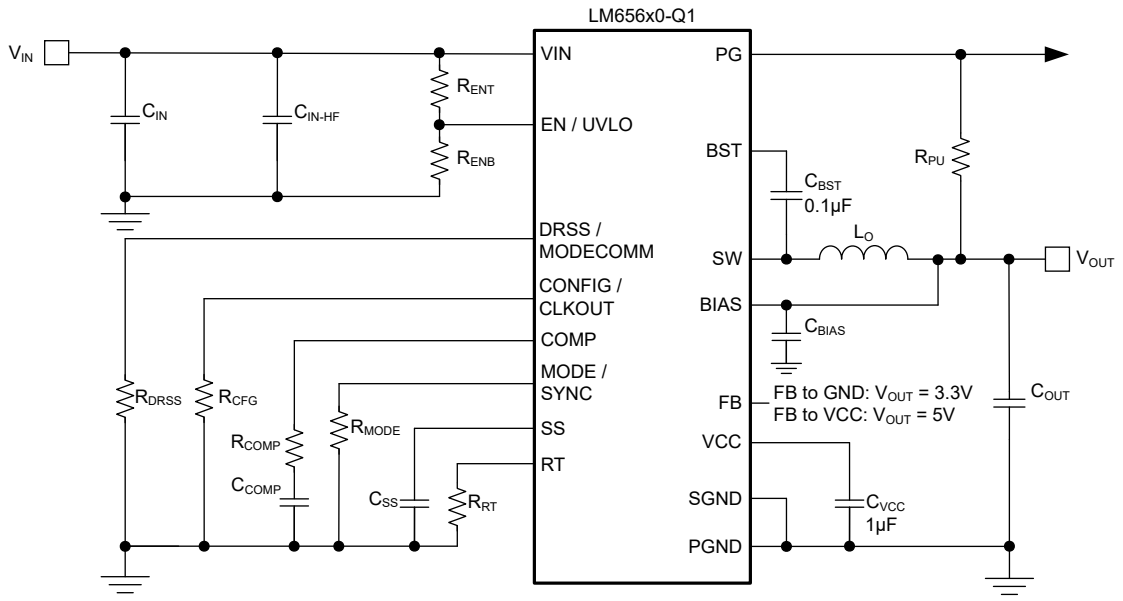

Figure 8-7. Example Application Circuit for Fixed Output Voltage With LM656x0-Q1

Table 8-1. Typical External Components for Fixed Output Voltage (Internally Compensated)

OUTPUT VOLTAGE	FREQUENCY	FB	LM65640-Q1		LM65660-Q1		LM65680-Q1	
			L	COUT (1)	L	COUT (1)	L	COUT (1)
3.3V	400kHz	GND	6.8µH	150µF	4.7µH	180µF	3.3µH	220µF
3.3V	2200kHz	GND	1µH	50µF	0.82µH	60µF	0.68µH	75µF
5V	400kHz	VCC	8.2µH	100µF	6.8µH	125µF	4.7µH	150µF
5V	2200kHz	VCC	1.5µH	30µF	1.2µH	40µF	1µH	50µF

(1) Please note all COUT values are the derated output capacitor values in the tables.

Table 8-2. Typical External Components for LM65640-Q1 in Adjustable Output Voltage (Internally Compensated)

OUTPUT VOLTAGE	FREQUENCY	L	COUT (1)	R_{FBT}	R_{FBB}	C_{FF}
3.3V	400kHz	6.8µH	120µF	100kΩ	31.6kΩ	10pF
5V	400kHz	8.2µH	80µF	100kΩ	19.1kΩ	10pF
12V	400kHz	22µH	35µF	100kΩ	7.15kΩ	10pF
3.3V	2200kHz	1µH	50µF	100kΩ	31.6kΩ	4.7pF
5V	2200kHz	1.5µH	30µF	100kΩ	19.1kΩ	4.7pF
12V	2200kHz	3.3µH	10µF	100kΩ	7.15kΩ	4.7pF

(1) Please note all COUT values are the derated output capacitor values in the tables.

Table 8-3. Typical External Components for LM65660-Q1 in Adjustable Output Voltage (Internally Compensated)

OUTPUT VOLTAGE	FREQUENCY	L	COUT (1)	R_{FBT}	R_{FBB}	C_{FF}
3.3V	400kHz	4.7µH	130µF	100kΩ	31.6kΩ	10pF
5V	400kHz	6.8µH	90µF	100kΩ	19.1kΩ	10pF
12V	400kHz	15µH	40µF	100kΩ	7.15kΩ	10pF
3.3V	2200kHz	0.82µH	60µF	100kΩ	31.6kΩ	4.7pF

Table 8-3. Typical External Components for LM65660-Q1 in Adjustable Output Voltage (Internally Compensated) (continued)

OUTPUT VOLTAGE	FREQUENCY	L	COUT (1)	R_{FBT}	R_{FBB}	C_{FF}
5V	2200kHz	1.2µH	40µF	100kΩ	19.1kΩ	4.7pF
12V	2200kHz	3.3µH	17µF	100kΩ	7.15kΩ	4.7pF

(1) Please note all COUT values are the derated output capacitor values in the tables.

Table 8-4. Typical External Components for LM65680-Q1 in Adjustable Output Voltage (Internally Compensated)

OUTPUT VOLTAGE	FREQUENCY	L	COUT (1)	R_{FBT}	R_{FBB}	C_{FF}
3.3V	400kHz	3.3µH	180µF	100kΩ	31.6kΩ	10pF
5V	400kHz	4.7µH	120µF	100kΩ	19.1kΩ	10pF
12V	400kHz	12µH	50µF	100kΩ	7.15kΩ	10pF
3.3V	2200kHz	0.68µH	80µF	100kΩ	31.6kΩ	4.7pF
5V	2200kHz	1µH	50µF	100kΩ	19.1kΩ	4.7pF
12V	2200kHz	2.2µH	20µF	100kΩ	7.15kΩ	4.7pF

(1) Please note all COUT values are the derated output capacitor values in the tables.

8.2.1 Design Requirements

The following example provides a detailed design procedure based on the specifications found in Table 8-5.

Table 8-5. Detailed Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	8V to 65V
Min transient input voltage (cold crank)	4.5V
Max transient input voltage (load dump)	70V
Output voltage	5V
Output current	0A to 8A
Switching frequency	400kHz
Output voltage regulation	±1%
Active current, no load	15µA
Shutdown current	1.3µA
Soft-start time	5.3ms

The switching frequency is set at 400kHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 50kHz with a phase margin greater than 50°.

The selected buck regulator powertrain components are cited in Table 8-6, and many of the components are available from multiple vendors. This design uses a low-DCR, metal-powder composite inductor, and ceramic output capacitor implementation.

Table 8-6. List of Materials for Application Circuit

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	4	CAP, CERM, 4.7µF, 100V, +/- 10%, X7S, 1210, AEC-Q200	Murata	GCM32DC72A475KE02L
			TDK	CGA6M3X7S2A475K200
C_O	2	47µF ±10% 10VDC, X7S, 1210 Embossed T/R, AEC-Q200	Murata	GCM32EC71A476KE02K
		47µF, 10V, X7S, 1210, ceramic, AEC-Q200	TDK	CGA6P1X7S1A476M250AC

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Table 8-6. List of Materials for Application Circuit (continued)

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
L_O	1	3.3µH, 5.9mΩ, 10.1A, 6.71 × 6.51 × 6.1mm, AEC-Q200	Coilcraft	XGL6060-332MEC
		3.3µH, 15.7mΩ, 17.7A, 6.95 × 6.6 × 4.3mm, AEC-Q200	Cyntec	VCUW064E-3R3MS5
		3.3µH, 10.8mΩ, 15A, 6.45 × 6.65 × 5.8mm, AEC-Q200	Würth Electronik	74439346033
U_1	1	LM656x0-Q1 70V buck converter, AEC-Q100	Texas Instruments	LM65680RZYRQ1

8.2.2 Detailed Design Procedure

The following design procedure applies to Figure 8-6 and Table 8-5.

8.2.2.1 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 30% to 50% of the maximum output current *rating* of the device. Experience shows that the best value for inductor ripple current is 40% of the maximum output current rating for systems with a fixed input voltage.

Larger values of ripple current can restrict the maximum output current, before current limit is reached. Smaller values of ripple current reduce the SNR of the current mode controller and can lead to increased jitter in the duty cycle. Both the inductor and switching frequency tolerance have an impact on the selection of ripple current, and, therefore, inductor value. Use the maximum device current rating when calculating the ripple current for applications with much smaller maximum load than the maximum available from the device. The ratio of inductor ripple current over maximum output current is designated as K. Equation 25 is used to determine the value of inductance:

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times K \times I_{OUT-rated} \times F_{SW}} \quad (25)$$

The typical input voltage for the application is usually used in Equation 25. However, if the application requires very wide range of input voltages, then some voltage near the upper end of the range can be used. In any case, after the inductor has been selected, the ripple current must be checked at the maximum input voltage. Too large a ripple current can limit the maximum output current, as mentioned above. Use Equation 26 to check for these concerns.

$$I_{OUT-max} \cong I_{HS-LIM} - \frac{1}{2} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times L \times F_{SW}} \quad (26)$$

During inductor selection, the saturation current rating of the inductor needs to be as large as the high-side switch current limit, I_{HS-LIM}. This size makes sure that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This rise can lead to component damage. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, powered iron cores have more core losses at frequencies above about 1MHz In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

To avoid subharmonic oscillation, the inductance value must not be less than that given in Equation 27. This limit applies to applications where the switch duty cycle becomes greater than or equal to 50%, under any operating condition.

$$L_{min} \geq M \times \frac{V_{OUT}}{F_{SW}} \quad (27)$$

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where

- M = 0.273 for the 4A device
- M = 0.203 for the 6A device
- M = 0.156 for the 8A device

The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

For this example, assuming a 48V input with a K = 0.4, Equation 25 gives an inductor value of 3.5µH. Use the closest standard value of 3.3µH. Alternatively, Table 8-4 can be used to select the inductor value for a typical input voltage of 48V.

8.2.2.2 Output Capacitors

1. Use Equation 28 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 7% (350mV for a 5V output).

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} = \frac{3.3\mu H \times (8A)^2}{(5V + 350mV)^2 - 5V^2} = 58\mu F \quad (28)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select two 47µF, 10V, X7S, 1210 ceramic output capacitors. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory. For this example, choosing two TDK 47µF CGA6P1X7S1A476M250AC gives an effective capacitance of 80µF for a 5V output.
3. Use Equation 29 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \sqrt{\left(\frac{\Delta I_{LO}}{8 \times F_{SW} \times C_{OUT}}\right)^2 + \left(R_{ESR} \times \Delta I_{LO}\right)^2} = \sqrt{\left(\frac{3.2A}{8 \times 400kHz \times 80\mu F}\right)^2 + \left(1m\Omega \times 3.2A\right)^2} = 12.9mV \quad (29)$$

where

- ΔI_{LO} is the desired peak-to-peak ripple inductor current. For this example, an 8A load with K = 0.4 yields an inductor ripple current of 3.2A.
- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 80µF is the total effective (derated) ceramic output capacitance at 5V.

4. Use Equation 30 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_{LO}}{\sqrt{12}} = \frac{3.2A}{\sqrt{12}} = 0.924A \quad (30)$$

8.2.2.3 Feed-forward Capacitor (C_{FF})

The value of the C_{FF} capacitor is calculated so that the resulting phase margin of the overall system is improved. The addition of the C_{FF} capacitor does not change the response of the system at the DC level or at lower frequencies. At higher frequencies, the capacitor helps reduce the impedance from V_{OUT} to FB. This action helps propagate any high frequency change due to a fast load transient at the output to the feedback, and allows the error amplifier to correct for this.

In the frequency domain, the addition of the C_{FF} capacitor creates an additional zero and a pole. The zero is caused by the interaction of C_{FF} with the upper feedback resistor R_{FBT}. This action helps increase the gain by 20dB/decade and gives the necessary phase boost. The zero frequency is given in Equation 31:

$$f_Z = \frac{1}{2 \times \pi \times R_{FBT} \times C_{FF}} \quad (31)$$

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The pole is caused by the interaction of C_{FF} with the parallel combination of the upper feedback resistors R_{FBT} and the lower feedback resistor R_{FBB}. The pole decreases the gain by 20dB/dec, and helps to roll off the gain after the system crossover. Gain margin is also increased. The pole frequency is given in Equation 32:

$$f_P = \frac{1}{2 \times \pi \times (R_{FBT} \,||\, R_{FBB}) \times C_{FF}} \quad (32)$$

From Equation 31 and Equation 32, if the C_{FF} increases, the zero moves to lower frequencies. The pole also moves to lower frequencies, and if the value of C_{FF} is not optimized, the actions of the zero and the pole nearly cancel each other out. This event is exacerbated at relatively lower outputs, where the pole and zero frequencies are very close. To obtain the best performance from the C_{FF} capacitor, the value of C_{FF} must be optimized.

The C_{FF} capacitor optimization relies on the idea that if the zero and pole frequencies are aligned so that the system crossover frequency without the use of C_{FF} (f_{NO_CFF}) is exactly between the pole and zero frequencies caused by the C_{FF}, then the most optimum phase boost is obtained at the crossover frequency. The C_{FF} pole follows after the crossover frequency and assists the gain roll off for better gain margin. The equation is as follows:

$$f_{NO\_CFF} = \sqrt{f_Z \times f_P} \quad (33)$$

Substituting Equation 31 and Equation 32 into Equation 33 results in Equation 34, which is now a function of R_{FBT}, R_{FBB}, and f_{NO_CFF}.

$$C_{FF\_OPT} = \frac{\sqrt{R_{FBT} + R_{FBB}}}{2 \times \pi \times f_{NO\_CFF} \times R_{FBT} \times \sqrt{R_{FBB}}} \quad (34)$$

Where,

- C_{FF_OPT} = optimized feed-forward capacitor
- R_{FBT} = upper feedback resistor
- R_{FBB} = lower feedback resistor
- f_{NO_CFF} = system crossover frequency without the use of C_{FF}

8.2.2.4 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 2 × 4.7µF is required on the input of the regulator. Place one capacitor on each side of the package and connected directly to the VIN and GND pins of the device. This capacitance must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. The value can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a high frequency bypass capacitance of 2 × 100nF ceramic capacitor must be used at the input, as close a possible to the regulator. Place one capacitor on each side of the package and connected directly to the VIN and GND pins of the device. This requirement provides a high frequency bypass for the control circuits internal to the device.

For this example, 4 × 4.7µF, 100V, X7R (or better) ceramic capacitors are chosen. The 100nF capacitors must also be rated at 100V with an X7R dielectric.

Using an electrolytic capacitor on the input in parallel with the ceramics is often desirable. This statement is especially true if long leads or traces are used to connect the input supply to the regulator, or an input EMI filter is used. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by any inductance on the input. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from the following equation and must be checked against the manufacturers maximum ratings.

$$I_{CIN(RMS)} \cong \frac{I_{OUT}}{2} \quad (35)$$

8.2.2.5 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this application example, select a frequency of 400kHz. In this case, the RT pin is connected to a resistor of 40.2kΩ. See section *Adjustable Switching Frequency* for more details.

8.2.2.6 Setting the Output Voltage

The adjustable output voltage version of the LM656x0-Q1 uses a feedback divider network to set the output voltage. The divider network comprises top and bottom feedback resistors designated as R_{FBT} and R_{FBB}, respectively. The resistances of the feedback divider are a compromise between excessive noise pickup and quiescent current consumption. Lower resistance values reduce noise sensitivity but also impact light-load efficiency. The recommended value for R_{FBT} is 100kΩ with a maximum value of 1MΩ. Adding a feed forward capacitor in parallel with R_{FBT} can be used to optimize the loop performance. Use Equation 36 to find R_{FBB} for a given value of R_{FBT}.

$$R_{FBB} = R_{FBT} \times \frac{0.8}{V_{OUT} - 0.8} \quad (36)$$

Note that Equation 37 states that the parallel combination of R_{FBB} and R_{FBT} must be greater than 4kΩ and less than 100kΩ. This limit is required because the regulator must reliably detect the state of the FB pin during the start-up sequence to set the output voltage configuration (fixed or adjustable output voltage setting) correctly.

$$100\text{k}\Omega \geq R_{FBB} \| R_{FBT} \geq 4\text{k}\Omega \quad (37)$$

Choosing R_{FBT} and R_{FBB} values of 78.7kΩ and 15kΩ, respectively, sets the output voltage to 5V and satisfy both Equation 36 and Equation 37.

If an output voltage is either 3.3V or 5V, a fixed output voltage option is available by either connecting the FB pin to GND or VCC, respectively. For more details on fixed output or adjustable output voltage option, see Output Voltage Selection.

8.2.2.7 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows.

1. Based on a specified loop gain crossover frequency, f_C, of 50kHz, use Equation 38 to calculate R_{COMP}, assuming an effective output capacitance of 80µF (2 × 47µF TDK CGA6P1X7S1A476M250AC capacitors). Choose a standard value for R_{COMP} of 8.66kΩ.

$$R_{COMP} = 2 \times \pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{C_{OUT}}{g_{m1} \times G_{m2}} = 2 \times \pi \times 50\text{kHz} \times \frac{5\text{V}}{0.8\text{V}} \times \frac{80\mu\text{F}}{1\text{mS} \times 18.6\text{A/V}} = 8.44\text{k}\Omega \quad (38)$$

2. To provide adequate phase boost at crossover while also allowing a fast settling time during a load or line transient, select C_{COMP} to place a zero at the higher of (1) one eighth of the crossover frequency, or (2) the load pole. Choose a standard value for C_{COMP} of 2.2nF.

$$C_{COMP} = \frac{8}{2 \times \pi \times f_C \times R_{COMP}} = \frac{8}{2 \times \pi \times 50\text{kHz} \times 8.66\text{k}\Omega} = 2.94\text{nF} \quad (39)$$

   Such a low capacitance value also helps to avoid output voltage overshoot when recovering from dropout (when the input voltage is less than the output voltage set point and V_{COMP} is railed high).

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Note

Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

8.2.2.8 C_{BST}

The LM656x0-Q1 requires a bootstrap capacitor connected between the BST pin and the SW pin. This capacitor stores energy that is used to supply the high-side gate driver for the power MOSFET, along with other critical control circuits. A high-quality ceramic capacitor of 100nF and at least 16V is required.

8.2.2.9 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This need can be accomplished by using the circuit shown in Figure 8-8. The turn-on voltage is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ, then use Equation 40 and Equation 41 to calculate R_{ENT} and V_{OFF}.

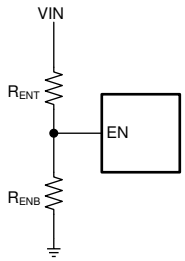

Figure 8-8. Setup for External UVLO Application

$$R_{ENT} = R_{ENB} \times \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \quad (40)$$

$$V_{OFF} = V_{EN-L} \times \left(\frac{V_{ON}}{V_{EN-H}} \right) \quad (41)$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

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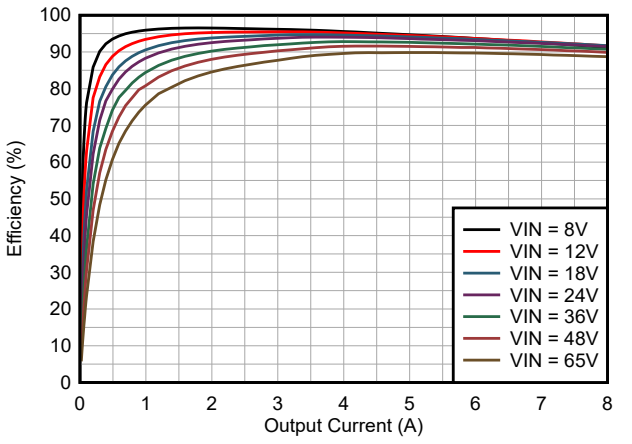
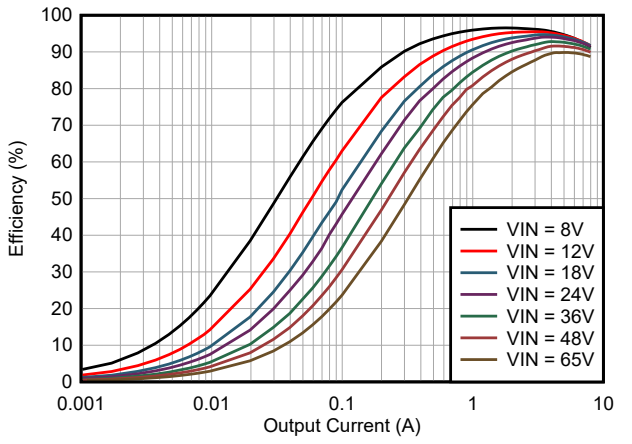
8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 48V, T_A = 25°C.



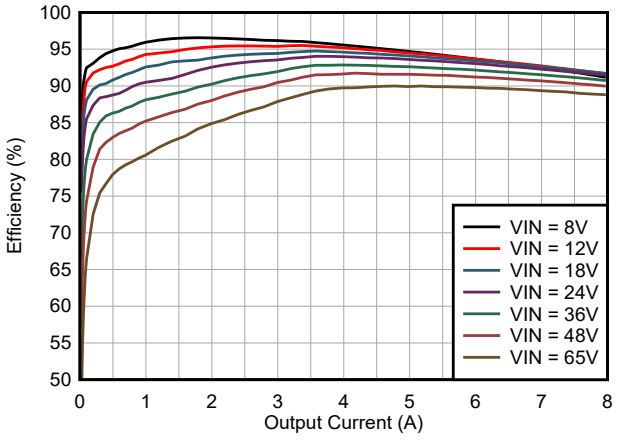
V_{OUT} = 5V F_{SW} = 400kHz FPWM

Figure 8-9. Efficiency vs I_{OUT}, Linear Scale



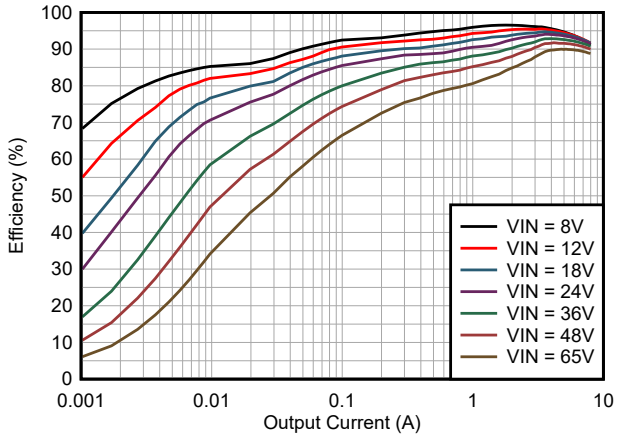
V_{OUT} = 5V F_{SW} = 400kHz FPWM

Figure 8-10. Efficiency vs I_{OUT}, Log Scale



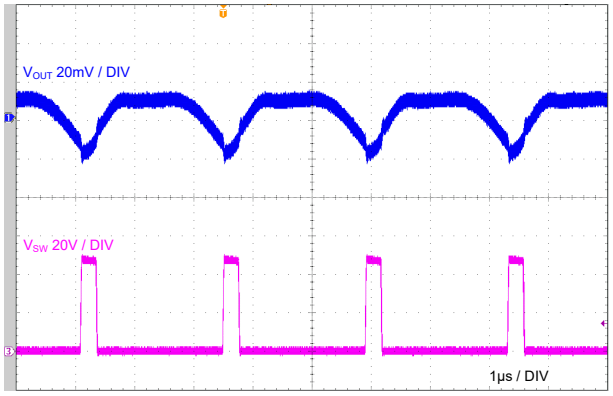
V_{OUT} = 5V F_{SW} = 400kHz PFM

Figure 8-11. Efficiency vs I_{OUT}, Linear Scale



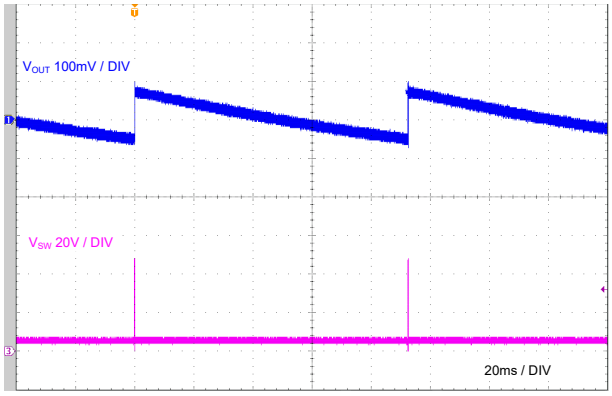
V_{OUT} = 5V F_{SW} = 400kHz PFM

Figure 8-12. Efficiency vs I_{OUT}, Log Scale



V_{IN} = 48V I_{OUT} = 8A FPWM
V_{OUT} = 5V F_{SW} = 400kHz

Figure 8-13. Full Load Switching



V_{IN} = 48V No load PFM
V_{OUT} = 5V

Figure 8-14. PFM Switching

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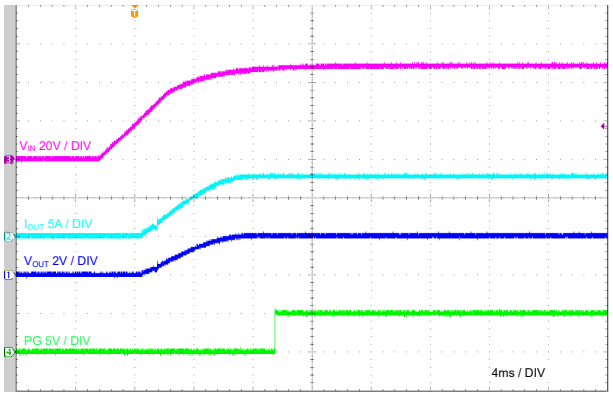
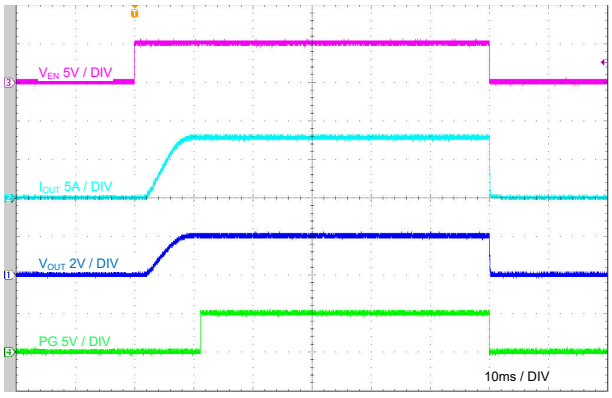


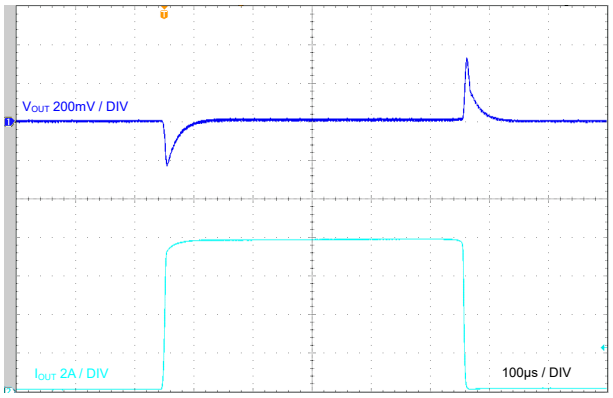
V_{IN} stepped to 48V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz

Figure 8-15. V_{IN} Start-Up Characteristic



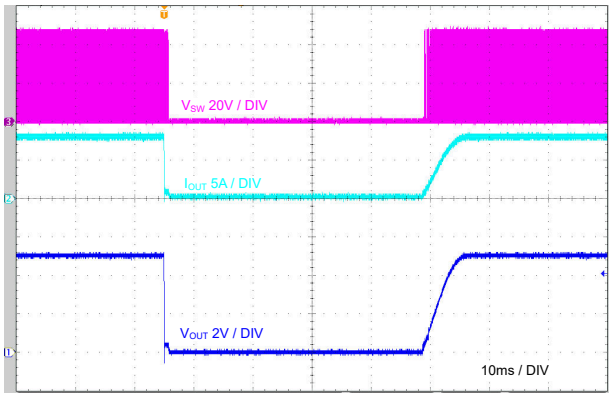
V_{IN} = 48V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz

Figure 8-16. EN Start-Up and Shutdown Characteristic



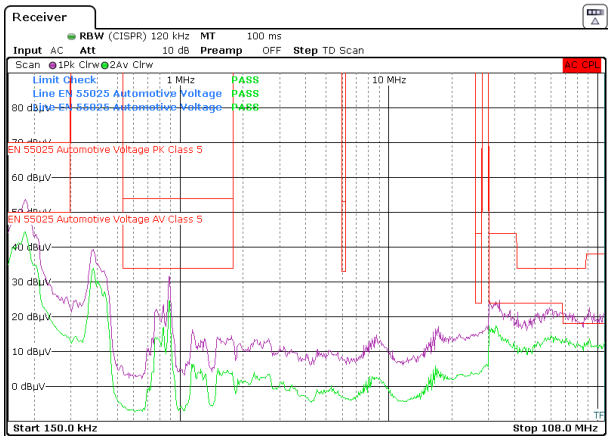
V_{IN} = 48V FPWM
V_{OUT} = 5V

Figure 8-17. Load Transient, 0A to 8A



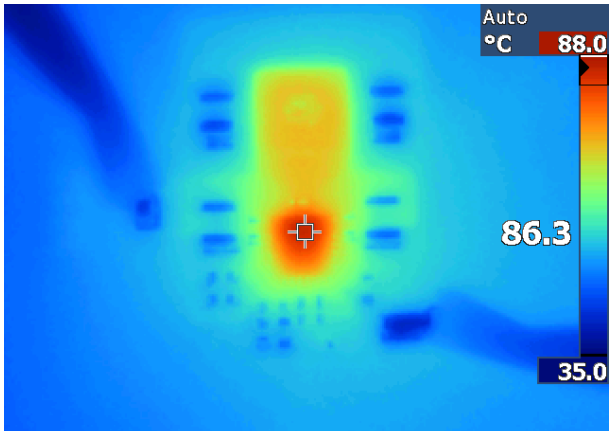
V_{IN} = 48V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz

Figure 8-18. Short-Circuit Recovery



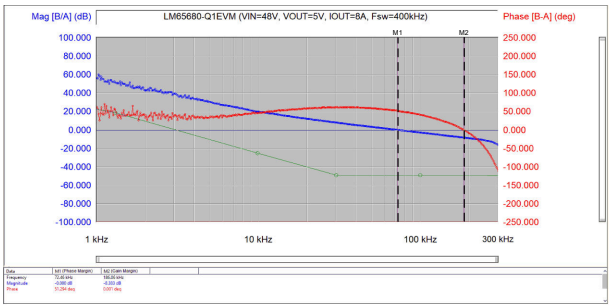
V_{IN} = 48V F_{SW} = 400kHz FPWM
V_{OUT} = 5V I_{OUT} = 8A (resistive) DRSS = ON

Figure 8-19. Typical CISPR 25 Conducted EMI 150kHz - 108MHz Green: Average Detect, Purple = Peak Detect



V_{IN} = 48V F_{SW} = 400kHz FPWM
V_{OUT} = 5V I_{OUT} = 8A (resistive)

Figure 8-20. Thermal Performance, T_{AMB} = 25°C, No Airflow



V_{IN} = 48V
V_{OUT} = 5V
I_{OUT} = 8A (resistive)
F_c = 72.46kHz
FPWM
L = 3.3µH
F_{SW} = 400kHz
PM = 51.29°

Figure 8-21. Bode Plot

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8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*
- Do not exceed the *Recommended Operating Conditions*
- Do not exceed the *ESD Ratings*
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique design and PCB layout to help make the project a success.

8.4 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with the following equation.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (42)$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an underdamped resonant circuit. This can result in overvoltage transients at the input to the regulator or tripping UVLO. Consider that the supply voltage can dip when a load transient is applied to the output depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). TI does not recommend to use a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the excellent performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most EMI-critical PCB feature is the loop formed by the input capacitor or capacitors and power ground. This feature is shown in Figure 8-22. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. Excessive transient voltages can disrupt the proper operation of the converter. Because of this disrupt, the traces in this loop must be wide and short while keeping the loop area as small as possible to reduce the parasitic inductance.

- *Place the input capacitor or capacitors as close as possible to the input pin pairs*: VIN1 to PGND1 and VIN2 to PGND2. Place the small capacitors closest. Each pair of pins are adjacent, simplifying the input capacitor placement. With the QFN package, there are two VIN/PGND pairs on either side of the package. This pair provides a symmetrical layout and helps minimize switching noise and EMI generation. Use a wide VIN plane on a mid-layer to connect both of the VIN pairs together to the input supply. Routing symmetrically from the supply to each VIN pin to best use the benefits of the symmetric pinout is best.
- *Place the bypass capacitor for VCC close to the VCC pin and PGND2 pin:* This capacitor must be routed with short, wide traces to the VCC and PGND2 pins.
- *Place the BST capacitor as close as possible to the device with short, wide traces to the BST and SW pins:*
- *Place the feedback divider as close as possible to the FB pin of the device*: Place R_{FBB}, R_{FBT}, C_{FF} if used, physically close to the device. The connections to FB and PGND through R_{FBB} must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Make layer 2 of the PCB a ground plane*: This plane acts as a noise shield and as a heat dissipation path. Using layer 2 reduces the inclosed area in the input circulating current in the input loop, reducing inductance.
- *Provide wide paths for V_{IN}, V_{OUT}, and PGND*: These paths must be as wide and direct as possible to reduce any voltage drops on the input or output paths of the converter to maximize efficiency.
- *Provide enough PCB area for proper heat sinking*: Enough copper area must be used to make sure of a low $R_{\theta JA}$, considering maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces can be used for all pins except where noise considerations dictate minimization of area.
- *Keep switch area small*: Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

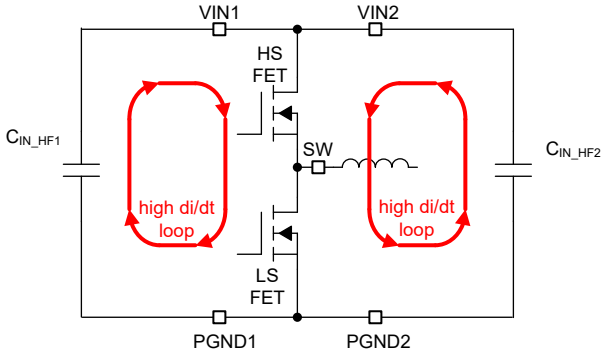

Figure 8-22. Input Current Loop

8.5.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. A ground plane also provides a quiet reference potential for the control circuitry. The PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET, and connect directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and must be used for sensitive traces.

TI recommends providing adequate device heat sinking by using vias near PGND and VIN pins to connect to the system ground plane or V_{IN} strap, both of which dissipate heat. Use as much copper as possible for the system ground plane on the top and bottom layers and avoid plane cuts and bottlenecks for the heat flow for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as:

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2oz / 1oz / 1oz / 2oz. A four-layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding, and low thermal resistance.

8.5.2 Layout Example

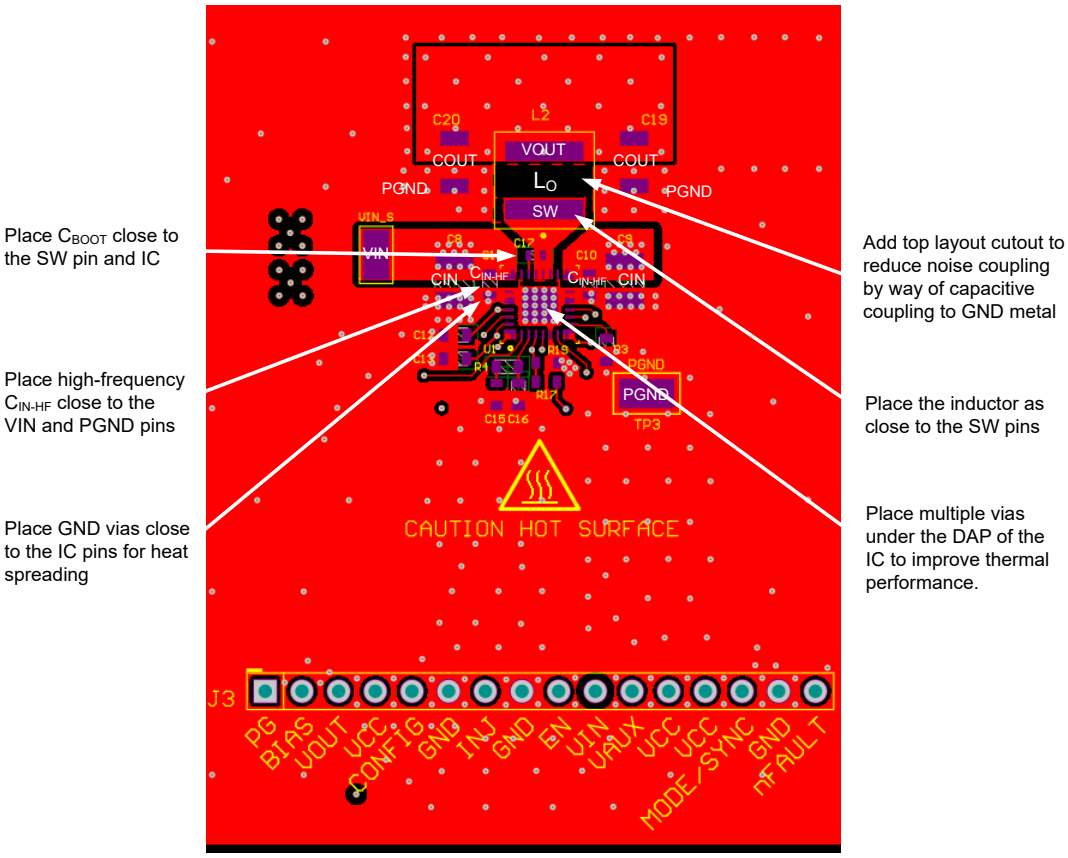

Figure 8-23. Layout Example

9 Device and Documentation Support

9.1 Development Support

For development support, see the following:

- For TI's reference design library, visit TI Designs
- TI Designs:
  - *ADAS 8-Channel Sensor Fusion Hub Reference Design with Two 4-Gbps Quad Deserializers*
  - *Automotive EMI and Thermally Optimized Synchronous Buck Converter Reference Design*
  - *Automotive High Current, Wide V_{IN} Synchronous Buck Controller Reference Design Featuring LM5141-Q1*
  - *25W Automotive Start-Stop Reference Design Operating at 2.2 MHz*
  - *Synchronous Buck Converter for Automotive Cluster Reference Design*
  - *Automotive Synchronous Buck With 3.3V @ 12.0A Reference Design*
  - *Automotive Synchronous Buck Reference Design*
  - *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- Technical articles:
  - *High-Density PCB Layout of DC/DC Converters*
  - *Synchronous Buck Controller Solutions Support Wide V_{IN} Performance and Flexibility*
  - *How to Use Slew Rate for EMI Control*

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Application notes:
  - Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  - Texas Instruments, *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
  - Texas Instruments, *Multiphase Buck Design From Start to Finish.*
- Analog design journal:
  - Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
  - Texas Instruments, *Benefits of a Multiphase Buck Converter*
- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

9.2.1.1 PCB Layout Resources

- Application notes:
  - Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*
  - Texas Instruments, *AN-1229 Simple Switcher PCB Layout Guidelines*
  - Texas Instruments, *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - Texas Instruments, *Constructing Your Power Supply – Layout Considerations*

9.2.1.2 Thermal Design Resources

- Application notes:
  - Texas Instruments, *AN-2020 Thermal Design by Insight, Not Hindsight*

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- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics*
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
- Texas Instruments, *PowerPAD Made Easy*
- Texas Instruments, *Using New Thermal Metrics*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

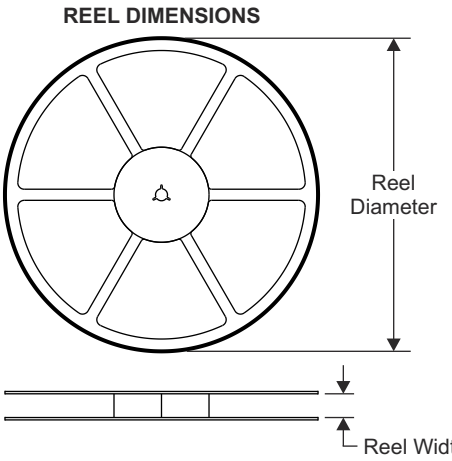
DATE	REVISION	NOTES
October 2024	*	Initial Release

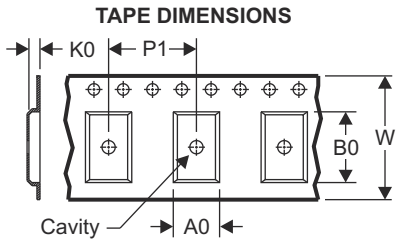
ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

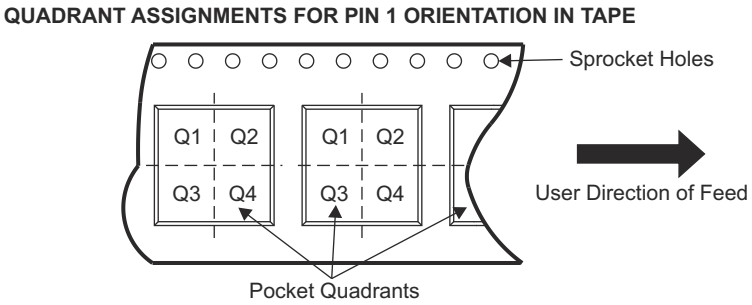
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLM65680RZYRQ1	VQFN-FCRLF	RZY	26	3000	330	12.4	3.79	3.79	0.71	8.0	12.0	Q1

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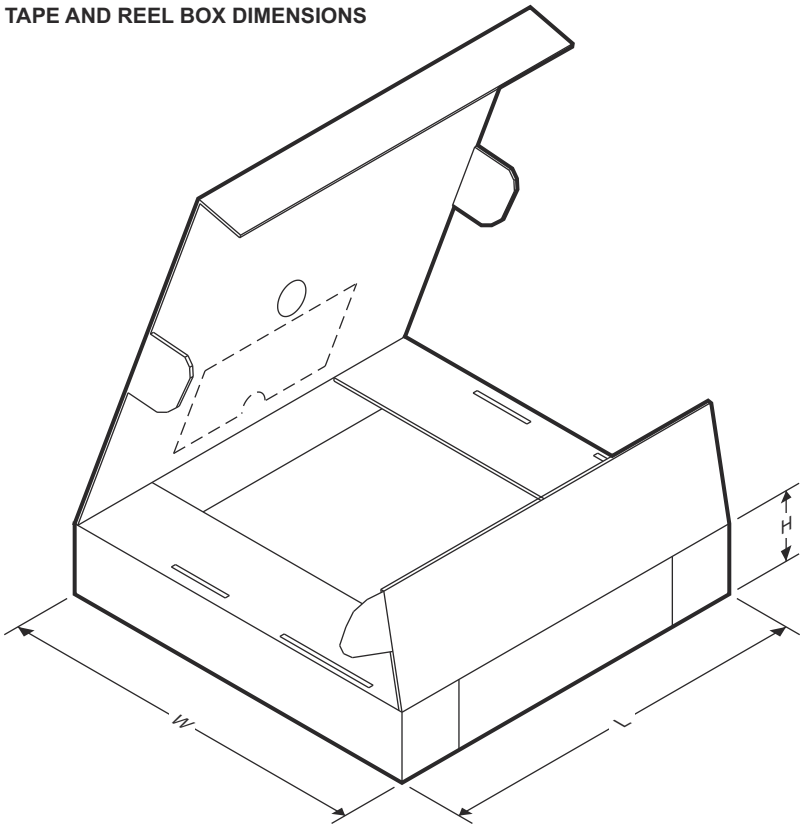
TAPE AND REEL BOX DIMENSIONS



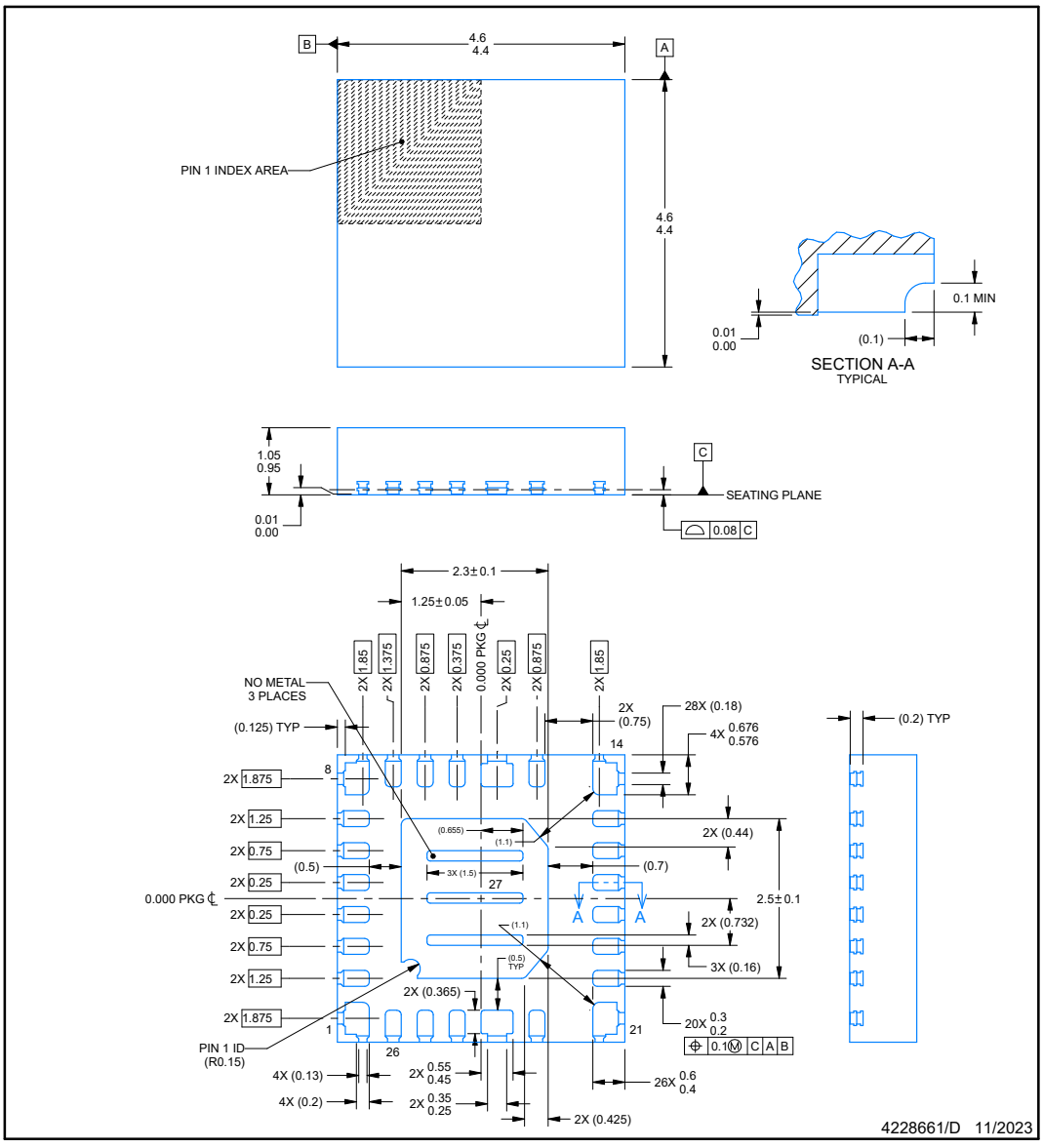
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLM65680RZYRQ1	VQFN-FCRLF	RZY	26	3000	367	367	35

PACKAGE OUTLINE

RZY0026A

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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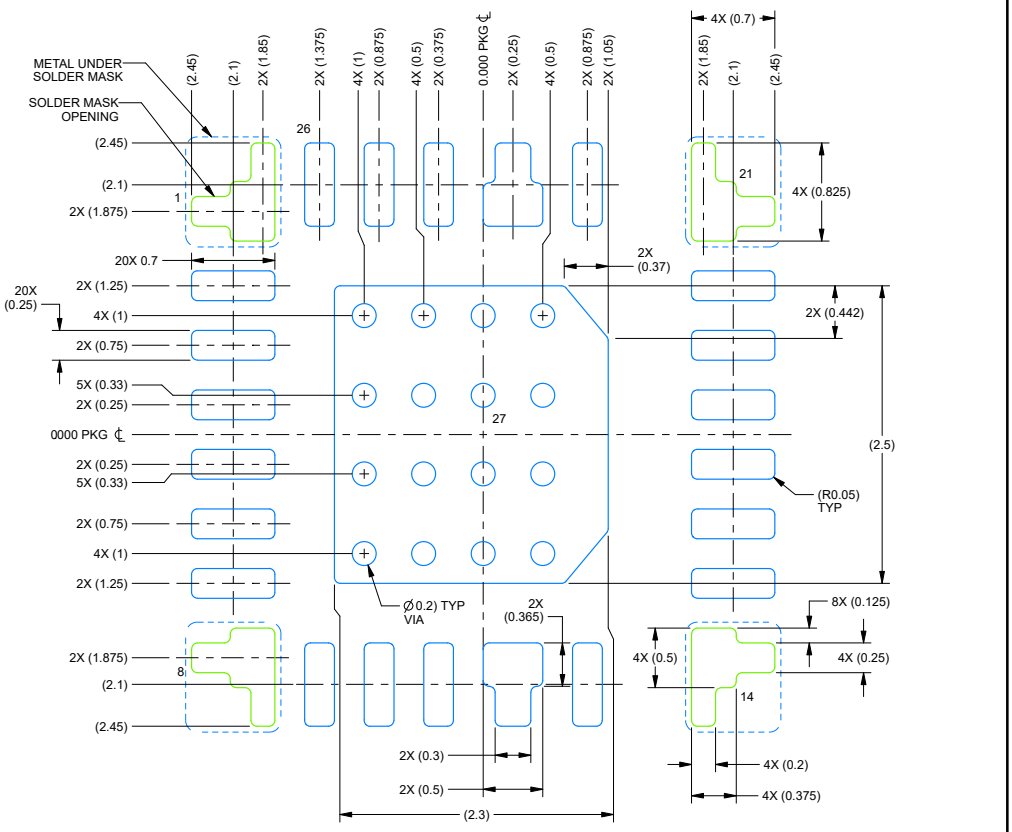
EXAMPLE BOARD LAYOUT

RZY0026A

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



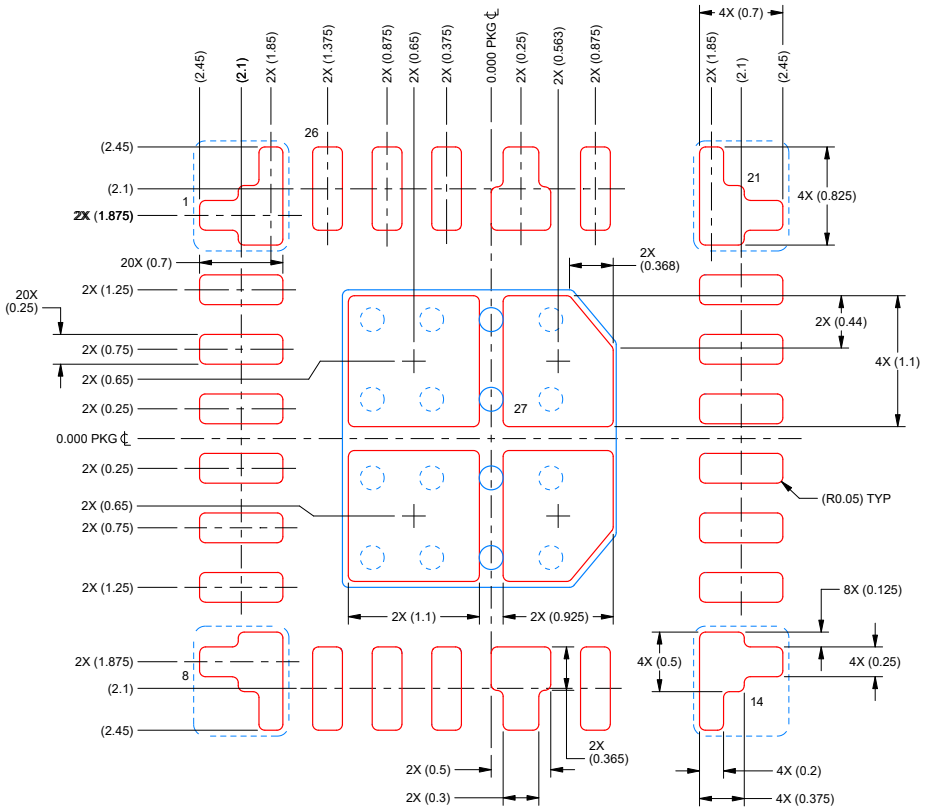
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RZY0026A — **VQFN-FCRLF - 1.05 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 27: 84%

4228661/D 11/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM65680RZYRQ1	ACTIVE	WQFN-FCRLF	RZY	26	3000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM65680-Q1 :

- Catalog : LM65680

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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