LM74670-Q1 Zero I_Q Smart Diode Rectifier Controller

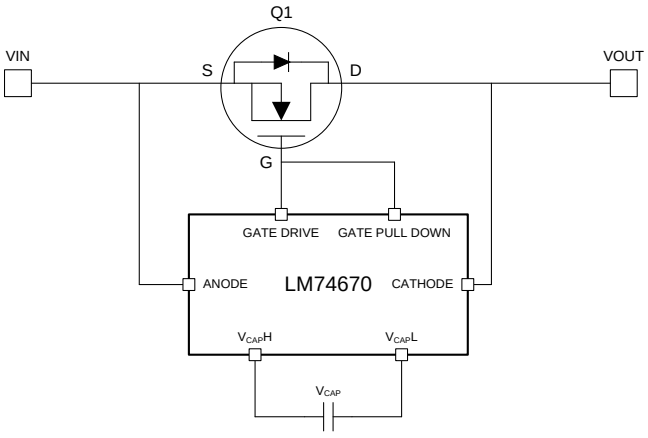
1 Features

- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Exceeds HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Peak Input AC Voltage: 42 V
- Zero I_Q
- Charge Pump Gate Driver for external N-Channel MOSFET
- Low Forward-Voltage Drop and Less Power Dissipation Compared to Schottky Diode
- Capable of handling AC signal up to 300-Hz Frequency

2 Applications

- AC Rectifier
- Alternator
- Power Tools
- Reverse Polarity Protection

Smart Diode Configuration



3 Description

The LM74670-Q1 is a controller device that can be used with an N-Channel MOSFET in full or half bridge rectifier architectures for alternators. It is designed to drive an external MOSFET to emulate an ideal diode. A unique advantage of this scheme is that it is not ground referenced, thus it has zero I_Q. The schottky diodes in full or half bridge rectifiers and alternators can be replaced with the LM74670-Q1 solution to avoid forward conduction diode losses and produce more efficient AC-DC converters.

The LM74670-Q1 controller provides a gate drive for external N-Channel MOSFET and a fast response internal comparator to pull-down the MOSFET Gate in the event of reverse polarity. This device can support an AC signal frequency up to 300Hz.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74670-Q1	VSSOP (8)	3.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Smart Diode Full Bridge Rectifier Application

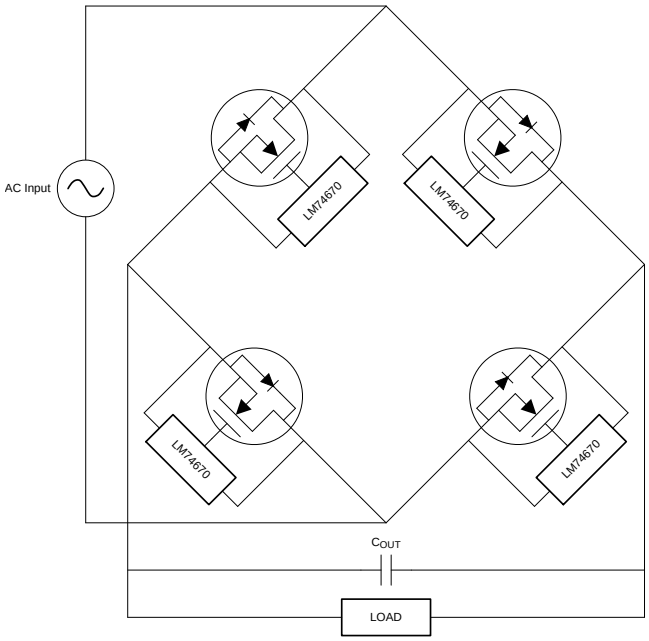


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 4
6.6 Typical Characteristics ... 6
7 Detailed Description ... 7
7.1 Overview ... 7
7.2 Functional Block Diagram ... 7
7.3 Feature Description ... 7
7.4 Device Functional Modes ... 10
8 Application and Implementation ... 12
8.1 Typical Rectifier Application ... 12
8.2 Design Requirements ... 16
9 Power Supply Recommendations ... 17
10 Layout ... 17
10.1 Layout Guidelines ... 17
10.2 Layout Example ... 18
11 Device and Documentation Support ... 19
11.1 Community Resources ... 19
11.2 Trademarks ... 19
11.3 Electrostatic Discharge Caution ... 19
11.4 Glossary ... 19
12 Mechanical, Packaging, and Orderable Information ... 19

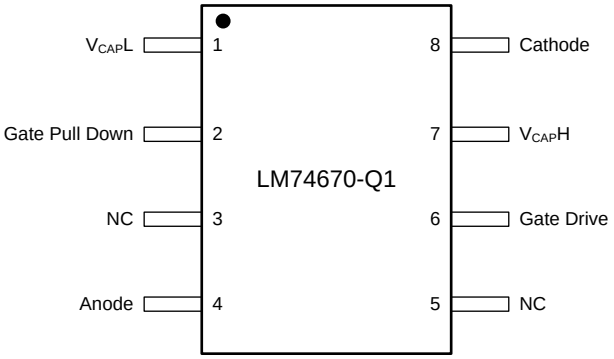
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2015) to Revision A	Page
• Product Preview to Production Data	1

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN NO.	NAME	I/O	DESCRIPTION
1	VcapL		Charge Pump Output, connect to an external charge pump capacitor
2	Gate Pull Down		Connect to the gate of the external MOSFET for fast turn OFF in the case of reverse polarity
3	NC		No connect. Leave floating or connect to Anode pin
4	Anode		Anode of the diode, connect to source of the external MOSFET
5	NC		No connect. Leave floating or connect to gate drive pin
6	Gate Drive		Gate Drive output, Connect to the Gate of the external MOSFET
7	VcapH		Charge Pump Output, connect to an external charge pump capacitor
8	Cathode		Cathode of the diode, connect to Drain of the external MOSFET

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Cathode to Anode (For a 2ms time duration) (2), (3)	-3	45	V
Cathode to Anode (Continuous)(3)	-3	42	V
VcapH to VcapL	-0.3	7	V
Anode to VcapL	-0.3	3	V
Gate Drive, Gate Pull Down to VcapL	-0.3	7	V
Ambient Temperature (TA-MAX) (4)	-40	125	°C
Case Temperature (TC-MAX)	-40	125	°C
Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 42V continuous (and 45V transients for 2ms) absmax condition from Cathode to Anode. Suitable to use with TVS SMBJ28A and SMBJ14A at the anode.
(3) Reverse voltage rating only. There is no positive voltage limitation for the LM74670-Q1 Anode terminal.
(4) The device performance is ensured over this Ambient Temperature range as long the Case Temperature does not exceed the MAX value.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per AEC Q100-002(2)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Cathode To Anode			42	V
Ambient Temperature (TA-MAX)	-40		125	°C
Case Temperature (TC-MAX)			125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM74670-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	181	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73	
$R_{\theta JB}$	Junction-to-board thermal resistance	102	
ψ_{JT}	Junction-to-top characterization parameter	11	
ψ_{JB}	Junction-to-board characterization parameter	100	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953

6.5 Electrical Characteristics

(1)T_A= 25°C unless otherwise noted. Minimum and Maximum limits are specified through test, design, validation or statistical correlation. Typical values represent the most likely parametric norm at T_A= 25°C and are provided for reference purpose

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the table of Electrical Characteristics.

Electrical Characteristics (continued)

(1) T_A= 25°C unless otherwise noted. Minimum and Maximum limits are specified through test, design, validation or statistical correlation. Typical values represent the most likely parametric norm at T_A= 25°C and are provided for reference purpose only. $V_{Anode-Cathode}$= 0.55V for all tests.

only. $V_{Anode-Cathode}$= 0.55V for all tests.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{Anode\ to\ Cathode}$	Minimum Startup Voltage across External MOSFET's Body Diode	External MOSFET V_{GS} = 0V	0.48			V
V_{cap}Threshold	Charge Pump Capacitor Drive Thresholds	Vcap Upper Threshold		6.3		V
		Vcap Lower Threshold		5.15		V
$I_{Gate\ up}$	Gate Drive Pull up current	$V_{Gate\ to\ Anode}$ = 2V	60	67		µA
$I_{Gate\ down}$	Gate Drive pull down current during forward voltage	$V_{Gate\ to\ Anode}$ = 4V	55	62		µA
$I_{Gate\ pull\ down}$	Gate drive pull down current when reverse voltage is sensed	$V_{Gate\ Pull\ Down}$ = V_{Anode} + 2V		160		mA
I_{Charge}	Charging current for the charge pump capacitor	$V_{Anode\ to\ Cathode}$ = 0.55 V	40	46		µA
$I_{Discharge}$	VCAP Current Consumption to power the controller when MOSFET is ON	V_{cap} = 6.6V		0.95		µA
$T_{Recovery}$	Time to shut off MOSFET when voltage is reversed (Equivalent to diode reverse recovery time)	$V_{Anode\ to\ Cathode}$ = -20 mV Cgate = 4 nF		2.2	5 (2)	µs
D	Duty Cycle	Iload = 3 A, T_A = 25°C		98%		
		Iload = 3 A, T_A = 125°C		92%		
I_{LKG}	Reverse Leakage Current	$V_{Anode\ to\ Cathode}$ = -13.5 V		60	110 (2)	µA
Iq	Quiescent Current to GND			0		µA
I_{Anode}	Current into Anode pin	Current into Anode pin when $V_{Anode\ -\ Cathode}$ = 0.3V.		30		µA

(2) Limit applies over the full Operating Temperature Range T_A = -40°C to +125°C.

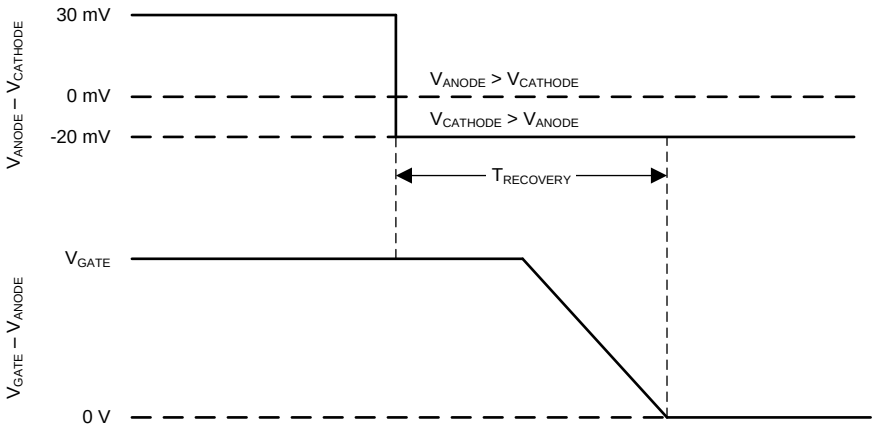


Figure 1. Gate Shut Down Timing in the Event of Reverse Polarity

6.6 Typical Characteristics

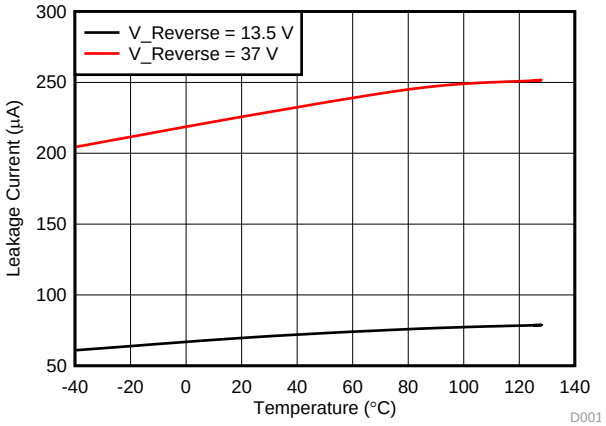


Figure 2. Reverse Leakage at Negative Voltages

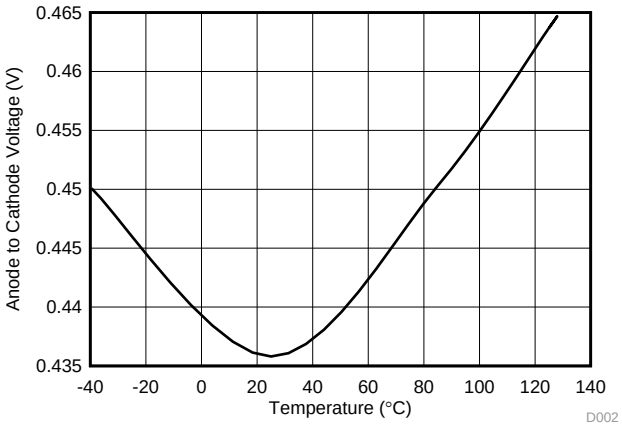


Figure 3. Anode to Cathode Startup Voltage

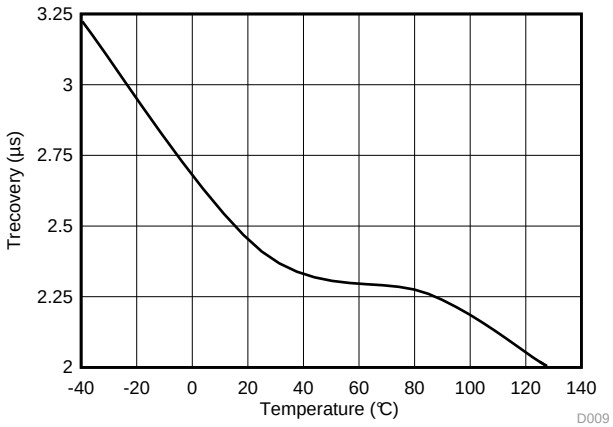


Figure 4. Reverse Recovery Time ($T_{Recovery}$)

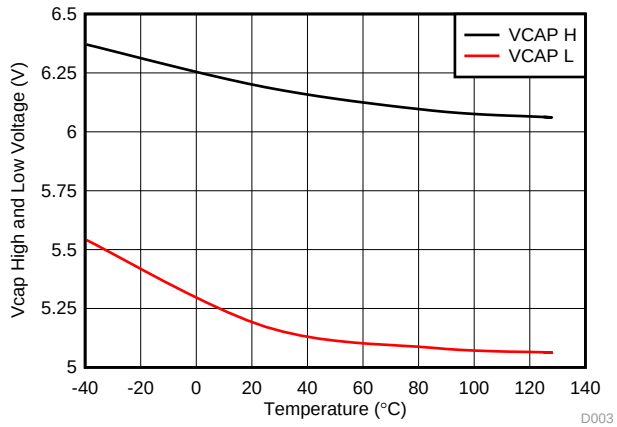


Figure 5. VcapH and VcapL Voltage Threshold

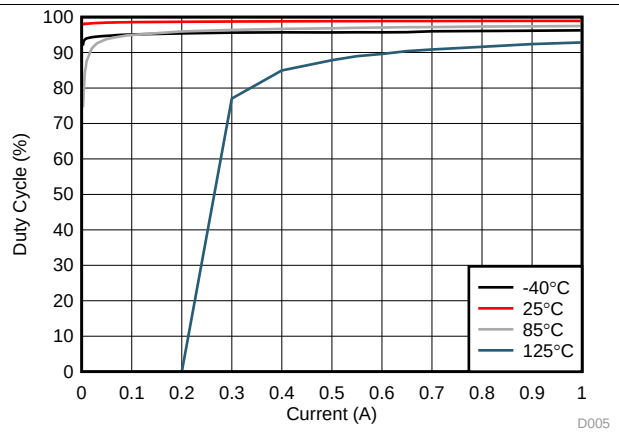


Figure 6. Duty Cycle of the Output Voltage at Startup

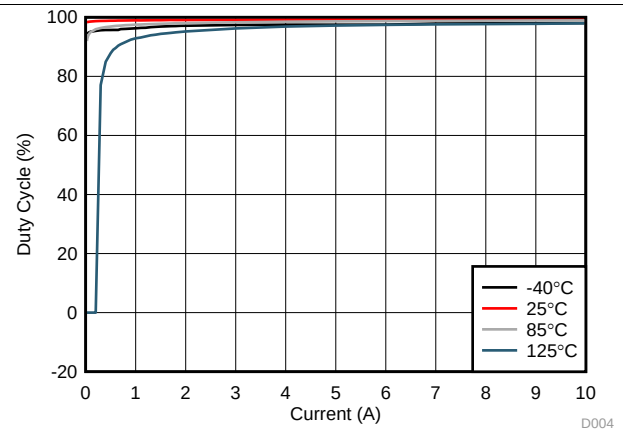


Figure 7. Duty Cycle of the Output Voltage

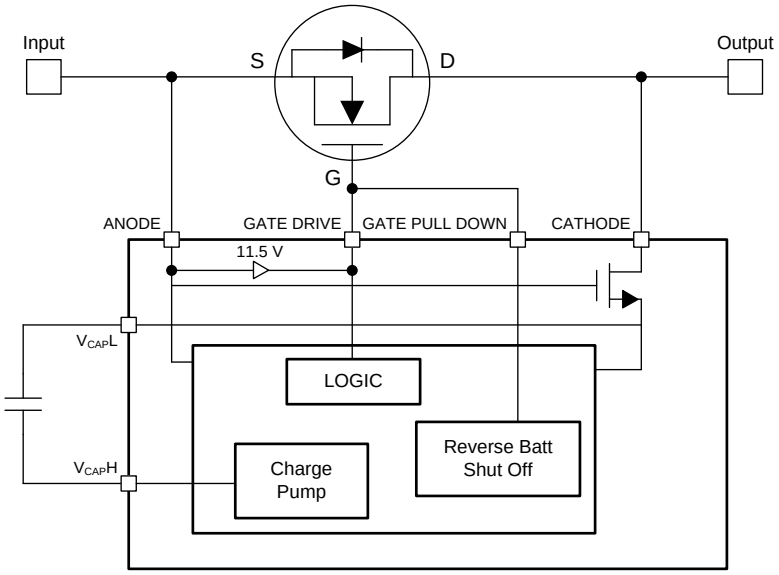
7 Detailed Description

7.1 Overview

Using N-Channel MOSFETs with controller ICs can be highly effective and more efficient substitutes of lossy diodes in a bridge rectifier application. The LM74670-Q1 is designed to control a single N-Channel MOSFET in a full or half bridge rectifier as replacement for diode. In a full bridge rectifier, each diode can be replaced by the LM74670-Q1 and a MOSFET. Diodes used in bridge rectifiers cause high power losses associated with the forward voltage drop of each diode. In each cycle of sinusoidal AC voltage, two diodes conduct at the same time. Power losses during diode forward conduction increase as the output current increases. Diode rectification also increases peak current for applications that require high value output capacitance due to charge and discharge with the diode drop voltage. The ON state forward voltage loss in a MOSFET depends upon the R_{DSON} of the MOSFET. The power losses become substantially lower than diodes for the equivalent current. This solution has a small increase in complexity; however it eliminates the need for diode heatsinks and thermal management for high power AC bridge rectifier applications.

The LM74670-Q1 is a zero Iq controller that is combined with an external N-channel MOSFET to replace each diode in a bridge rectifier. The voltage across the MOSFET source and drain is constantly monitored by the LM74670-Q1 Anode and Cathode pins. An internal charge pump is used to provide the GATE drive for the external MOSFET. The forward conduction is through the MOSFET 98% of the time. The forward conduction is through the MOSFET body diode for 2% of time when energy is stored in an external charge pump capacitor Vcap Figure 9. This stored energy is used to drive the gate of MOSFET. The voltage drop and power losses depend on the $R_{DSON}$of MOSFETs used to replace the rectifier diodes. The LM74670-Q1 has no ground reference which makes it identical to a diode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 During T0

When power is initially applied, the load current (I_D) will flow through the body diode of the MOSFET and produce a voltage drop (V_f) during T0 in Figure 8. This forward voltage drop (V_f) across the body diode of the MOSFET is used to charge up the charge pump capacitor Vcap. During this time, the charge pump capacitor Vcap is charged to a higher threshold of 6.3V (typical).

Feature Description (continued)

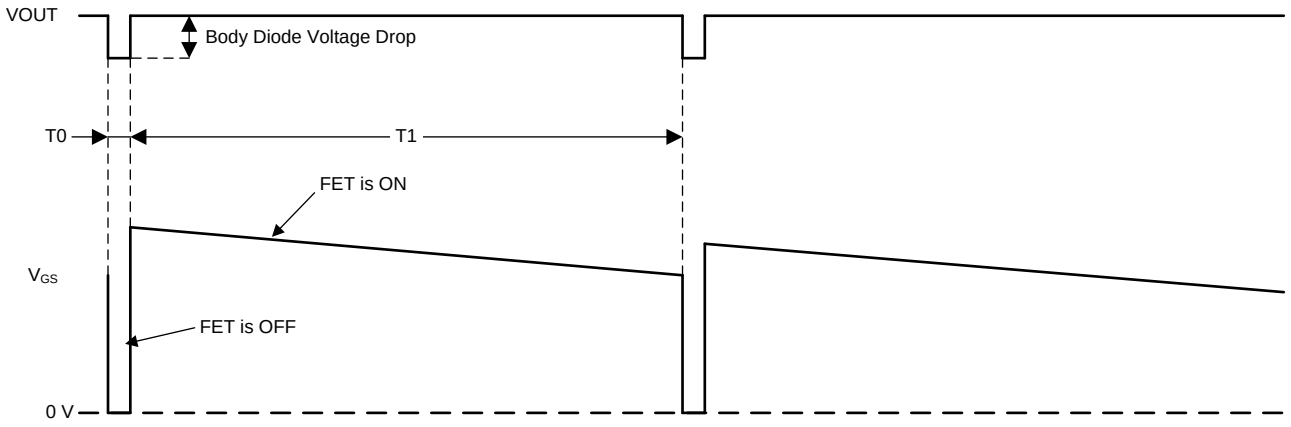


Figure 8. Output Voltage and V_{GS} Operation at 1A Output Current

7.3.2 During T1

Once the voltage on the capacitor reaches a higher voltage level of 6.3V (typical), the charge pump is disabled and the MOSFET turns ON. The energy stored in the capacitor is used to provide the gate drive for the MOSFET (T1 in Figure 8). When the MOSFET is ON, it provides a low resistive path for the drain current to flow and minimizes the power dissipation associated with forward conduction. The power losses during the MOSFET ON state depend primarily on the R_{DSON} of the selected MOSFET and load current. At time when the capacitor voltage reaches its lower threshold VcapL 5.15V (typical), the MOSFET gate turns OFF. The drain current I_D will then begin to flow through the body diode of the MOSFET, causing the MOSFET body diode voltage drop to appear across Anode and Cathode pins. The charge pump circuitry is re-activated and begins charging the Vcap. The LM74670-Q1 operation keeps the MOSFET ON at approximately 98% duty cycle (typical) regardless of the external charge pump capacitor value. This is the key factor to minimizing the power losses. The forward voltage drop during this time is limited by the R_{DSON} of the MOSFET.

7.3.3 Pin Operation

7.3.3.1 Anode and Cathode Pins

The LM74670-Q1 Anode and Cathode pins are connected to the source and drain of the external MOSFET. The current into the Anode pin is 30 µA (typical). When power is initially applied, the load current flows through the body diode of the external MOSFET, the voltage across Anode and Cathode pins is equal to the forward diode drop . The minimum value of diode voltage drop required to enable the charge pump circuitry is 0.48V. Once the MOSFET is turned ON, the Anode and Cathode pins constantly sense the voltage difference across the MOSFET to determine the magnitude and polarity of the voltage across it. When the MOSFET is on, the voltage difference across Anode and Cathode pins depends on the R_{DSON} and load current. If voltage difference across source and drain of the external MOSFET becomes negative, this is sensed as a fault condition by Anode and Cathode pins and gate is turned off by Gate Pull Down pin as shown in Figure 1. The reverse voltage threshold across Anode and Cathode to detect the fault condition is -20 mV. The consistent sensing of voltage polarity across the MOSFET enables the LM74670-Q1 to provide a fast response to the power source failure and limit the amount and duration of the reverse current flow.

7.3.3.2 VcapH and VcapL Pins

VcapH and VcapL are high and low voltage thresholds respectively that the LM74670-Q1 uses to detect when to turn the charge pump circuitry ON and OFF. The capacitor charging and discharging time can be correlated to the duty cycle of the MOSFET gate. Figure 9 shows the voltage behavior across the Vcap. During the time period T0, the capacitor is storing energy from the charge pump. The MOSFET is turned off and current flow is only through the body diode during this time period. The conduction though body diode of the MOSFET is for a

Feature Description (continued)

very small period of time (2% typical) which rules out the chances of overheating the MOSFET, regardless of the output current. Once the capacitor voltage reaches its high threshold, the MOSFET is turned off and charge pump circuity is deactivated until the Vcap reaches its low voltage threshold (T1). The voltage difference between Vcap high and low threshold is typically 1.15V. The LM74670-Q1 charge pump has 46µA charging capability with 5-8MHz frequency.

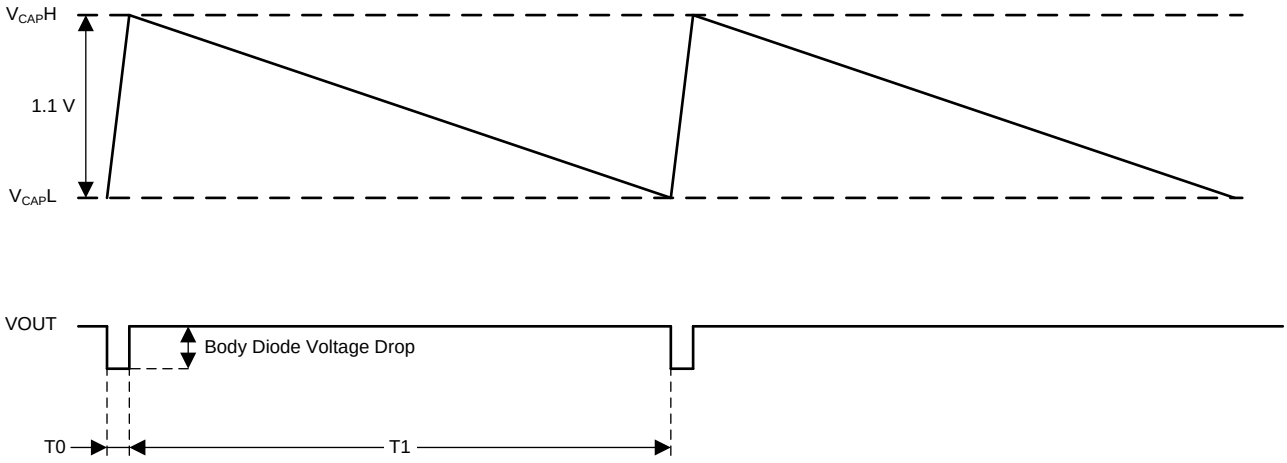


Figure 9. Vcap Charging and Discarding by the Charge Pump

The Vcap current consumption is 0.95µA (typical) to drive the gate. The MOSFET OFF time (T0) and ON time (T1) can be calculated using the following expression

$$\Delta T = C\frac{dV}{dI} \quad (1)$$

Where:

- C = Vcap Capacitance
- dV = 1.15V
- dI = 46 µA for charging
- dI = 0.95 µA for discharging

Note: Temperature dependence of these parameters – The duty cycle is dependent on temperature since the capacitance variation over temperature has a direct correlation to the MOSFET OFF and ON periods and the frequency. If the capacitor varies 20% the periods and the frequency will also vary by 20% so it is recommended to use a quality X7R/COG cap and not to place the cap in close proximity to high temperature devices. The variation of the capacitor does not have a thermal impact in the application as the duty cycle does not change.

7.3.3.3 Gate Drive Pin

When the charge pump capacitor is charged to the high voltage level of 6.3V (typ), the Gate Drive pin provides a 67µA (typ) of drive current. When the charge pump capacitor reaches its lower voltage threshold of 5.15V (typ), Gate is pulled down to the Anode voltage (Vin). During the positive cycle of AC sinusoid, the MOSFET gate is turned ON by the LM74670-Q1 gate drive to ensure the forward conduction through the MOSFET.

7.3.3.4 Gate Pull Down Pin

The Gate Pull Down pin of the LM74670-Q1 is connected to the Gate Drive pin in a bridge rectifier application. When the controller detects negative polarity during the negative cycle of AC sinusoidal, the Pull-Down quickly discharges the MOSFET gate through a discharge transistor. This fast pull down reacts regardless of the Vcap charge level. When the negative voltage across the Anode and Cathode pins due to reverse current reaches -20mV (typical), the LM74670-Q1 immediately reacts and discharges the MOSFET gate capacitance as shown in Figure 10 . The Gate voltage is pulled down to Anode voltage with 160mA pull down current when the negative

Feature Description (continued)

cycle of the AC input starts. . A MOSFET with 4nF of effective gate capacitance can be turned off by the LM74670-Q1 within 2.2µs (typical). The fast turnoff time minimizes the reverse current flow from MOSFET drain by opening the circuit. The reverse leakage current does not exceed 110µA for a constant 13.5V reverse voltage across Anode and Cathode pins. The reverse leakage current for a Schottky diode is 15mA under the same voltage and temperature conditions.

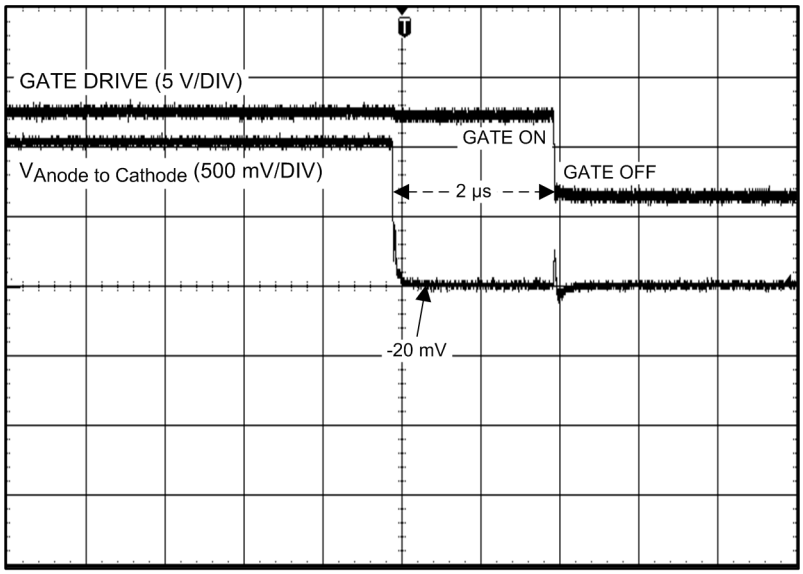


Figure 10. Gate Pull Down in the Event of Reverse Polarity

7.4 Device Functional Modes

The LM74670-Q1 operates in two modes:

- **Body Diode Conduction Mode**

  The LM74670-Q1 solution works like a conventional diode during this time with higher forward voltage drop. The power dissipation during this time can be given as:

$$P_{Dissipation} = \left(V_{Forward\,Drop}\right) \times \left(I_{Drain\,Current}\right) \quad (2)$$

  However, the current only flows through the body diode while the MOSFET gate is being charged to $V_{GS(TH)}$. This conduction is only for 2% duty cycle, therefore it does not cause any thermal issues.

$$\text{Body Diode ON Time} = \frac{C \times (VcapH - VcapL)}{I_{Charge\,Current}} \quad (3)$$

- **The MOSFET Conduction Mode**

  The MOSFET is turned on during this time and current flow is only through the MOSFET. The forward voltage drop and power losses are limited by the R_{DSON} of the specific MOSFET used in the solution. The LM74670-Q1 solution output is comprised of the MOSFET conduction mode for 98% of its duty cycle. This time period is given by the following expression:

$$\text{MOSFET ON Time} = \frac{C \times (VcapH - VcapL)}{I_{Discharge\,Current}} \quad (4)$$

Device Functional Modes (continued)

7.4.1 Duty Cycle Calculation

The LM74670-Q1 has an operating duty cycle of 98% at 25 ℃ and >90% at 125 ℃. The duty cycle doesn't depend on the Vcap capacitance value. However, the variation in capacitance value over temperature has direct correlation to the switching frequency between the MOSFET and body diode. If the capacitance value decreases, the charging and discharging time will also decrease, causing more frequent switching between body diode and the MOSFET condition. The following expression can be used to calculate the duty cycle of the LM74670-Q1:

$$\text{Duty Cycle (\%)} = \frac{\text{(MOSFET ON Time)}}{\text{(MOSFET ON Time} + \text{Body Diode ON Time)}} \times 100 \quad (5)$$

7.4.2 Startup Voltage

The LM74670-Q1 will not initiate the charge pump operation if a closed loop system is in standby mode or the drain current is smaller than 1mA (typical). This is due to a minimum body diode voltage requirement of the LM74670-Q1 controller. If the drain current is too small to produce a minimum voltage drop of 0.48V at 25℃, the charge pump circuitry will remain off and the MOSFET will act just like a diode. It is very important to know the body diode voltage parameter of a MOSFET before implementing it into the Smart Diode solution. Some N-channels MOSFETs have very low body diode voltage at higher temperature. This makes their drain current requirement higher to achieve 0.48V across the body diode in order to initiate the LM74670-Q1 controller at higher temperatures.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Rectifier Application

The LM74670-Q1 can be used with appropriate N-channel MOSFET to replace a diode in a typical rectifier application. The rectifier could be industrial for a 12/24AC supply or an automotive rectifier for a single phase or three phase field winding controlled alternator. The schematic for a typical implementation is shown in Figure 11 to implement a full bridge rectifier. The same schematic can also be extended to six legs for a three phase alternator rectification. Following considerations need to be made when selecting the appropriate MOSFET for this application:

1. An input voltage of 24V AC can reach a 34V peak. The MOSFET selected should have a V_{DS} greater than this voltage.
2. The Continuous drain current of the MOSFET should be nearly 2.5X I_{AVG} to cover peak currents during rectification.
3. The $V_{GS(TH)}$ threshold voltage of the selected MOSFET should be ≤3V to ensure error-free operation.

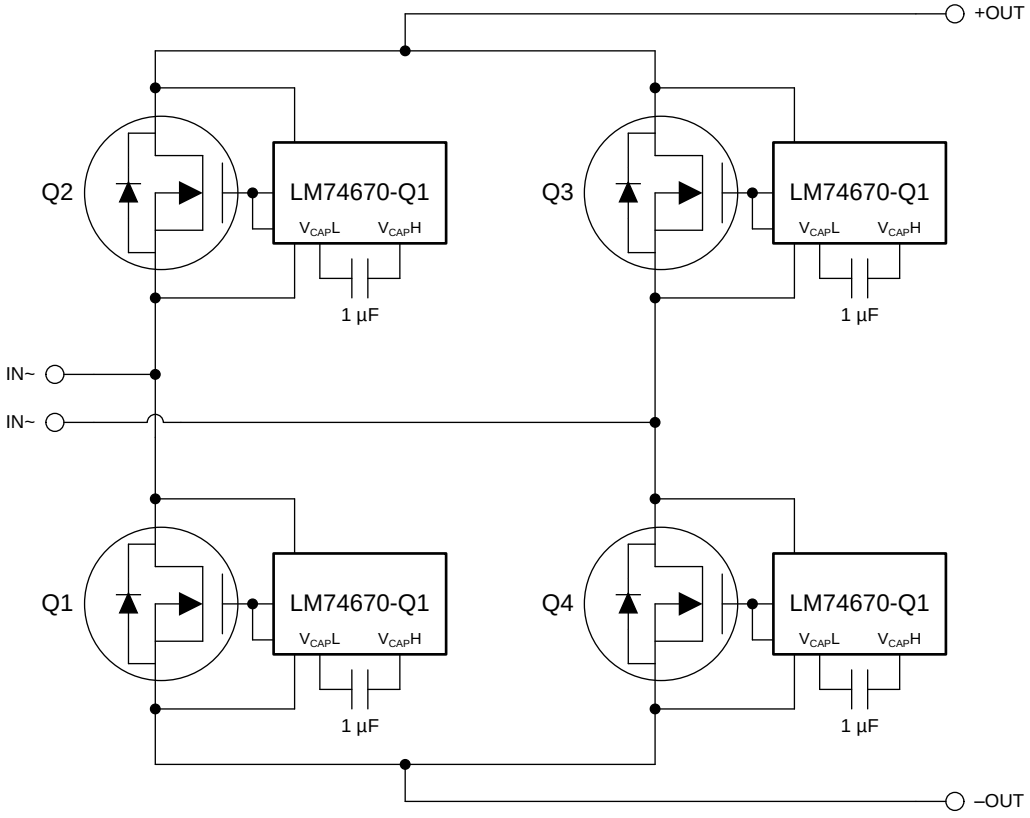


Figure 11. Typical Full Bridge Rectifier Application

Typical Rectifier Application (continued)

8.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	4 – 42V peak AC
Output Voltage	rectified positive amplitude
Output current range	Maximum Drain current of MOSFET
Threshold voltage of FET $V_{GS(TH)}$	3V Max
Vcap value	1µF

8.1.2 Detailed Design Procedure

To begin the design process, determine the following:

8.1.2.1 Design Considerations

- Input voltage range
- Output current range
- Body Diode forward voltage drop for the selected MOSFET
- MOSFET Gate threshold voltage

8.1.2.2 Capacitor Selection

A ceramic capacitor should be placed between VcapL and VcapH. The capacitor acts as a holding tank to power up the control circuitry when the MOSFET is on.

When the MOSFET is off, this capacitor is charged up to higher voltage threshold of ~6.3V. Once this voltage is reached, the Gate Drive of LM74670-Q1 will provide drive for the external MOSFET. When the MOSFET is ON, the voltage across its body diode is collapsed because the forward conduction is through the MOSFET. During this time, the capacitor acts as a supply for the Gate Drive to keep the MOSFET ON.

The capacitor voltage will gradually decay when the MOSFET is ON. Once the capacitor voltage reaches a lower voltage threshold of 5.15V, the MOSFET is turned off and the capacitor gets recharged again for the next cycle.

A capacitor value of 220nF to 2.2uF with X7R/COG characteristic and 16V rating or higher is recommended for this application. A higher value capacitor sets longer MOSFET ON time and OFF time; however, the duty cycle remains at ~98% for MOSFET ON time irrespective of capacitor value.

If the Vcap value is 1µF, the MOSFET ON time and OFF time can be calculated using Equation 1 :

MOSFET ON Time = (1µF x 1.15V)/0.95µA = 1.21 seconds (6)

Body Diode ON Time = (1µF x 1.15V)/46µA = 25 miliseconds (7)

The duty cycle can be calculated using Equation 5 :

Duty Cycle % = 1.21 sec / (1.21 sec + 0.025sec) = 98% (8)

8.1.2.3 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$ and the drain-to-source On resistance R_{DSON}. The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows for a small period while the MOSFET gate is being charged to $V_{GS(TH)}$.The LM74670-Q1 can provide up to 5V V_{GS} to drive the external MOSFET, therefore the V_{GS} threshold of the selected MOSFET must be ≤ 3V.

The voltage across the MOSFET's body diode must be higher than 0.48V at low current. The body diode voltage for MOFETS typically decreases as the ambient temperature increases. This will increase the source current requirement to achieve the minimum body diode drain-to-source voltage for the charge pump to initiate. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. Although there are no positive V_{DS} limitation. However, it is recommended to use MOSFETS with voltage rating up to 45V for automotive applications, since the LM74670-Q1 has a reverse voltage limit of -45V. Table 2 shows the examples of recommended MOSFETs to be used with the LM74670-Q1.

8.1.3 Application Curves

In the following plots, the input voltage is 20V AC. The output current is 5A for all frequencies.

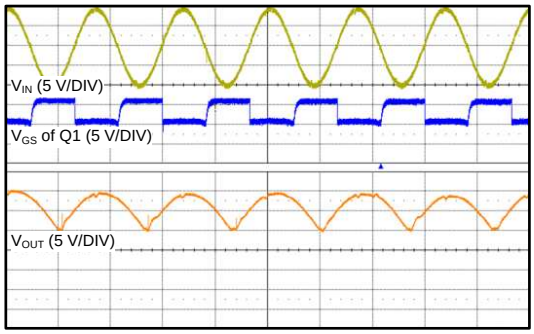


Figure 12. Response to 60Hz AC Input

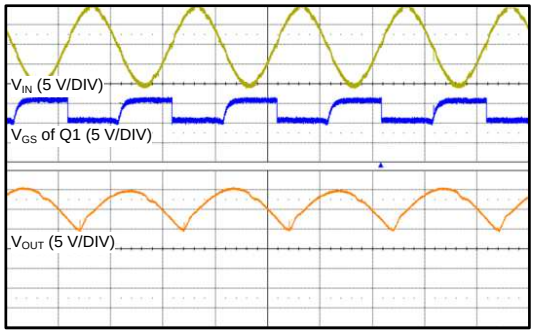


Figure 13. Response to 100Hz AC Input

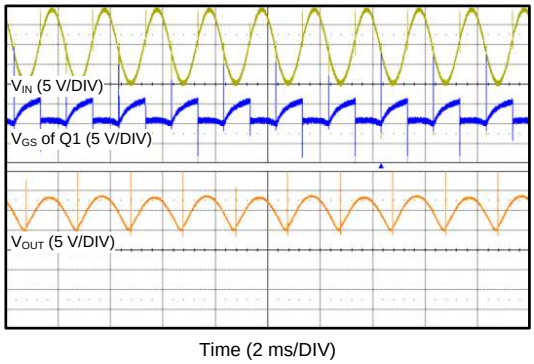


Figure 14. Response to a 300Hz AC Input

8.2 Design Requirements

NOTE

Startup voltage is the voltage drop is needed for the controller to turn ON. It directly influences the Minimum output current at which the MOSFET turns ON.

Table 2. Recommended MOSFET Examples(1)

Part No	Voltage (V) Current	Drain Current at 25C	Rdson mΩ @ 4.5V	Vgs Threshold (V)	Diode Voltage @ 2A at 125C/175C	Package; Footprint	Qual
CSD17313Q2Q1	30	5	26	1.8	0.65	SON; 2 x 2	Auto
SQJ886EP	40	60	5.5	2.5	0.5	PowerPAK SO-8L; 5 x 6	Auto
SQ4184EY	40	29	5.6	2.5	0.5	SO-8; 5 x 6	Auto
Si4122DY	40	23.5	6	2.5	0.5	SO-8; 5 x 6	Auto
RS1G120MN	40	12	20.7	2.5	0.6	HSOP8; 5 x 6	Auto
RS1G300GN	40	30	2.5	2.5	0.5	HSOP8; 5 x 6	Auto
CSD18501Q5A	40	22	3.3	2.3	0.53	SON; 5 x 6	Industrial
SQD40N06-14L	60	40	17	2.5	0.5	TO-252; 6 x 10	Auto
SQ4850EY	60	12	31	2.5	0.55	SO-8; 5 x 6	Auto
CSD18532Q5B	60	23	3.3	2.2	0.53	SON;5 x 6	Industrial
IPG20N04S4L-07A	40	20	7.2	2.2	0.48	PG-TDSON-8-10; 5 x 6	Auto
IPB057N06N	60	45	5.7	3.3	0.55	PG-TO263-3; 10 x 15	Auto
IPD50N04S4L	40	50	7.3	2.2	0.50	PG-TO252-3-313; 6 x10	Auto
BUK9Y3R5-40E	40	100	3.8	2.1	0.48	LFPAK56; Power-SO8 (SOT669); 5 x 6	Auto
IRF7478PbF-1	60	7	30	3	0.55	SO-8; 5 x 6	Industrial
SQJ422EP	40	75	4.3	2.5	0.50	PowerPAK SO-8L; 5 x 6	Auto
IRL1004	40	130	6.5	1	0.60	TO-220AB	Auto
AUIRL7736	40	112	2.2	3	0.65	DirectFET®; 5 x 6	Auto

(1) The LM74670-Q1 solution is not limited to the MOSFETs included in this table. It only shows examples of compatible MOSFETs.

9 Power Supply Recommendations

While testing the LM74670-Q1 solution, it is important to use low impedance power supply which allows current sinking. If the power supply does not allow current sinking, it would prevent the current flow in the reverse direction in the event of reverse polarity. The MOSFET gate won't get pulled down immediately due to the absence of reverse current flow.

10 Layout

10.1 Layout Guidelines

- The VIN terminal is recommended to have a low-ESR ceramic bypass-capacitor. The typical recommended bypass capacitance is a 10-μF ceramic capacitor with a X5R or X7R dielectric.
- The VIN terminal must be tied to the source of the MOSFET using a thick trace or polygon.
- The Anode pin of the LM74670-Q1 is connected to the Source of the MOSFET for sensing.
- The Cathode pin of the LM74670-Q1 is connected to the drain of the MOSFET for sensing.
- The high current path of for this solution is through the MOSFET, therefor it is important to use thick traces for source and drain of the MOSFET.
- The charge pump capacitor Vcap must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate Drive and Gate pull down pins of the LM74670-Q1 must be connected to the MOSFET gate without using vias.
- Obtaining acceptable performance with alternate layout schemes is possible, however this layout has been shown to produce good results and is intended as a guideline.

10.2 Layout Example

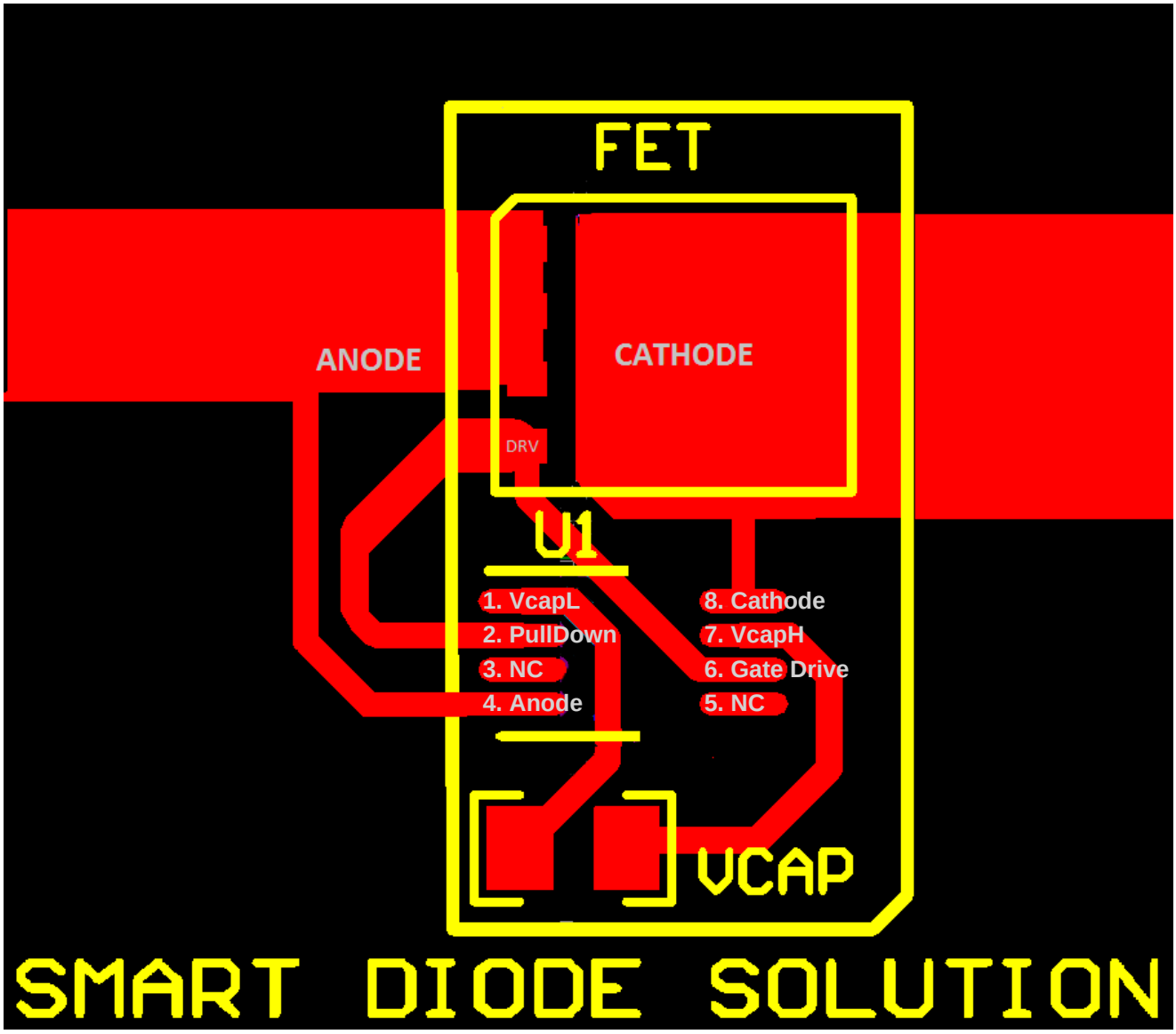


Figure 15. Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74670QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGPK	Samples
LM74670QDGKTQ1	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGPK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

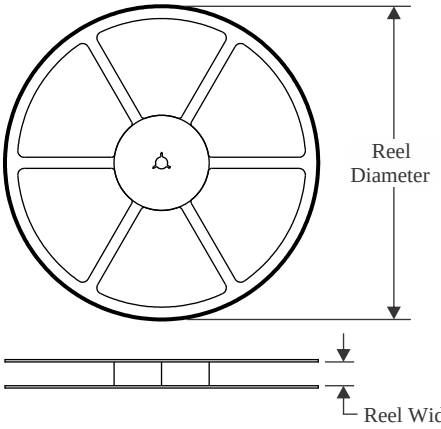
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

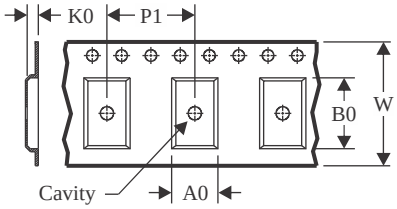
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

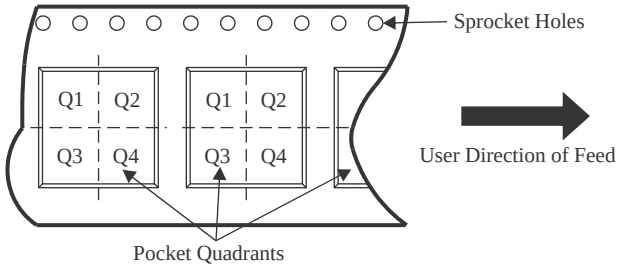


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

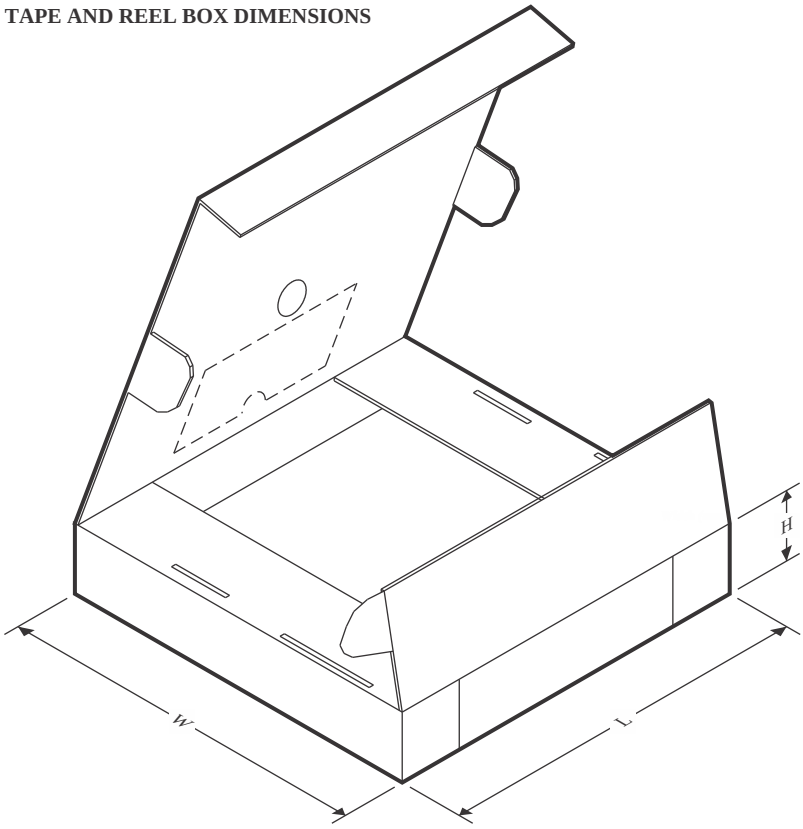
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74670QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM74670QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM74670QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM74670QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

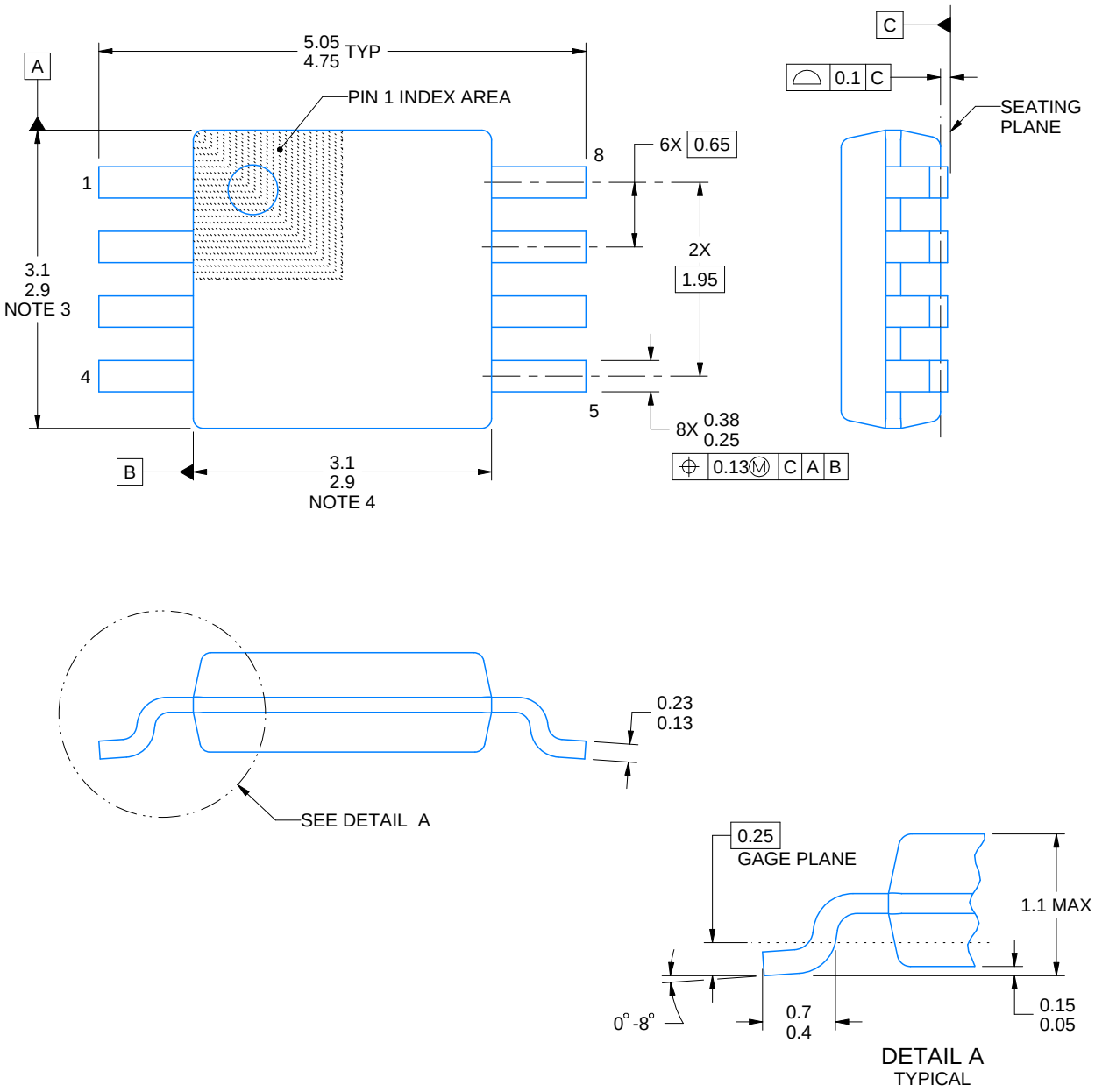
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74670QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
LM74670QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM74670QDGKTQ1	VSSOP	DGK	8	250	366.0	364.0	50.0
LM74670QDGKTQ1	VSSOP	DGK	8	250	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

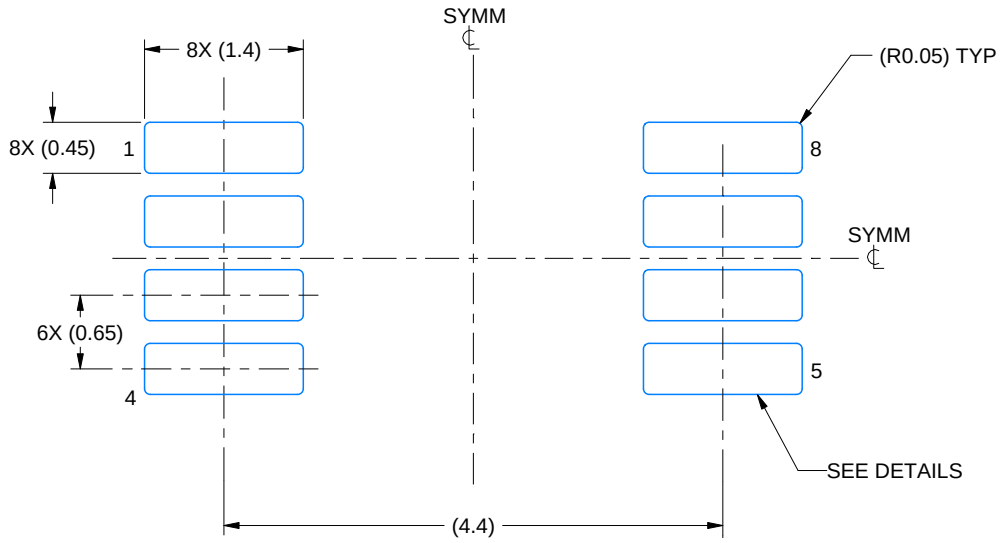
SMALL OUTLINE PACKAGE



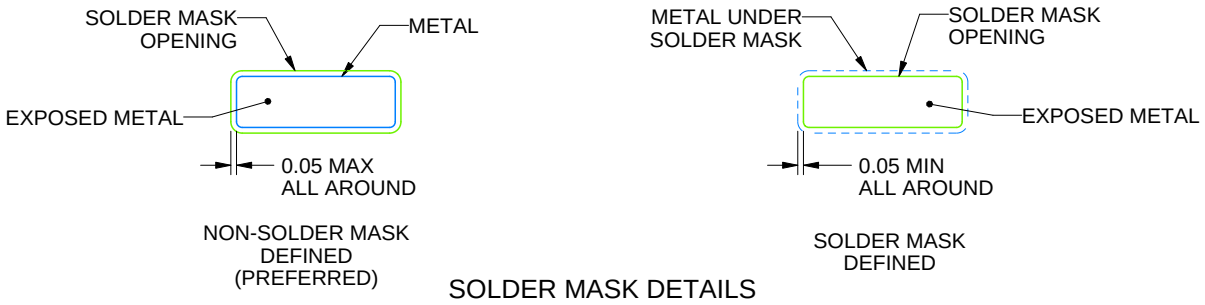
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

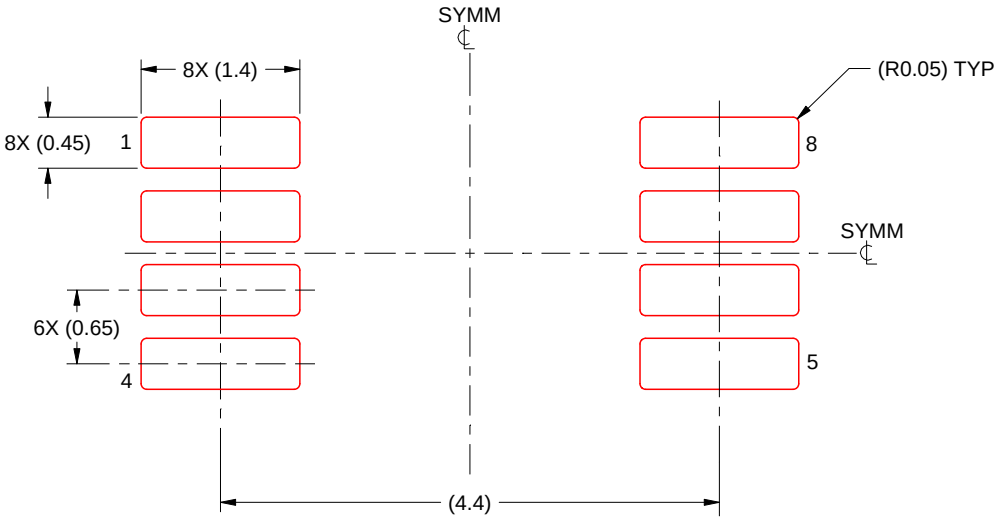


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265