

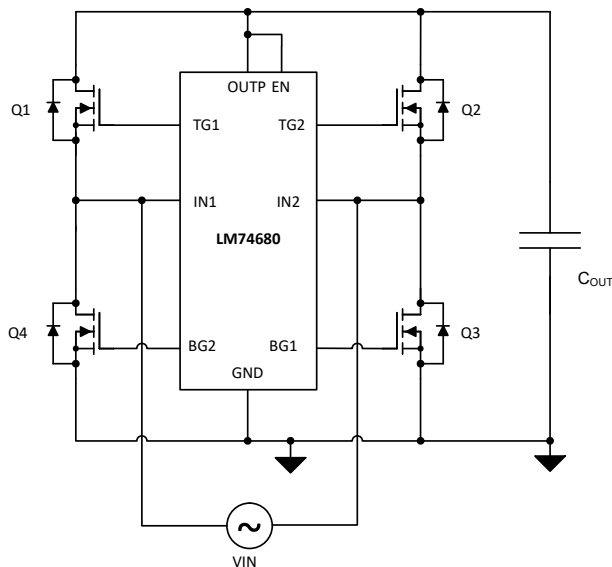
LM74680 Ideal Diode Bridge Controller for Low Loss Rectification

1 Features

- Input operating voltage range: 5V to 80V
 - 100V absolute maximum
- 4× integrated gate drive control
- 165µA gate pull-up strength
- 100mA gate pull-down strength
- Linear gate regulation control for supply ORing applications
 - $V_{TG_REG} = 11mV$
- Enable pin for user-controlled device on/off function
- $-40^{\circ}C$ to $125^{\circ}C$ operating junction temperature range
- Small footprint: 3mm × 3mm VQFN-12
 - Meets IPC-9592 spacing rules

2 Applications

- [Video door bell](#)
- [IP cameras](#)
- [Thermostat](#)
- [Power distribution systems \(24Vac\)](#)
- Polarity agnostic power inputs



Typical Application Schematic

3 Description

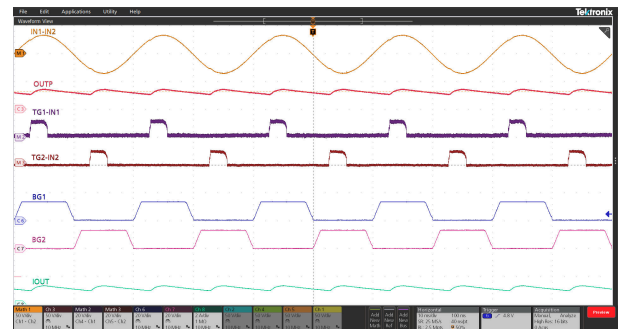
The LM74680 is an ideal diode bridge controller that provides voltage rectification by driving four N-channel MOSFETs in a full-bridge configuration. LM74680 enables lower voltage drop and reduced power dissipation as compared to conventional diode bridge rectifiers. This helps to simplify the power supply design, eliminate heat sinks, and reduce PCB area. The integrated charge pump allows use of N-channel MOSFETs, which are smaller and more cost-effective than P-channel MOSFETs for the same power level. It also offers fast response to reverse current conditions for protection against input short events. The LM74680 has an enable pin which allows for the gate driver to be either enabled or disabled by an external signal. The LM74680 supports voltage rectification from DC to 1kHz.

This device is characterized for operation over a junction temperature range of $-40^{\circ}C$ to $+125^{\circ}C$.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ |
|-------------|------------------------|-----------------------------|
| LM74680 | DRR (WSON, 12) | 3mm × 3mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



24V AC Input, $C_{OUT} = 1mF$, 30W Load, Steady State



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4 Pin Configuration and Functions

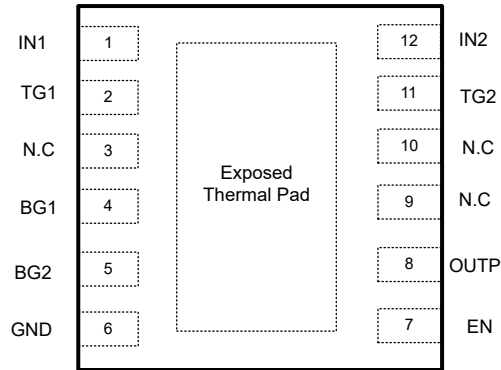


Figure 4-1. DRR Package, 12-Pin WSON (Top View)

Table 4-1. Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-----|------|--------------------|--|
| NO. | NAME | | |
| 1 | IN1 | I | Bridge rectifier input 1. Connect to top side MOSFET Q1 source and bottom side MOSFET Q4 drain. |
| 2 | TG1 | O | Top side MOSFET gate drive 1. |
| 3 | N.C | — | No connection. |
| 4 | BG1 | O | Bottom side MOSFET gate drive 1. |
| 5 | BG2 | O | Bottom side MOSFET gate drive 2. |
| 6 | GND | G | Device ground. Connect to bottom side MOSFETs Q3 and Q4 source and output ground. |
| 7 | EN | I | Enable pin. Can be connected to OUTP for always ON operation |
| 8 | OUTP | I | Bridge rectifier output. Connect to top side MOSFETs Q1 and Q2 drain. Connect a minimum of 0.1µF between OUTP and GND close to the IC. |
| 9 | N.C | — | No connection. |
| 10 | N.C | — | No connection. |
| 11 | TG2 | O | Top side MOSFET gate drive 2. |
| 12 | IN2 | I | Bridge rectifier input 2. Connect to top side MOSFET Q2 source and bottom side MOSFET Q3 drain. |

(1) I = input, O = output, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---|---------------------------|------|--------|------|
| Input Pins | OUTP to GND | -0.3 | 100 | V |
| | IN1, IN2 to GND | -2 | OUTP+2 | |
| | EN to GND | -0.3 | OUTP | |
| | IN1-IN2 | -100 | 100 | |
| Output Pins | BG1, BG2 to GND | -0.3 | 15 | V |
| | TG1 to IN1 and TG2 to IN2 | -0.3 | 15 | |
| Operating junction temperature ⁽²⁾ | | -40 | 150 | °C |
| Storage temperature, T _{stg} | | -40 | 150 | °C |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JS-002 ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|--|---|-----|-----|------|------|
| Input Pins | OUTP to GND | 5 | | 80 | V |
| | EN to GND | 0 | | OUTP | |
| Input to Output pins | OUTP to INx | -80 | | | V |
| External MOSFET max V _{GS} rating | GATE to SOURCE | 15 | | | V |
| T _J | Operating junction temperature range ⁽²⁾ | -40 | | 150 | °C |

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see [Section 5.5](#).
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LM74680 | UNIT |
|-------------------------------|--|------------|------|
| | | DRR (WSON) | |
| | | 12 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 60.9 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 48 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 31.5 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 1.2 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 31.4 | °C/W |

5.4 Thermal Information (continued)

| THERMAL METRIC ⁽¹⁾ | | LM74680 | UNIT |
|-------------------------------|--|------------|------|
| | | DRR (WSON) | |
| | | 12 PINS | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 7.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $\text{OUTP} = 24\text{ V}$, $V_{EN} = \text{OUTP}$, $C_{OUT} = 1\ \mu\text{F}$ over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|---|-------|------|-------|---------------|
| SUPPLY VOLTAGE | | | | | | |
| V_{OUTP} | OUTP voltage range | | 5 | | 80 | V |
| V_{OUTP_PORR} | OUTP POR rising threshold | | 3.72 | 4.3 | 4.8 | V |
| V_{OUTP_PORF} | OUTP POR falling threshold | | 3.4 | 4.0 | 4.5 | V |
| $V_{OUTP_POR_Hys}$ | OUTP POR Hysteresis | | | 0.3 | | V |
| I_Q | Operating Quiescent Current | $\text{OUTP} = 24\text{ V}$ | | 270 | 450 | μA |
| I_{SHDN} | Shutdown Supply Current | $V_{EN} = 0\text{ V}$ | | 0.27 | 3.82 | μA |
| I_{INx} | Input pin current | $V_{INx} - V_{OUTP} = 30\text{ mV}$ | | 10 | 16 | μA |
| ENABLE INPUT | | | | | | |
| V_{EN_IL} | Enable input low threshold | | 0.413 | 0.7 | 0.96 | V |
| V_{EN_IH} | Enable input high threshold | | 0.631 | 0.9 | 1.15 | |
| V_{EN_Hys} | Enable Hysteresis | | 0.134 | 0.2 | 0.265 | V |
| I_{EN} | Enable sink current | $V_{EN} = 48\text{ V}$ | | 72 | 241 | nA |
| V_{IN} to V_{OUTP} | | | | | | |
| V_{FWD} | Reverse to forward turn ON threshold | | 169 | 195 | 226 | mV |
| V_{REV} | Threshold for reverse current blocking | | -17 | -11 | -5 | mV |
| V_{TG_REG} | Top side gate regulation voltage | | 7 | 11 | 16 | mV |
| $V_{TG_REG_SINK}$ | Top side regulation sink current | | 5 | 10 | 16 | μA |
| V_{TG_FC} | Full conduction threshold | | | 56 | | mV |
| GATE DRIVE | | | | | | |
| $V_{TGx} - V_{INx}$ | Top Gate Drive Voltage | | 8.7 | 10 | 11.1 | V |
| $V_{BGx} - V_{GND}$ | Bottom Gate Drive Voltage | | 11.96 | 13 | 13.85 | V |
| I_{TGx} | Peak source current | $V_{INx} - V_{GND} = 100\text{ mV}$, $V_{TGx} - V_{INx} = 5\text{ V}$ | 124 | 165 | 210 | μA |
| | Peak sink current | $V_{INx} - V_{GND} = -50\text{ mV}$, $V_{TGx} - V_{INx} = 5\text{ V}$ | | 100 | | mA |
| I_{BGx} | Peak source current | $V_{BGx} - V_{GND} = 5\text{ V}$ | 1.8 | 2.5 | 3.5 | mA |
| | Peak sink current | $V_{BGx} - V_{GND} = 5\text{ V}$ | | 80 | | mA |

5.6 Switching Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $\text{OUTP} = 24\text{ V}$, $V_{EN} = \text{OUTP}$, $C_{OUT} = 1\ \mu\text{F}$ over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|---|-----------------|-----|-----|-----|---------------|
| EN_{TDLY} | Enable (low to high) to TGx Turn On delay | | | 175 | 300 | μs |
| EN_{TDLY} | Enable (low to high) to BGx Turn On delay | | | 6.5 | 11 | μs |

5.6 Switching Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $\text{OUTP} = 24\text{ V}$, $V_{\text{EN}} = \text{OUTP}$, $C_{\text{OUT}}: 1\mu\text{F}$ over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---|--|-----|-----|-----|---------------|
| $t_{\text{Reverse Delay}}$ | Reverse voltage detection to TGx Turn Off delay | $V_{(\text{IN})} - V_{(\text{OUTP})} = 100\text{ mV to } -100\text{ mV}$ | | 2 | 3.5 | μs |
| $t_{\text{Forward Recovery}}$ | Forward voltage detection to TGx Turn On delay | $V_{(\text{IN})} - V_{(\text{OUTP})} = -100\text{ mV to } 700\text{ mV}$ | | 5 | 9.1 | μs |

5.7 Typical Characteristics

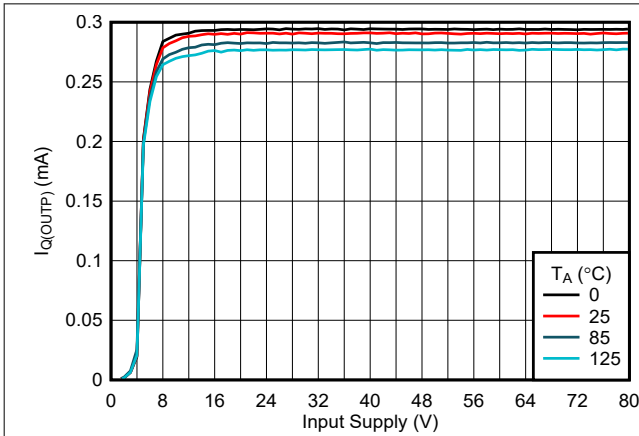


Figure 5-1. I_Q vs Supply Voltage

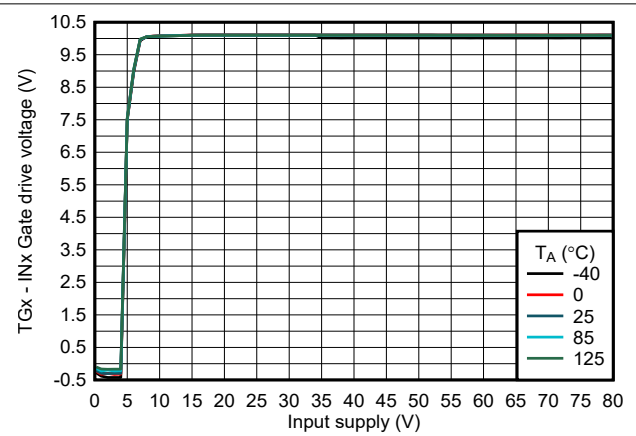


Figure 5-2. Top Side Gate Drive Voltage vs Supply Voltage

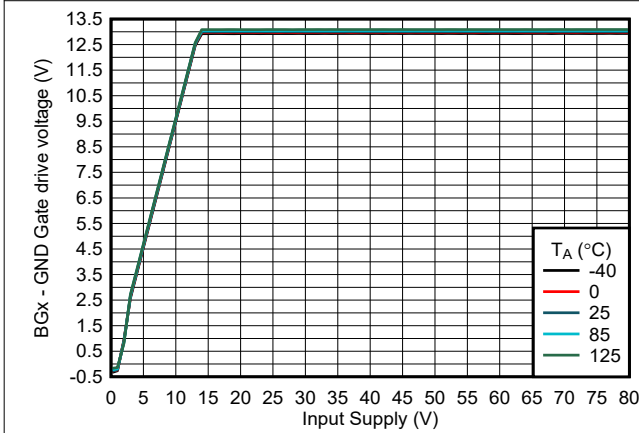


Figure 5-3. Bottom Side Gate Drive Voltage vs Supply Voltage

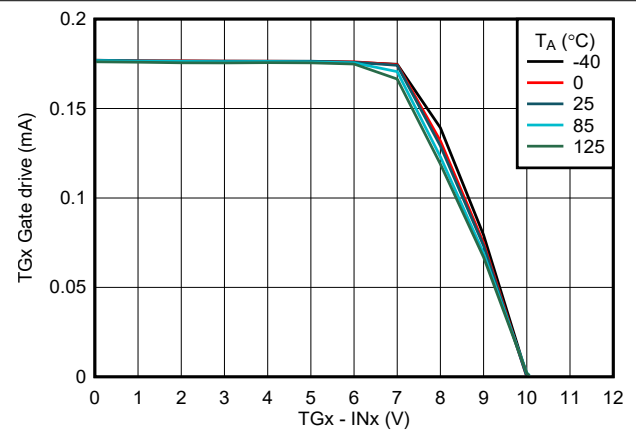


Figure 5-4. Top Side Gate Drive Source Current vs Gate Drive Voltage

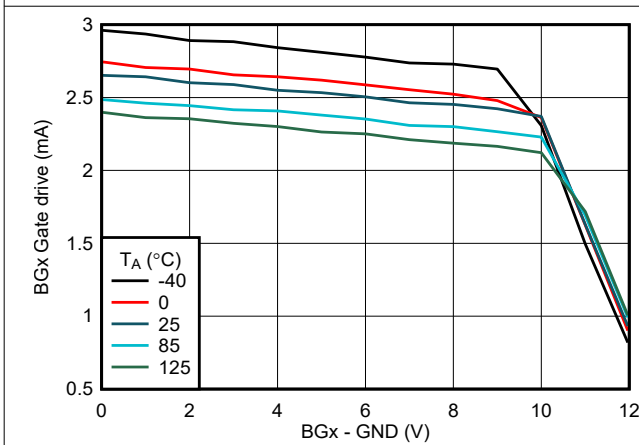


Figure 5-5. Bottom Side Gate Drive Source Current vs Gate Drive Voltage

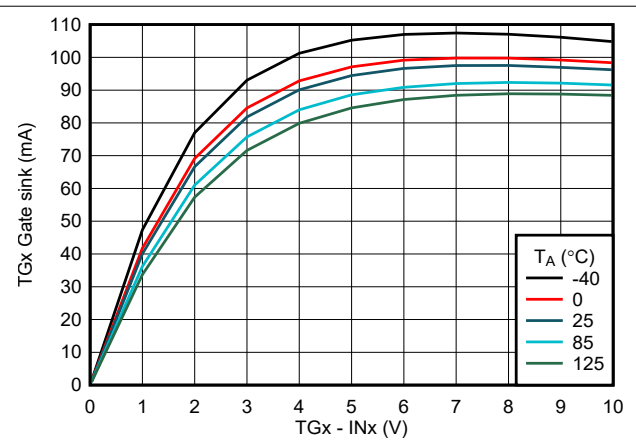
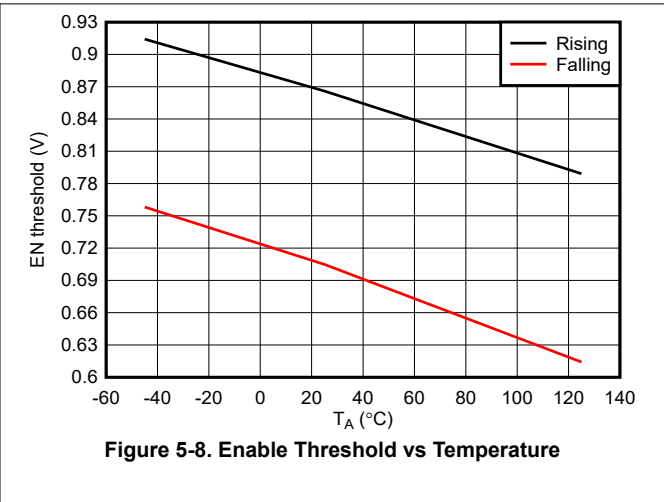
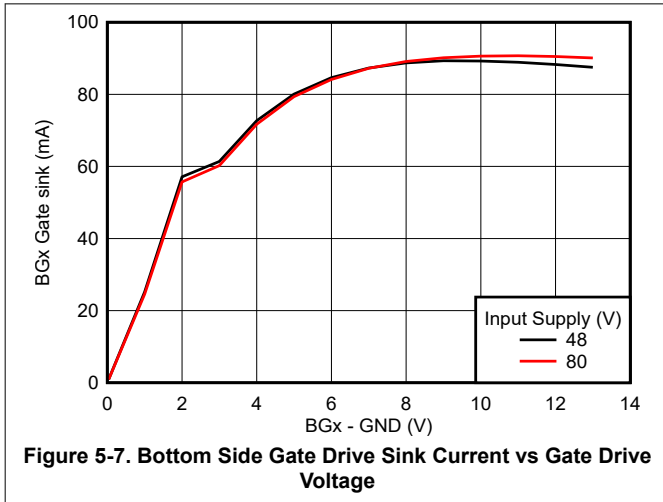


Figure 5-6. Top Side Gate Drive Sink Current vs Gate Drive Voltage

5.7 Typical Characteristics (continued)



6 Parameter Measurement Information

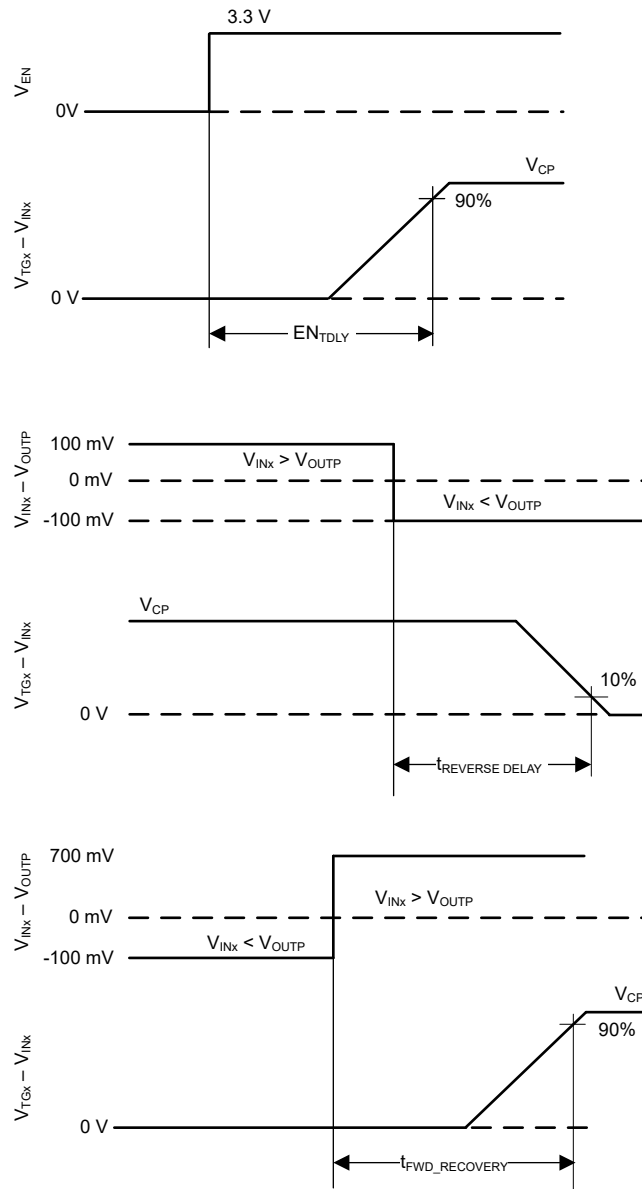


Figure 6-1. Timing Waveforms

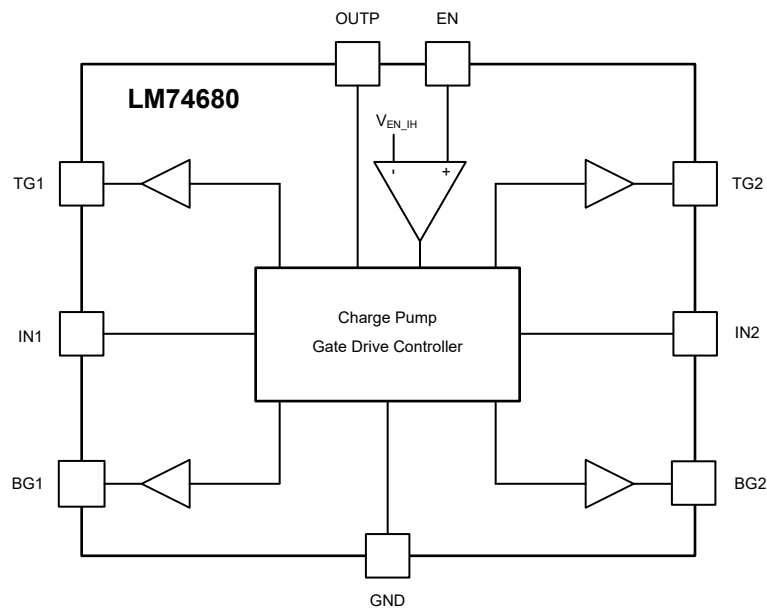
7 Detailed Description

7.1 Overview

The LM74680 is an ideal diode bridge controller designed for efficient input voltage rectification in applications requiring high performance and low power loss. It operates by driving four external N-channel MOSFETs in a full-bridge configuration. During startup, the MOSFET body diodes conduct and rectify the input voltage. Once the output voltage is above the power-on-reset threshold ($V_{\text{OUTP_PORR}}$) and the EN pin voltage is above high threshold ($V_{\text{EN_IH}}$), the LM74680 transitions to active control mode.

In active mode, the controller utilizes an internal charge pump to drive the MOSFET gates high, enabling low voltage drop forward conduction. Internal comparators monitor current flow to ensure the MOSFETs are turned off during reverse current conditions, effectively emulating an ideal diode bridge. The LM74680 is well suited for power critical applications such as video surveillance systems, building automation, and other electronics requiring robust and efficient power delivery.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input and Output Voltage

LM74680 supports power sources with wide input voltage range enabling both AC power source (12VAC, 24VAC) or a DC polarity-agnostic power source to be connected to its IN1 and IN2 pins. LM74680 is designed to operate with IN1 and IN2 designed to vary from 80V to –80V.

The OOTP pin is used to power the LM74680 internal circuitry, typically drawing I_Q when enabled and I_{SHDN} when disabled. If the OOTP pin voltage is greater than the power-on-reset rising threshold, then LM74680 operates in either shutdown mode or active mode in accordance with the EN pin voltage. LM74680 supports an OOTP voltage up to 80V during normal operation and can withstand voltage transients up to 100V ensuring protection against surges.

7.3.2 Charge Pump

The internal charge pump supplies the voltage necessary to drive the gate of the external N-channel MOSFETs. The charge pump is activated once the EN pin voltage is above the specified input high threshold, V_{EN_IH} . If EN pin is pulled low, then the charge pump remains disabled. By enabling and disabling the charge pump, the operating quiescent current of the LM74680 can be optimized as per system requirements.

7.3.3 Gate Drivers

The gate drivers are used to control the external N-Channel MOSFETs by setting the GATE to SOURCE voltage to the corresponding mode of operation. The FETs on the top side Q1 and Q2 are driven by gates TG1 and TG2 and the FETs on the bottom side Q3 and Q4 are driven by gates BG1 and BG2 respectively.

The internal charge pump powers the top side gate drivers and depending on the DRAIN to SOURCE voltage of each MOSFET, LM74680 has three defined modes of operation the gate driver operates under which are forward regulation, full conduction mode and reverse current protection. These modes are described in more detail in [Section 7.4.1.1](#), [Section 7.4.1.2](#), and [Section 7.4.2](#). [Figure 7-1](#) depicts how the modes of operation vary according to the DRAIN to SOURCE voltage. The threshold between forward regulation and conduction modes is when the DRAIN to SOURCE voltage is V_{TG_REG} . The threshold between forward regulation mode and reverse current protection mode is when the DRAIN to SOURCE voltage is V_{REV} .

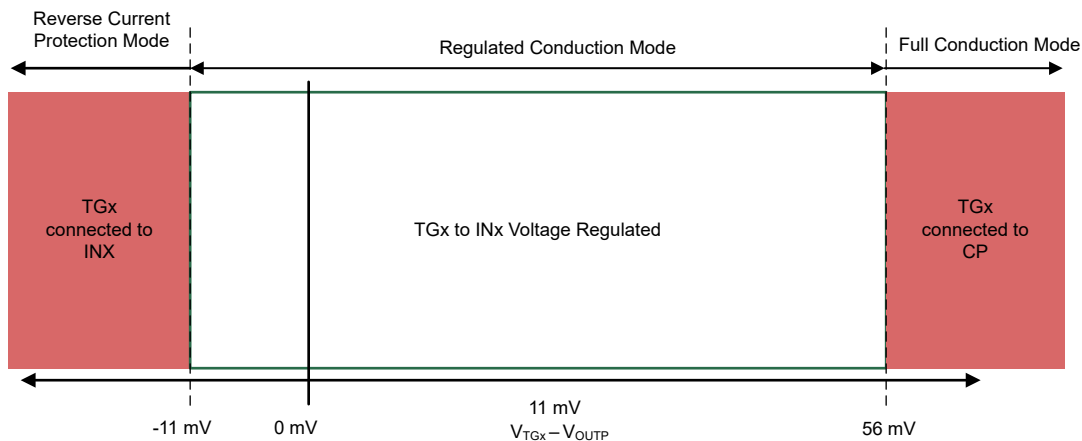


Figure 7-1. Gate Driver Mode Transitions

The bottom-side gate drivers of the LM74680 are powered directly from the IN1 or IN2 voltage and operate in two distinct modes which are forward full conduction and reverse current blocking. These gate drivers are controlled by the following logic to ensure efficient power flow and protection against reverse current.

- BG1 is enabled and in full conduction when the voltage at IN1 is greater than that GND+2V and is disabled when IN1 falls below IN2 to block reverse current flow.
- Similarly, BG2 is enabled when IN2 exceeds GND+2V and is disabled when IN2 is lower than IN1.

7.3.4 Enable

The LM74680 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump are activated as described in Section 7.3.3 and Section 7.3.2. If the enable pin voltage is less than the input low threshold, the charge pump and gate drivers are disabled placing the LM74680 in shutdown mode.

If the application doesn't need external ON/OFF control, the EN pin can be connected directly to OUTP pin.

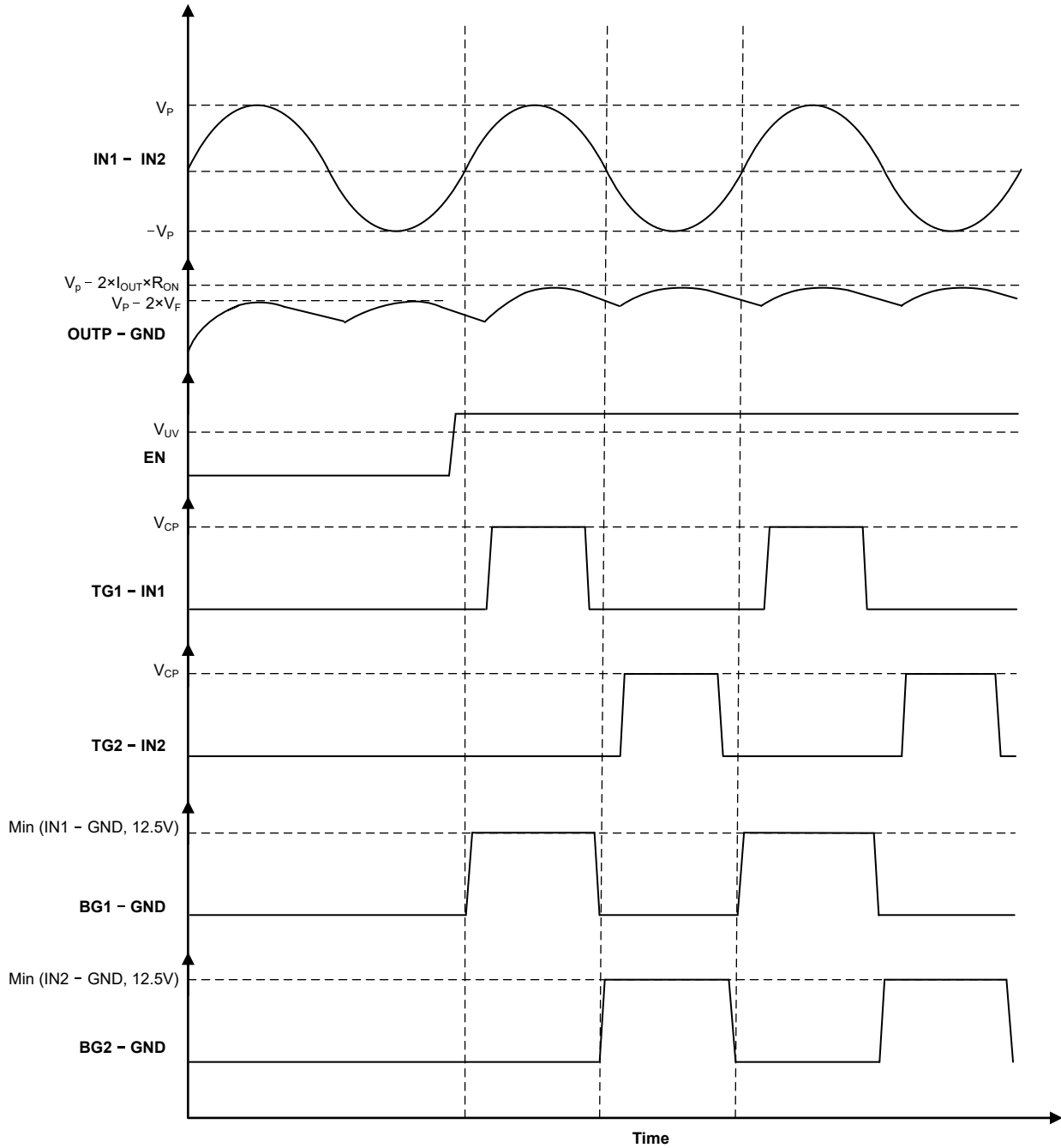


Figure 7-2. Enable Response and Gate Drivers Operation

7.4 Device Functional Modes

7.4.1 Conduction Mode

Conduction mode occurs when the top gate drivers are enabled and there are two regions of operating in this mode based on the source to drain voltage of the FETs driven by LM74680. The modes are described in [Section 7.4.1.1](#) and [Section 7.4.1.2](#).

7.4.1.1 Regulated Conduction Mode

For the LM74680 to operate its top gates TG1 and TG2 in regulated conduction mode, the gate driver must be enabled as described in [Section 7.3.3](#) and the current from source to drain of the external MOSFET must be within the range to result in an INx to OUPV voltage drop of V_{REV} to V_{TG_FC} . During forward regulation mode, the INx to OUPV voltage is regulated to V_{TG_REG} by adjusting the gate to source voltage. This closed loop regulation scheme enables graceful turn-off of the MOSFET at very light loads and ensures zero DC reverse current flow.

7.4.1.2 Full Conduction Mode

For the LM74680 to operate its top gates TG1 and TG2 in full conduction mode the gate driver must be enabled as described in [Section 7.3.3](#) and the current from source to drain of the external MOSFET must be large enough to result in an INx to OUPV voltage drop of greater than V_{TG_FC} . If these conditions are achieved the GATE pin is internally connected to the charge pump resulting in the INx to OUPV voltage being equal to $V_{TGx} - V_{INx}$. By connecting the internal charge pump to GATE the external MOSFET $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

7.4.2 Reverse Current Protection Mode

For the LM74680 to operate in reverse current protection mode, the gate driver must be enabled as described in [Section 7.3.3](#) and the current of the external MOSFET must be flowing from the drain to the source. When the INx to OUPV voltage is typically less than V_{REV} , reverse current protection mode is entered and the FET gates is internally connected to the source. This connection of the TGx to INx pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM74680 drives four external N-channel MOSFETs in a diode bridge configuration, making it ideal for rectifying an AC power supplies or polarity-agnostic DC power supplies. By replacing traditional diodes with MOSFETs, the device minimizes conduction losses, resulting in improved thermal performance and increased overall system efficiency. This makes it suitable for applications such as video door bell, industrial automation, HVAC systems, and other AC-powered equipment where low power loss and high reliability are critical. The schematic for a 24V AC input application is shown in [Figure 8-1](#) where the LM74680 is driving the high side MOSFETs Q1, Q2 and low side MOSFETs Q3, Q4 in diode bridge configuration.

8.2 Typical Application

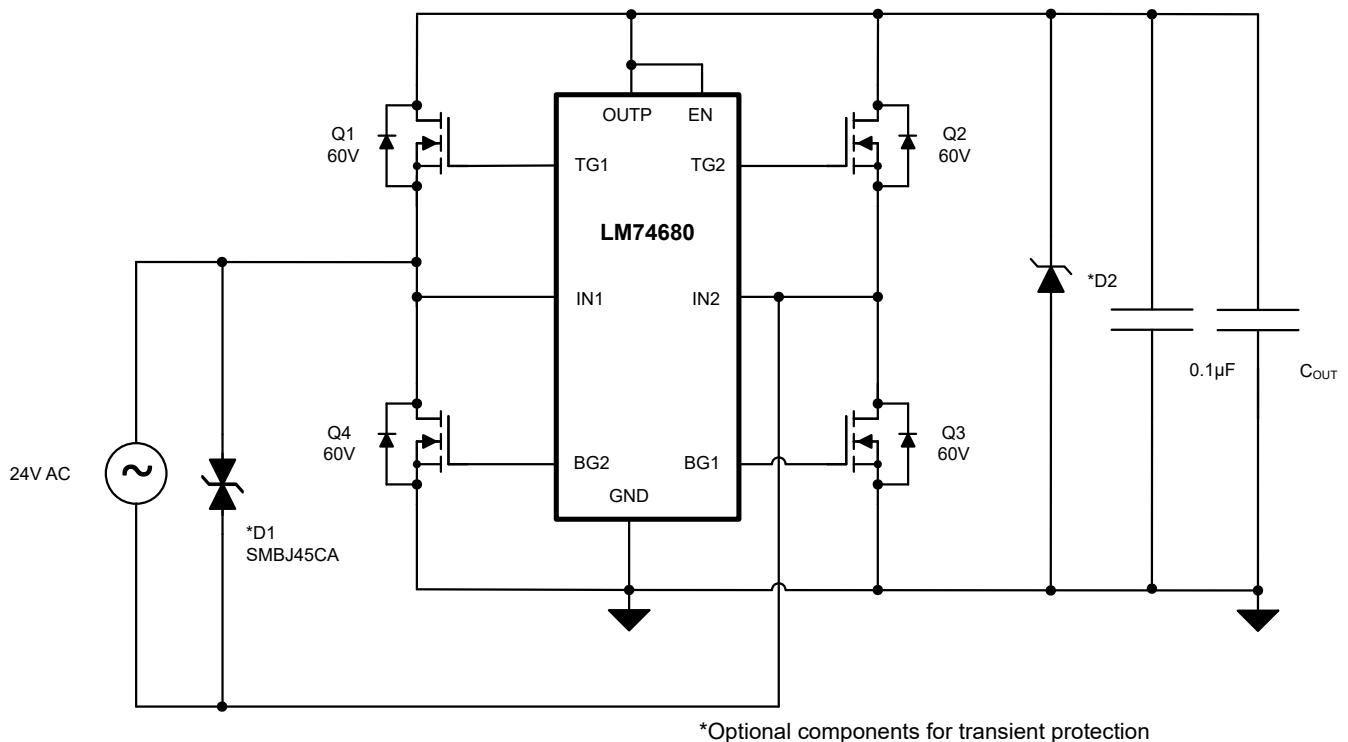


Figure 8-1. Typical Application Circuit

8.2.1 Design Requirements

A design example, with system design parameters listed in [Table 8-1](#) is presented.

Table 8-1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|-------------------------|--------------------|
| Input voltage and range | 24V AC \pm 10% |
| Maximum load current | 2A |
| Output voltage ripple | 10V _{p-p} |

8.2.2 Detailed Design Procedure

8.2.2.1 Design Considerations

- Input operating voltage range, including line transients
- Maximum load current
- Maximum ripple of output voltage

8.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D , the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum gate-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance $R_{DS(ON)}$.

The $V_{DS(MAX)}$ rating of the MOSFET must be high enough to withstand the highest differential voltage seen in the application, including any anticipated transients during fault conditions. For a 24V AC system, a MOSFET with a voltage rating of 60V is recommended. The LM74680 can drive a maximum gate-to-source voltage of 13.8V. A MOSFET with a minimum $V_{GS(MAX)}$ rating of 15V should be selected. For MOSFETs with lower V_{GS} ratings, a Zener diode can be used to clamp the voltage to a safe level.

The MOSFET I_D rating must exceed the maximum continuous load current to ensure reliable operation under full load conditions. Additionally, the MOSFET thermal resistance should be considered to ensure the junction temperature (T_J) remains within safe limits under the expected maximum power dissipation including the initial inrush phase when the output capacitors are charged through the MOSFETs body diode. This helps maintain reliability and performance in the application.

To reduce the MOSFET conduction losses, the lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not always be beneficial. Higher $R_{DS(ON)}$ will provide increased voltage information to LM74680 reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with $R_{DS(ON)}$ that develops <30mV forward voltage drop at maximum current is a good starting point. Usually, $R_{DS(ON)}$ increases drastically below 4.5V V_{GS} and $R_{DS(ON)}$ is highest when V_{GS} is close to MOSFET V_{th} . For stable regulation at light load conditions, it is recommended to operate the MOSFET close to 4.5V V_{GS} , that is, much higher than the MOSFET gate threshold voltage. It is recommended to choose MOSFET gate threshold voltage V_{th} of 2.5V to 3.5V maximum. Choosing a lower V_{th} MOSFET also reduces the turn ON time.

CSD88537ND Dual N-channel MOSFET from Texas Instruments is selected to meet this 24VAC bridge rectifier design and it is rated at:

- $V_{DS(MAX)}$: 60V
- $V_{GS(MAX)}$: $\pm 20V$
- $R_{DS(ON)}$: 12.5m Ω (typical) and 15m Ω (maximum) at 10V V_{GS}

8.2.2.3 Output Capacitance

A minimum ceramic capacitor of 0.1 μ F is recommended to be placed across the OOTP and GND pins as close to the LM74680 as possible for decoupling. Additional output capacitance C_{OUT} may be required to ensure that the rectified output voltage remains within the recommended operating range of the LM74680 and also to meet the output voltage ripple requirements of downstream circuitry depending on the system's tolerance.

The additional capacitance required between OOTP and GND is based on the downstream power demands and the allowable voltage ripple. C_{OUT} in the hundreds to thousands of microfarads is common. A good starting point is selecting C_{OUT} such that:

$$C_{OUT} \geq I_{LOAD} / (V_{RIPPLE} \times 2 \times Freq) \quad (1)$$

Where,

- I_{LOAD} is the average output load current
- V_{RIPPLE} is the maximum tolerable output ripple voltage
- Freq is the frequency of the input AC source

For example, in a 50Hz, 24V AC application where the load current is 1A and the tolerable ripple is 1V, choose $C_{OUT} \geq 1A/(10V \times 2 \times 50Hz) = 1mF$.

8.2.3 Application Curves

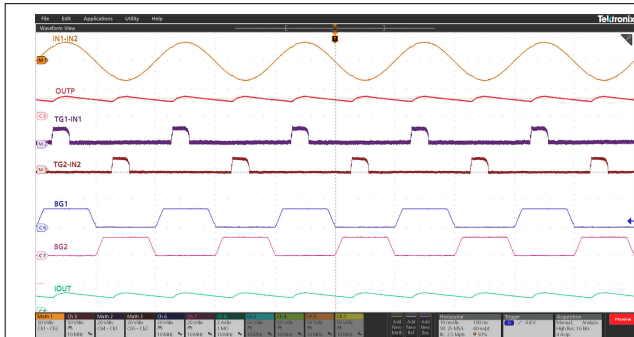


Figure 8-2. 24V AC Input, $C_{OUT} = 1mF$, 30W Load, Steady State

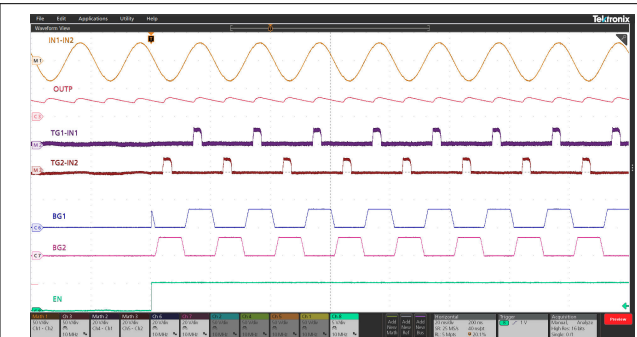


Figure 8-3. 24V AC Input, $C_{OUT} = 1mF$, 30W Load, EN Toggle High

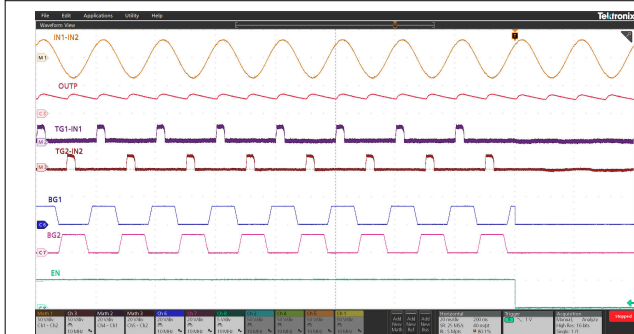


Figure 8-4. 24V AC Input, $C_{OUT} = 1mF$, 30W Load, EN Toggle Low

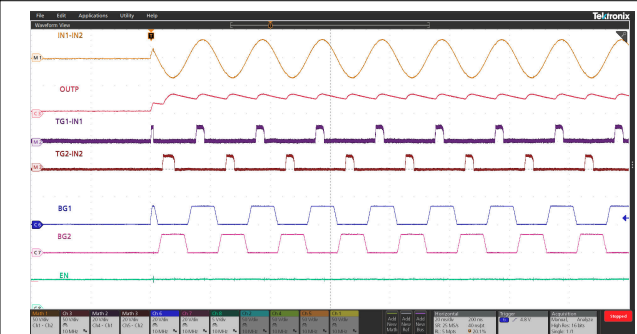


Figure 8-5. 24V AC Input, $C_{OUT} = 1mF$, 30W Load, EN High, Input Hotplug

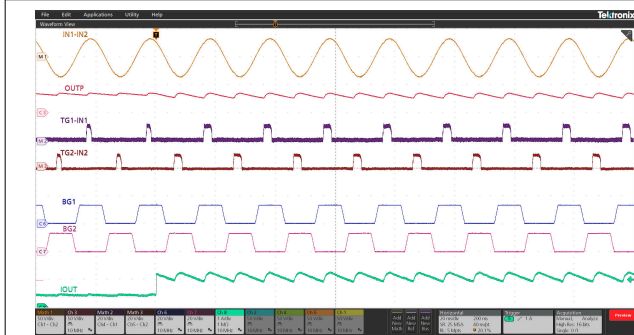


Figure 8-6. 24V AC Input, $C_{OUT} = 1mF$, Load Step From 10W to 30W

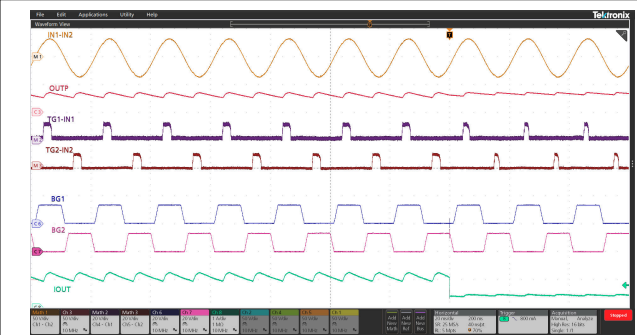


Figure 8-7. 24V AC Input, $C_{OUT} = 1mF$, Load Step From 30W to 10W

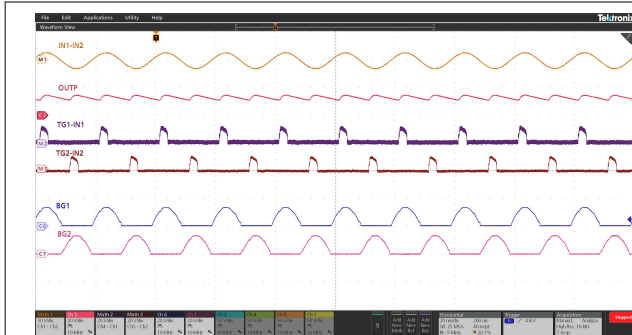


Figure 8-8. 10V AC Input, $C_{OUT} = 1\text{mF}$, Steady State

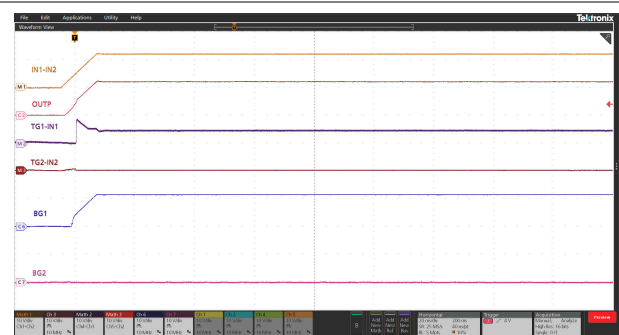


Figure 8-9. 12V DC Input, Startup

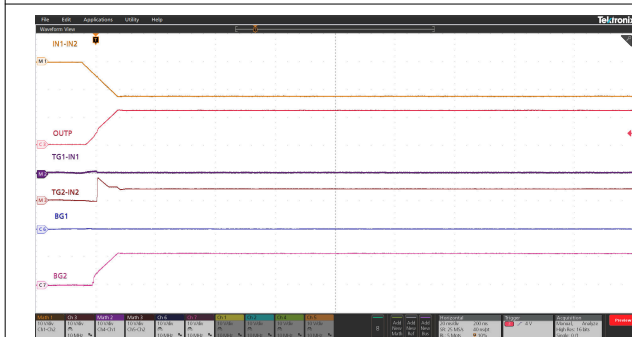


Figure 8-10. -12V DC Input, Startup

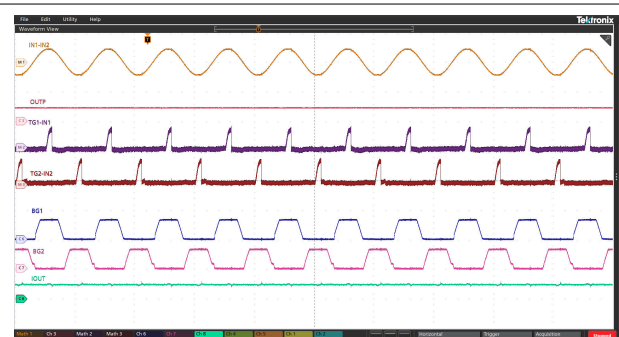


Figure 8-11. 24V AC Input, Freq = 1kHz, $C_{OUT} = 1\text{mF}$, Steady State

8.3 Power Supply Recommendations

8.3.1 Transient Protection

The TVS at input or output is not required for the LM74680 to operate, but it may be required to clamp the voltage transients caused by lightning, switching surges, or power disturbances that can exceed the voltage ratings of MOSFETs and the controller possibly causing damage. A TVS diode protects against such events by clamping the transient voltages to safe levels. For 24V AC systems, a bidirectional TVS with a standoff voltage above the AC peak and a clamping voltage below the MOSFET's maximum rating is recommended. In well-regulated applications with minimal transient risks, a TVS diode may not be necessary.

To avoid output voltage buildup during input hotplug conditions due to coupling from MOSFET gate capacitance using MOSFETs with input capacitance of at least 1nF is recommended. If the input capacitance of the selected MOSFET is less than 1nF, add a 1nF capacitor between the gate and source of the top-side MOSFETs.

8.4 Layout

8.4.1 Layout Guidelines

- Place the decoupling capacitor close to the OUPF pin and IC GND.
- For the top side MOSFETs, connect the INx, TGx, and OUPF pins of LM74680 close to the MOSFET SOURCE, GATE, and DRAIN pins.
- The high current path is through the MOSFETs, therefore it is important to use thick and short traces for the source and drain of the MOSFET to minimize resistive losses.
- The TGx and BGx pins of the LM74680 must be connected to the respective MOSFET gate with a short trace.
- Place transient suppression components close to LM74680.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in [Section 8.4.2](#) is intended as a guideline and to produce good results.

8.4.2 Layout Example

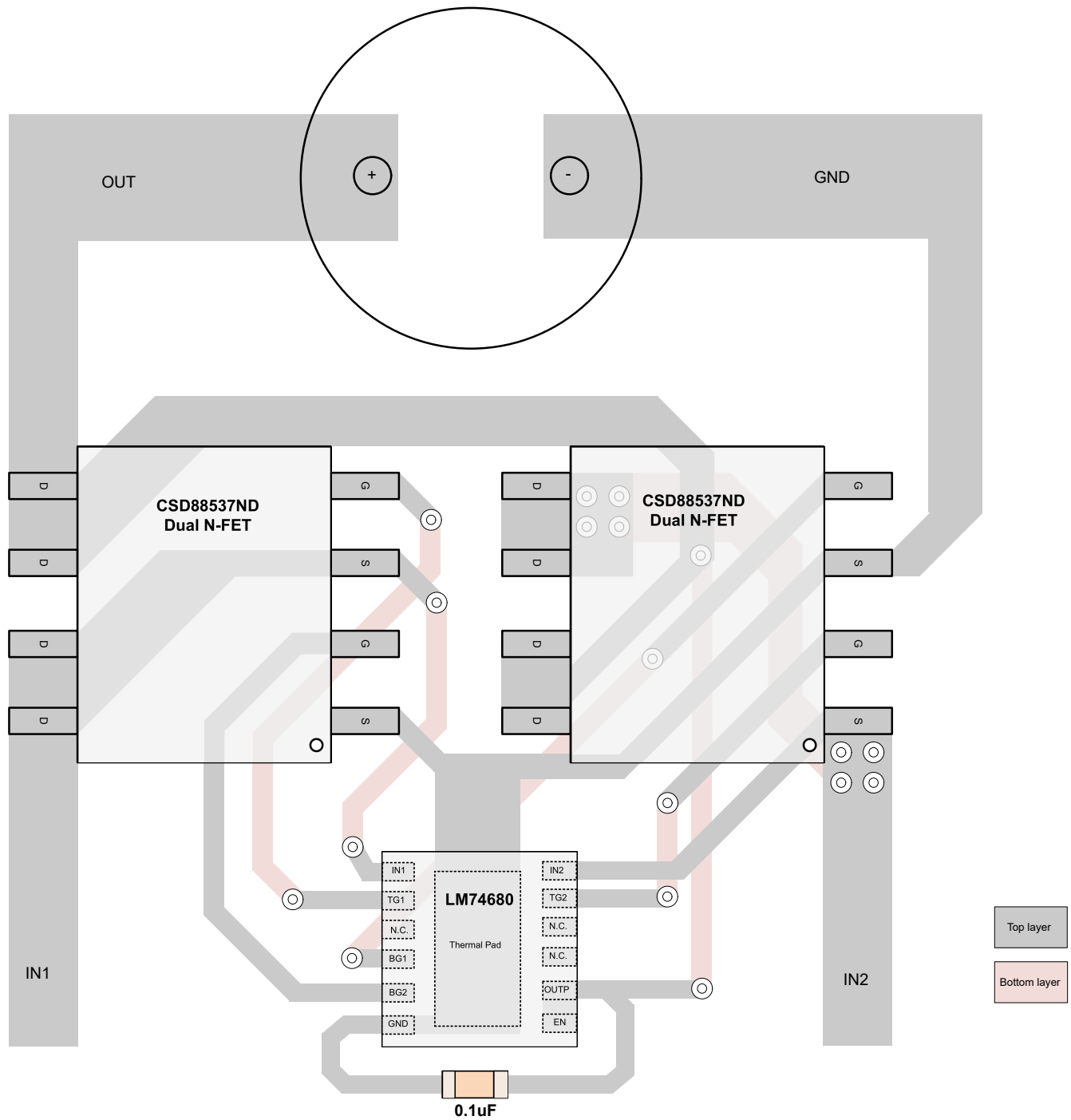


Figure 8-12. LM74680 Example Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| December 2024 | * | Initial Release |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| LM74680DRRR | ACTIVE | WSON | DRR | 12 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | L74680 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM74680DRRR | WSO | DRR | 12 | 5000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM74680DRRR | WSON | DRR | 12 | 5000 | 367.0 | 367.0 | 35.0 |

GENERIC PACKAGE VIEW

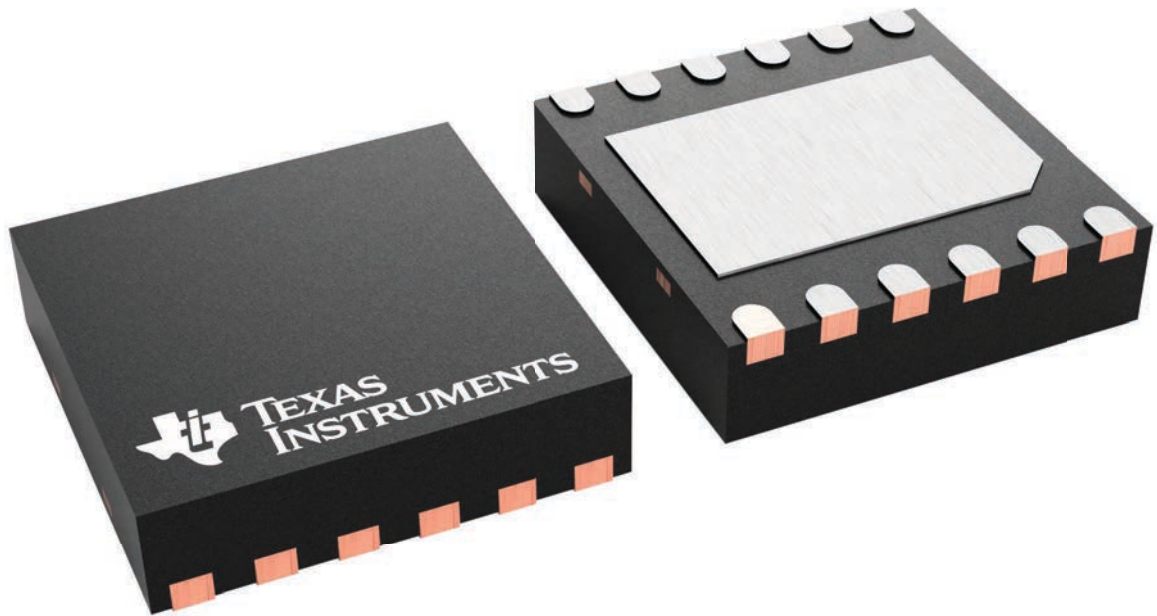
DRR 12

WSON - 0.8 mm max height

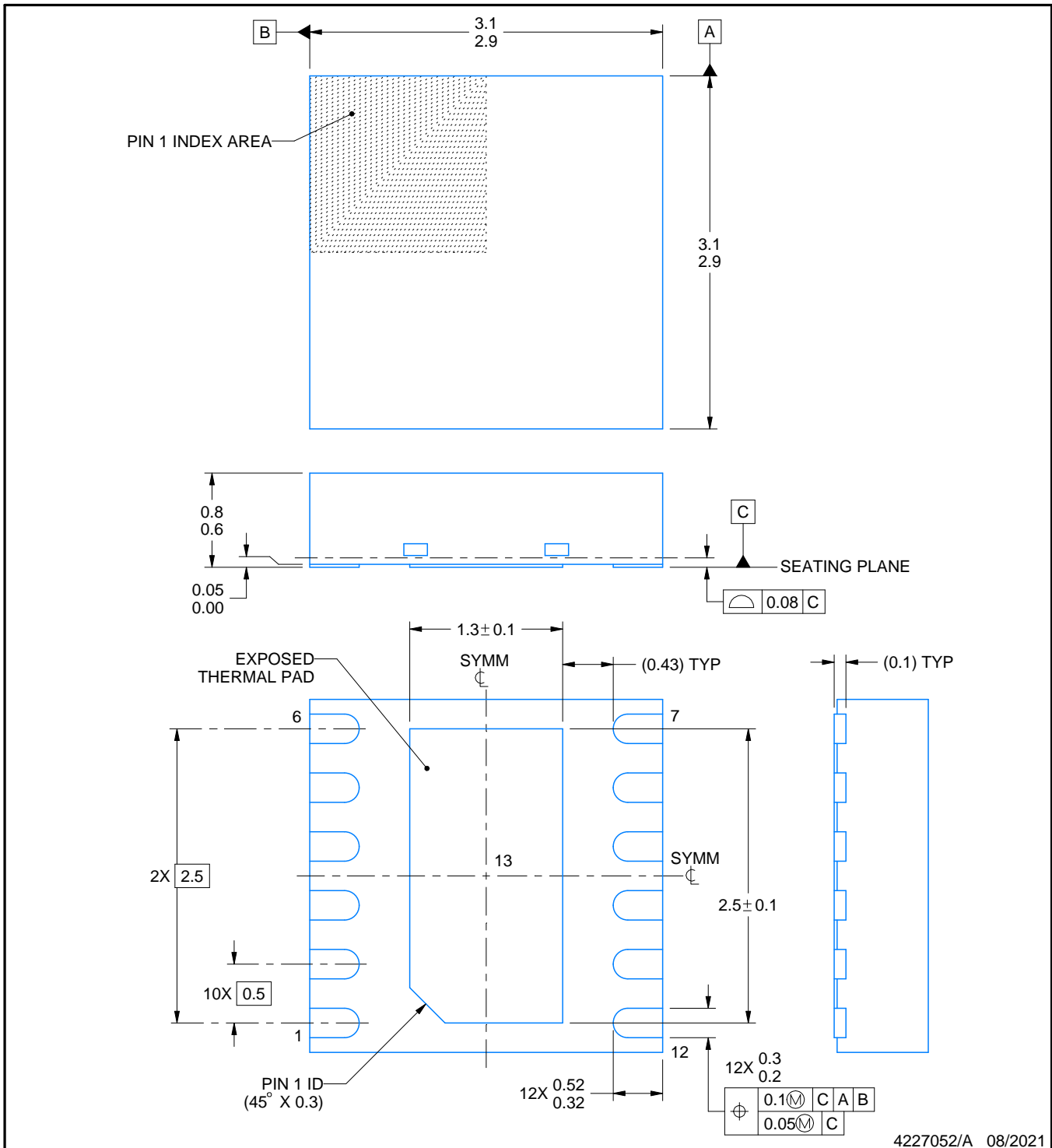
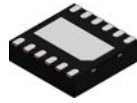
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4223490/B



NOTES:

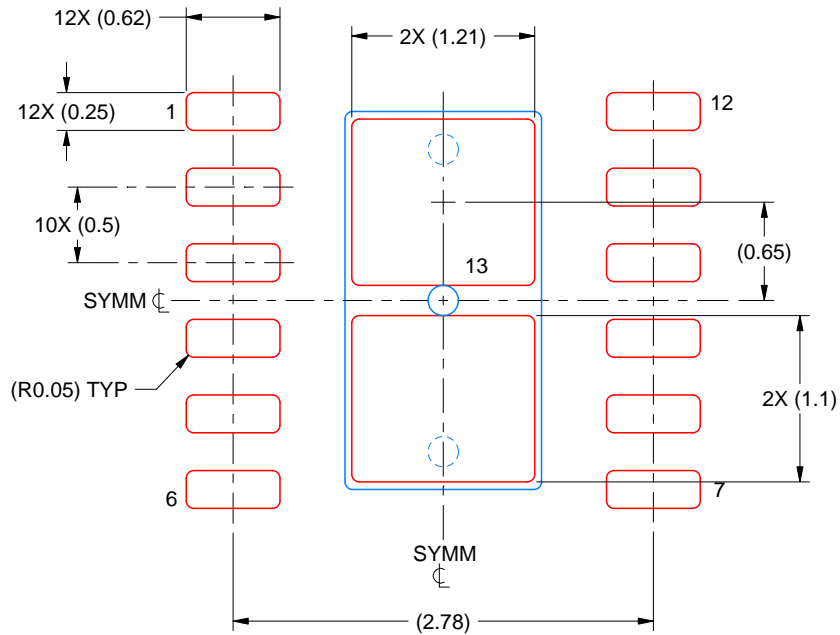
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

DRR0012G

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 13
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227052/A 08/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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