LMG310xR0xx 100V GaN Power Stage With Integrated Protection and Smart-Switching Features

ADVANCE INFORMATION

1 Features

- 100V GaN power stage with integrated driver: (GaN FET $R_{DS(ON)}$ options: 1.1mΩ and 1.7mΩ)
- Integrated high-side level shift and bootstrap
  - Two LMG310xR0xx can form a half-bridge
  - No external level shifter is required
- Efficient and high-density power conversion with
  - Ultra-low propagation delay (20ns) and matching (7ns)
  - Independent turn-on and turn-off slew-rate control for the GaN FET
  - Zero-voltage detection (ZVD) reporting for dead-time optimization
  - Ideal diode mode turn-on (IDM) and turn-off (zero current detection ZCD) to reduce third quadrant losses in soft switching application
- Input control flexibility
  - Independent input mode (IIM) control
  - Single PWM input with resistor programmable dead time option for IO-limited controllers
- Robust protection
  - Interlock protection in IIM (LMG3104R0xx)
  - Internal bootstrap supply voltage regulation to prevent GaN FET overdrive
  - V_{DS} monitoring based cycle-by-cycle short-circuit protection
  - Fault indication for overtemperature, supply undervoltage, and short-circuit events
- External bias power supply: 5V
  - Supports 3.3V and 5V input logic levels
- Parasitic optimized QFN package with exposed top pad to support top-side cooling

2 Applications

- Buck, boost, and buck-boost converters
- LLC converters
- Solar inverters
- Telecom and server power
- Motor drives
- Power tools
- Class-D audio amplifiers

3 Description

The LMG310xR0xx devices are a family of 100V enhancement-mode Gallium Nitride (GaN) HEMT with integrated high frequency driver. The LMG310xR0xx incorporates a high side level shifter and bootstrap circuit, so that two LMG310xR0xx devices can be used to form a half bridge without an additional level shifter. LMG3104R0xx offers logic input interlock in Independent Input Mode (IIM).

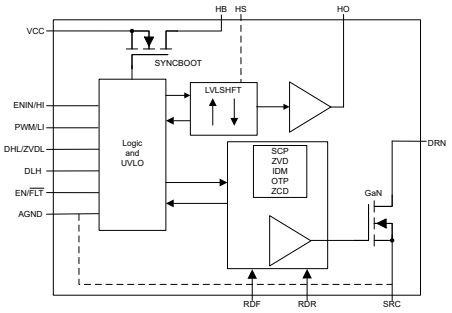
GaN FETs provide significant advantages for power conversion as GaN FETs have zero reverse recovery, very small input capacitance C_{ISS}, and output capacitance C_{OSS}. The driver and the GaN FET are mounted on a completely bond-wire free package platform with minimized package parasitic elements. The LMG310xR0xx device is available in a 6.5mm × 4mm lead-free package and can be easily mounted on PCBs.

The TTL logic compatible inputs support 3.3V and 5V logic levels, regardless of the VCC voltage. A proprietary bootstrap voltage control technique regulates the gate voltages of the enhancement mode GaN FETs within the safe operating range. The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. The device is an excellent option for applications requiring high-frequency, high-efficiency operation in a small form factor.

Device Information

PART NUMBER(3)	PACKAGE (1)	PACKAGE SIZE(2)
LMG310xR011	VBE (VQFN-FCRLF, 15)	6.5mm × 4mm
LMG310xR017		

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Tables*.



Simplified Block Diagram

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ADVANCE INFORMATION

4 Device Comparison

Table 4-1. Device Comparison

DEVICE		$RDS_{(ON)}$(mΩ)
LMG3105R011VBER	LMG3104R011VBER	1.1
LMG3105R017VBER(1)	LMG3104R017VBER	1.7

(1) Preview information (not Advance Information)

Table 4-2. Feature Comparison

PART NUMBER	INTERLOCK IN IIM MODE	IDM IN TURN-OFF TRANSITION
LMG3104Rxxx	Enabled	Enabled
LMG3105Rxxx	Disabled	Disabled

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Device and Documentation Support

5.1 Documentation Support

5.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Layout Considerations for LMG5200 GaN Power Stage* application note
- Texas Instruments, *Using the LMG5200: GaN Half-Bridge Power Stage EVM* user's guide
- Texas Instruments, *AN-2029 Handling and Process Recommendations* application note

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.4 Trademarks

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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

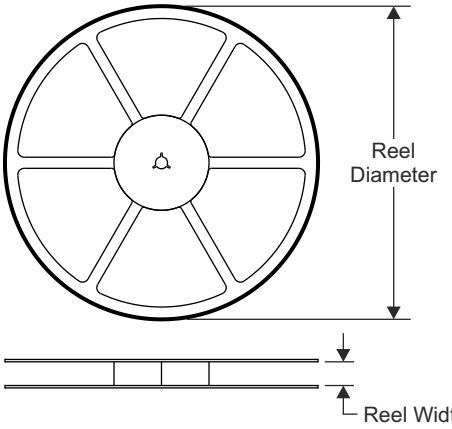
DATE	REVISION	NOTES
May 2026	*	Initial Release

7 Mechanical, Packaging, and Orderable Information

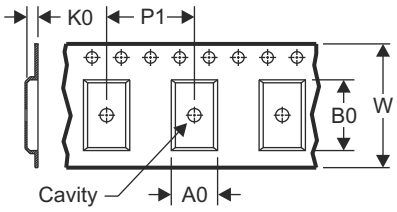
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information

REEL DIMENSIONS

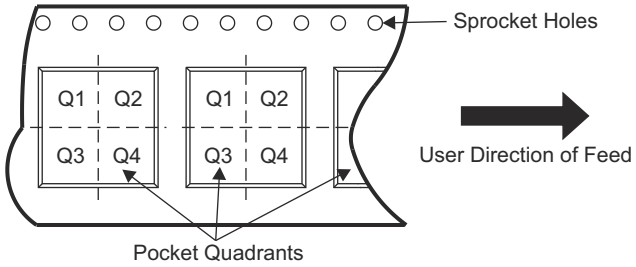


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

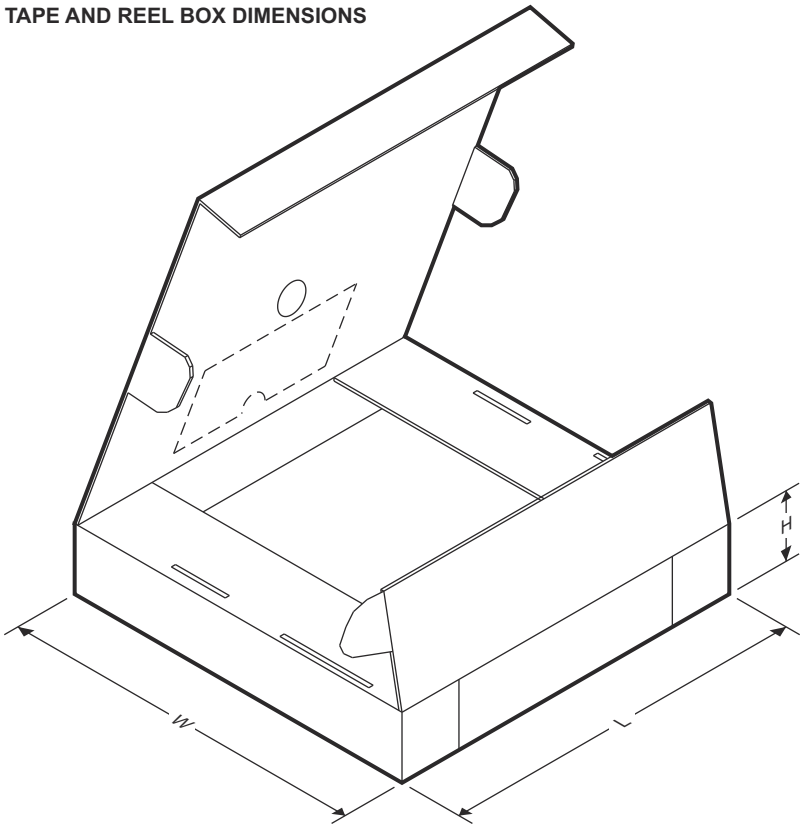
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG3104R011VBER	VQFN-FCRLF	VBE	15	2000	330	16.4	4.3	6.8	1.1	8.0	16.0	Q1
LMG3104R017VBER	VQFN-FCRLF	VBE	15	2000	330	16.4	4.3	6.8	1.1	8.0	16.0	Q1
LMG3105R011VBER	VQFN-FCRLF	VBE	15	2000	330	16.4	4.3	6.8	1.1	8.0	16.0	Q1
LMG3105R017VBER (Preview)	VQFN-FCRLF	VBE	15	2000	330	16.4	4.3	6.8	1.1	8.0	16.0	Q1

ADVANCE INFORMATION

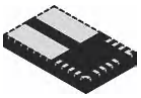
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG3104R011VBER	VQFN-FCRLF	VBE	15	2000	336.6	336.6	28.6
LMG3104R017VBER	VQFN-FCRLF	VBE	15	2000	336.6	336.6	28.6
LMG3105R011VBER	VQFN-FCRLF	VBE	15	2000	336.6	336.6	28.6
LMG3105R017VBER (Preview)	VQFN-FCRLF	VBE	15	2000	336.6	336.6	28.6

7.2 Mechanical Data

The LMG310xR0xx device package is rated as an MSL3 package (Moisture Sensitivity Level 3). Refer to *AN-2029 Handling and Process Recommendations* application note for specific handling and process recommendations of an MSL3 package.

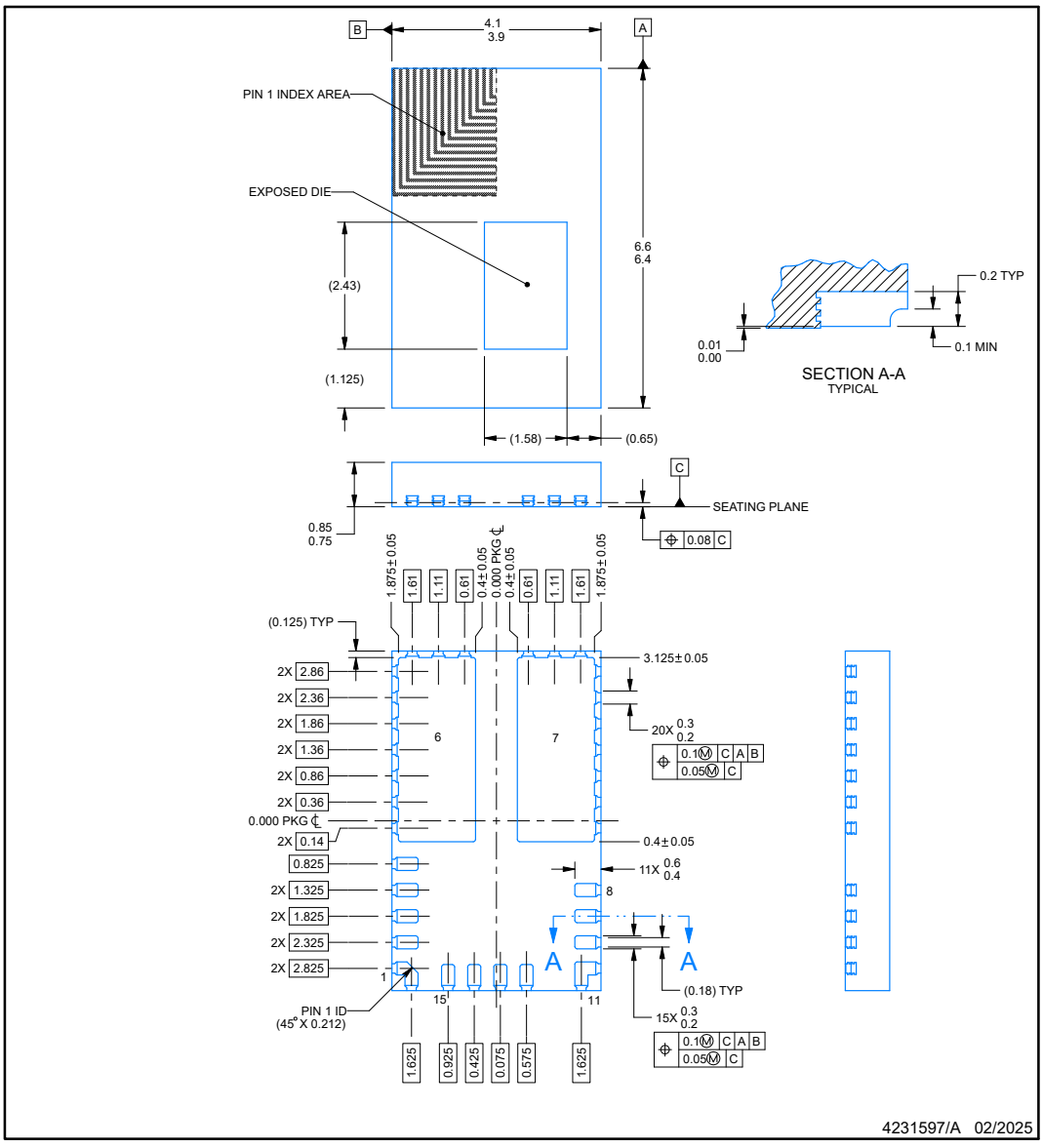


PACKAGE OUTLINE

VBE0015A-C01

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

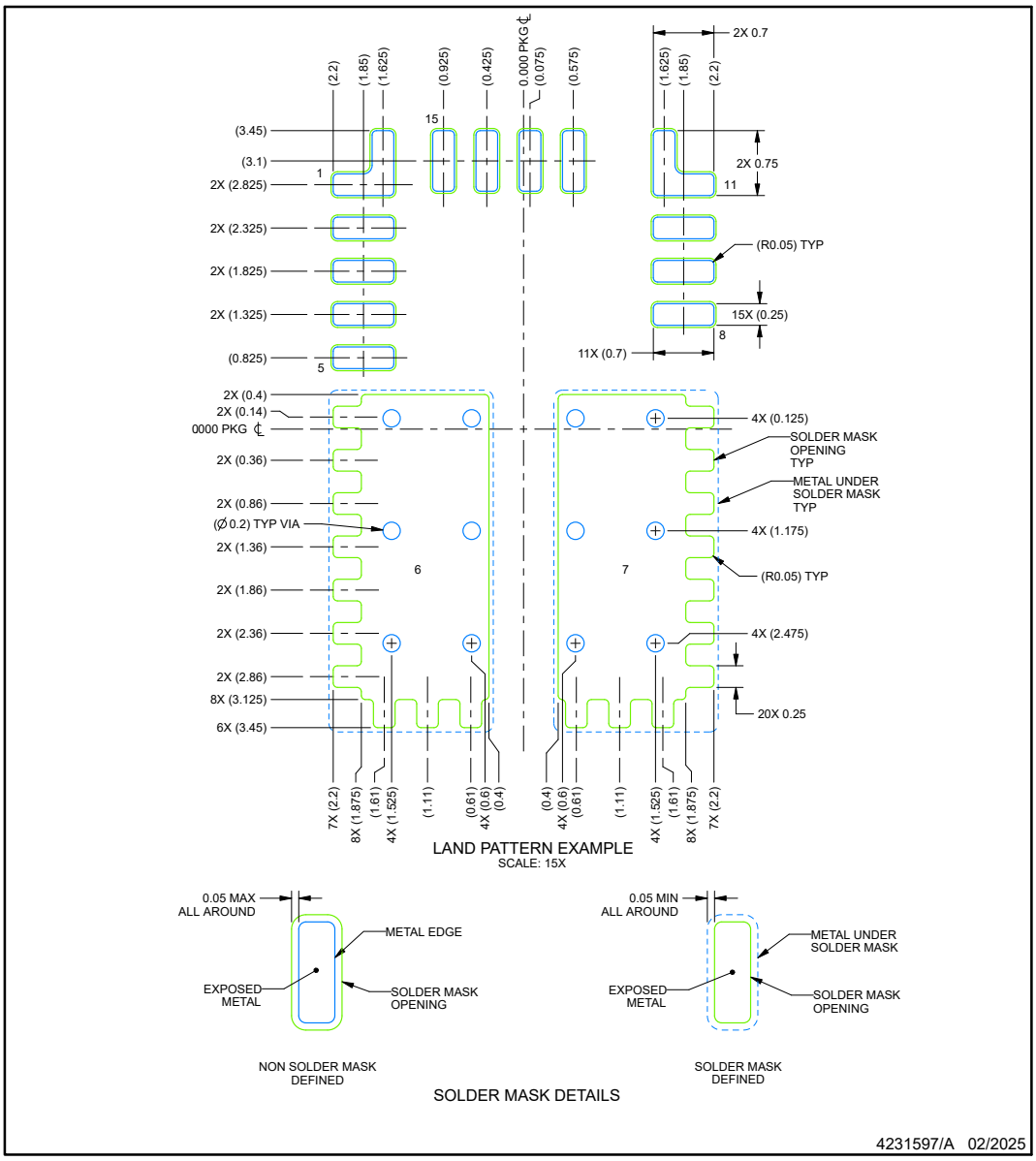
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

VBE0015A-C01 — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



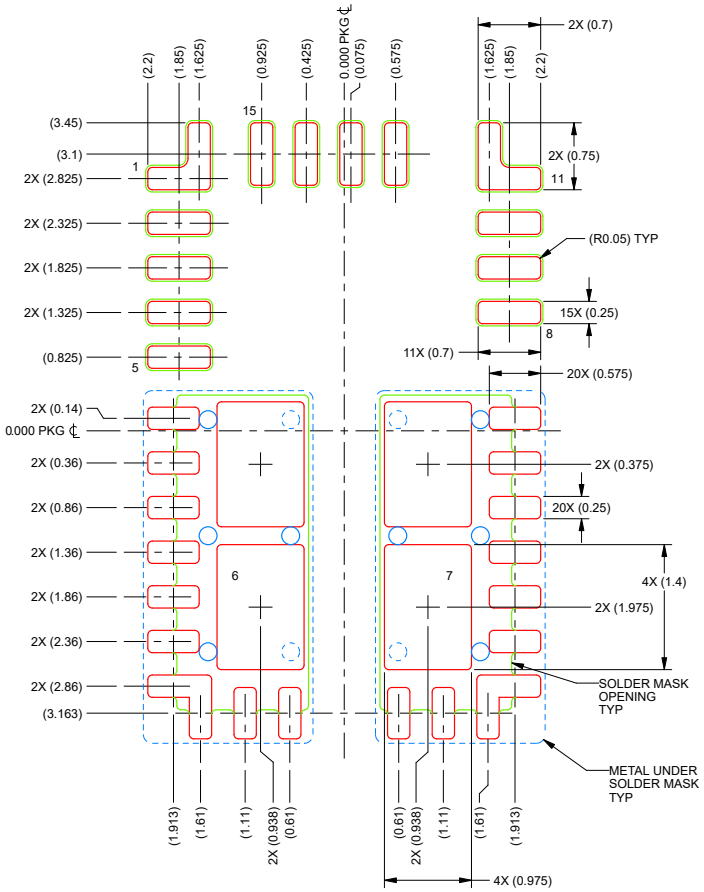
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VBE0015A-C01 **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 74%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XLMG3104R011VBER	Active	Preproduction	VQFN-FCRLF (VBE) | 15	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

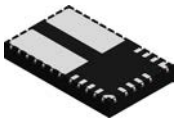
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

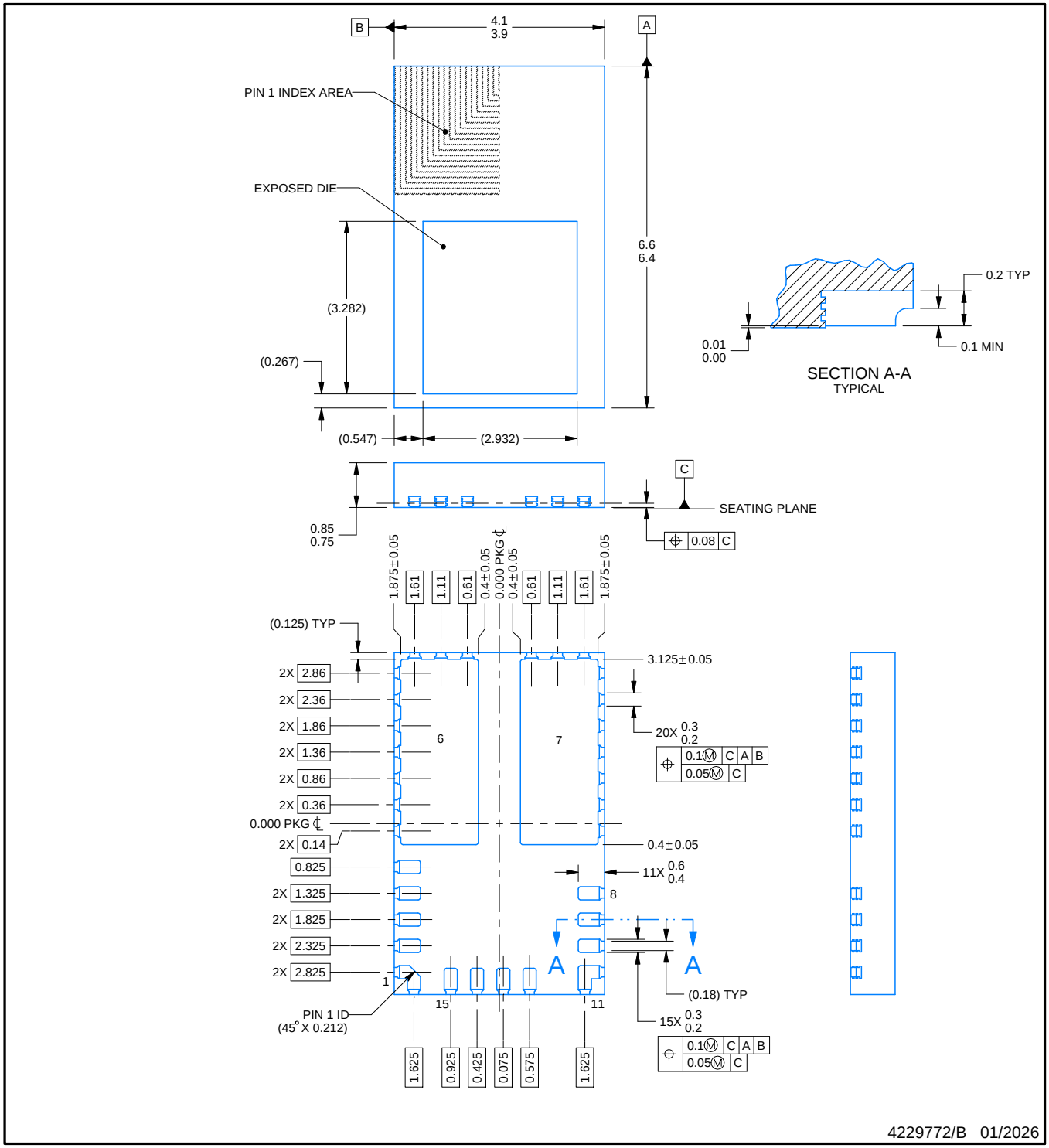


PACKAGE OUTLINE

VBE0015A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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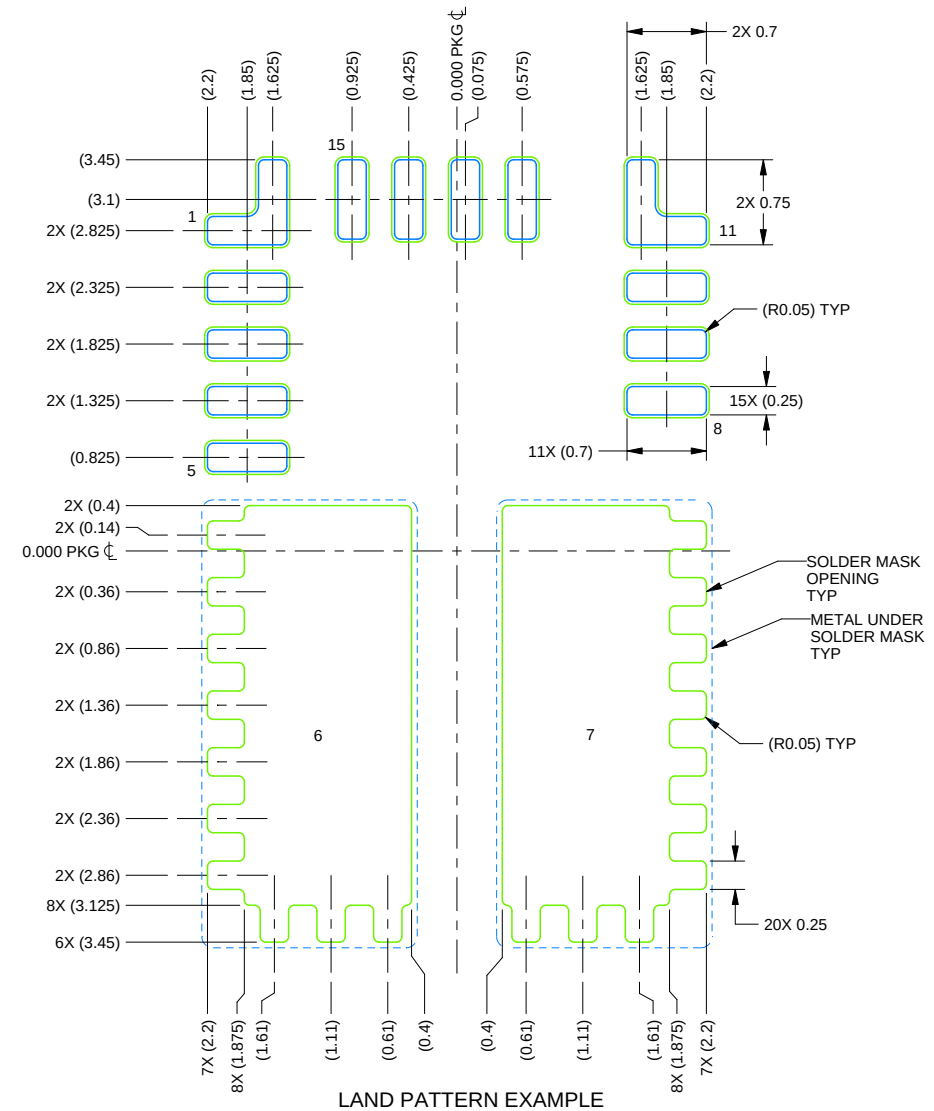
EXAMPLE BOARD LAYOUT

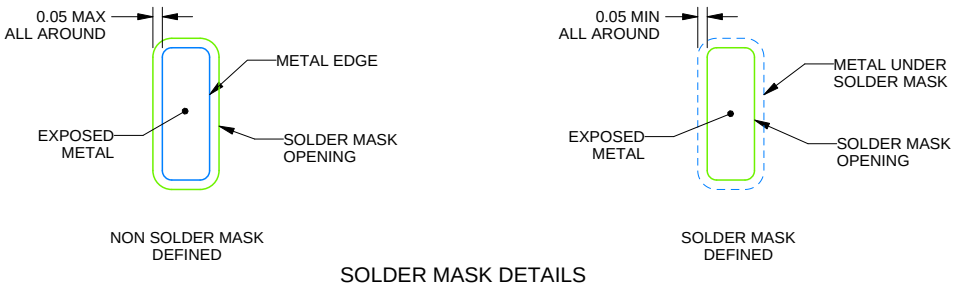
VBE0015A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

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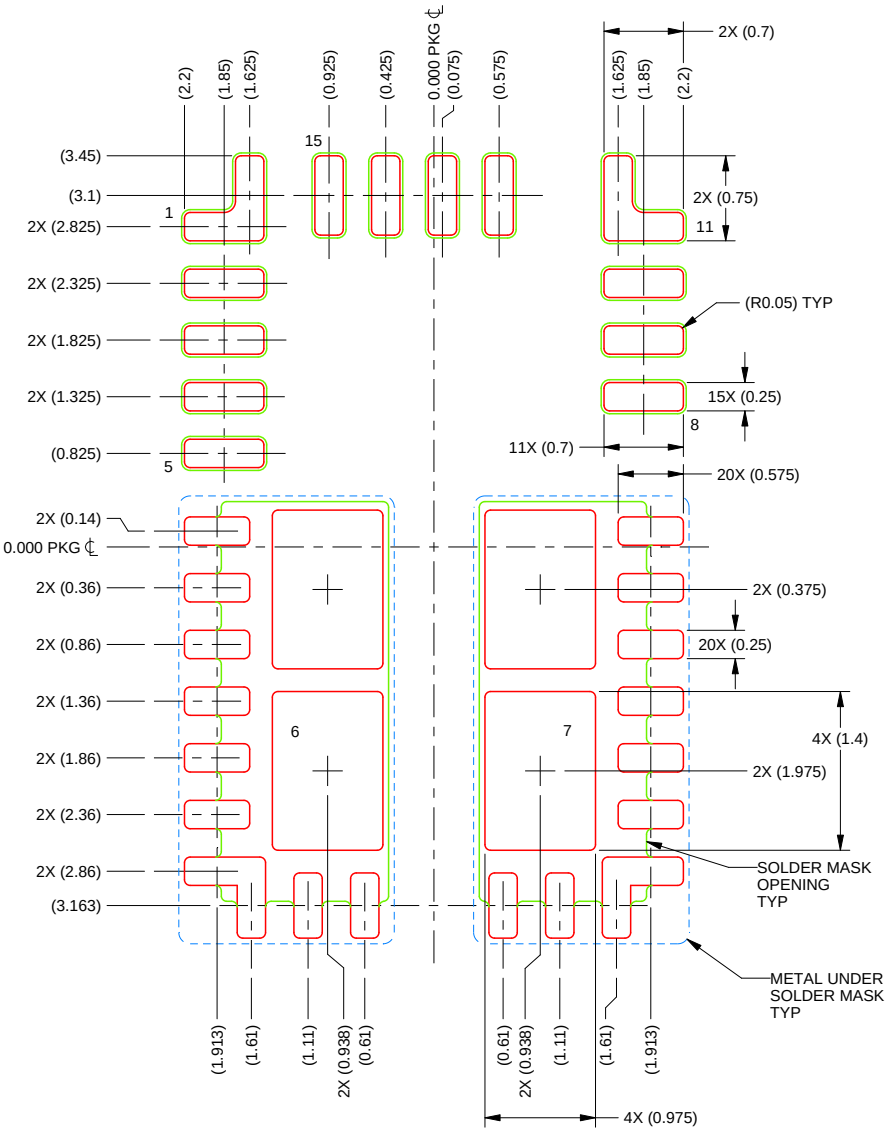
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VBE0015A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 74%

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NOTES: (continued)

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