

## LMH6601 and LMH6601-Q1 250-MHz, 2.4-V CMOS Operational Amplifier With Shutdown

### 1 Features

- LMH6601-Q1 Qualified for Automotive Applications
  - AEC-Q100 Grade 3
  - 40°C to 85°C Ambient Operating Temperature Range
- $V_S = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $A_V = 2\text{ V/V}$ ,  $R_L = 150\ \Omega$  to  $V^-$ , Unless Specified
- 125 MHz –3 dB Small Signal Bandwidth
- 75 MHz –3 dB Large Signal Bandwidth
- 30 MHz Large Signal 0.1-dB Gain Flatness
- 260 V/ $\mu\text{s}$  Slew Rate
- 0.25%/0.25° Differential Gain and Differential Phase
- Rail-to-Rail Output
- 2.4-V to 5.5-V Single-Supply Operating Range
- 6-Pin SC70 Package

### 2 Applications

- Video Amplifiers
- Charge Amplifiers
- Set-Top Boxes
- Sample and Holds
- Transimpedance Amplifiers
- Line Drivers
- High-Impedance Buffers
- Automotive

### 3 Description

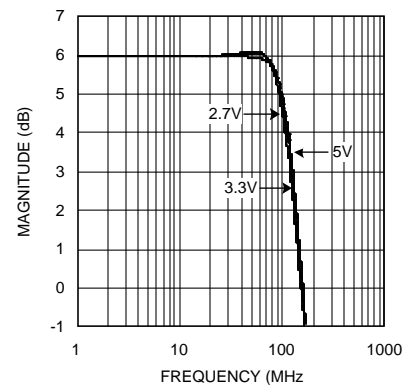
The LMH6601 device is a low-voltage (2.4 V to 5.5 V), high-speed voltage feedback operational amplifier suitable for use in a variety of consumer and industrial applications. With a bandwidth of 125 MHz at a gain of +2 and ensured high-output current of 100 mA, the LMH6601 is an ideal choice for video line driver applications, including HDTV. Low-input bias current (50 pA maximum), rail-to-rail output, and low current noise allow the use of the LMH6601 in various industrial applications such as transimpedance amplifiers, active filters, or high-impedance buffers. The LMH6601 is an attractive solution for systems which require high performance at low supply voltages. The LMH6601 is available in a 6-pin SC70 package, and includes a micropower shutdown feature.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6601	SC70 (6)	2.00 mm x 1.25 mm
LMH6601-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Response at a Gain of +2 for Various Supply Voltages



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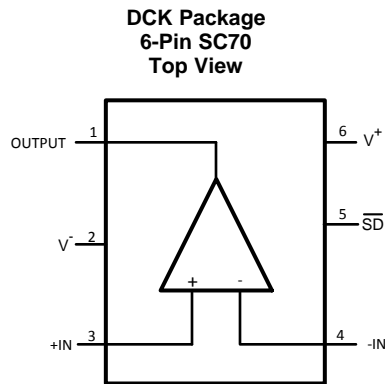
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision E (March 2013) to Revision F</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Removed $I_{OS}$ over temperature limit in <i>Electrical Characteristics, 2.7 V</i> .....	<b>8</b>
• Moved the <i>SAG Compensation</i> section to the <i>Typical Application</i> section.....	<b>25</b>
• Changed section titled <i>Other Applications</i> to <i>Charge Preamplifier</i> .....	<b>28</b>

<b>Changes from Revision D (March 2013) to Revision E</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<b>1</b>

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUTPUT	O	Output
2	V <sup>-</sup>	I	Negative supply
3	+IN	I	Noninverting input
4	-IN	I	Inverting input
5	$\overline{SD}$	I	Shutdown
6	V <sup>+</sup>	I	Positive supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub> Differential			±2.5	V
Input Current <sup>(2)</sup>			±10	mA
Output Current			200 mA <sup>(3)</sup>	mA
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )			6	V
Voltage at Input/Output Pins			V <sup>+</sup> +0.5, V <sup>-</sup> -0.5	V
Junction Temperature			150	°C
Soldering Information	Infrared or Convection (20 sec.)		235	°C
	Wave Soldering (10 sec.)		260	
Storage Temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Negative input current implies current flowing out of the device.
- (3) The maximum continuous output current (I<sub>OUT</sub>) is determined by device power dissipation limitations.

### 6.2 ESD Ratings - for LMH6601

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - for LMH6601-Q1

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000
			V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.4 Recommended Operating Conditions<sup>(1)</sup>

	MIN	MAX	UNIT
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )	2.4	5.5	V
Operating Temperature	-40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LMH6601, LMH6601-Q1	UNIT	
	DCK (SC70)		
	6 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	414	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.6 Electrical Characteristics, 5 V

Single-Supply with V<sub>S</sub> = 5 V, A<sub>V</sub> = +2, R<sub>F</sub> = 604 Ω,  $\overline{SD}$  tied to V<sup>+</sup>, V<sub>OUT</sub> = V<sub>S</sub>/2, R<sub>L</sub> = 150 Ω to V<sup>-</sup> unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
<b>FREQUENCY DOMAIN RESPONSE</b>						
SSBW	-3-dB Bandwidth Small Signal	V <sub>OUT</sub> = 0.25 V <sub>PP</sub>		130		MHz
SSBW_1		V <sub>OUT</sub> = 0.25 V <sub>PP</sub> , A <sub>V</sub> = +1		250		
Peak	Peaking	V <sub>OUT</sub> = 0.25 V <sub>PP</sub> , A <sub>V</sub> = +1		2.5		dB
Peak_1	Peaking	V <sub>OUT</sub> = 0.25 V <sub>PP</sub>		0		dB
LSBW	-3-dB Bandwidth Large Signal	V <sub>OUT</sub> = 2 V <sub>PP</sub>		81		MHz
Peak_2	Peaking	V <sub>OUT</sub> = 2 V <sub>PP</sub>		0		dB
0.1 dB BW	0.1-dB Bandwidth	V <sub>OUT</sub> = 2 V <sub>PP</sub>		30		MHz
GBWP_1k	Gain Bandwidth Product	Unity Gain, R <sub>L</sub> = 1 kΩ to V <sub>S</sub> /2		155		MHz
GBWP_150		Unity Gain, R <sub>L</sub> = 150 Ω to V <sub>S</sub> /2		125		
A <sub>VOL</sub>	Large Signal Open-Loop Gain	0.5 V < V <sub>OUT</sub> < 4.5 V	56	66		dB
PBW	Full Power BW	-1 dB, A <sub>V</sub> = +4, V <sub>OUT</sub> = 4.2 V <sub>PP</sub> , R <sub>L</sub> = 150 Ω to V <sub>S</sub> /2		30		MHz
DG	Differential Gain	4.43 MHz, 1.7 V ≤ V <sub>OUT</sub> ≤ 3.3 V, R <sub>L</sub> = 150 Ω to V <sup>-</sup>		0.06%		
DP	Differential Phase	4.43 MHz, 1.7 V ≤ V <sub>OUT</sub> ≤ 3.3 V, R <sub>L</sub> = 150 Ω to V <sup>-</sup>		0.10		deg
<b>TIME DOMAIN RESPONSE</b>						
OS	Overshoot	0.25-V Step		10%		
C <sub>L</sub>	Capacitor Load Tolerance	A <sub>V</sub> = -1, 10% Overshoot, 75 Ω in Series		50		pF

(1) *Electrical Characteristics, 5 V* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

## Electrical Characteristics, 5 V (continued)

Single-Supply with  $V_S = 5\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT	
<b>DISTORTION and NOISE PERFORMANCE</b>								
HD2	Harmonic Distortion (2 <sup>nd</sup> )	2 $V_{PP}$ , 10 MHz			-56		dBc	
HD2_1		4 $V_{PP}$ , 10 MHz, $R_L = 1\text{ k}\Omega$ to $V_S/2$			-61			
HD3	Harmonic Distortion (3 <sup>rd</sup> )	2 $V_{PP}$ , 10 MHz			-73		dBc	
HD3_1		4 $V_{PP}$ , 10 MHz, $R_L = 1\text{ k}\Omega$ to $V_S/2$			-64			
THD	Total Harmonic Distortion	4 $V_{PP}$ , 10 MHz, $R_L = 1\text{ k}\Omega$ to $V_S/2$			-58			
$V_{N1}$	Input Voltage Noise	>10 MHz			7		nV/ $\sqrt{\text{Hz}}$	
$V_{N2}$		1 MHz			10			
$I_N$	Input Current Noise	>1 MHz			50		fA/ $\sqrt{\text{Hz}}$	
<b>STATIC, DC PERFORMANCE</b>								
$V_{IO}$	Input Offset Voltage	At temperature extremes			$\pm 1$	$\pm 2.4$	mV	
$DV_{IO}$	Input Offset Voltage Average Drift	See <sup>(3)</sup>			-5	$\pm 5$		
$I_B$	Input Bias Current	See <sup>(4)</sup>			5	50	pA	
$I_{OS}$	Input Offset Current	See <sup>(4)</sup>			2	25	pA	
$R_{IN}$	Input Resistance	$0\text{ V} \leq V_{IN} \leq 3.5\text{ V}$			10		T $\Omega$	
$C_{IN}$	Input Capacitance				1.3		pF	
+PSRR	Positive Power Supply Rejection Ratio	DC			55	59	dB	
			At temperature extremes		51			
-PSRR	Negative Power Supply Rejection Ratio	DC			53	61	dB	
			At temperature extremes		50			
CMRR	Common-Mode Rejection Ratio	DC			56	68	dB	
			At temperature extremes		53			
CMVR	Input Voltage Range	CMRR > 50 dB (At temperature extremes)		$V^- - 0.20$	-	$V^+ - 1.5$	V	
$I_{CC}$	Supply Current	Normal Operation $V_{OUT} = V_S/2$			9.6	11.5	mA	
		Shutdown $\overline{SD}$ tied to $\leq 0.5\text{ V}$ <sup>(5)</sup>			100			
VOH1	Output High Voltage (Relative to $V^+$ )	$R_L = 150\ \Omega$ to $V^-$			-210	-190	mV	
			At temperature extremes		-480			
VOH2		$R_L = 75\ \Omega$ to $V_S/2$				-190		
VOH3		$R_L = 10\text{ k}\Omega$ to $V^-$			-60	-12		
	At temperature extremes			-110				

(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

(4) This parameter is ensured by design and/or characterization and is not tested in production.

(5)  $\overline{SD}$  logic is CMOS compatible. To ensure proper logic level and to minimize power supply current,  $\overline{SD}$  should typically be less than 10% of total supply voltage away from either supply rail.

**Electrical Characteristics, 5 V (continued)**

 Single-Supply with  $V_S = 5\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
VOL1	Output Low Voltage (Relative to $V^-$ )	$R_L = 150\ \Omega$ to $V^-$	At temperature extremes	5	45	mV
VOL2				120		
VOL3		$R_L = 10\ \text{k}\Omega$ to $V^-$	5	45		
$I_o$	Output Current	$V_{OUT} < 0.6\text{ V}$ from Respective Supply	Source	150	180	mA
$I_{O\_1}$			Sink			
		$V_{OUT} = V_S/2$ , $V_{ID} = \pm 18\text{ mV}$ <sup>(6)</sup>	$\pm 100$			
Load	Output Load Rating	THD $< -30\text{ dBc}$ , $f = 200\text{ kHz}$ , $R_L$ tied to $V_S/2$ , $V_{OUT} = 4\text{ V}_{PP}$	20			$\Omega$
$R_{O\_Enabled}$	Output Resistance	Enabled, $A_V = +1$	0.2			$\Omega$
$R_{O\_Disabled}$	Output Resistance	Shutdown	$> 100$			M $\Omega$
$C_{O\_Disabled}$	Output Capacitance	Shutdown	5			pF
<b>MISCELLANEOUS PERFORMANCE</b>						
VDMAX	Voltage Limit for Disable (Pin 5)	See <sup>(5)</sup> (At temperature extremes)	0		0.5	V
VDMIN	Voltage Limit for Enable (Pin 5)	See <sup>(5)</sup> (At temperature extremes)	4.5		5	V
$I_i$	Logic Input Current (Pin 5)	$\overline{SD} = 5\text{ V}$ <sup>(5)</sup>	10			pA
$V_{glitch}$	Turnon Glitch		2.2			V
Isolation <sub>OFF</sub>	Off Isolation	1 MHz, $R_L = 1\ \text{k}\Omega$	60			dB

(6) “ $V_{ID}$ ” is input differential voltage (input overdrive).

**6.7 Electrical Characteristics, 3.3 V**

 Single-Supply with  $V_S = 3.3\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
<b>FREQUENCY DOMAIN RESPONSE</b>						
SSBW	–3-dB Bandwidth Small Signal	$V_{OUT} = 0.25\text{ V}_{PP}$	125		250	MHz
SSBW <sub>_1</sub>		$V_{OUT} = 0.25\text{ V}_{PP}$ , $A_V = +1$				
Peak	Peaking	$V_{OUT} = 0.25\text{ V}_{PP}$ , $A_V = +1$	3			dB
Peak <sub>_1</sub>	Peaking	$V_{OUT} = 0.25\text{ V}_{PP}$	0.05			dB
LSBW	–3-dB Bandwidth Large Signal	$V_{OUT} = 2\text{ V}_{PP}$	75			MHz
Peak <sub>_2</sub>	Peaking	$V_{OUT} = 2\text{ V}_{PP}$	0			dB
0.1 dB BW	0.1-dB Bandwidth	$V_{OUT} = 2\text{ V}_{PP}$	30			MHz
GBWP <sub>_1k</sub>	Gain Bandwidth Product	Unity Gain, $R_L = 1\ \text{k}\Omega$ to $V_S/2$	115		105	MHz
GBWP <sub>_150</sub>		Unity Gain, $R_L = 150\ \Omega$ to $V_S/2$				
$A_{VOL}$	Large Signal Open-Loop Gain	$0.3\text{ V} < V_{OUT} < 3\text{ V}$	56	67		dB
PBW	Full Power BW	–1 dB, $A_V = +4$ , $V_{OUT} = 2.8\text{ V}_{PP}$ , $R_L = 150\ \Omega$ to $V_S/2$	30			MHz
DG	Differential Gain	4.43 MHz, $0.85\text{ V} \leq V_{OUT} \leq 2.45\text{ V}$ , $R_L = 150\ \Omega$ to $V^-$	0.06%			
DP	Differential Phase	4.43 MHz, $0.85\text{ V} \leq V_{OUT} \leq 2.45\text{ V}$ , $R_L = 150\ \Omega$ to $V^-$	0.23			deg

- (1) *Electrical Characteristics, 3.3 V* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

## Electrical Characteristics, 3.3 V (continued)

Single-Supply with  $V_S = 3.3$  V,  $A_V = +2$ ,  $R_F = 604\Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
<b>TIME DOMAIN RESPONSE</b>						
OS	Overshoot	0.25-V Step		10%		
$C_L$	Capacitor Load Tolerance	$A_V = -1$ , 10% Overshoot, 82 $\Omega$ in Series		50		pF
<b>DISTORTION and NOISE PERFORMANCE</b>						
HD2	Harmonic Distortion (2 <sup>nd</sup> )	2 $V_{PP}$ , 10 MHz		-61		dBc
HD2_1		2 $V_{PP}$ , 10 MHz $R_L = 1\ \text{k}\Omega$ to $V_S/2$		-79		
HD3	Harmonic Distortion (3 <sup>rd</sup> )	2 $V_{PP}$ , 10 MHz		-53		dBc
HD3_2		2 $V_{PP}$ , 10 MHz $R_L = 1\ \text{k}\Omega$ to $V_S/2$		-69		
THD	Total Harmonic Distortion	2 $V_{PP}$ , 10 MHz $R_L = 1\ \text{k}\Omega$ to $V_S/2$		-66		dBc
$V_{N1}$	Input Voltage Noise	>10 MHz		7		nV/ $\sqrt{\text{Hz}}$
$V_{N2}$		1 MHz		10		
$I_N$	Input Current Noise	>1 MHz		50		fA/ $\sqrt{\text{Hz}}$
<b>STATIC, DC PERFORMANCE</b>						
$V_{IO}$	Input Offset Voltage			$\pm 1$	$\pm 2.6$	mV
		At temperature extremes			$\pm 5.5$	
$DV_{IO}$	Input Offset Voltage Average Drift	See <sup>(3)</sup>		-4.5		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	See <sup>(4)</sup>		5	50	pA
$I_{OS}$	Input Offset Current	See <sup>(4)</sup>		2	25	pA
$R_{IN}$	Input Resistance	$0\ \text{V} \leq V_{IN} \leq 1.8\ \text{V}$		15		T $\Omega$
$C_{IN}$	Input Capacitance			1.4		pF
+PSRR	Positive Power Supply Rejection Ratio	DC	61	80		dB
		At temperature extremes	51			
-PSRR	Negative Power Supply Rejection Ratio	DC	57	72		dB
		At temperature extremes	52			
CMRR	Common-Mode Rejection Ratio	DC	58	73		dB
		At temperature extremes	55			
CMVR	Input Voltage	CMRR > 50 dB (At temperature extremes)	$V^- - 0.20$		$V^+ - 1.5$	V
$I_{CC}$	Supply Current	Normal Operation $V_{OUT} = V_S/2$		9.2	11	mA
		At temperature extremes			13	
		Shutdown: $\overline{SD}$ tied to $\leq 0.33\ \text{V}$ <sup>(5)</sup>		100		nA
VOH1	Output High Voltage (Relative to $V^+$ )	$R_L = 150\ \Omega$ to $V^-$		-210	-190	mV
			At temperature extremes	-360		
VOH2		$R_L = 75\ \Omega$ to $V_S/2$			-190	
VOH3		$R_L = 10\ \text{k}\Omega$ to $V^-$		-50	-10	
	At temperature extremes		-100			

(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

(4) This parameter is ensured by design and/or characterization and is not tested in production.

(5)  $\overline{SD}$  logic is CMOS compatible. To ensure proper logic level and to minimize power supply current,  $\overline{SD}$  should typically be less than 10% of total supply voltage away from either supply rail.

## Electrical Characteristics, 3.3 V (continued)

Single-Supply with  $V_S = 3.3\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
VOL1	Output Low Voltage (Relative to $V^-$ )	$R_L = 150\ \Omega$ to $V^-$	At temperature extremes		4	45	mV
VOL2						125	
VOL3		$R_L = 75\ \Omega$ to $V_S/2$			105		
$I_O$	Output Current	$V_{OUT} < 0.6\text{ V}$ from Respective Supply	Source		50		mA
			Sink		75		
$I_{O\_1}$					$\pm 75$		
Load	Output Load Rating	THD < -30 dBc, $f = 200\text{ kHz}$ , $R_L$ tied to $V_S/2$ , $V_{OUT} = 2.6\text{ V}_{PP}$			25		$\Omega$
$R_{O\_Enabled}$	Output Resistance	Enabled, $A_V = +1$			0.2		$\Omega$
$R_{O\_Disabled}$	Output Resistance	Shutdown			>100		M $\Omega$
$C_{O\_Disabled}$	Output Capacitance	Shutdown			5.6		pF
<b>MISCELLANEOUS PERFORMANCE</b>							
VDMAX	Voltage Limit for Disable (Pin 5)	See <sup>(5)</sup> (At temperature extremes)		0		0.33	V
VDMIN	Voltage Limit for Enable (Pin 5)	See <sup>(5)</sup> (At temperature extremes)		2.97		3.3	V
$I_i$	Logic Input Current (Pin 5)	$\overline{SD} = 3.3\text{ V}^{(5)}$			8		pA
$V_{glitch}$	Turnon Glitch				1.6		V
$Isolation_{OFF}$	Off Isolation	1 MHz, $R_L = 1\text{ k}\Omega$			60		dB

(6) " $V_{ID}$ " is input differential voltage (input overdrive).

## 6.8 Electrical Characteristics, 2.7 V

Single-Supply with  $V_S = 2.7\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
<b>FREQUENCY DOMAIN RESPONSE</b>							
SSBW	-3-dB Bandwidth Small Signal	$V_{OUT} = 0.25\text{ V}_{PP}$			120		MHz
SSBW_1		$V_{OUT} = 0.25\text{ V}_{PP}$ , $A_V = +1$			250		
Peak	Peaking	$V_{OUT} = 0.25\text{ V}_{PP}$ , $A_V = +1$			3.1		dB
Peak_1	Peaking	$V_{OUT} = 0.25\text{ V}_{PP}$			0.1		dB
LSBW	-3-dB Bandwidth Large Signal	$V_{OUT} = 2\text{ V}_{PP}$			73		MHz
Peak_2	Peaking	$V_{OUT} = 2\text{ V}_{PP}$			0		dB
0.1 dB BW	0.1-dB Bandwidth	$V_{OUT} = 2\text{ V}_{PP}$			30		MHz
GBWP_1k	Gain Bandwidth Product	Unity Gain, $R_L = 1\text{ k}\Omega$ to $V_S/2$			110		MHz
GBWP_150		Unity Gain, $R_L = 150\ \Omega$ to $V_S/2$			81		
$A_{VOL}$	Large Signal Open-Loop Gain	$0.25\text{ V} < V_{OUT} < 2.5\text{ V}$		56	65		dB
PBW	Full Power BW	-1 dB, $A_V = +4$ , $V_{OUT} = 2\text{ V}_{PP}$ , $R_L = 150\ \Omega$ to $V_S/2$			13		MHz
DG	Differential Gain	4.43 MHz, $0.45\text{ V} \leq V_{OUT} \leq 2.05\text{ V}$ , $R_L = 150\ \Omega$ to $V^-$			0.12%		

- (1) *Electrical Characteristics, 2.7 V* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.



**Electrical Characteristics, 2.7 V (continued)**

Single-Supply with  $V_S = 2.7\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
DP	Differential Phase	4.43 MHz, $0.45\text{ V} \leq V_{OUT} \leq 2.05\text{ V}$ $R_L = 150\ \Omega$ to $V^-$		0.62		deg
<b>TIME DOMAIN RESPONSE</b>						
OS	Overshoot	0.25-V Step		10%		
<b>DISTORTION and NOISE PERFORMANCE</b>						
HD2	Harmonic Distortion (2 <sup>nd</sup> )	1 $V_{PP}$ , 10 MHz		-58		dBc
HD3	Harmonic Distortion (3 <sup>rd</sup> )	1 $V_{PP}$ , 10 MHz		-60		dBc
$V_{N1}$	Input Voltage Noise	>10 MHz		8.4		nV/ $\sqrt{\text{Hz}}$
$V_{N2}$		1 MHz		12		
$I_N$	Input Current Noise	>1 MHz		50		fA/ $\sqrt{\text{Hz}}$
<b>STATIC, DC PERFORMANCE</b>						
$V_{IO}$	Input Offset Voltage			$\pm 1$	$\pm 3.5$	mV
		At temperature extremes			$\pm 6.5$	
$DV_{IO}$	Input Offset Voltage Average Drift	See <sup>(3)</sup>		-6.5		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	See <sup>(4)</sup>		5	50	pA
$I_{OS}$	Input Offset Current	See <sup>(4)</sup>		2	25	pA
$R_{IN}$	Input Resistance	$0\text{ V} \leq V_{IN} \leq 1.2\text{ V}$		20		T $\Omega$
$C_{IN}$	Input Capacitance			1.6		pF
+PSRR	Positive Power Supply Rejection Ratio	DC		58	68	dB
			At temperature extremes		53	
-PSRR	Negative Power Supply Rejection Ratio	DC		56	69	dB
			At temperature extremes		53	
CMRR	Common-Mode Rejection Ratio	DC		57	77	dB
			At temperature extremes		52	
CMVR	Input Voltage	CMRR > 50 dB (At temperature extremes)	$V^- - 0.20$	-	$V^+ - 1.5$	V
$I_{CC}$	Supply Current	Normal Operation $V_{OUT} = V_S/2$		9	10.6	mA
			At temperature extremes			
		Shutdown $\overline{SD}$ tied to $\leq 0.27\text{ V}$ <sup>(5)</sup>		100		nA
VOH1	Output High Voltage (Relative to $V^+$ )	$R_L = 150\ \Omega$ to $V^-$		-260	-200	mV
			At temperature extremes		-420	
VOH2		$R_L = 75\ \Omega$ to $V_S/2$		-200		
VOH3		$R_L = 10\ \text{k}\Omega$ to $V^-$		-50	-10	
	At temperature extremes			100		

(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

(4) This parameter is ensured by design and/or characterization and is not tested in production.

(5)  $\overline{SD}$  logic is CMOS compatible. To ensure proper logic level and to minimize power supply current,  $\overline{SD}$  should typically be less than 10% of total supply voltage away from either supply rail.

## Electrical Characteristics, 2.7 V (continued)

Single-Supply with  $V_S = 2.7\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(2)</sup>	MAX <sup>(2)</sup>	UNIT
VOL1	Output Low Voltage (Relative to $V^-$ )	$R_L = 150\ \Omega$ to $V^-$			4	45	mV
VOL2						125	
VOL3		$R_L = 10\ \text{k}\Omega$ to $V^-$	At temperature extremes		4	45	
$I_O$	Output Current	$V_{OUT} \leq 0.6\text{ V}$ from Respective Supply	Source		25		mA
$I_{O-1}$			Sink		62		
			Source	25			
			Sink	35			
Load	Output Load Rating	THD < -30 dBc, $f = 200\ \text{kHz}$ , $R_L$ tied to $V_S/2$ , $V_{OUT} = 2.2\ V_{PP}$			40		$\Omega$
$R_{O\_Enable}$	Output Resistance	Enabled, $A_V = +1$			0.2		$\Omega$
$R_{O\_Disabled}$	Output Resistance	Shutdown			>100		M $\Omega$
$C_{O\_Disabled}$	Output Capacitance	Shutdown			5.6		pF
<b>MISCELLANEOUS PERFORMANCE</b>							
VDMAX	Voltage Limit for Disable (Pin 5)	See <sup>(5)</sup> (At temperature extremes)		0		0.27	V
VDMIN	Voltage Limit for Enable (Pin 5)	See <sup>(5)</sup> (At temperature extremes)		2.43		2.7	V
$I_i$	Logic Input Current (Pin 5)	$\overline{SD} = 2.7\text{ V}$ <sup>(5)</sup>			4		pA
$V_{\_glitch}$	Turnon Glitch				1.2		V
Isolation <sub>OFF</sub>	Off Isolation	1 MHz, $R_L = 1\ \text{k}\Omega$			60		dB

(6) " $V_{ID}$ " is input differential voltage (input overdrive).

## 6.9 Switching Characteristics, 5 V

Single-Supply with  $V_S = 5\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>TIME DOMAIN RESPONSE</b>							
TRS/TRL	Rise and Fall Time	0.25-V Step			2.6		ns
SR	Slew Rate	2-V Step			275		V/ $\mu\text{s}$
$T_S$	Settling Time	1-V Step, $\pm 0.1\%$			50		ns
$T_{S-1}$		1-V Step, $\pm 0.02\%$			220		
PD	Propagation Delay	Input to Output, 250-mV Step, 50%			2.4		ns
<b>MISCELLANEOUS PERFORMANCE</b>							
$T_{on}$	Turnon Time				1.4		$\mu\text{s}$
$T_{off}$	Turnoff Time				520		ns
$T_{OL}$	Overload Recovery				<20		ns

## 6.10 Switching Characteristics, 3.3 V

Single-Supply with  $V_S = 3.3\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIME DOMAIN RESPONSE</b>						
TRS/TRL	Rise and Fall Time	0.25-V Step		2.7		ns
SR	Slew Rate	2-V Step		260		V/ $\mu$ s
$T_S$	Settling Time	1-V Step, $\pm 0.1\%$		70		ns
$T_{S,1}$		1-V Step, $\pm 0.02\%$		300		
PD	Propagation Delay	Input to Output, 250-mV Step, 50%		2.6		ns
<b>MISCELLANEOUS PERFORMANCE</b>						
$T_{on}$	Turnon Time			3.5		$\mu$ s
$T_{off}$	Turnoff Time			500		ns

- (1) *Electrical Characteristics, 3.3 V* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .

## 6.11 Switching Characteristics, 2.7 V

Single-Supply with  $V_S = 2.7\text{ V}$ ,  $A_V = +2$ ,  $R_F = 604\ \Omega$ ,  $\overline{SD}$  tied to  $V^+$ ,  $V_{OUT} = V_S/2$ ,  $R_L = 150\ \Omega$  to  $V^-$  unless otherwise specified.<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIME DOMAIN RESPONSE</b>						
TRS/TRL	Rise and Fall Time	0.25-V Step		2.7		ns
SR	Slew Rate	2-V Step		260		V/ $\mu$ s
$T_S$	Settling Time	1-V Step, $\pm 0.1\%$		147		ns
$T_{S,1}$		1-V Step, $\pm 0.02\%$		410		
PD	Propagation Delay	Input to Output, 250-mV Step, 50%		3.4		ns
<b>MISCELLANEOUS PERFORMANCE</b>						
$T_{on}$	Turnon Time			5.2		$\mu$ s
$T_{off}$	Turnoff Time			760		ns

- (1) *Electrical Characteristics, 2.7 V* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .

### 6.12 Typical Characteristics

Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .

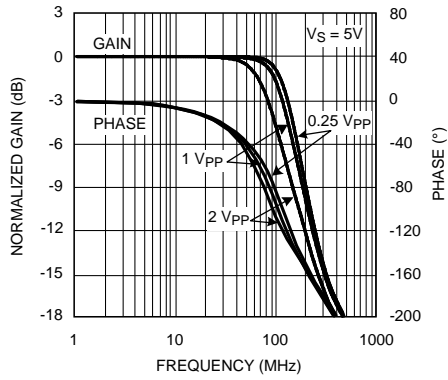


Figure 1. Frequency Response for Various Output Amplitudes

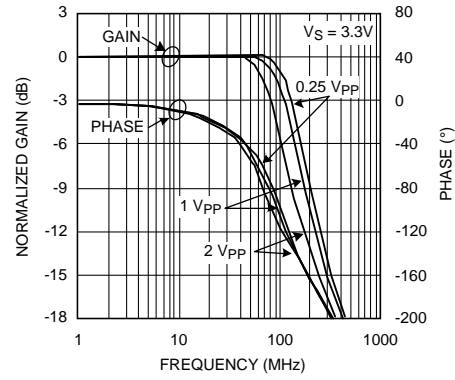


Figure 2. Frequency Response for Various Output Amplitudes

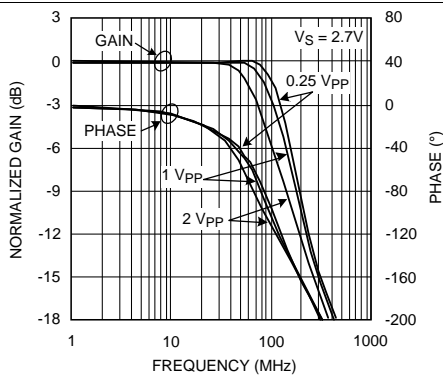


Figure 3. Frequency Response for Various Output Amplitudes

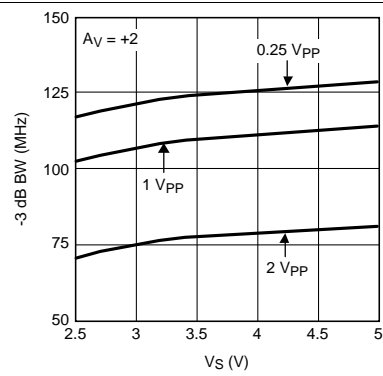


Figure 4. -3 dB BW vs. Supply Voltage for Various Output Swings

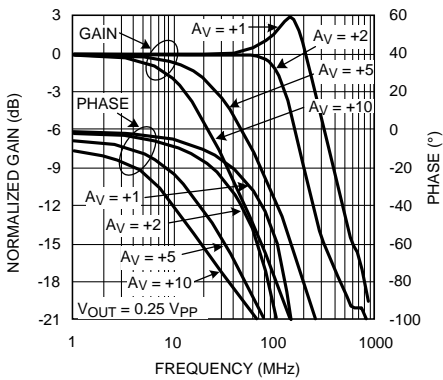


Figure 5. Noninverting Frequency Response for Various Gain

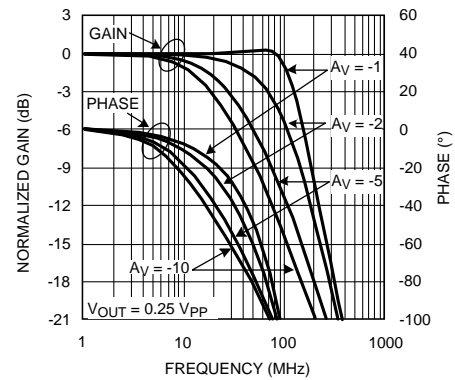


Figure 6. Inverting Frequency Response for Various Gain

Typical Characteristics (continued)

Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .

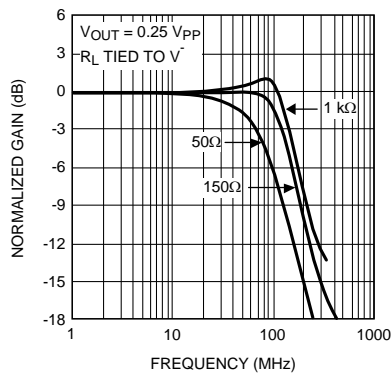


Figure 7. Frequency Response for Various Loads

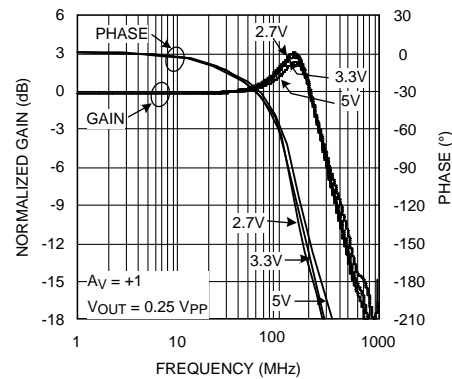


Figure 8. Frequency Response for Various Supply Voltages

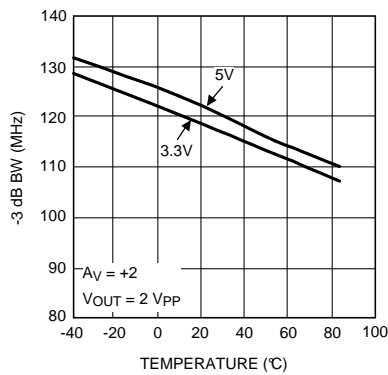


Figure 9. -3 dB BW vs. Ambient Temperature

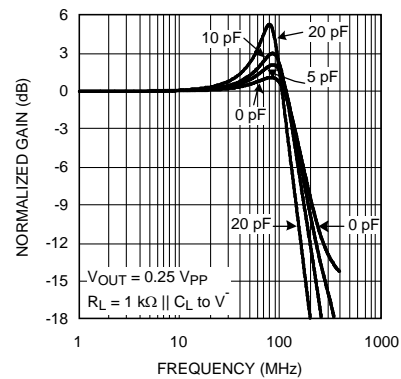


Figure 10. Frequency Response for Various Capacitor Load

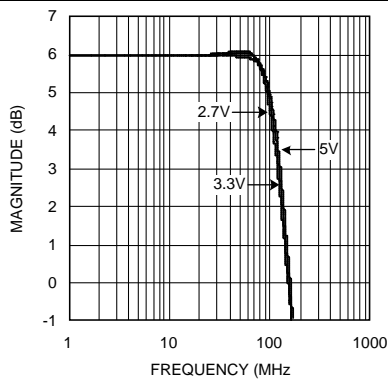


Figure 11. Frequency Response for Various Supply Voltage

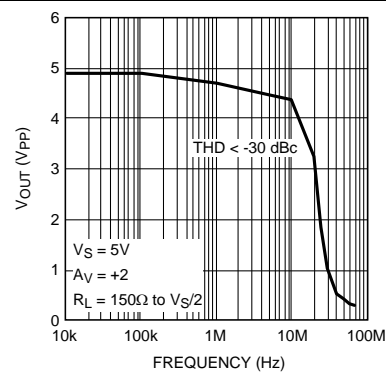


Figure 12. Maximum Output Swing vs. Frequency

### Typical Characteristics (continued)

Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .

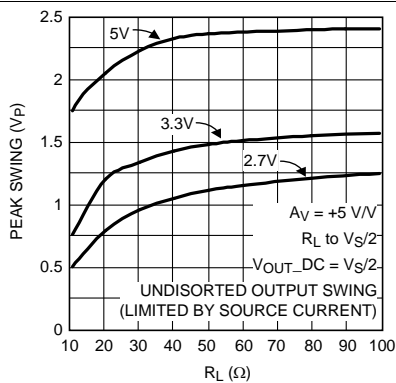


Figure 13. Peak Output Swing vs.  $R_L$

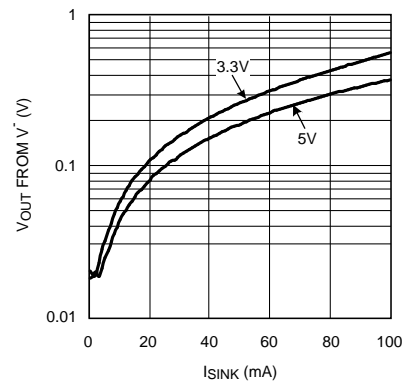


Figure 14. Output Swing vs. Sink Current for Various Supply Voltages

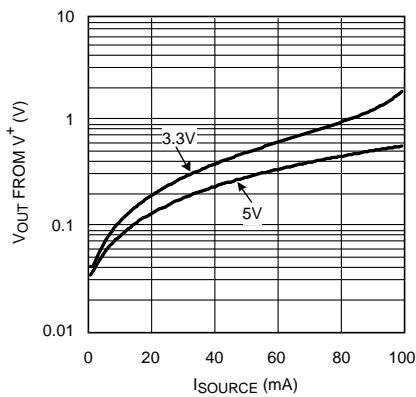


Figure 15. Output Swing vs. Source Current for Various Supply Voltages

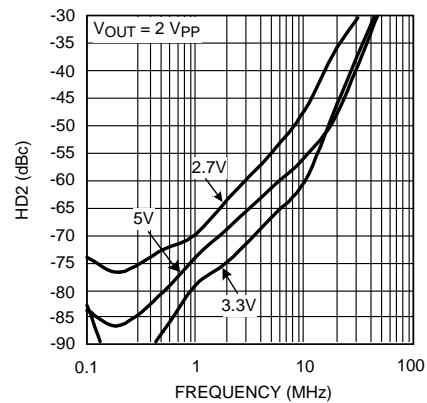


Figure 16. HD2 vs. Frequency

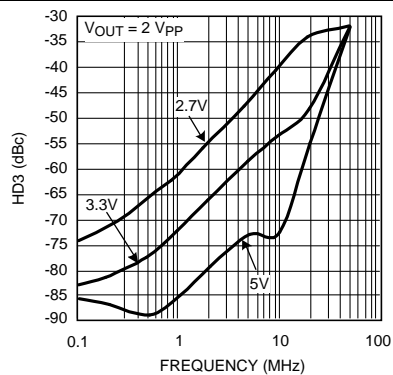


Figure 17. HD3 vs. Frequency

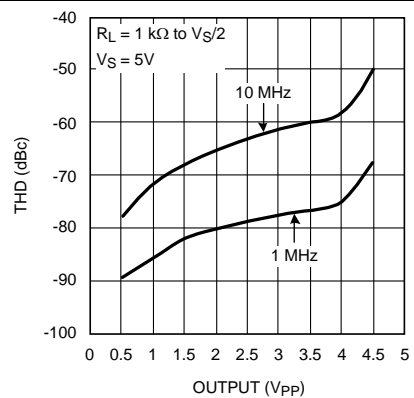


Figure 18. THD vs. Output Swing

Typical Characteristics (continued)

Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .

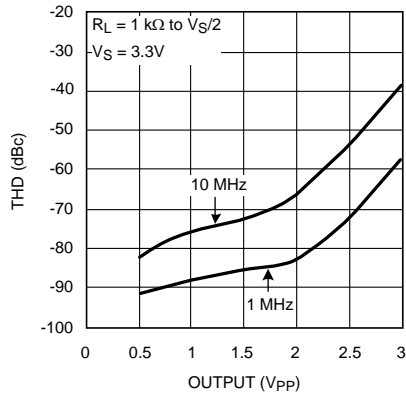


Figure 19. THD vs. Output Swing

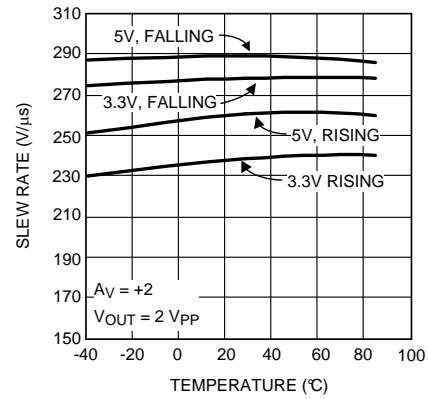


Figure 20. Slew Rate vs. Ambient Temperature

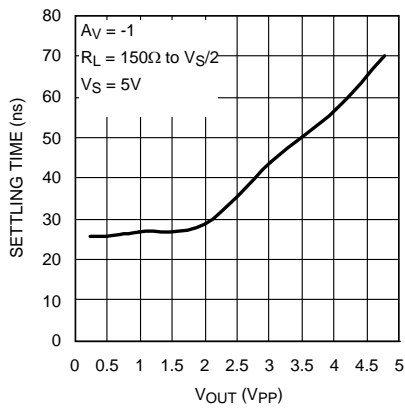


Figure 21. Settling Time ( $\pm 1\%$ ) vs. Output Swing

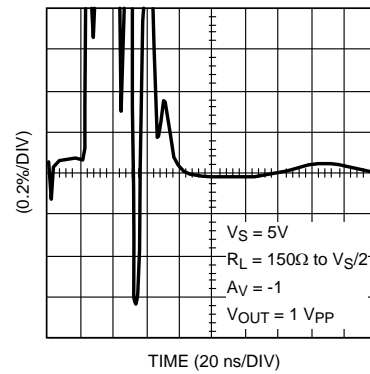


Figure 22. Output Settling

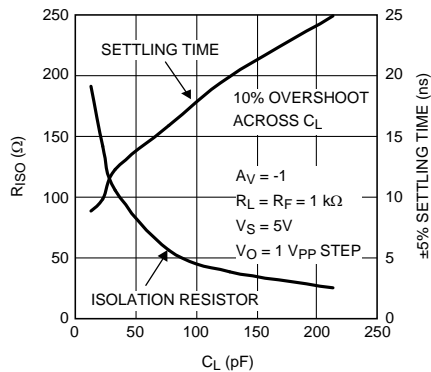


Figure 23. Isolation Resistor and Settling Time vs.  $C_L$

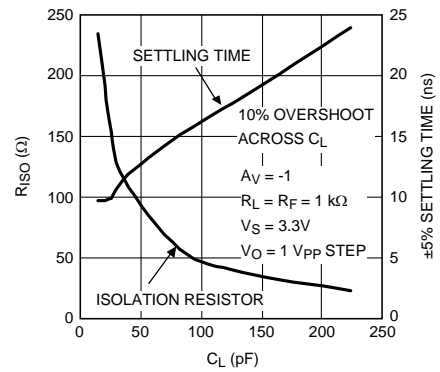


Figure 24. Isolation Resistor and Settling Time vs.  $C_L$

Typical Characteristics (continued)

Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .

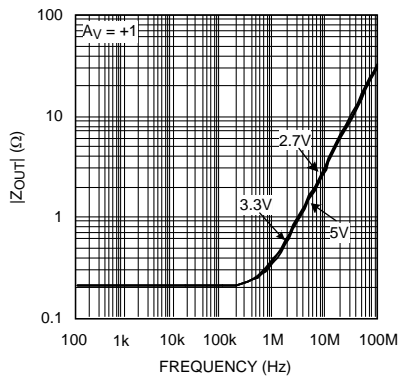


Figure 25. Closed-Loop Output Impedance vs. Frequency for Various Supply Voltages

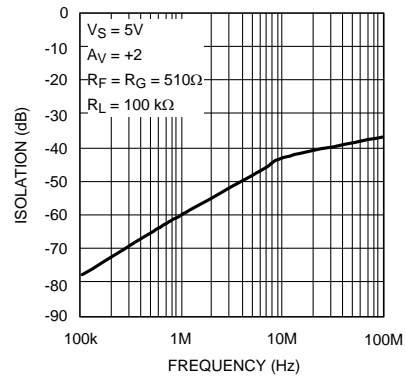


Figure 26. Off Isolation vs. Frequency

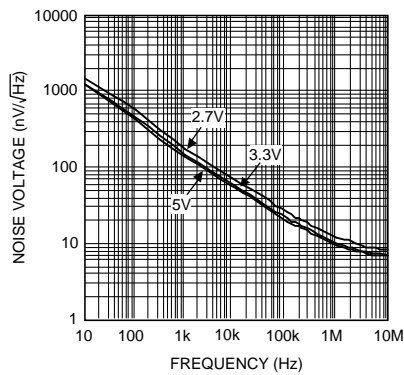


Figure 27. Noise Voltage vs. Frequency

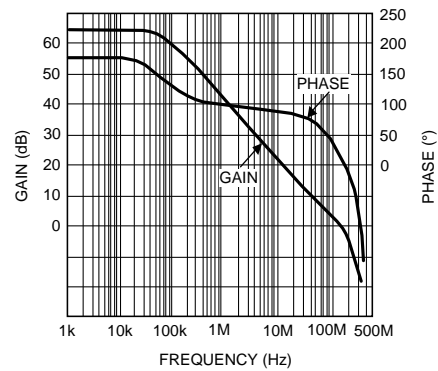


Figure 28. Open-Loop Gain and Phase

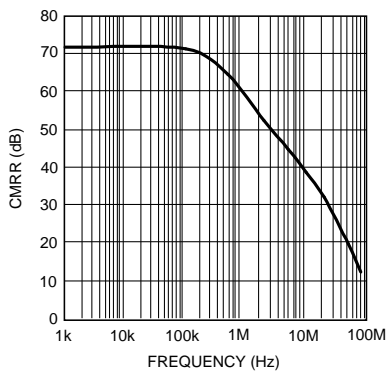


Figure 29. CMRR vs. Frequency

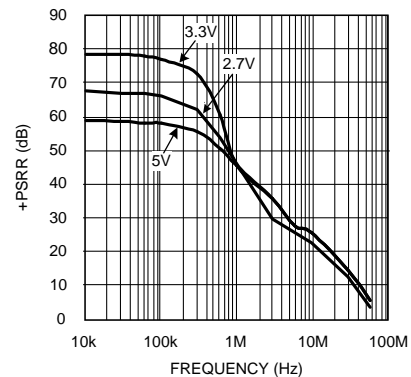
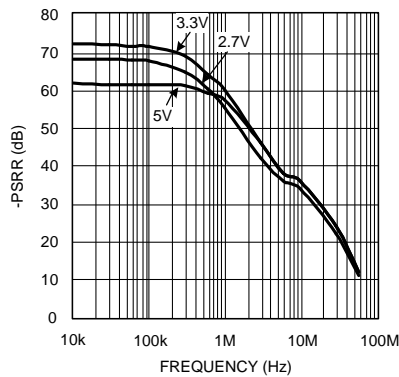


Figure 30. +PSRR vs. Frequency

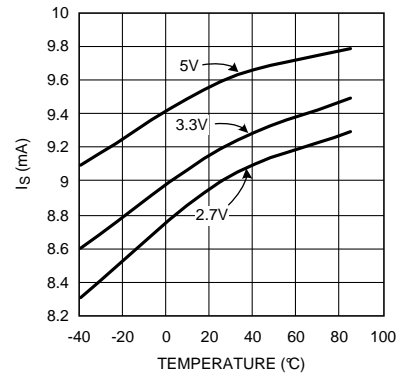


**Typical Characteristics (continued)**

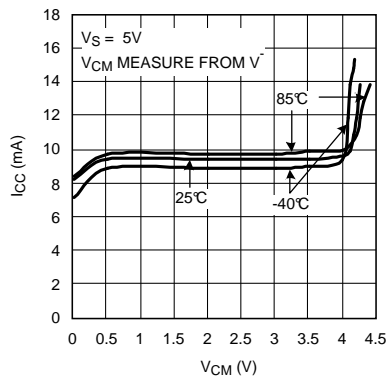
Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .



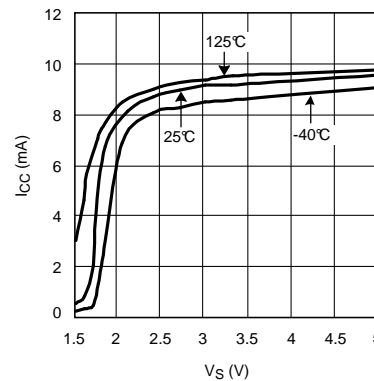
**Figure 31. -PSRR vs. Frequency**



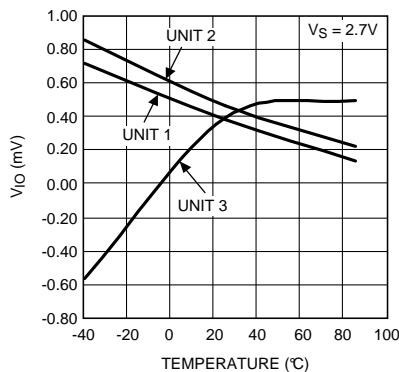
**Figure 32. Supply Current vs. Ambient Temperature**



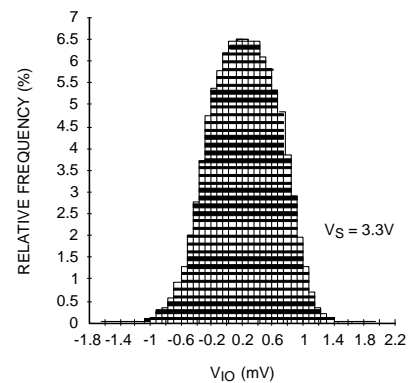
**Figure 33. Supply Current vs.  $V_{CM}$**



**Figure 34. Supply Current vs. Supply Voltage**



**Figure 35. Offset Voltage vs. Ambient Temperature for 3 Representative Units**



**Figure 36. Offset Voltage Distribution**

### Typical Characteristics (continued)

Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .

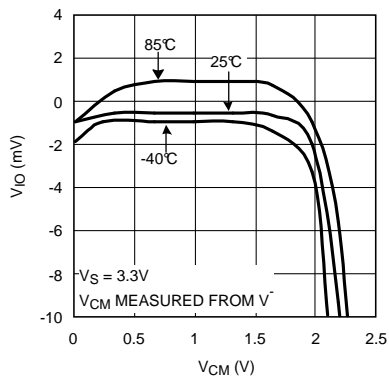


Figure 37. Offset Voltage vs.  $V_{CM}$  (Typical Part)

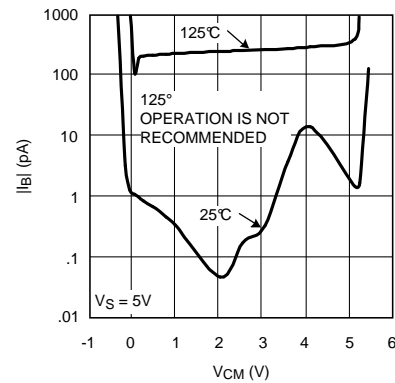


Figure 38. Input Bias Current vs. Common Mode Voltage

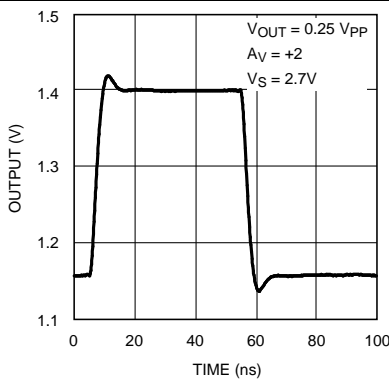


Figure 39. Small Signal Step Response

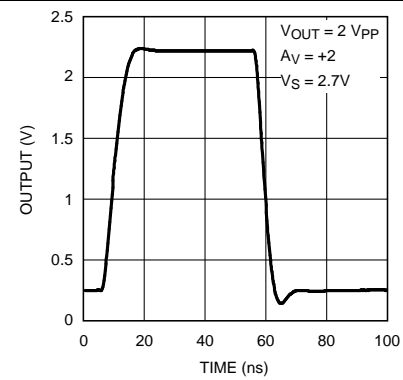


Figure 40. Large Signal Step Response

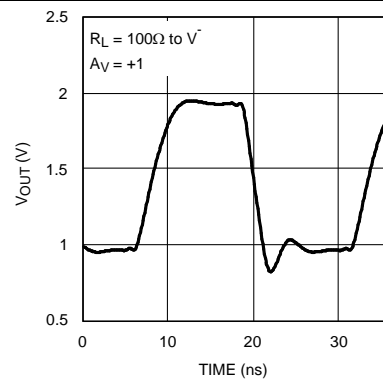


Figure 41. Large Signal Step Response

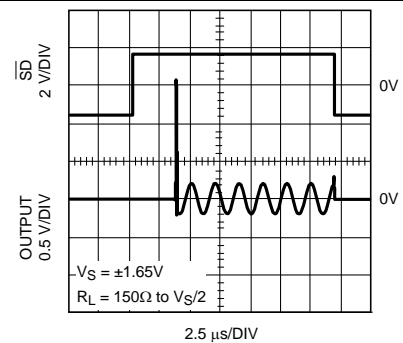


Figure 42. Turn On/Off Waveform

Typical Characteristics (continued)

Unless otherwise noted, all data is with  $A_V = +2$ ,  $R_F = R_G = 604 \Omega$ ,  $V_S = 3.3V$ ,  $V_{OUT} = V_S/2$ ,  $\overline{SD}$  tied to  $V^+$ ,  $R_L = 150 \Omega$  to  $V^-$ ,  $T = 25^\circ C$ .

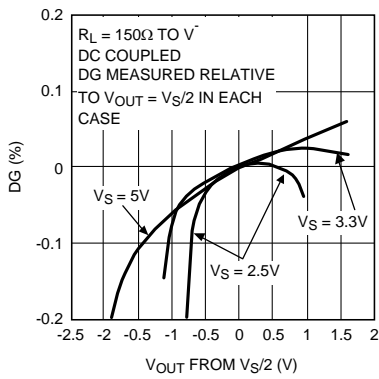


Figure 43. DG vs.  $V_{OUT}$  for Various  $V_S$

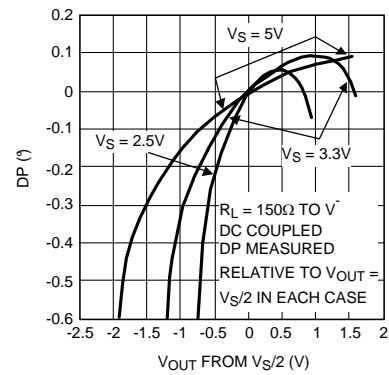


Figure 44. DP vs.  $V_{OUT}$  for Various  $V_S$

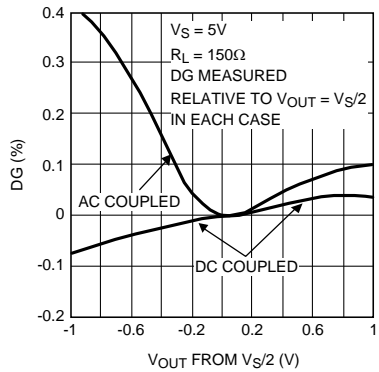


Figure 45. DG vs.  $V_{OUT}$   
(DC- and AC-Coupled Load Compared)

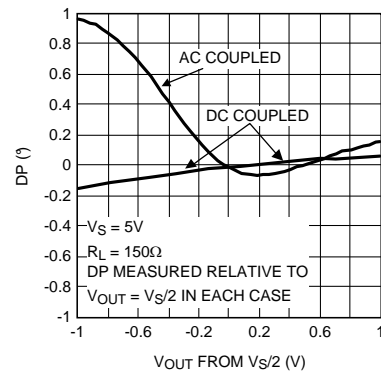


Figure 46. DP vs.  $V_{OUT}$   
(DC- and AC-Coupled Load Compared)

## 7 Detailed Description

### 7.1 Overview

The high-speed, ultra-high input impedance of the LMH6601 and its fast slew rate make the device an ideal choice for video amplifier and buffering applications. There are cost benefits in having a single operating supply. Single-supply video systems can take advantage of the low supply voltage operation of the LMH6601 along with its ability to operate with input common-mode voltages at or slightly below the  $V^-$  rail. Additional cost savings can be achieved by eliminating or reducing the value of the input and output AC-coupling capacitors commonly employed in single-supply video applications.

### 7.2 Feature Description

#### 7.2.1 Shutdown Capability and Turn On/Off Behavior

With the device in shutdown mode, the output goes into high-impedance ( $R_{OUT} > 100\text{ M}\Omega$ ) mode. In this mode, the only path between the inputs and the output pin is through the external components around the device. So, for applications where there is active signal connection to the inverting input, with the LMH6601 in shutdown, the output could show signal swings due to current flow through these external components. For noninverting amplifiers in shutdown, no output swings would occur, because of complete input-output isolation, with the exception of capacitive coupling.

For maximum power saving, the LMH6601 supply current drops to around  $0.1\text{ }\mu\text{A}$  in shutdown. All significant power consumption within the device is disabled for this purpose. Because of this, the LMH6601 turnon time is measured in microseconds whereas its turnoff is fast (nanoseconds) as would be expected from a high speed device like this.

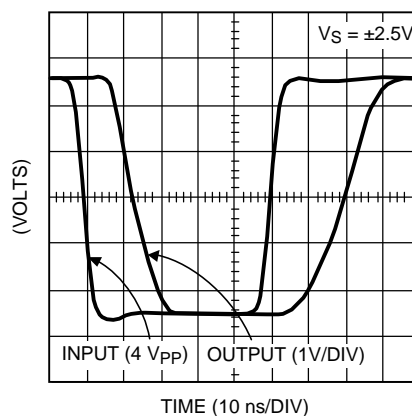
The LMH6601  $\overline{\text{SD}}$  pin is a CMOS compatible input with a pico-ampere range input current drive requirement. This pin must be tied to a level or otherwise the device state would be indeterminate. The device shutdown threshold is half way between the  $V^+$  and  $V^-$  pin potentials at any supply voltage. For example, with  $V^+$  tied to 10 V and  $V^-$  equal to 5 V, you can expect the threshold to be at 7.5 V. The state of the device (shutdown or normal operation) is ensured over temperature as long as the  $\overline{\text{SD}}$  pin is held to within 10% of the total supply voltage.

For  $V^+ = 10\text{ V}$ ,  $V^- = 5\text{ V}$ , as an example:

- Shutdown Range  $5\text{ V} \leq \overline{\text{SD}} \leq 5.5\text{ V}$
- Normal Operation Range  $9.5\text{ V} \leq \overline{\text{SD}} \leq 10\text{ V}$

#### 7.2.2 Overload Recovery and Swing Close to Rails

The LMH6601 can recover from an output overload in less than 20 ns. See [Figure 47](#) for the input and output scope photos:



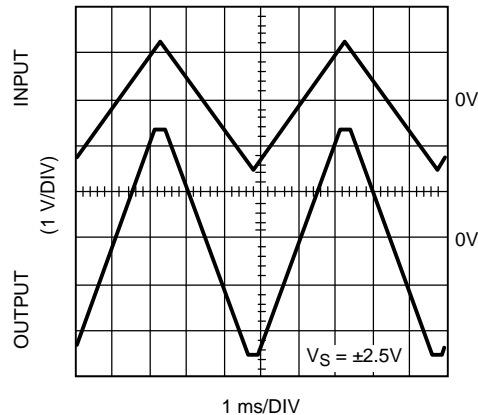
**Figure 47. LMH6601 Output Overload Recovery Waveform**

In [Figure 47](#), the input step function is set so that the output is driven to one rail and then the other and then the output recovery is measured from the time the input crosses 0 V to when the output reaches this point.

## Feature Description (continued)

Also, when the LMH6601 input voltage range is exceeded near the  $V^+$  rail, the output does not experience output phase reversal, as do some op amps. This is particularly advantageous in applications where output phase reversal must be avoided at all costs, such as in servo loop control among others. This adds to the set of features of the LMH6601, which make this device easy to use.

In addition, the LMH6601 output swing close to either rail is well-behaved as shown in the scope photo of [Figure 48](#).



**Figure 48. Clean Swing of the LMH6601 to Either Rail**

With some op amps, when the output approaches either one or both rails and saturation starts to set in, there is significant increase in the transistor parasitic capacitances which leads to loss of Phase Margin. That is why with these devices, there are sometimes hints of instability with output close to the rails. With the LMH6601, as can be seen in [Figure 48](#), the output waveform remains free of instability throughout its range of voltages.

## 7.3 Device Functional Modes

### 7.3.1 Optimizing Performance

With many op amps, additional device nonlinearity and sometimes less loop stability arises when the output must switch from current-source mode to current-sink mode or vice versa. When it comes to achieving the lowest distortion and the best Differential Gain/ Differential Phase (DG/ DP, broadcast video specs), the LMH6601 is optimized for single-supply DC-coupled output applications where the load current is returned to the negative rail ( $V^-$ ). That is where the output stage is most linear (lowest distortion) and which corresponds to unipolar current flowing out of this device. To that effect, it is easy to see that the distortion specifications improve when the output is only sourcing current which is the distortion-optimized mode of operation for the LMH6601. In an application where the LMH6601 output is AC-coupled or when it is powered by separate dual supplies for  $V^+$  and  $V^-$ , the output stage supplies both source and sink current to the load and results in less than optimum distortion (and DG/DP). [Figure 49](#) compares the distortion results between a DC- and an AC-coupled load to show the magnitude of this difference. See the DG/DP plots, [Figure 43](#) through [Figure 46](#), in [Typical Characteristics](#), for a comparison between DC- and AC-coupling of the video load.

Device Functional Modes (continued)

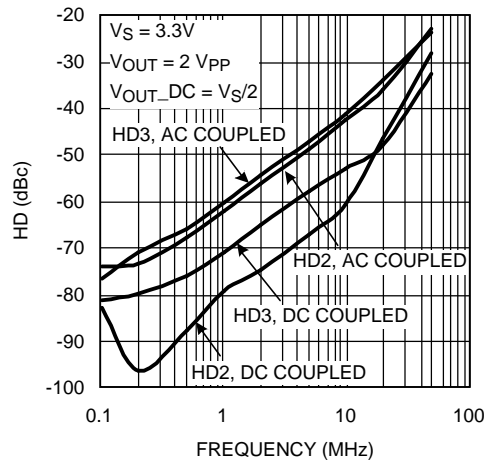


Figure 49. Distortion Comparison between DC- and AC-Coupling of the Load

In certain applications, it may be possible to optimize the LMH6601 for best distortion (and DG/DP) even though the load may require bipolar output current by adding a pulldown resistor to the output. Adding an output pulldown resistance of appropriate value could change the LMH6601 output loading into source-only. This comes at the price of higher total power dissipation and increased output current requirement.

Figure 50 shows how to calculate the pulldown resistor value for both the dual-supply and for the AC-coupled load applications.

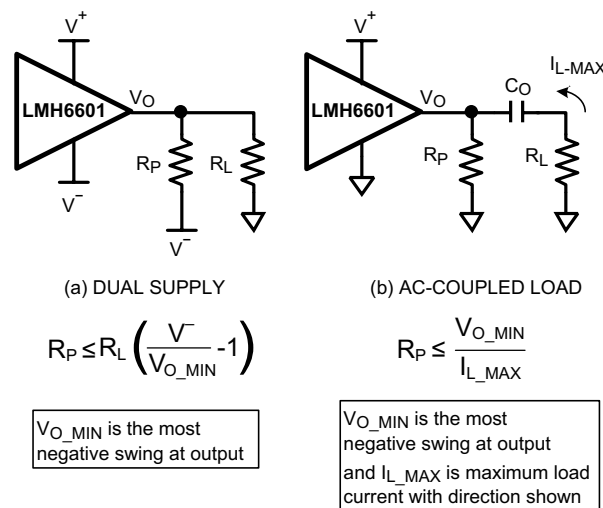


Figure 50. Output Pulldown Value for Dual-Supply and AC-Coupling

Furthermore, with a combination of low closed-loop gain setting (that is,  $A_V = +1$  for example where device bandwidth is the highest), light output loading ( $R_L > 1 \text{ k}\Omega$ ), and with a significant capacitive load ( $C_L > 10 \text{ pF}$ ), the LMH6601 is most stable if output sink current is kept to less than about 5 mA. The pulldown method described in Figure 50 is applicable in these cases as well where the current that would normally be sunk by the op amp is diverted to the  $R_P$  path instead.

## 8 Application and Implementation

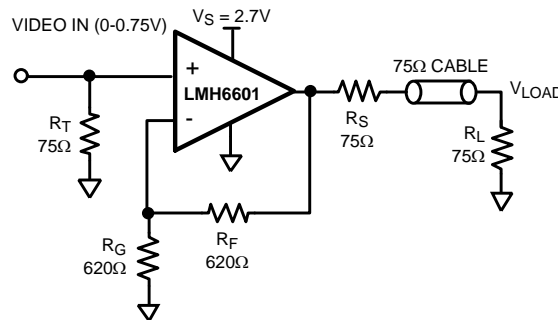
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 DC-Coupled, Single-Supply Baseband Video Amplifier and Driver

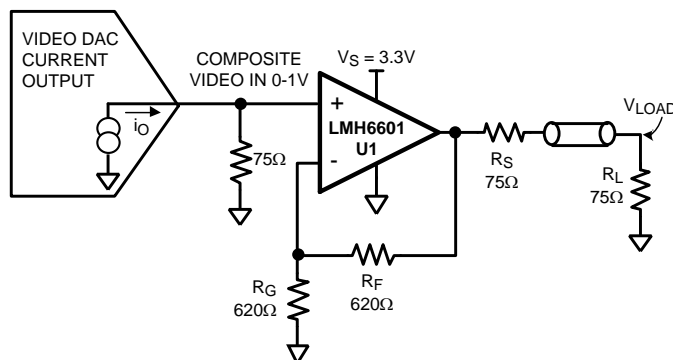
The LMH6601 output can swing very close to either rail to maximize the output dynamic range which is of particular interest when operating in a low-voltage, single-supply environment. Under light output load conditions, the output can swing as close as a few mV of either rail. This also allows a video amplifier to preserve the video black level for excellent video integrity. In the example shown in Figure 51, the baseband video output is amplified and buffered by the LMH6601 which then drives the 75-Ω back-terminated video cable for an overall gain of +1 delivered to the 75-Ω load. The input video would normally have a level between 0 V to approximately 0.75 V.



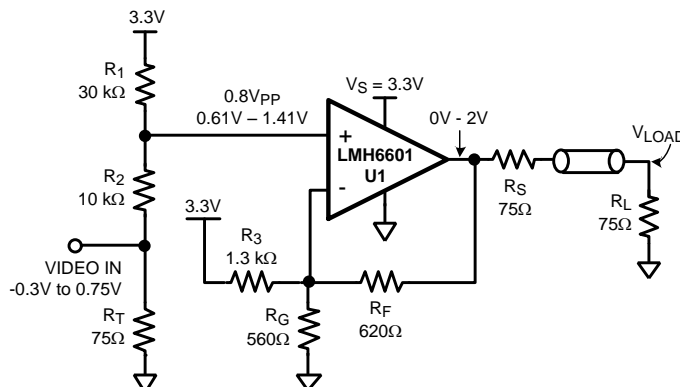
**Figure 51. Single-Supply Video Driver Capable of Maintaining Accurate Video Black Level**

With the LMH6601 input common-mode range including the  $V^-$  (ground) rail, there will be no need for AC-coupling or level shifting and the input can directly drive the noninverting input which has the additional advantage of high amplifier input impedance. With LMH6601's wide rail-to-rail output swing, as stated earlier, the video black level of 0 V is maintained at the load with minimal circuit complexity and using no AC-coupling capacitors. Without true rail-to-rail output swing of the LMH6601, and more importantly without the LMH6601's ability of exceedingly close swing to  $V^-$ , the circuit would not operate properly as shown at the expense of more complexity. This circuit will also work for higher input voltages. The only significant requirement is that there is at least 1.8 V from the maximum input voltage to the positive supply ( $V^+$ ).

The Composite Video Output of some low-cost consumer video equipment consists of a current source which develops the video waveform across a load resistor (usually 75 Ω), as shown in Figure 52. With these applications, the same circuit configuration just described and shown in Figure 52 will be able to buffer and drive the Composite Video waveform which includes sync and video combined. However, with this arrangement, the LMH6601 supply voltage must be at least 3.3 V or higher to allow proper input common-mode voltage headroom because the input can be as high as 1-V peak.

**Application Information (continued)**

**Figure 52. Single-Supply Composite Video Driver for Consumer Video Outputs**

If the Video In signal is Composite Video with negative going Sync tip, a variation of the previous configurations should be used. This circuit produces a unipolar (more than 0 V) DC-coupled single-supply video signal as shown in [Figure 53](#).


**Figure 53. Single-Supply, DC-Coupled Composite Video Driver for Negative Going Sync Tip**

In the circuit of [Figure 53](#), the input is shifted positive by means of  $R_1$ ,  $R_2$ , and  $R_T$  in order to satisfy the common-mode input range of the U1. The signal will lose 20% of its amplitude in the process. The closed-loop gain of U1 must be set to make up for this 20% loss in amplitude. This gives rise to the gain expression shown in [Equation 1](#), which is based on getting a 2 V<sub>PP</sub> output with a 0.8 V<sub>PP</sub> input:

$$\frac{R_F}{R_G \parallel R_3} = \frac{2V}{0.8V} - 1 = 1.5V/V \quad (1)$$

$R_3$  will produce a negative shift at the output due to  $V_S$  (3.3 V in this case).  $R_3$  must be set so that the Video In sync tip (–0.3 V at  $R_T$  or 0.61 V at U1 noninverting input) corresponds to near 0 V at the output.

$$\frac{R_F}{R_3} = \frac{0.61}{3.3V - 0.61} \left( 1 + \frac{R_F}{R_G} \right) = 0.227 \left( 1 + \frac{R_F}{R_G} \right) \quad (2)$$

[Equation 1](#) and [Equation 2](#) must be solved simultaneously to arrive at the values of  $R_3$ ,  $R_F$ , and  $R_G$  which will satisfy both. From the data sheet, one can set  $R_F = 620 \Omega$  to be close to the recommended value for a gain of +2. It is easier to solve for  $R_G$  and  $R_3$  by starting with a good estimate for one and iteratively solving [Equation 1](#) and [Equation 2](#) to arrive at the results. Here is one possible iteration cycle for reference:

$$R_F = 620 \Omega \quad (3)$$



## Application Information (continued)

**Table 1. Finding External Resistor Values by Iteration for Figure 53**

ESTIMATE R <sub>G</sub> (Ω)	CALCULATED (from Equation 2) R <sub>3</sub> (Ω)	Equation 1 LHS CALCULATED	COMMENT (COMPARE Equation 1 LHS calculated to RHS)
1k	1.69k	0.988	Increase Equation 1 LHS by reducing R <sub>G</sub>
820	1.56k	1.15	Increase Equation 1 LHS by reducing R <sub>G</sub>
620	1.37k	1.45	Increase Equation 1 LHS by reducing R <sub>G</sub>
390	239	4.18	Reduce Equation 1 LHS by increasing R <sub>G</sub>
<b>560</b>	<b>1.30k</b>	1.59	Close to target value of 1.5V/V for Equation 1

The final set of values for R<sub>G</sub> and R<sub>3</sub> in Table 1 are values which will result in the proper gain and correct video levels (0 V to 1 V) at the output (V<sub>LOAD</sub>).

### 8.1.2 How to Pick the Right Video Amplifier

Apart from output current drive and voltage swing, the op amp used for a video amplifier and cable driver should also possess the minimum requirement for speed and slew rate. For video type loads, it is best to consider Large Signal Bandwidth (or LSBW in the TI data sheet tables) as video signals could be as large as 2 V<sub>PP</sub> when applied to the commonly used gain of +2 configuration. Because of this relatively large swing, the op amp Slew Rate (SR) limitation should also be considered. Table 2 shows these requirements for various video line rates calculated using a rudimentary technique and intended as a first-order estimate only.

**Table 2. Rise Time, –3 dB BW, and Slew Rate Requirements for Various Video Line Rates**

VIDEO STANDARD	LINE RATE (HxV)	REFRESH RATE (Hz)	HORIZONTAL ACTIVE (KH%)	VERTICAL ACTIVE (KV%)	PIXEL TIME (ns)	RISE TIME (ns)	LSBW (MHz)	SR (V/μs)
TV_NTSC	451x483	30	84	92	118.3	39.4	9	41
VGA	640x480	75	80	95	33	11	32	146
SVGA	800x600	75	76	96	20.3	6.8	52	237
XGA	1024x768	75	77	95	12.4	4.1	85	387
SXGA	1280x1024	75	75	96	7.3	2.4	143	655
UXGA	1600x1200	75	74	96	4.9	1.6	213	973

For any video line rate (HxV corresponding to the number of Active horizontal and vertical lines), the speed requirements can be estimated if the Horizontal Active (KH%) and Vertical Active (KV%) numbers are known. These percentages correspond to the percentages of the active number of lines (horizontal or vertical) to the total number of lines as set by VESA standards. Here are the general expressions and the specific calculations for the SVGA line rate shown in Table 2.

$$\begin{aligned}
 \text{PIXEL\_TIME (ns)} &= \frac{1}{\text{REFRESH\_RATE}} \times \text{KH} \times \text{KV} \times 1 \times 10^5 \\
 &= \frac{1}{75 \text{ Hz}} \times 76 \times 96 \times 1 \times 10^5 = 20.3 \text{ ns}
 \end{aligned}
 \tag{4}$$

Requiring that an “On” pixel is illuminated to at least 90 percent of its final value before changing state will result in the rise/fall time equal to, at most, 1/3 the pixel time as shown in Equation 5:

$$\text{RISE/FALL\_TIME} = \frac{\text{PIXEL\_TIME}}{3} = \frac{20.3 \text{ ns}}{3} = 6.8 \text{ ns}
 \tag{5}$$

Assuming a single pole frequency response roll-off characteristic for the closed-loop amplifier used, we have:

$$-3 \text{ dB\_BW} = \frac{0.35}{\text{RISE/FALL\_TIME}} = \frac{0.35}{6.8 \text{ ns}} = 52 \text{ MHz}
 \tag{6}$$

Rise/Fall times are 10%-90% transition times, which for a 2 V<sub>PP</sub> video step would correspond to a total voltage shift of 1.6V (80% of 2 V). So, the Slew Rate requirement can be calculated as follows:

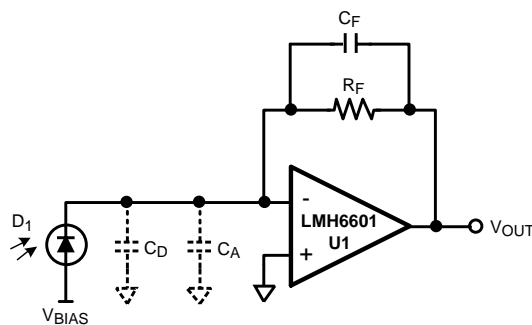
$$SR(V/\mu s) = \frac{1.6V}{RISE/FALL\_TIME (ns)} \times 1 \times 10^3 = \frac{1.6V}{6.8 ns} = 237(V/\mu s) \quad (7)$$

The LMH6601 specifications show that it would be a suitable choice for video amplifiers up to and including the SVGA line rate as demonstrated above.

For more information about this topic and others relating to video amplifiers, see Application Note 1013, *Video Amplifier Design for Computer Monitors* ([SNVA031](#)).

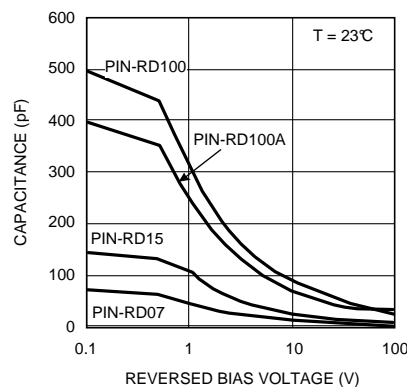
### 8.1.3 Current to Voltage Conversion (Transimpedance Amplifier (TIA))

Being capable of high speed and having ultra low input bias current makes the LMH6601 a natural choice for Current to Voltage applications such as photodiode I-V conversion. In these type of applications, as shown in [Figure 54](#), the photodiode is tied to the inverting input of the amplifier with R<sub>F</sub> set to the proper gain (gain is measured in Ω).



**Figure 54. Typical Connection of a Photodiode Detector to an Op Amp**

With the LMH6601 input bias current in the femto-amperes range, even large values of gain (R<sub>F</sub>) do not increase the output error term appreciably. This allows circuit operation to a lower light intensity level which is always of special importance in these applications. Most photo-diodes have a relatively large capacitance (C<sub>D</sub>) which would be even larger for a photo-diode designed for higher sensitivity to light because of its larger area. Some applications may run the photodiode with a reverse bias to reduce its capacitance with the disadvantage of increased contributions from both dark current and noise current. [Figure 55](#) shows a typical photodiode capacitance plot vs. reverse bias for reference.



**Figure 55. Typical Capacitance vs. Reverse Bias (Source: OSI Optoelectronics)**

The diode capacitance ( $C_D$ ) combined with the input capacitance of the LMH6601 ( $C_A$ ) has a bearing on the stability of this circuit and how it is compensated. With large transimpedance gain values ( $R_F$ ), the total combined capacitance on the amplifier inverting input ( $C_{IN} = C_D + C_A$ ) will work against  $R_F$  to create a zero in the Noise Gain (NG) function (see Figure 56). If left untreated, at higher frequencies where NG equals the open-loop transfer function excess phase shift around the loop (approaching 180°) and therefore, the circuit could be unstable. This is illustrated in Figure 56.

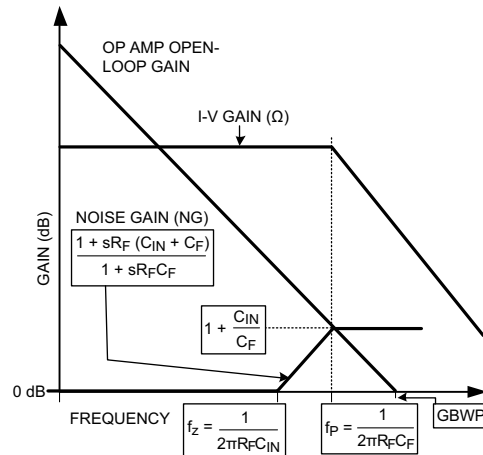


Figure 56. Transimpedance Amplifier Graphical Stability Analysis and Compensation

Figure 56 shows that placing a capacitor,  $C_F$ , with the proper value, across  $R_F$  will create a pole in the NG function at  $f_p$ . For optimum performance, this capacitor is usually picked so that NG is equal to the open-loop gain of the op amp at  $f_p$ . This will cause a “flattening” of the NG slope beyond the point of intercept of the two plots (open-loop gain and NG) and will result in a Phase Margin (PM) of 45° assuming  $f_p$  and  $f_z$  are at least a decade apart. This is because at the point of intercept, the NG pole at  $f_p$  will have a 45° phase lead contribution which leaves 45° of PM. For reference, Figure 56 also shows the transimpedance gain (I-V ( $\Omega$ ))

Here is the theoretical expression for the optimum  $C_F$  value and the expected -3-dB bandwidth:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}} \tag{8}$$

$$f_{-3\text{ dB}} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}} \tag{9}$$

Table 3 lists the results, along with the assumptions and conditions, of testing the LMH6601 with various photodiodes having different capacitances ( $C_D$ ) at a transimpedance gain ( $R_F$ ) of 10 k $\Omega$ .

Table 3. Transimpedance Amplifier Compensation and Performance Results for Figure 54

$C_D$ (pF)	$C_{IN}$ (pF)	$C_{F\_CALCULATED}$ (pF)	$C_F$ USED (pF)	-3 dB BW CALCULATED (MHz)	-3 dB BW MEASURED (MHz)	STEP RESPONSE OVERSHOOT (%)
10	12	1.1	1	14	15	6
50	52	2.3	3	7	7	4
500	502	7.2	8	2	2.5	9

$$C_A = 2 \text{ pF } GBWP = 155 \text{ MHz } V_S = 5 \text{ V} \tag{10}$$

### 8.1.4 Transimpedance Amplifier Noise Considerations

When analyzing the noise at the output of the I-V converter, it is important to note that the various noise sources (that is, op amp noise voltage, feedback resistor thermal noise, input noise current, photodiode noise current) do not all operate over the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account.

The op amp noise voltage will be gained up in the region between the noise gain's “zero” and its “pole” ( $f_z$  and  $f_p$  in Figure 56). The higher the values of  $R_F$  and  $C_{IN}$ , the sooner the noise gain peaking starts and therefore its contribution to the total output noise would be larger. It is obvious to note that it is advantageous to minimize  $C_{IN}$  (for example, by proper choice of op amp, by applying a reverse bias across the diode at the expense of excess dark current and noise). However, most low noise op amps have a higher input capacitance compared to ordinary op amps. This is due to the low noise op amp's larger input stage.

### 8.1.5 Charge Preampfier

$R_F = 10\text{ M}\Omega$  to  $10\text{ G}\Omega$   
 $R_S = 1\text{ M}\Omega$  or SMALLER FOR HIGH COUNTING RATES  
 $C_F = 1\text{ pF}$   
 $C_D = 1\text{ pF}$  to  $10\text{ }\mu\text{F}$   
 $V_{OUT} = Q/C_F$  WHERE Q is CHARGE  
 CREATED BY ONE PHOTON or PARTICLE  
 ADJUST  $V_{BIAS}$  FOR MAXIMUM SNR

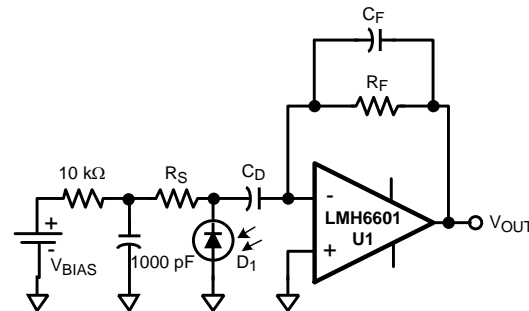


Figure 57. Charge Preampfier Taking Advantage of the Femto-Ampere Range Input Bias Current of the LMH6601

### 8.1.6 Capacitive Load

The LMH6601 can drive a capacitive load of up to 1000 pF with correct isolation and compensation. Figure 58 illustrates the in-loop compensation technique to drive a large capacitive load.

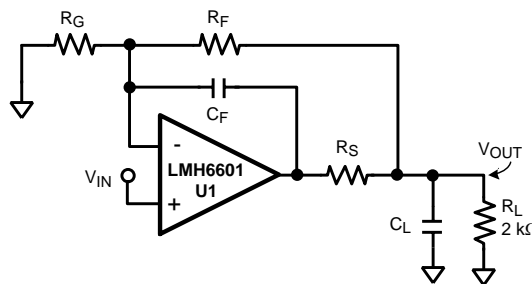


Figure 58. In-Loop Compensation Circuit for Driving a Heavy Capacitive Load

When driving a high-capacitive load, an isolation resistor ( $R_S$ ) should be connected in series between the op amp output and the capacitive load to provide isolation and to avoid oscillations. A small-value capacitor ( $C_F$ ) is inserted between the op amp output and the inverting input as shown such that this capacitor becomes the dominant feedback path at higher frequency. Together these components allow heavy capacitive loading while keeping the loop stable.

There are few factors which affect the driving capability of the op amp:

- Op amp internal architecture
- Closed-loop gain and output capacitor loading

Table 4 shows the measured step response for various values of load capacitors ( $C_L$ ), series resistor ( $R_S$ ) and feedback resistor ( $C_F$ ) with gain of +2 ( $R_F = R_G = 604\text{ }\Omega$ ) and  $R_L = 2\text{ k}\Omega$ :

Table 4. LMH6601 Step Response Summary for the Circuit of Figure 58

C <sub>L</sub> (pF)	R <sub>S</sub> (Ω)	C <sub>F</sub> (pF)	t <sub>rise</sub> / t <sub>fall</sub> (ns)	OVERSHOOT (%)
10	0	1	6 <sup>(1)</sup>	8
50	0	1	7 <sup>(1)</sup>	6
110	47	1	10	16
300	6	10	12	20
500	80	10	33	10
910	192	10	65	10

(1) Response limited by input step generator rise time of 5 ns

Figure 59 shows the increase in rise/fall time (bandwidth decrease) at V<sub>OUT</sub> with larger capacitive loads, illustrating the trade-off between the two:

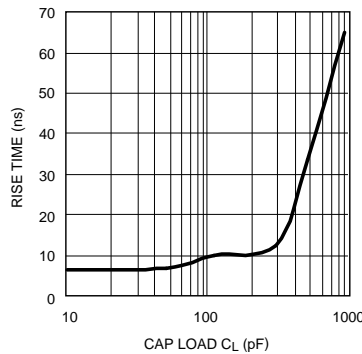


Figure 59. LMH6601 In-Loop Compensation Response

## 8.2 Typical Application

### 8.2.1 SAG Compensation for AC-Coupled Video

Many monitors and displays accept AC-coupled inputs. This simplifies the amplification and buffering task in some respects. The capacitors shown in Figure 60 (except C<sub>G2</sub>), and especially C<sub>O</sub>, are the large electrolytic type which are considerably costly and take up valuable real estate on the board. It is possible to reduce the value of the output coupling capacitor, C<sub>O</sub>, which is the largest of all, by using what is called SAG compensation. SAG refers to what the output video experiences due to the low frequency video content it contains which cannot adequately go through the output AC-coupling scheme due to the low frequency limit of this circuit. The -3 dB low frequency limit of the output circuit is given by:

$$f_{\text{low\_frequency}} (-3 \text{ dB}) = 1 / (2 * \pi * 75 * 2(\Omega) * C_o) = \sim 4.82 \text{ Hz for } C_o = 220 \mu\text{F} \quad (11)$$

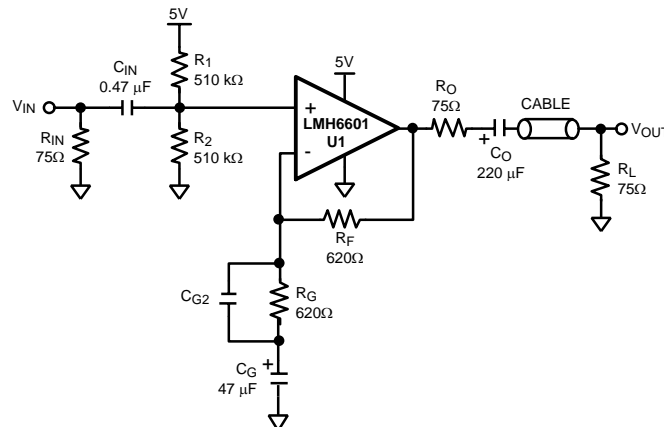


Figure 60. AC-Coupled Video Amplifier and Driver

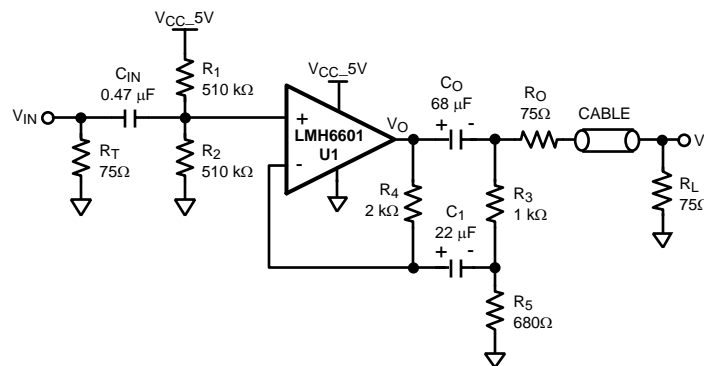
## Typical Application (continued)

### 8.2.2 Design Requirements

As shown in [Figure 60](#),  $R_1$  and  $R_2$  simply set the input to the center of the input linear range while  $C_{IN}$  AC couples the video onto the input of the op amp. The op amp is set for a closed-loop gain of 2 with  $R_F$  and  $R_G$ .  $C_G$  is there to make sure the device output is also biased at mid-supply. Because of the DC bias at the output, the load must be AC-coupled as well through  $C_O$ . Some applications implement a small valued ceramic capacitor (not shown) in parallel with  $C_O$  which is electrolytic. The reason for this is that the ceramic capacitor will tend to shunt the inductive behavior of the Electrolytic capacitor at higher frequencies for an improved overall low impedance output.

$C_{G2}$  is intended to boost the high-frequency gain to improve the video frequency response. This value is to be set and trimmed on the board to meet the specific system requirements of the application.

A possible implementation of the SAG compensation is shown in [Figure 61](#).



**Figure 61. AC-Coupled Video Amplifier/Driver With SAG Compensation**

### 8.2.3 Detailed Design Procedure

In the circuit of [Figure 61](#), the output coupling capacitor value and size is reduced at the expense of a slightly more complicated circuitry. Note that  $C_1$  is not only part of the SAG compensation, but it also sets the amplifier's DC gain to 0 dB so that the output is set to mid-rail for linearity purposes. Also, exceptionally high values are chosen for the  $R_1$  and  $R_2$  biasing resistors (510 kΩ). The LMH6601 has extremely low input bias current which allows this selection thereby reducing the  $C_{IN}$  value in this circuit such that  $C_{IN}$  can even be a nonpolar capacitor which will reduce cost.

At high enough frequencies where both  $C_O$  and  $C_1$  can be considered to be shorted out,  $R_3$  shunts  $R_4$  and the closed-loop gain is determined by:

$$\text{Closed\_loop\_Gain (V/V)} = V_L/V_{IN} = (1 + (R_3 || R_4) / R_5) \times [R_L / (R_L + R_O)] = 0.99 \text{ V/V} \quad (12)$$

At intermediate frequencies, where the  $C_O$ ,  $R_O$ ,  $R_L$  path experiences low frequency gain loss, the  $R_3$ ,  $R_5$ ,  $C_1$  path provides feedback from the load side of  $C_O$ . With the load side gain reduced at these lower frequencies, the feedback to the op amp inverting node reduces, causing an increase at the output of the op amp as a response.

For NTSC video, low values of  $C_O$  influence how much video black level shift occurs during the vertical blanking interval (~1.5 ms) which has no video activity and thus is sensitive to the charge dissipation of the  $C_O$  through the load which could cause output SAG. An especially tough pattern is the NTSC pattern called "Pulse & Bar." With this pattern the entire top and bottom portion of the field is black level video where, for about 11 ms,  $C_O$  is discharging through the load with no video activity to replenish that charge.

## Typical Application (continued)

### 8.2.4 Application Curves

Figure 62 shows the output of the Figure 61 circuit highlighting the SAG.

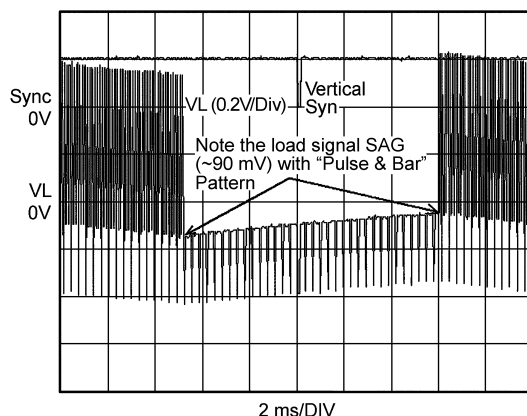


Figure 62. AC-Coupled Video Amplifier/Driver Output Scope Photo Showing Video SAG

With the circuit of Figure 61 and any other AC-coupled pulse amplifier, the waveform duty cycle variations exert additional restrictions on voltage swing at any node. This is illustrated in the waveforms shown in Figure 63.

If a stage has a  $3 V_{PP}$  unclipped swing capability available at a given node, as shown in Figure 63, the maximum allowable amplitude for an arbitrary waveform is  $\frac{1}{2}$  of  $3 V$  or  $1.5 V_{PP}$ . This is due to the shift in the average value of the waveform as the duty cycle varies. Figure 63 shows what would happen if a  $2 V_{PP}$  signal were applied. A low duty cycle waveform, such as the one in Figure 63B, would have high positive excursions. At low enough duty cycles, the waveform could get clipped on the top, as shown, or a more subtle loss of linearity could occur prior to full-blown clipping. The converse of this occurs with high duty cycle waveforms and negative clipping, as depicted in Figure 63C.

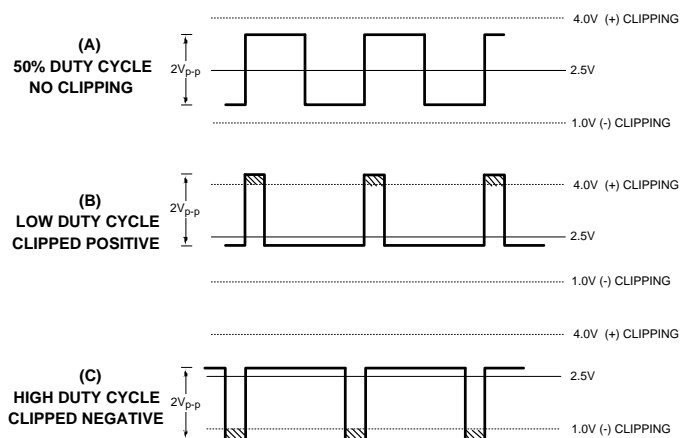


Figure 63. Headroom Considerations With AC-Coupled Amplifiers

## 9 Power Supply Recommendations

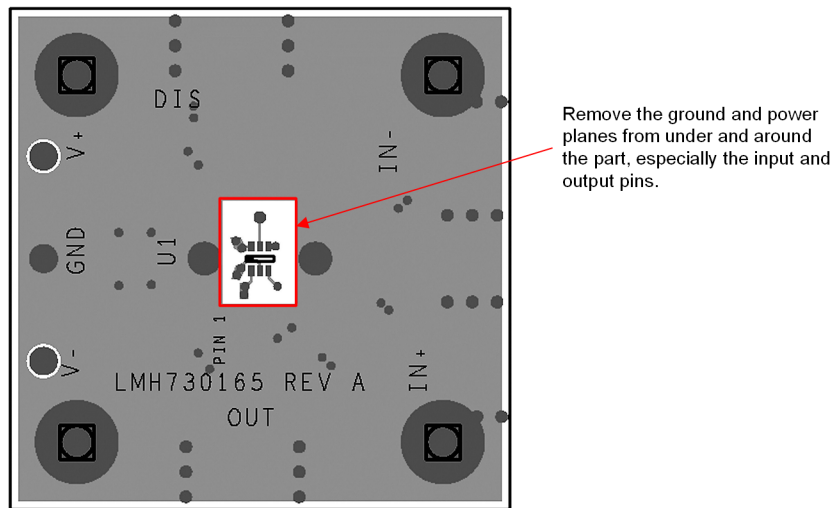
The LMH6601 can operate off a single-supply or with dual supplies. The input CM capability of the parts (CMVR) extends all the way down to the V- rail to simplify single-supply applications. Supplies should be decoupled with low-inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. TI recommends the use of ground plane, and as in most high-speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

## 10 Layout

### 10.1 Layout Guidelines

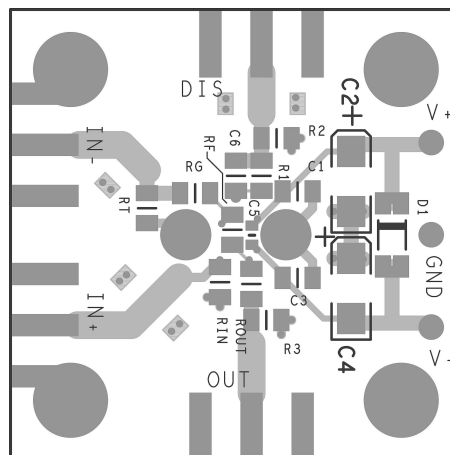
Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, [SNOA367](#), for more information).

### 10.2 Layout Examples



SC-70 Board Layout (Actual size = 1.5 in x 1.5 in)

**Figure 64. Layer 1 Silk**



SC-70 Board Layout (Actual size = 1.5 in x 1.5 in)

**Figure 65. Layer 2 Silk**



## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For additional information, see the following:

- Application Note 1013, *Video Amplifier Design for Computer Monitors*, [SNVA031](#)
- Application Note OA-15, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, [SNOA367](#)

### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6601	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LMH6601-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6601MG/NOPB	ACTIVE	SC70	DCK	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A95	<a href="#">Samples</a>
LMH6601MGX/NOPB	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A95	<a href="#">Samples</a>
LMH6601QMG/NOPB	ACTIVE	SC70	DCK	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AKA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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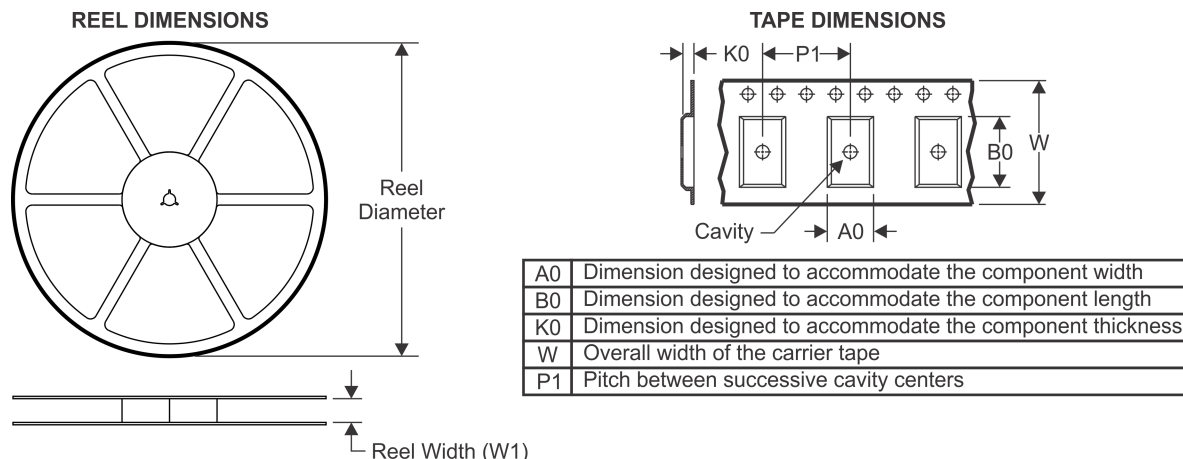
**OTHER QUALIFIED VERSIONS OF LMH6601, LMH6601-Q1 :**

- Catalog: [LMH6601](#)
- Automotive: [LMH6601-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

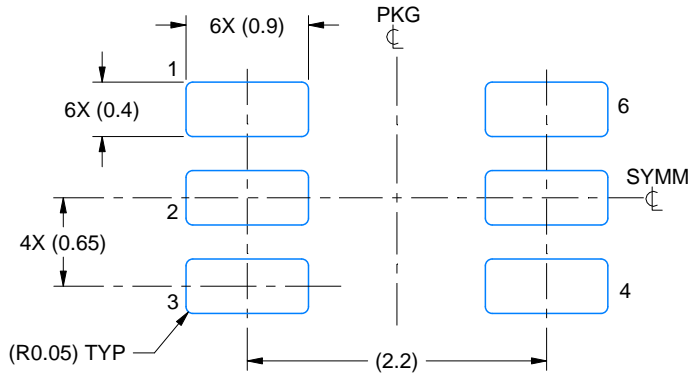
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6601MG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6601MGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6601QMG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**

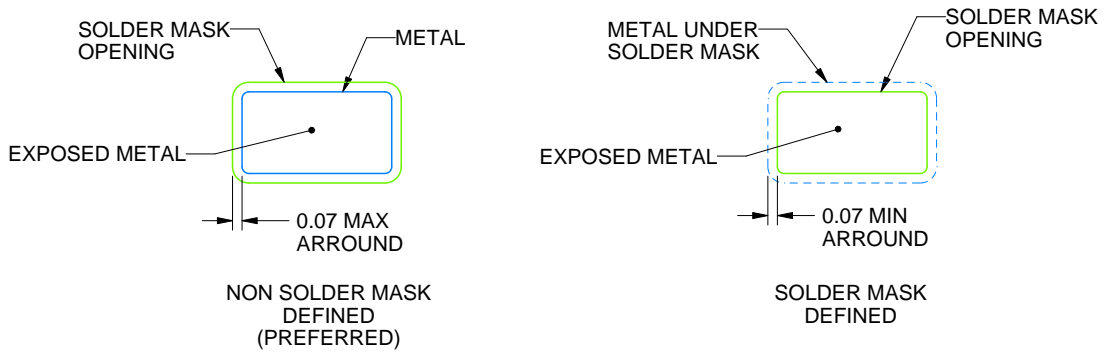

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6601MG/NOPB	SC70	DCK	6	1000	208.0	191.0	35.0
LMH6601MGX/NOPB	SC70	DCK	6	3000	208.0	191.0	35.0
LMH6601QMG/NOPB	SC70	DCK	6	1000	208.0	191.0	35.0





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

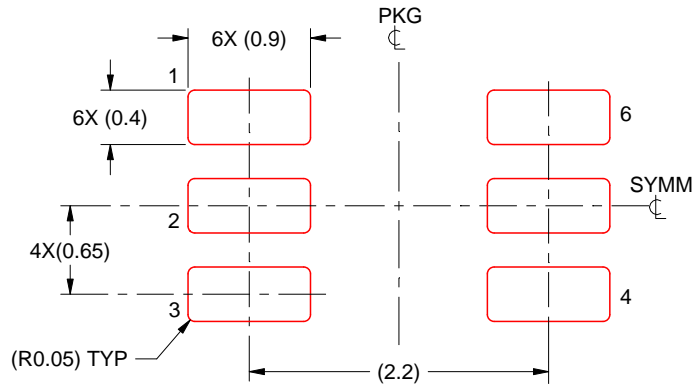


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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