

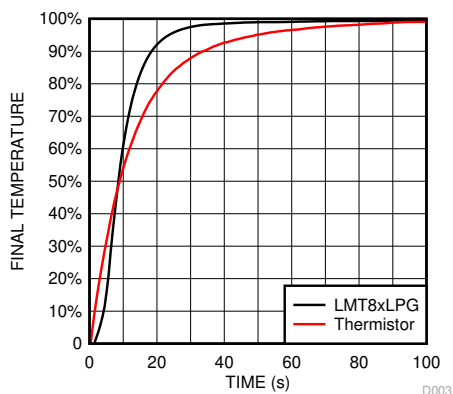
LMT87-Q1 2.7-V, SC70, Analog Temperature Sensors With Class-AB Output

1 Features

- LMT87-Q1-Q1 is AEC-Q100 Qualified for Automotive Applications:
 - Device Temperature Grade 0: -40°C to $+150^{\circ}\text{C}$
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C6
- Functional Safety-Capable
 - Documentation available to aid functional safety system design
- Very Accurate: $\pm 0.4^{\circ}\text{C}$ Typical
- Low 2.7-V Operation
- Average Sensor Gain of $-13.6\text{ mV}/^{\circ}\text{C}$
- Low $5.4\text{-}\mu\text{A}$ Quiescent Current
- Wide Temperature Range: -50°C to 150°C
- Output is Short-Circuit Protected
- Push-Pull Output With $\pm 50\text{-}\mu\text{A}$ Drive Capability
- Footprint Compatible With the Industry-Standard LM20/19 and LM35 Temperature Sensors
- Cost-Effective Alternative to Thermistors

2 Applications

- Automotive
- Infotainment and Cluster
- Powertrain Systems
- Smoke and Heat Detectors
- Drones
- Appliances



* Fast thermal response NTC

Thermal Time Constant

3 Description

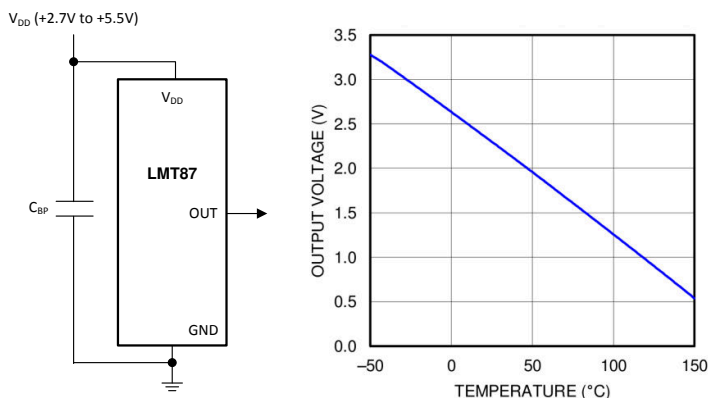
The LMT87-Q1 device is a precision CMOS temperature sensor with $\pm 0.4^{\circ}\text{C}$ typical accuracy ($\pm 2.7^{\circ}\text{C}$ maximum) and a linear analog output voltage that is inversely proportional to temperature. The 2.7-V supply voltage operation, $5.4\text{-}\mu\text{A}$ quiescent current, and 0.7-ms power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered applications such as drones and sensor nodes. The LMT87-Q1-Q1 device is AEC-Q100 Grade 0 qualified and maintains $\pm 2.7^{\circ}\text{C}$ maximum accuracy over the full operating temperature range without calibration; this makes the LMT87-Q1-Q1 suitable for automotive applications such as infotainment, cluster, and powertrain systems. The accuracy over the wide operating range and other features make the LMT87-Q1 an excellent alternative to thermistors.

For devices with different average sensor gains and comparable accuracy, refer to [Comparable Alternative Devices](#) for alternative devices in the LMT8x family.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMT87-Q1	SOT (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Output Voltage vs Temperature



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2017) to Revision A (June 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added Functional Safety bullets to the <i>Features</i> section.....	1

5 Device Comparison

Table 5-1. Available Device Packages

ORDER NUMBER ⁽¹⁾	PACKAGE	PIN	BODY SIZE (NOM)	MOUNTING TYPE
LMT87DCK	SOT (AKA ⁽²⁾ : SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount
LMT87LP	TO-92 (AKA ⁽²⁾ : LP)	3	4.30 mm × 3.50 mm	Through-hole; straight leads
LMT87LPG	TO-92S (AKA ⁽²⁾ : LPG)	3	4.00 mm × 3.15 mm	Through-hole; straight leads
LMT87LPM	TO-92 (AKA ⁽²⁾ : LPM)	3	4.30 mm × 3.50 mm	Through-hole; formed leads
LMT87DCK-Q1	SOT (AKA ⁽²⁾ : SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount

- (1) For all available packages and complete order numbers, see the Package Option addendum at the end of the data sheet.
 (2) AKA = Also Known As

Table 5-2. Comparable Alternative Devices

DEVICE NAME	AVERAGE OUTPUT SENSOR GAIN	POWER SUPPLY RANGE
LMT84-Q1	-5.5 mV/°C	1.5 V to 5.5 V
LMT85-Q1	-8.2 mV/°C	1.8 V to 5.5 V
LMT86-Q1	-10.9 mV/°C	2.2 V to 5.5 V
LMT87-Q1	-13.6 mV/°C	2.7 V to 5.5 V

6 Pin Configuration and Functions

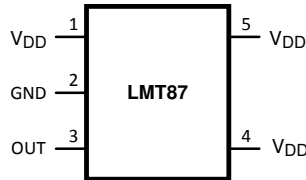
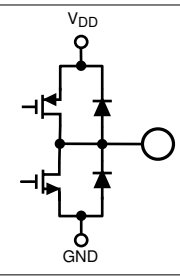


Figure 6-1. DCK Package 5-Pin SOT (SC70) Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	SOT (SC70)		EQUIVALENT CIRCUIT	FUNCTION
GND	2 ⁽¹⁾	Ground	N/A	Power Supply Ground
OUT	3	Analog Output		Outputs a voltage that is inversely proportional to temperature
V _{DD}	1, 4, 5	Power	N/A	Positive Supply Voltage

- (1) Direct connection to the back side of the die

7 Specifications

7.1 Absolute Maximum Ratings

See (1) (3)

	MIN	MAX	UNIT
Supply voltage	-0.3	6	V
Voltage at output pin	-0.3	(V _{DD} + 0.5)	V
Output current	-7	7	mA
Input current at any pin ⁽²⁾	-5	5	mA
Maximum junction temperature (T _{JMAX})		150	°C
Storage temperature T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > V), the current at that pin should be limited to 5 mA.
- (3) *Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.*

7.2 ESD Ratings

		VALUE	UNIT
LMT87DCK-Q1 in SC70 package			
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	V
		Charged-device model (CDM), per AEC Q100-011	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Specified temperature	T _{MIN} ≤ T _A ≤ T _{MAX}		°C
	-50 ≤ T _A ≤ 150		°C
Supply voltage (V _{DD})	2.7	5.5	V

7.4 Thermal Information

THERMAL METRIC ^{(1) (2)}		LMT87-Q1	UNIT
		DCK (SOT/SC70)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ^{(3) (4)}	275	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	84	°C/W
R _{θJB}	Junction-to-board thermal resistance	56	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	55	°C/W

- (1) For information on self-heating and thermal response time see section [Mounting and Thermal Conductivity](#).
- (2) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.
- (3) The junction to ambient thermal resistance (R_{θJA}) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
- (4) Changes in output due to self-heating can be computed by multiplying the internal dissipation by the thermal resistance.

7.5 Accuracy Characteristics

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in [Table 8-1](#).

PARAMETER	CONDITIONS	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNIT
Temperature accuracy ⁽²⁾	70°C to 150°C; V _{DD} = 3.0 V to 5.5 V	-2.7	±0.4	2.7	°C
	20°C to 40°C; V _{DD} = 2.7 V to 5.5 V		±0.6		°C
	20°C to 40°C; V _{DD} = 3.4 V to 5.5 V		±0.3		°C
	0°C; V _{DD} = 3.0 V to 5.5 V	-2.7	±0.6	2.7	°C
	0°C; V _{DD} = 3.6 V to 5.5 V		±0.3		°C
	-50°C; V _{DD} = 3.6 V to 5.5 V	-2.7	±0.6	2.7	°C
	-50°C; V _{DD} = 4.2 V to 5.5 V		±0.3		°C

- (1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
- (2) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Transfer Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

7.6 Electrical Characteristics

Unless otherwise noted, these specifications apply for +V_{DD} = 2.7 V to 5.5 V. MIN and MAX limits apply for T_A = T_J = T_{MIN} to T_{MAX}; typical limits apply for T_A = T_J = 25°C.

PARAMETER	TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽¹⁾	MAX ⁽²⁾	UNIT
Sensor gain (output transfer function slope)			-13.6		mV/°C
Load regulation ⁽³⁾	Source ≤ 50 μA, (V _{DD} - V _{OUT}) ≥ 200 mV	-1	-0.22		mV
	Sink ≤ 50 μA, V _{OUT} ≥ 200 mV		0.26	1	mV
Line regulation ⁽⁴⁾			200		μV/V
I _S Supply current	T _A = 30°C to 150°C, (V _{DD} - V _{OUT}) ≥ 100 mV		5.4	8.1	μA
	T _A = -50°C to 150°C, (V _{DD} - V _{OUT}) ≥ 100 mV		5.4	9	μA
C _L Output load capacitance			1100		pF
Power-on time ⁽⁵⁾	C _L = 0 pF to 1100 pF		0.7	1.9	ms
Output drive	T _A = T _J = 25°C	-50		50	μA

- (1) Typical values are at T_J = T_A = 25°C and represent most likely parametric norm.
- (2) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
- (3) Source currents are flowing out of the LMT87-Q1. Sink currents are flowing into the LMT87-Q1.
- (4) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in [Output Voltage Shift](#).
- (5) Specified by design and characterization.

7.7 Typical Characteristics

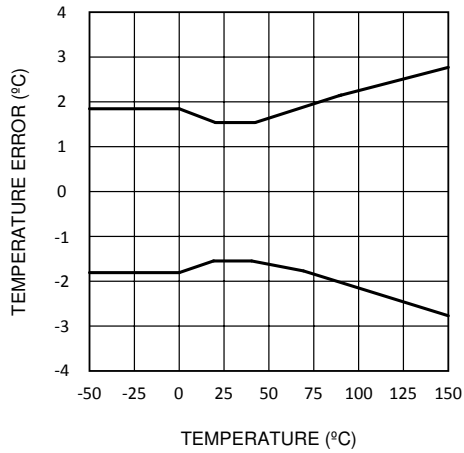


Figure 7-1. Temperature Error vs Temperature

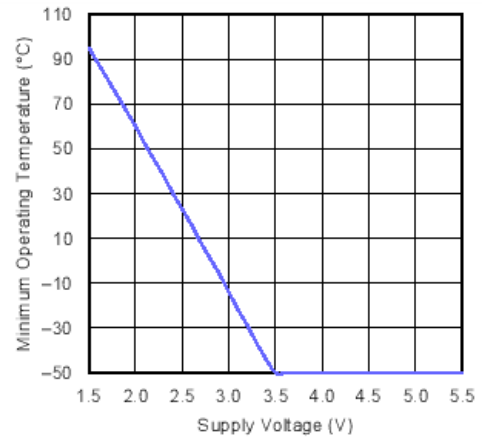


Figure 7-2. Minimum Operating Temperature vs Supply Voltage

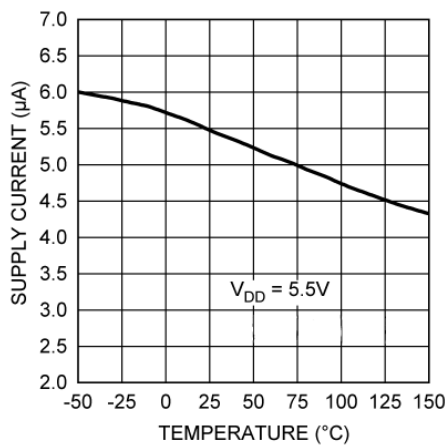


Figure 7-3. Supply Current vs Temperature

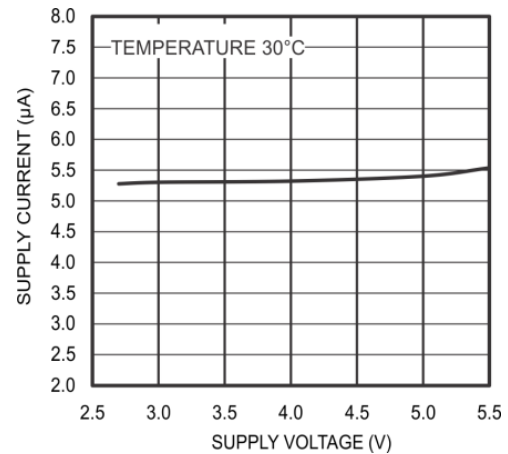


Figure 7-4. Supply Current vs Supply Voltage

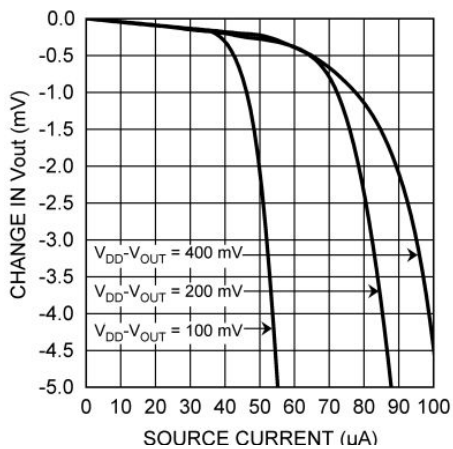


Figure 7-5. Load Regulation, Sourcing Current

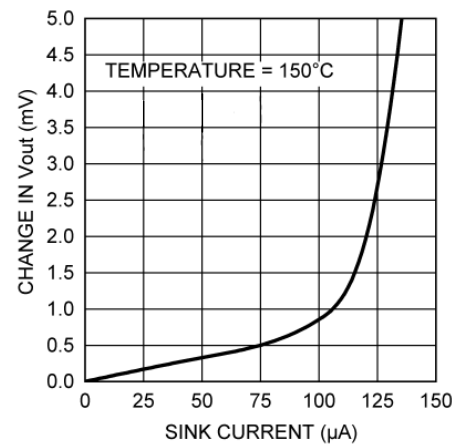


Figure 7-6. Load Regulation, Sinking Current

7.7 Typical Characteristics (continued)

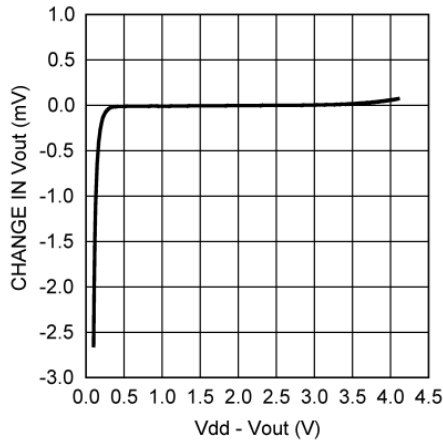


Figure 7-7. Change in V_{OUT} vs Overhead Voltage

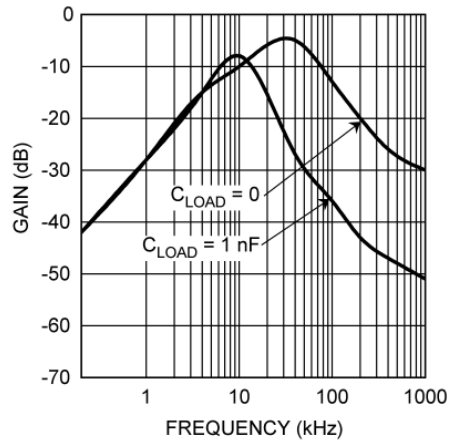


Figure 7-8. Supply-Noise Gain vs Frequency

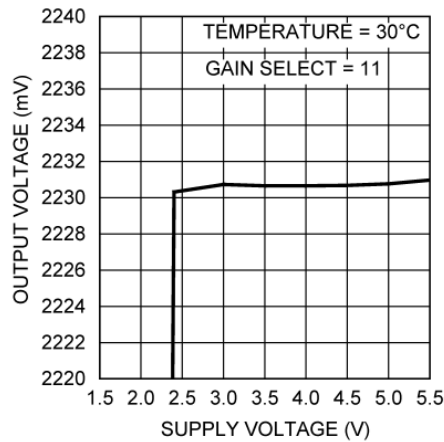


Figure 7-9. Output Voltage vs Supply Voltage

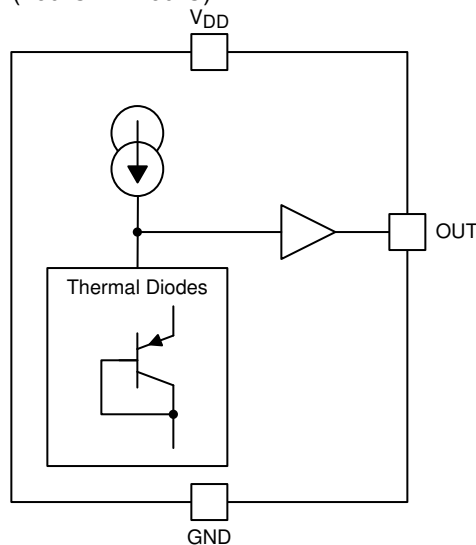
8 Detailed Description

8.1 Overview

The LMT87-Q1 is an analog output temperature sensor. The temperature-sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature-sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source.

8.2 Functional Block Diagram

Full-Range Celsius Temperature Sensor (–50°C to +150°C)



8.3 Feature Description

8.3.1 LMT87-Q1 Transfer Function

Table 8-1 shows the output voltage of the LMT87-Q1 across the complete operating temperature range. This table is the reference from which the LMT87-Q1 accuracy specifications (listed in the *Accuracy Characteristics* table) are determined. This table can be used, for example, in a host processor look-up table. A file containing this data is available for download at the [LMT87-Q1](#) product folder under *Tools and Software Models*.

Table 8-1. LMT87-Q1 Transfer Table

TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)
–50	3277	–10	2767	30	2231	70	1679	110	1115
–49	3266	–9	2754	31	2217	71	1665	111	1101
–48	3254	–8	2740	32	2204	72	1651	112	1087
–47	3243	–7	2727	33	2190	73	1637	113	1073
–46	3232	–6	2714	34	2176	74	1623	114	1058
–45	3221	–5	2700	35	2163	75	1609	115	1044
–44	3210	–4	2687	36	2149	76	1595	116	1030
–43	3199	–3	2674	37	2136	77	1581	117	1015
–42	3186	–2	2660	38	2122	78	1567	118	1001
–41	3173	–1	2647	39	2108	79	1553	119	987
–40	3160	0	2633	40	2095	80	1539	120	973
–39	3147	1	2620	41	2081	81	1525	121	958
–38	3134	2	2607	42	2067	82	1511	122	944
–37	3121	3	2593	43	2054	83	1497	123	929
–36	3108	4	2580	44	2040	84	1483	124	915
–35	3095	5	2567	45	2026	85	1469	125	901

Table 8-1. LMT87-Q1 Transfer Table (continued)

TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)	TEMP (°C)	V _{OUT} (mV)
-34	3082	6	2553	46	2012	86	1455	126	886
-33	3069	7	2540	47	1999	87	1441	127	872
-32	3056	8	2527	48	1985	88	1427	128	858
-31	3043	9	2513	49	1971	89	1413	129	843
-30	3030	10	2500	50	1958	90	1399	130	829
-29	3017	11	2486	51	1944	91	1385	131	814
-28	3004	12	2473	52	1930	92	1371	132	800
-27	2991	13	2459	53	1916	93	1356	133	786
-26	2978	14	2446	54	1902	94	1342	134	771
-25	2965	15	2433	55	1888	95	1328	135	757
-24	2952	16	2419	56	1875	96	1314	136	742
-23	2938	17	2406	57	1861	97	1300	137	728
-22	2925	18	2392	58	1847	98	1286	138	713
-21	2912	19	2379	59	1833	99	1272	139	699
-20	2899	20	2365	60	1819	100	1257	140	684
-19	2886	21	2352	61	1805	101	1243	141	670
-18	2873	22	2338	62	1791	102	1229	142	655
-17	2859	23	2325	63	1777	103	1215	143	640
-16	2846	24	2311	64	1763	104	1201	144	626
-15	2833	25	2298	65	1749	105	1186	145	611
-14	2820	26	2285	66	1735	106	1172	146	597
-13	2807	27	2271	67	1721	107	1158	147	582
-12	2793	28	2258	68	1707	108	1144	148	568
-11	2780	29	2244	69	1693	109	1130	149	553
								150	538

Although the LMT87-Q1 is very linear, the response does have a slight umbrella parabolic shape. Table 8-1 very accurately reflects this shape. The transfer table can be calculated by using the parabolic equation (Equation 1).

$$V_{TEMP} (mV) = 2230.8mV - \left[13.582 \frac{mV}{^{\circ}C} (T - 30^{\circ}C) \right] - \left[0.00433 \frac{mV}{^{\circ}C^2} (T - 30^{\circ}C)^2 \right] \quad (1)$$

The parabolic equation is an approximation of the transfer table and the accuracy of the equation degrades slightly at the temperature range extremes. Equation 1 can be solved for T resulting in:

$$T = \frac{13.582 - \sqrt{(-13.582)^2 + 4 \times 0.00433 \times (2230.8 - V_{TEMP} (mV))}}{2 \times (-0.00433)} + 30 \quad (2)$$

For an even less accurate linear transfer function approximation, a line can easily be calculated over the desired temperature range from Table 8-1 using the two-point equation (Equation 3):

$$V - V_1 = \left(\frac{V_2 - V_1}{T_2 - T_1} \right) \times (T - T_1) \quad (3)$$

where

- V is in mV,
- T is in °C,
- T₁ and V₁ are the coordinates of the lowest temperature,
- and T₂ and V₂ are the coordinates of the highest temperature.

For example, if the user wanted to resolve this equation, over a temperature range of 20°C to 50°C, they would proceed as follows:

$$V - 2365 \text{ mV} = \left(\frac{1958 \text{ mV} - 2365 \text{ mV}}{50^\circ\text{C} - 20^\circ\text{C}} \right) \times (T - 20^\circ\text{C}) \quad (4)$$

$$V - 2365 \text{ mV} = (-13.6 \text{ mV} / ^\circ\text{C}) \times (T - 20^\circ\text{C}) \quad (5)$$

$$V = (-13.6 \text{ mV} / ^\circ\text{C}) \times T + 2637 \text{ mV} \quad (6)$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

8.4 Device Functional Modes

8.4.1 Mounting and Thermal Conductivity

The LMT87-Q1 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good thermal conductivity, the backside of the LMT87-Q1 die is directly attached to the GND pin. The temperatures of the lands and traces to the other leads of the LMT87-Q1 will also affect the temperature reading.

Alternatively, the LMT87-Q1 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT87-Q1 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the output to ground or V_{DD} , the output from the LMT87-Q1 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction to ambient ($R_{\theta JA}$ or θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. Use [Equation 7](#) to calculate the rise in the LMT87-Q1 die temperature:

$$T_J = T_A + \theta_{JA} [(V_{DD} I_S) + (V_{DD} - V_{OUT}) I_L] \quad (7)$$

where

- T_A is the ambient temperature,
- I_S is the supply current,
- I_L is the load current on the output,
- and V_O is the output voltage.

For example, in an application where $T_A = 30^\circ\text{C}$, $V_{DD} = 5 \text{ V}$, $I_S = 5.4 \mu\text{A}$, $V_{OUT} = 2231 \text{ mV}$, and $I_L = 2 \mu\text{A}$, the junction temperature would be 30.014°C , showing a self-heating error of only 0.014°C . Because the junction temperature of the LMT87-Q1 is the actual temperature being measured, take care to minimize the load current that the LMT87-Q1 is required to drive. The *Thermal Information* table shows the thermal resistance of the LMT87-Q1.

8.4.2 Output Noise Considerations

A push-pull output gives the LMT87-Q1 the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. The LMT87-Q1 is ideal for this and other applications which require strong source or sink current.

The LMT87-Q1 supply-noise gain (the ratio of the AC signal on V_{OUT} to the AC signal on V_{DD}) was measured during bench tests. [Figure 7-8](#) shows the typical attenuation found in the [Typical Characteristics](#) section. A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 5 centimeters of the LMT87-Q1.

8.4.3 Capacitive Loads

The LMT87-Q1 handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, [Figure 8-1](#) shows how the LMT87-Q1 can drive a capacitive load less than or equal to 1100 pF. For capacitive loads greater than 1100 pF, [Figure 8-2](#) shows how a series resistor may be required on the output.

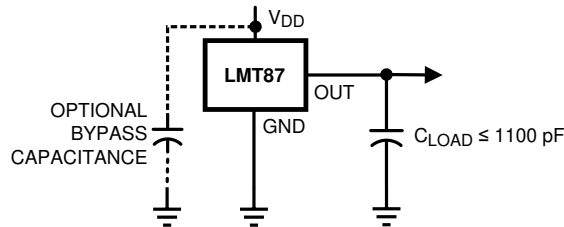


Figure 8-1. LMT87 No Decoupling Required for Capacitive Loads Less Than 1100 pF

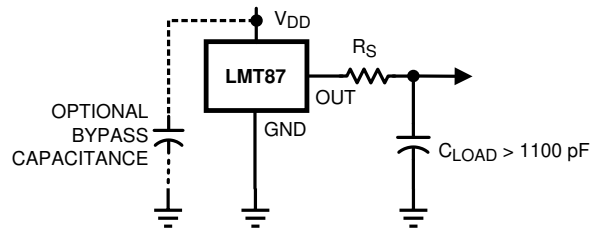


Figure 8-2. LMT87 with Series Resistor for Capacitive Loading Greater Than 1100 pF

Table 8-2. Recommended Series Resistor Values

C_{LOAD}	MINIMUM R_S
1.1 nF to 99 nF	3 k Ω
100 nF to 999 nF	1.5 k Ω
1 μ F	800 Ω

8.4.4 Output Voltage Shift

The LMT87-Q1 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{OUT} . The shift typically occurs when $V_{DD} - V_{OUT} = 1$ V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{OUT} . Because the shift takes place over a wide temperature change of 5°C to 20°C, V_{OUT} is always monotonic. The accuracy specifications in the *Accuracy Characteristics* table already include this possible shift.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMT87-Q1 features make it suitable for many general temperature-sensing applications. It can operate down to 2.7-V supply with 5.4- μ A power consumption.

9.2 Typical Applications

9.2.1 Connection to ADC

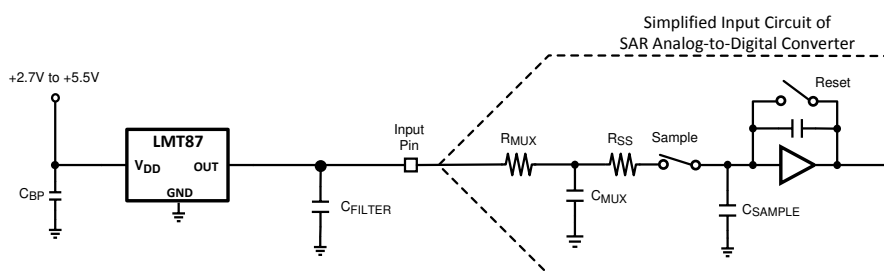


Figure 9-1. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

9.2.1.1 Design Requirements

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT87-Q1 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor (C_{FILTER}).

9.2.1.2 Detailed Design Procedure

The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Because not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

9.2.1.3 Application Curve

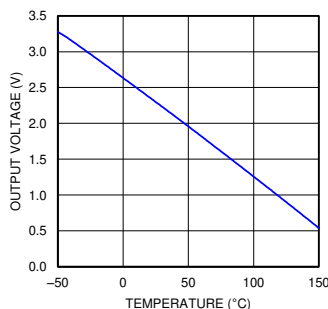


Figure 9-2. Analog Output Transfer Function

9.2.2 Conserving Power Dissipation With Shutdown

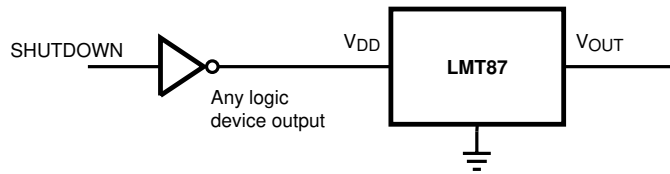


Figure 9-3. Simple Shutdown Connection of the LMT87-Q1

9.2.2.1 Design Requirements

Because the power consumption of the LMT87-Q1 is less than 9 μA , it can simply be powered directly from any logic gate output and therefore not require a specific shutdown pin. The device can even be powered directly from a microcontroller GPIO. In this way, it can easily be turned off for cases such as battery-powered systems where power savings are critical.

9.2.2.2 Detailed Design Procedure

Simply connect the V_{DD} pin of the LMT87-Q1 directly to the logic shutdown signal from a microcontroller.

9.2.2.3 Application Curves

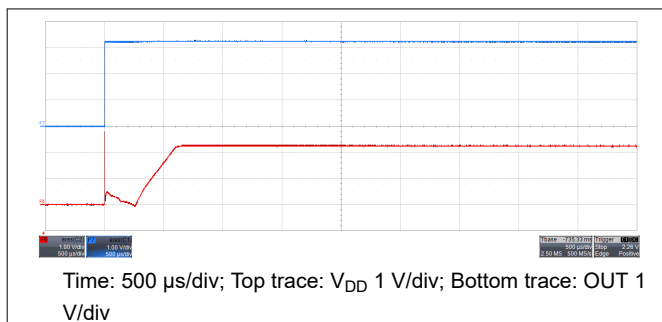


Figure 9-4. Output Turnon Response Time Without a Capacitive Load and $V_{\text{DD}} = 3.3 \text{ V}$

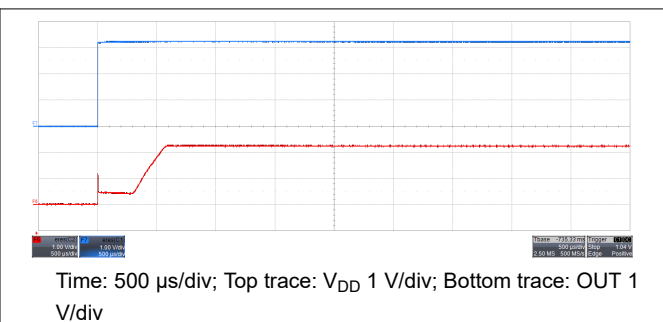


Figure 9-5. Output Turnon Response Time With a 1.1-nF Capacitive Load and $V_{\text{DD}} = 3.3 \text{ V}$

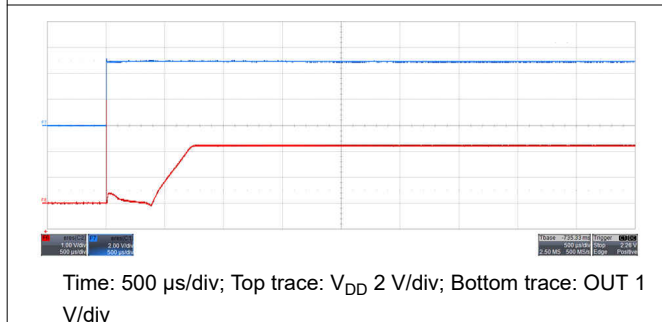


Figure 9-6. Output Turnon Response Time Without a Capacitive Load and $V_{\text{DD}} = 5 \text{ V}$

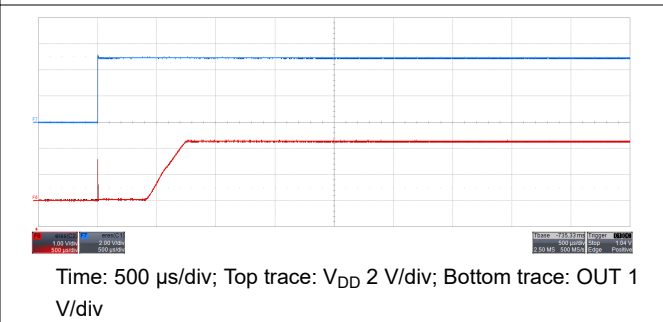


Figure 9-7. Output Turnon Response Time With a 1.1-nF Capacitive Load and $V_{\text{DD}} = 5 \text{ V}$

10 Power Supply Recommendations


The low supply current and supply range (2.7 V to 5.5 V) of the LMT87-Q1 allow the device to easily be powered from many sources. Power supply bypassing is optional and is mainly dependent on the noise on the power supply used. In noisy systems it may be necessary to add bypass capacitors to lower the noise that is coupled to the output of the LMT87-Q1.


11 Layout

11.1 Layout Guidelines

The LMT87-Q1 is extremely simple to layout. If a power-supply bypass capacitor is used, the [Layout Example](#) shows how to connect the capacitor to the device.

11.2 Layout Example

 VIA to ground plane

 VIA to power plane

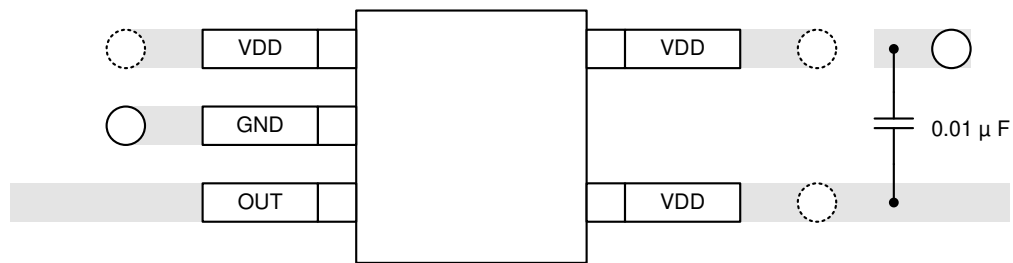


Figure 11-1. SC70 Package Recommended Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMT87QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-50 to 150	BVA	Samples
LMT87QDCKTQ1	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-50 to 150	BVA	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMT87-Q1 :

- Catalog : [LMT87](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMT87QDCKRQ1	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMT87QDCKRQ1	SC70	DCK	5	3000	208.0	191.0	35.0

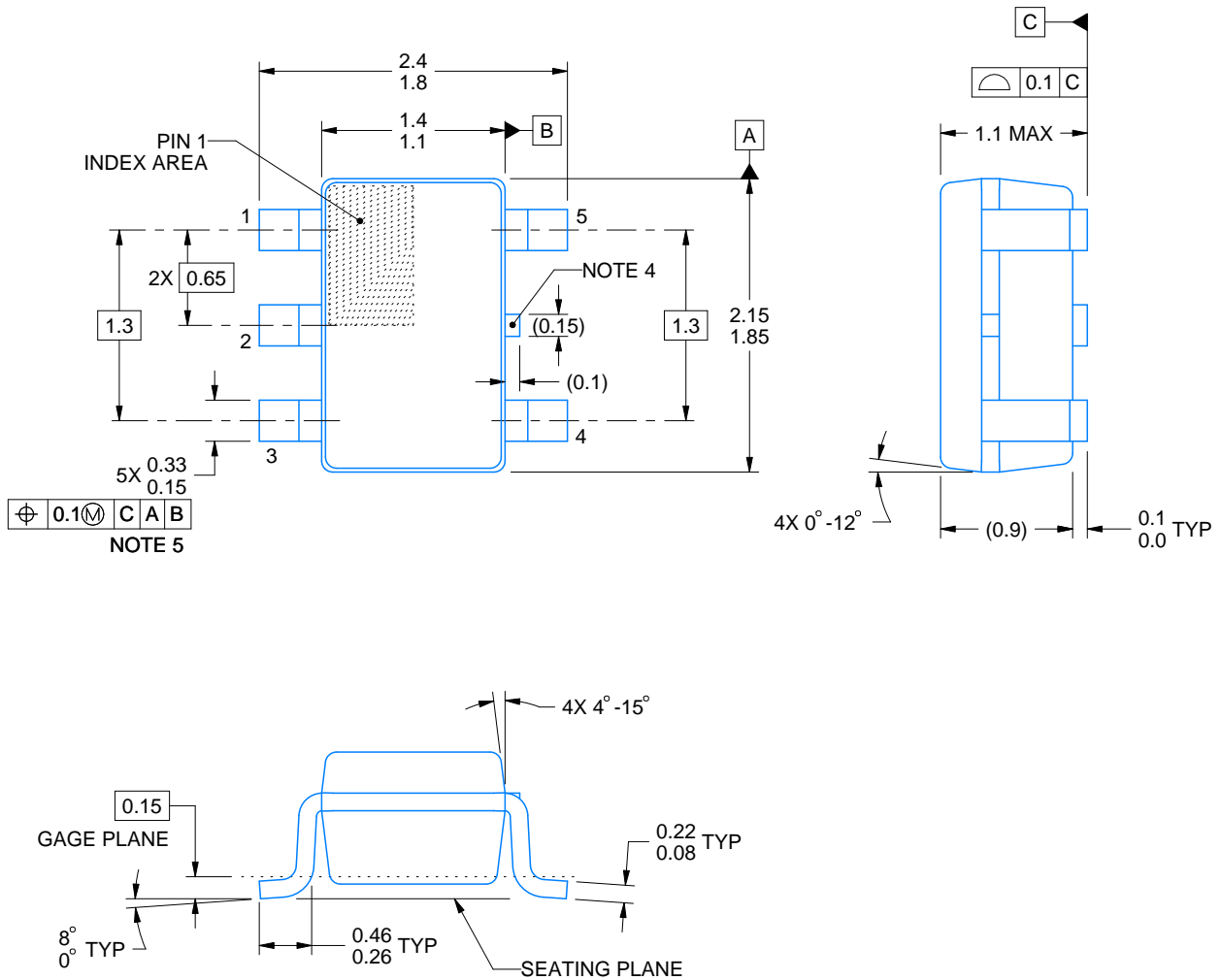
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

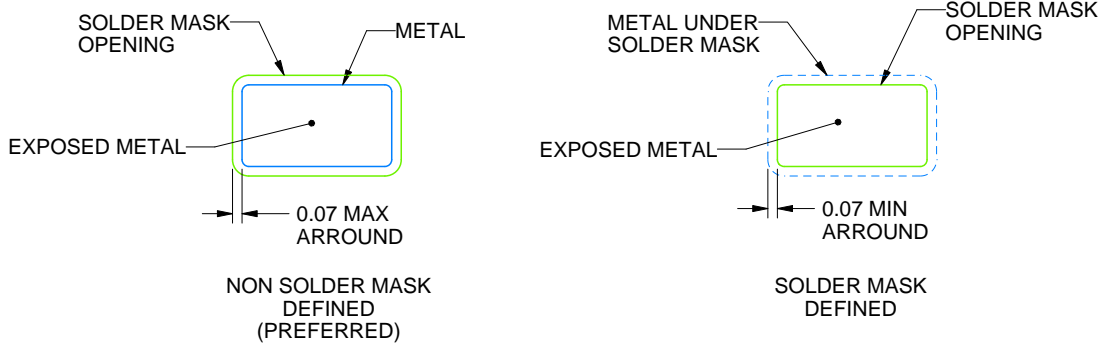
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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