

## LMV7275-Q1 Automotive Single 1.8-V Low Power Comparator With Rail-to-Rail Input

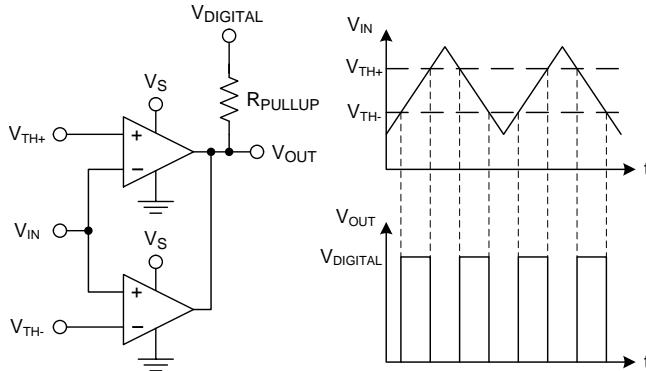
### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 3: -40°C to 85°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- ( $V_S = 1.8$  V,  $T_A = 25$ °C, Typical Values Unless Specified).
- Single or Dual Supplies
- Open Drain Output
- Ultra Low Supply Current 9  $\mu$ A Per Channel
- Low Input Bias Current 10 nA
- Low Input Offset Current 200 pA
- Low Ensured  $V_{OS}$  4 mV
- Propagation Delay 880 ns (20-mV Overdrive)
- Input Common Mode Voltage Range 0.1 V Beyond Rails

### 2 Applications

- Wearable Devices
- Mobile Phones and Tablets
- Battery-Powered Electronics
- General Purpose Low Voltage Applications

#### LMV7275-Q1 as a Window Comparator



### 3 Description

The LMV7275-Q1 is a single rail-to-rail input low power comparator, characterized at supply voltages of 1.8 V, 2.7 V, and 5 V. It consumes as little as 9- $\mu$ A supply current per channel while achieving a 800-ns propagation delay.

The LMV7275-Q1 is available in a SC-70 package. With these tiny packages, the PCB area can be significantly reduced. They are ideal for low voltage, low power, and space-critical designs.

The LMV7275-Q1 features an open-drain output stage that allows for wired-OR configurations. The open-drain output also offers the advantage of allowing the output to be pulled to any voltage up to 5.5 V, regardless of the supply voltage of the LMV7275-Q1, which is useful for level-shifting applications.

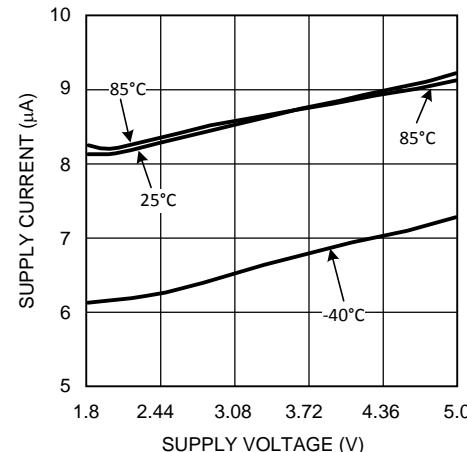
The LMV7275-Q1 is built with Texas Instruments' advance submicron silicon-gate BiCMOS process. It has bipolar inputs for improved noise performance, and CMOS outputs for lowest negative output swing.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV7275-Q1	SC70 (5)	1.25 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Low Supply Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

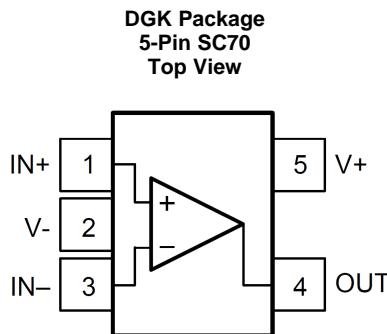
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## 4 Revision History

DATE	REVISION	NOTES
September 2015	*	Initial release.

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	SC70		
IN+	1	I	Non-Inverting Input
V-	2	P	Negative Supply Voltage
IN-	3	I	Inverting Input
OUT	4	O	Output
V+	5	P	Positive Supply Voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings <sup>(1)</sup>

	MIN	MAX	UNIT
V <sub>IN</sub> Differential		±Supply Voltage	V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	6		V
Voltage at Input/Output pins	(V <sup>-</sup> ) - 0.1	(V <sup>+</sup> ) + 0.1	V
Junction Temperature <sup>(2)</sup>	150		°C
Storage Temperature, T <sub>stg</sub>	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PCB.

### 6.2 ESD Ratings LMV7275-Q1

	VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
	Charged-device model (CDM), per AEC Q100-011	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage	1.8	5.5	V
Temperature <sup>(1)</sup>	-40	85	°C

(1) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PCB.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMV7275-Q1	UNIT
		DGK (SC70)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	273.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	106.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	54.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PCB.

## 6.5 1.8-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T<sub>J</sub> = 25°C, V<sup>+</sup> = 1.8 V, V<sup>-</sup> = 0 V.

PARAMETER	CONDITION	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
V <sub>OS</sub>	Input Offset Voltage At the temperature extremes	0.3	4	6	mV
TC V <sub>OS</sub>					
TC V <sub>OS</sub>	V <sub>CM</sub> = 0.9 V <sup>(3)</sup>	20			uV/°C
I <sub>B</sub>	Input Bias Current	10			nA
I <sub>OS</sub>	Input Offset Current	200			pA
I <sub>S</sub>	Supply Current At the temperature extremes	9	12	14	μA
I <sub>SC</sub>					
I <sub>SC</sub>	Sinking, V <sub>O</sub> = 0.9 V	4	6		mA
V <sub>OL</sub>	Output Voltage Low I <sub>O</sub> = -0.5 mA	52	100	166	mV
V <sub>OL</sub>	I <sub>O</sub> = -1.5 mA				
V <sub>CM</sub>	Input Common-Mode Voltage Range	CMRR > 45 dB	-0.1	1.9	V
CMRR	Common-Mode Rejection Ratio	0 < V <sub>CM</sub> < 1.8 V	46	78	dB
PSRR	Power Supply Rejection Ratio	V <sup>+</sup> = 1.8 V to 5 V	55	80	dB
I <sub>LEAKAG</sub>	Output Leakage Current V <sub>O</sub> = 1.8 V	2			pA
E					

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Offset Voltage average drift determined by dividing the change in V<sub>OS</sub> at temperature extremes into the total temperature change.

## 6.6 1.8-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T<sub>J</sub> = 25°C, V<sup>+</sup> = 1.8 V, V<sup>-</sup> = 0 V, V<sub>CM</sub> = 0.5 V, V<sub>O</sub> = V<sup>+</sup>/2 and R<sub>L</sub> > 1 MΩ to V<sup>-</sup>.

PARAMETER	CONDITION	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
t <sub>PHL</sub>	Propagation Delay (High to Low) Input Overdrive = 20 mV Load = 50 pF//5 kΩ	880			ns
t <sub>PLH</sub>	Propagation Delay (Low to High) Input Overdrive = 20 mV Load = 50 pF//5 kΩ	570			ns
t <sub>PLH</sub>	Propagation Delay (Low to High) Input Overdrive = 50 mV Load = 50 pF//5 kΩ	1100			ns
t <sub>PLH</sub>	Propagation Delay (Low to High) Input Overdrive = 50 mV Load = 50 pF//5 kΩ	800			ns

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

## 6.7 2.7-V Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{ V}$ ,  $V^- = 0\text{ V}$ .

PARAMETER	CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
V <sub>OS</sub> Input Offset Voltage		0.3	4		mV
	At the temperature extremes			6	
TC V <sub>OS</sub> Input Offset Temperature Drift	V <sub>CM</sub> = 1.35 V <sup>(3)</sup>		20		µV/°C
I <sub>B</sub> Input Bias Current			10		nA
I <sub>OS</sub> Input offset Current			200		pA
I <sub>S</sub> Supply Current		9	13		µA
	At the temperature extremes			15	
I <sub>SC</sub> Output Short Circuit Current	Sinking, V <sub>O</sub> = 1.35 V	10	15		mA
V <sub>OL</sub> Output Voltage Low	I <sub>O</sub> = -0.5 mA	50	70		mV
	I <sub>O</sub> = -2 mA	155	220		
V <sub>CM</sub> Input Common Voltage Range	CMRR > 45 dB	-0.1	2.8		V
CMRR Common-Mode Rejection Ratio	0 < V <sub>CM</sub> < 2.7 V	46	78		dB
PSRR Power Supply Rejection Ratio	V <sup>+</sup> = 1.8 V to 5 V	55	80		dB
I <sub>LEAKAGE</sub> Output Leakage Current	V <sub>O</sub> = 2.7 V		2		pA

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Offset Voltage average drift determined by dividing the change in V<sub>OS</sub> at temperature extremes into the total temperature change.

## 6.8 2.7-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = 0.5\text{ V}$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^-$ .

PARAMETER	CONDITION	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
t <sub>PHL</sub> Propagation Delay (High to Low)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1200		ns
	Input Overdrive = 50 mV Load = 50 pF//5 kΩ		810		ns
t <sub>PLH</sub> Propagation Delay (Low to High)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1300		ns
	Input Overdrive = 50 mV Load = 50 pF//5 kΩ		860		ns

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

## 6.9 5-V Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ .

PARAMETER	CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
V <sub>OS</sub> Input Offset Voltage		0.3	4		mV
	At the temperature extremes		6		
TC V <sub>OS</sub> Input Offset Temperature Drift	V <sub>CM</sub> = 2.5 V <sup>(3)</sup>		20		µV/°C
I <sub>B</sub> Input Bias Current			10		nA
I <sub>OS</sub> Input Offset Current			200		pA
I <sub>S</sub> Supply Current		10	14		µA
	At the temperature extremes			16	
I <sub>SC</sub> Output Short Circuit Current	Sinking, V <sub>O</sub> = 2.5 V	18	34		mA
V <sub>OL</sub> Output Voltage Low	I <sub>O</sub> = -0.5 mA	27	70		mV
	I <sub>O</sub> = -4.0 mA	225	315		

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Offset Voltage average drift determined by dividing the change in V<sub>OS</sub> at temperature extremes into the total temperature change.

## 5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ .

PARAMETER	CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{CM}$	Input Common Voltage Range	CMRR > 45 dB	-0.1	5.1	V
CMRR	Common-Mode Rejection Ratio	$0 < V_{CM} < 5.0\text{ V}$	46	78	dB
PSRR	Power Supply Rejection Ratio	$V^+ = 1.8\text{ V}$ to $5\text{ V}$	55	80	dB
$I_{LEAKAGE}$	$V_O = 5\text{ V}$		2		pA

## 6.10 5-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5.0\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = 0.5\text{ V}$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^-$ .

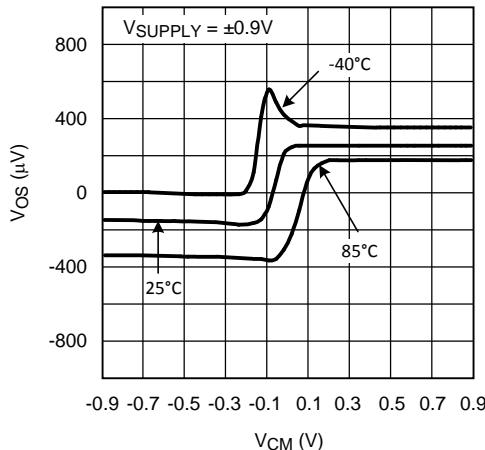
PARAMETER	CONDITION	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$t_{PHL}$	Propagation Delay (High to Low) Input Overdrive = 20 mV Load = 50 pF//5 k $\Omega$		2100		ns
	Input Overdrive = 50 mV Load = 50 pF//5 k $\Omega$		1380		ns
$t_{PLH}$	Propagation Delay (Low to High) Input Overdrive = 20 mV Load = 50 pF//5 k $\Omega$		1800		ns
	Input Overdrive = 50 mV Load = 50 pF//5 k $\Omega$		1100		ns

(1) All limits are ensured by testing or statistical analysis.

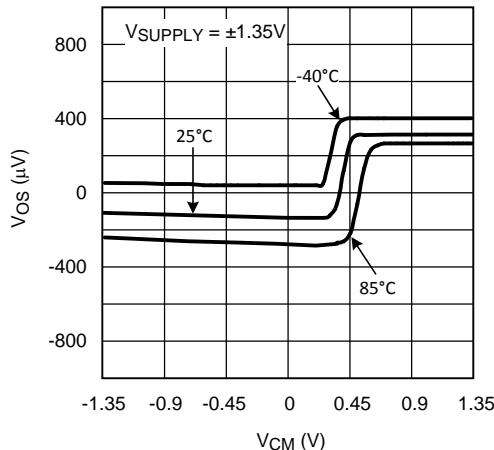
(2) Typical values represent the most likely parametric norm.

## 6.11 Typical Characteristics

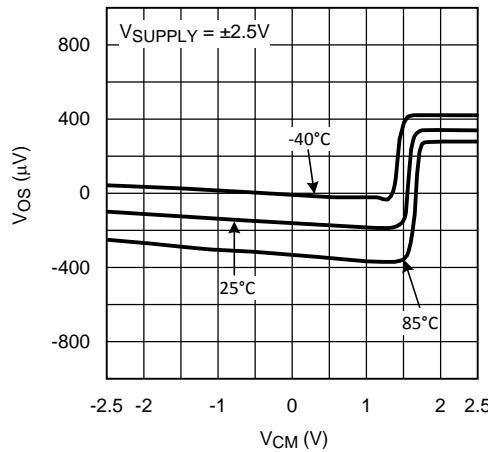
$T_A = 25^\circ\text{C}$ , Unless otherwise specified.



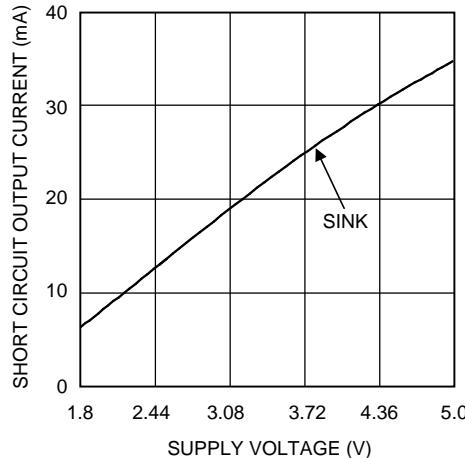
**Figure 1.  $V_{OS}$  vs.  $V_{CM}$**



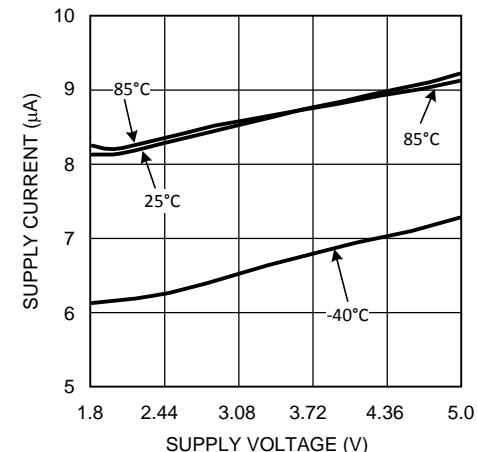
**Figure 2.  $V_{OS}$  vs.  $V_{CM}$**



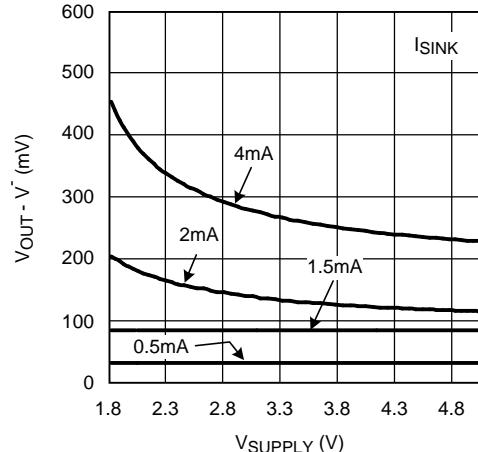
**Figure 3.  $V_{OS}$  vs.  $V_{CM}$**



**Figure 4. Short Circuit vs. Supply Voltage**



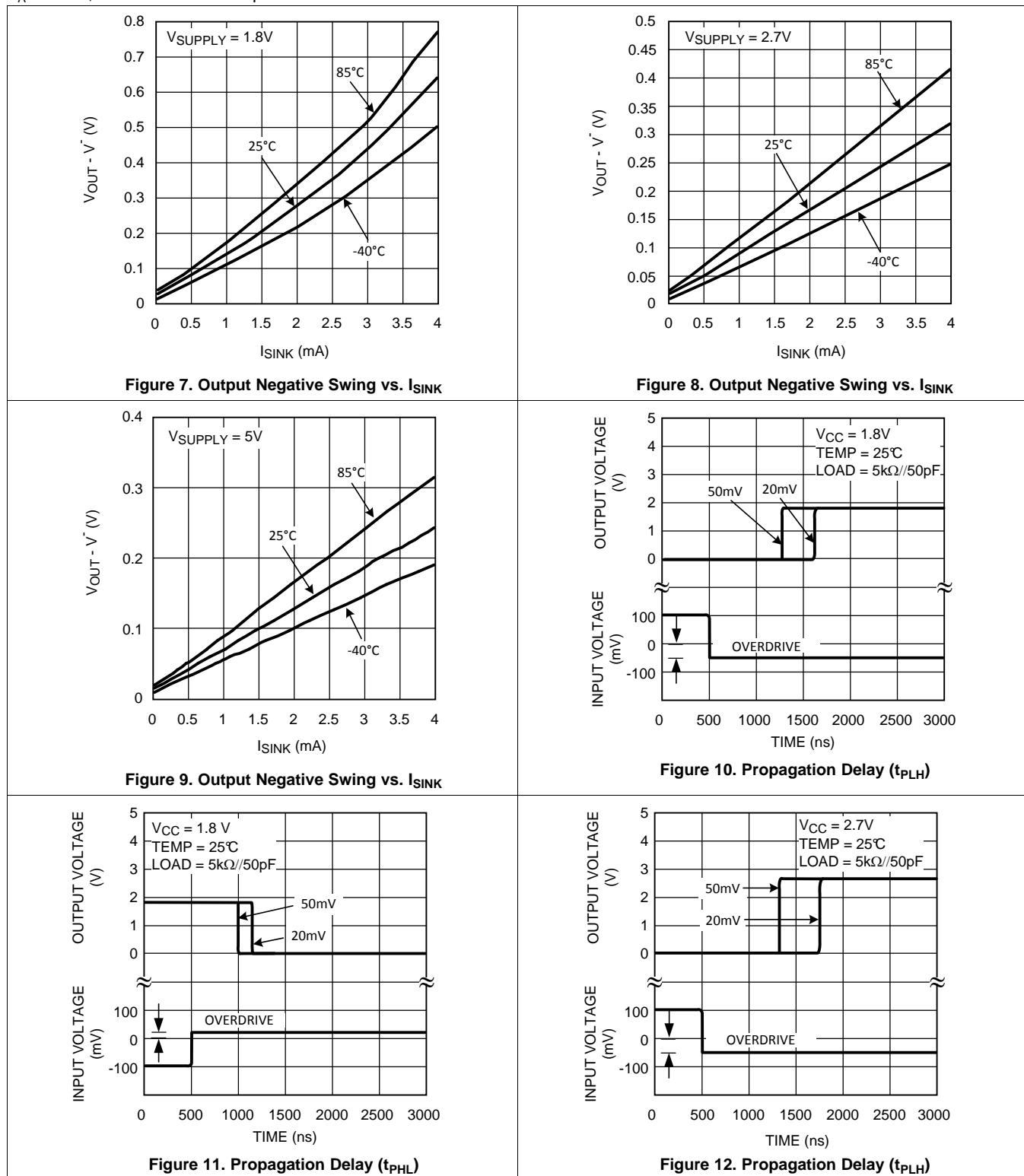
**Figure 5. Supply Current vs. Supply Voltage**



**Figure 6. Output Negative Swing vs.  $V_{SUPPLY}$**

## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ , Unless otherwise specified.



## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ , Unless otherwise specified.

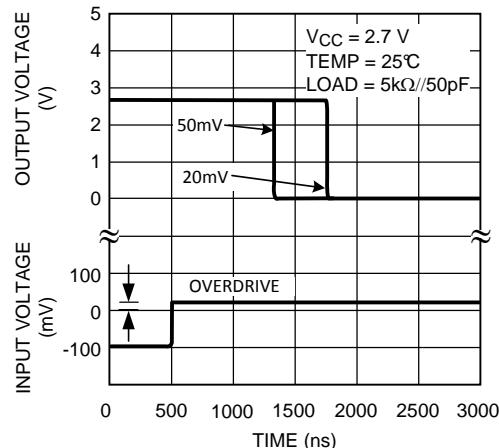


Figure 13. Propagation Delay ( $t_{\text{PHL}}$ )

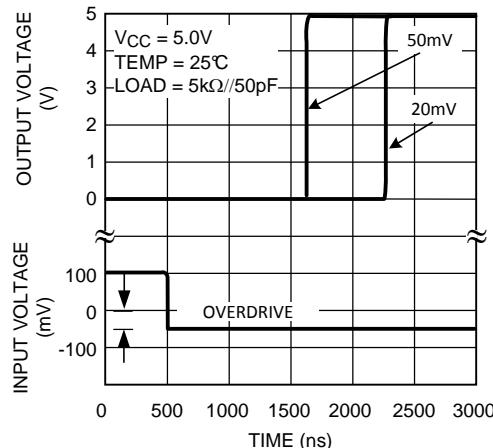


Figure 14. Propagation Delay ( $t_{\text{PLH}}$ )

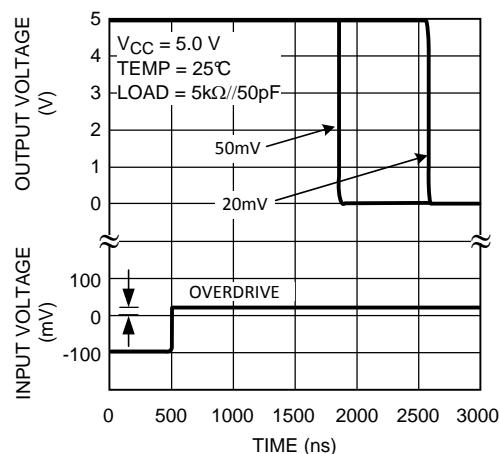


Figure 15. Propagation Delay ( $t_{\text{PHL}}$ )

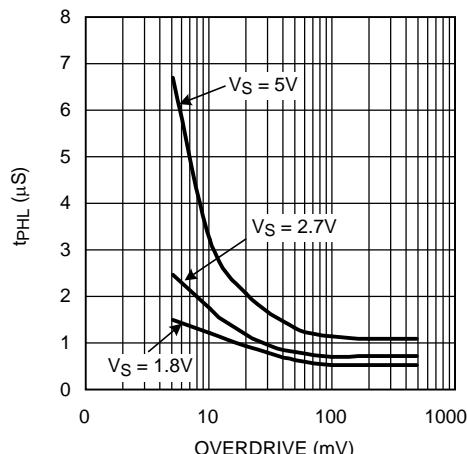


Figure 16.  $t_{\text{PHL}}$  vs. Overdrive

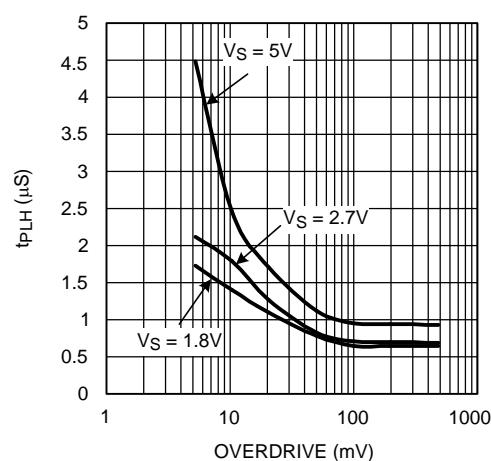


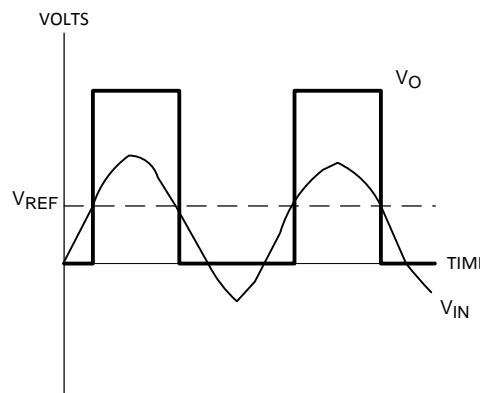
Figure 17.  $t_{\text{PLH}}$  vs. Overdrive

## 7 Detailed Description

### 7.1 Overview

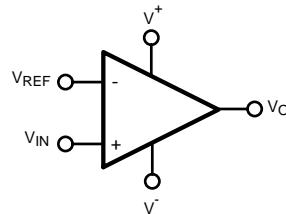
A comparator is often used to convert an analog signal to a digital signal. As shown in [Figure 18](#), the comparator compares an input voltage ( $V_{IN}$ ) to a reference voltage ( $V_{REF}$ ). If  $V_{IN}$  is less than  $V_{REF}$ , the output transistor turns on and pulls the output to  $V_-$ , and thus the output ( $V_O$ ) goes low.

However, if  $V_{IN}$  is greater than  $V_{REF}$ , the output transistor turns off and the voltage ( $V_O$ ) is pulled high by the external pull-up resistor.



**Figure 18. Basic Comparator**

### 7.2 Functional Block Diagram



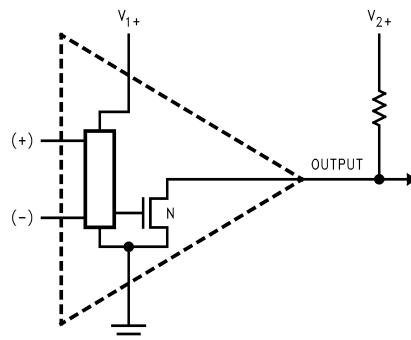
### 7.3 Feature Description

#### 7.3.1 Rail-to-Rail Input Stage

The LMV7275-Q1 has an input common mode voltage range ( $V_{CM}$ ) of  $-0.1\text{V}$  below the  $V^-$  to  $0.1\text{V}$  above  $V^+$ . This is achieved by using paralleled PNP and NPN differential input pairs. When the  $V_{CM}$  is near  $V^+$ , the NPN pair is on and the PNP pair is off. When the  $V_{CM}$  is near  $V^-$ , the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around  $950\text{mV}$  from  $V^+$ . Because each input stage has its own offset voltage ( $V_{OS}$ ), the  $V_{OS}$  of the comparator becomes a function of the  $V_{CM}$ . See curves for  $V_{OS}$  vs.  $V_{CM}$  in the [Typical Characteristics](#) section. In application design, it is recommended to keep the  $V_{CM}$  away from the crossover point to avoid problems. The wide input voltage range makes LMV7275-Q1 ideal in power supply monitoring circuits, where the comparators are used to sense signals close to ground and power supplies.

## Feature Description (continued)

### 7.3.2 Output Stage



**Figure 19. LMV7275-Q1 Open-Drain Output**

The LMV7275-Q1 has an open-drain output that requires a pull-up resistor to a positive supply voltage for the output to operate properly. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage ( $V_{2+}$ ) by the external pull-up resistor. This allows the output to be OR'ed with other open-drain outputs on the same bus.

The output pull-up resistor may be connected to any voltage level between  $V_-$  and  $V_+$  for level shifting applications.

## 7.4 Device Functional Modes

### 7.4.1 Capacitive and Resistive Loads

The propagation delay on the rising edge of the LMV7275-Q1 depends on the load resistance and capacitance values.

### 7.4.2 Noise

Most comparators have rather low gain. This allows the output to alternate between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero and triggers on noise. The high gain of this comparator eliminates this problem. Less than 1  $\mu$ V of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See [Hysteresis](#).)

### 7.4.3 Hysteresis

It is a standard procedure to use hysteresis (positive feedback) around a comparator to prevent oscillation due to the comparator triggering its own noise on slowly ramping signals. The following sections will describe various ways to apply hysteresis.

#### 7.4.3.1 Non-inverting Comparator With Hysteresis

Non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference ( $V_{ref}$ ) at the inverting input. When  $V_{in}$  is low, the output is also low. For the output to switch from low to high,  $V_{in}$  must rise up to  $V_{in1}$  where  $V_{in1}$  is calculated by:

$$V_{in1} = \frac{V_{ref} (R_1 + R_2)}{R_2} \quad (1)$$

When  $V_{in}$  is high, the output is also high. To make the comparator switch back to its low state,  $V_{in}$  must equal  $V_{ref}$  before  $V_A$  will again equal  $V_{ref}$ .  $V_{in}$  can be calculated by:

$$V_{in2} = \frac{V_{ref} (R_1 + R_2) - V_{CC} R_1}{R_2} \quad (2)$$

The hysteresis of this circuit is the difference between  $V_{in1}$  and  $V_{in2}$ .

## Device Functional Modes (continued)

$$\Delta V_{in} = V_{CC} R_1 / R_2 \quad (3)$$

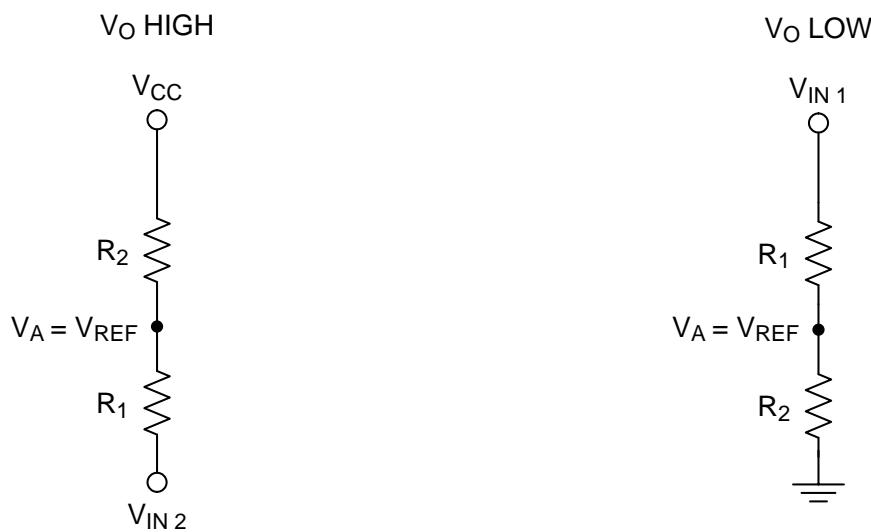
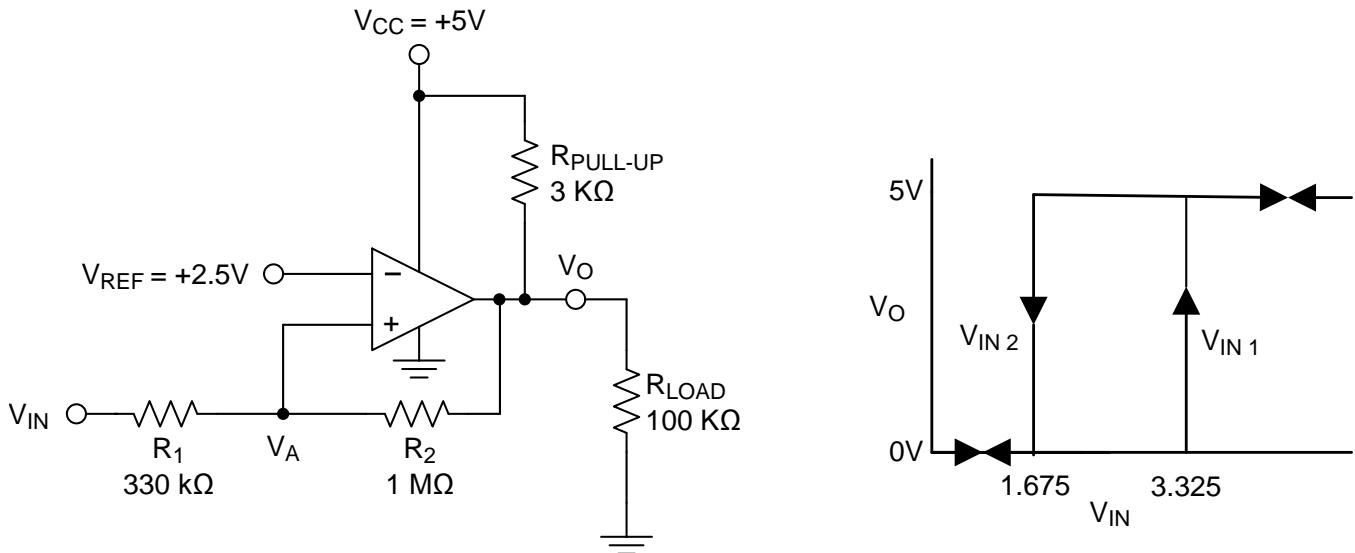


Figure 20. Non-Inverting Comparator With Hysteresis

### 7.4.3.2 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage  $V_{CC}$  of the comparator. When  $V_{in}$  at the inverting input is less than  $V_a$ , the voltage at the non-inverting node of the comparator ( $V_{in} < V_a$ ), the output voltage is high (for simplicity assume  $V_O$  switches as high as  $V_{CC}$ ). The three network resistors can be represented as  $R_1//R_3$  in series with  $R_2$ . The lower input trip voltage  $V_{a1}$  is defined as:

$$V_{a1} = \frac{V_{CC} R_2}{(R_1 // R_3) + R_2} \quad (4)$$

When  $V_{in}$  is greater than  $V_a$  ( $V_{in} > V_a$ ), the output voltage is low very close to ground. In this case the three network resistors can be presented as  $R_2//R_3$  in series with  $R_1$ . The upper trip voltage  $V_{a2}$  is defined as:

## Device Functional Modes (continued)

$$V_{a2} = \frac{V_{CC} (R_2 // R_3)}{R_1 + (R_2 // R_3)} \quad (5)$$

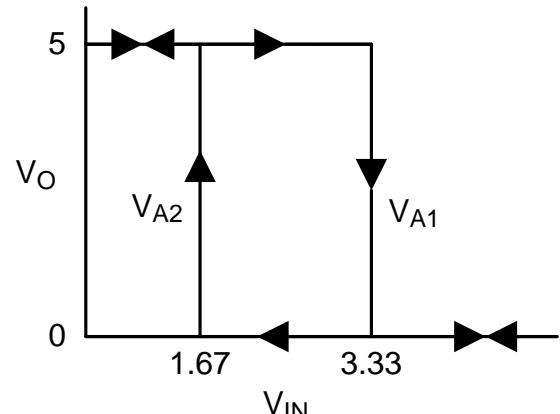
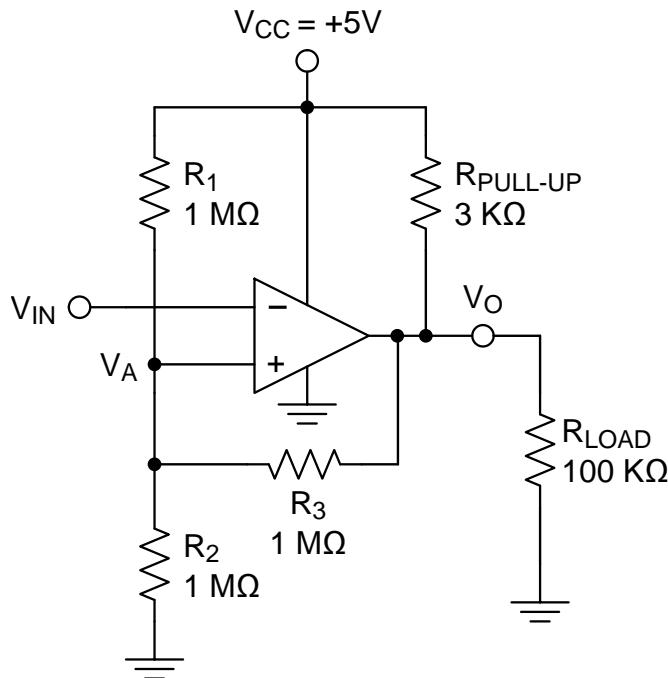
The total hysteresis provided by the network is defined as:

$$\Delta V_a = V_{a1} - V_{a2} \quad (6)$$

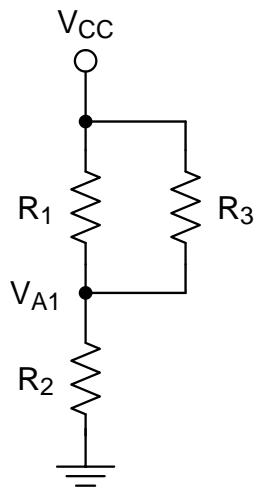
To assure that the comparator will always switch fully to  $V_{CC}$  and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{PULL-UP} \ll R_{LOAD} \quad (7)$$

$$\text{and } R_1 > R_{PULL-UP}. \quad (8)$$



$V_O$  HIGH



$V_O$  LOW

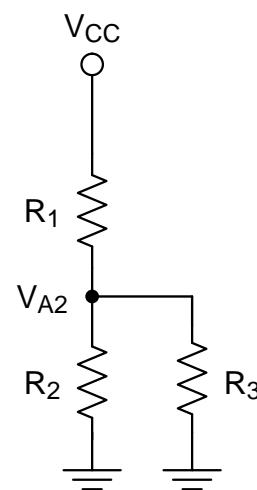


Figure 21. Inverting Comparator With Hysteresis

## Device Functional Modes (continued)

### 7.4.4 Zero Crossing Detector

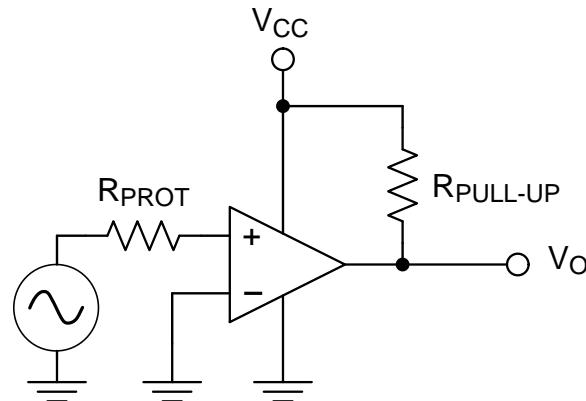


Figure 22. Simple Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the Non-Inverting input is connected to a 100 mV<sub>PP</sub> AC signal. As the signal at the Non-Inverting input crosses 0 V, the output of the comparator changes state.

R<sub>PROT</sub> is an optional input protection resistor to limit the current should the input voltage exceed the supply rails. R<sub>PROT</sub> should be a minimum of 1 kΩ per volt of expected over-voltage and limit the current to less than  $\pm 1\text{mA}$  under worst case fault conditions.

#### 7.4.4.1 Zero Crossing Detector With Hysteresis

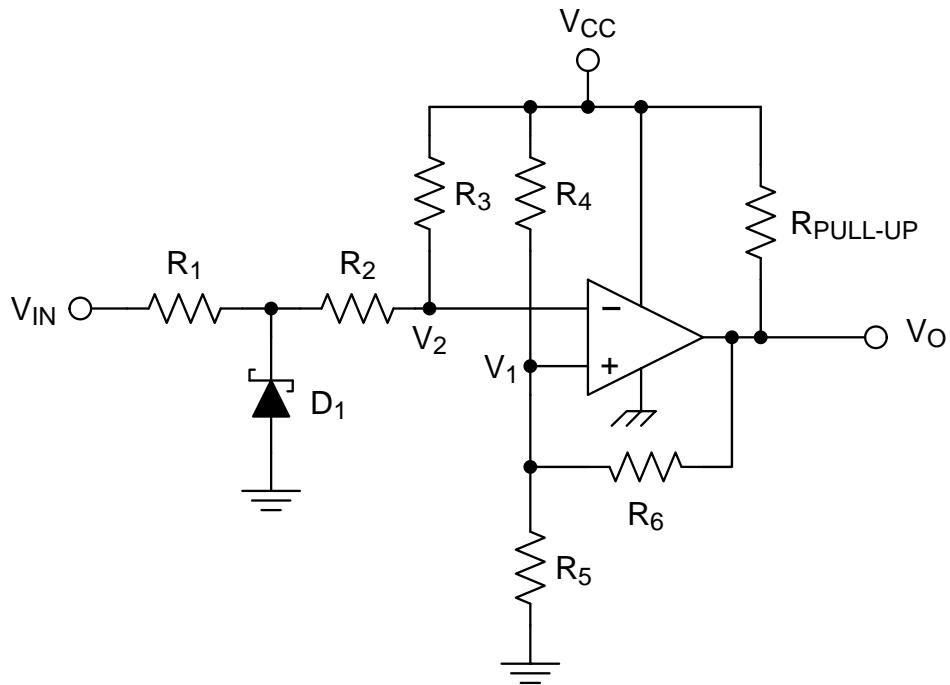


Figure 23. Zero Crossing Detector With Hysteresis

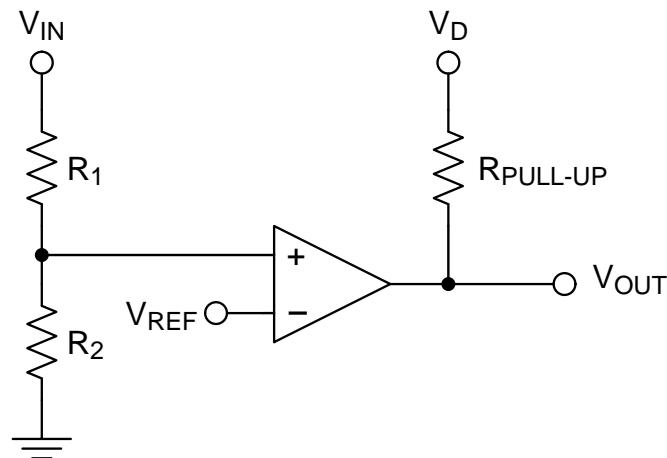
To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider R<sub>4</sub> and R<sub>5</sub> establishes a reference voltage, V<sub>1</sub>, at the positive input. By making the series resistance, R<sub>1</sub> plus R<sub>2</sub> equal to R<sub>5</sub>, the switching condition, V<sub>1</sub> = V<sub>2</sub>, will be satisfied when V<sub>IN</sub> = 0.

## Device Functional Modes (continued)

The positive feedback resistor,  $R_6$ , is made very large (with respect to  $R_5 \parallel R_6 = 2000 R_5$ ). The resultant hysteresis established by this network is very small ( $\Delta V_1 < 10$  mV) but it is sufficient to insure rapid output voltage transitions.

Diode  $D_1$  is used to insure that the inverting input terminal of the comparator never goes below approximately  $-100$  mV. As the input terminal goes negative,  $D_1$  will forward bias, clamping the node between  $R_1$  and  $R_2$  to approximately  $-300$  mV. This sets up a voltage divider with  $R_2$  and  $R_3$  preventing  $V_2$  from going below ground. The maximum negative input overdrive is limited by the current handling ability of  $D_1$ .

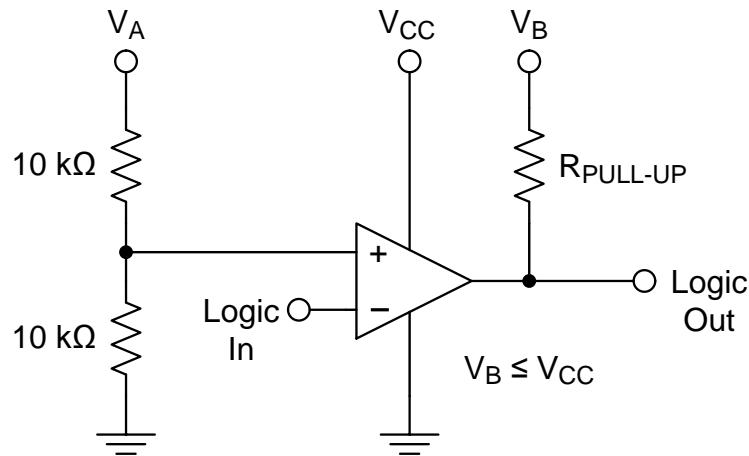
### 7.4.5 Threshold Detector



**Figure 24. Threshold Detector**

Instead of tying the inverting input to  $0$  V, the inverting input can be tied to a reference voltage. As the input on the Non-Inverting input passes the  $V_{REF}$  threshold, the output of the comparator changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

### 7.4.6 Universal Logic Level Shifter



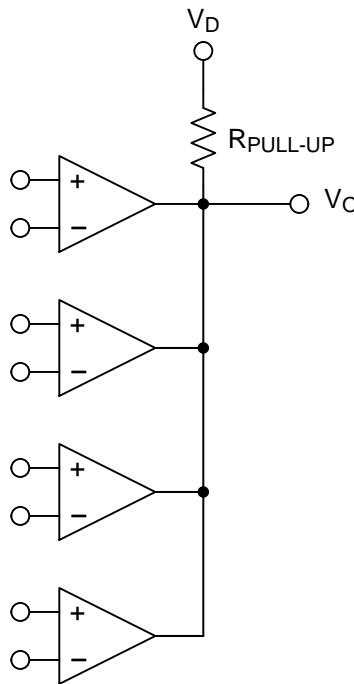
**Figure 25. Logic Level Shifter**

The output of LMV7275-Q1 is an unconnected drain of an NMOS device, which can be pulled up, through a resistor, to any desired output level below the comparators power supply voltage ( $V_B \leq V_{CC}$ ). Hence, the following simple circuit works as a universal logic level shifter, pulling up the signal to the desired level.

## Device Functional Modes (continued)

For example,  $V_A$  could be the 5-V analog supply voltage, where  $V_B$  could be the 3.3-V supply of the processor. The output will now be compatible with the 3.3-V logic.

### 7.4.7 OR'ING the Output



**Figure 26. OR'ing the Outputs**

Open-drain outputs may be tied together, pulled up to  $V_D$  by a common resistor to provide an output OR'ing function. If any of the comparator outputs goes low, the output  $V_O$  goes low.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LMV7275-Q1 is a single-supply comparator with 880 ns of propagation delay and only 12  $\mu$ A of supply current.

### 8.2 Typical Applications

#### 8.2.1 Square Wave Oscillator

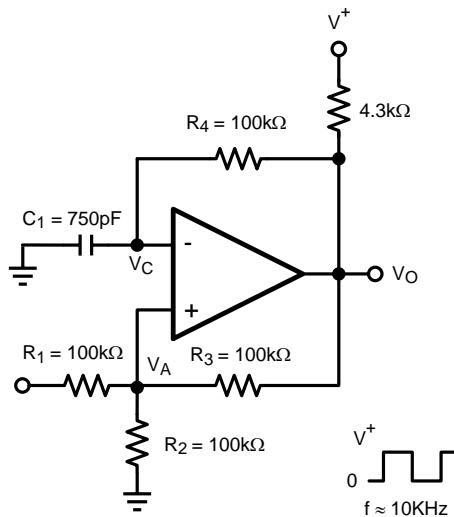


Figure 27. Square Wave Oscillator Application

##### 8.2.1.1 Design Requirements

A typical application for a comparator is as a square wave oscillator. Figure 27 generates a square wave whose period is set by the RC time constant of the capacitor  $C_1$  and resistor  $R_4$ . The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

##### 8.2.1.2 Detailed Design Procedure

To analyze the circuit, consider it when the output is high. That implies that the inverted input ( $V_C$ ) is lower than the Non-Inverting input ( $V_A$ ).

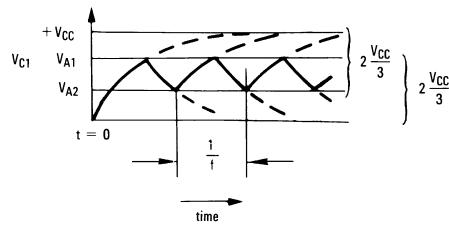


Figure 28. Squarewave Oscillator Timing Thresholds

## Typical Applications (continued)

This causes the  $C_1$  to get charged through  $R_4$ , and the voltage  $V_C$  increases till it is equal to the Non-Inverting input. The value of  $V_A$  at this point is

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \parallel R_3} \quad (9)$$

If  $R_1 = R_2 = R_3$ , then  $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of  $V_A$  at this point is

$$V_{A2} = \frac{V_{CC} (R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)} \quad (10)$$

If  $R_1 = R_2 = R_3$ , then  $V_{A2} = V_{CC}/3$

The capacitor  $C_1$  now discharges through  $R_4$ , and the voltage  $V_C$  decreases till it is equal to  $V_{A2}$ , at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge  $C_1$  from  $2V_{CC}/3$  to  $V_{CC}/3$ , which is given by  $R_4 C_1 \ln 2$ . Hence the formula for the frequency is:

$$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2)$$

### 8.2.1.3 Application Curve

Figure 29 shows the simulated results of an oscillator using the following values:

1.  $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
2.  $C_1 = 750 \text{ pF}$ ,  $C_L = 20 \text{ pF}$
3.  $V+ = 5 \text{ V}$ ,  $V- = \text{GND}$
4.  $C_{\text{STRAY}}$  (not shown) from  $V_a$  to  $\text{GND} = 10 \text{ pF}$

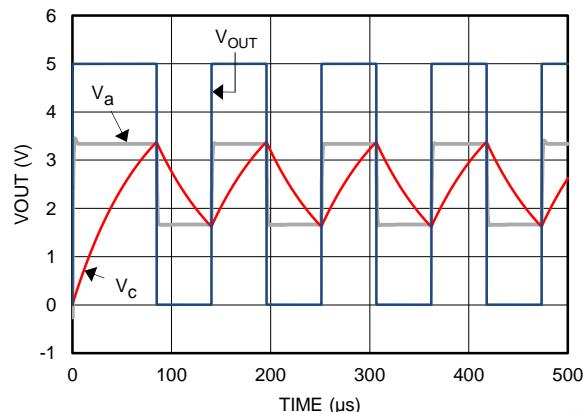
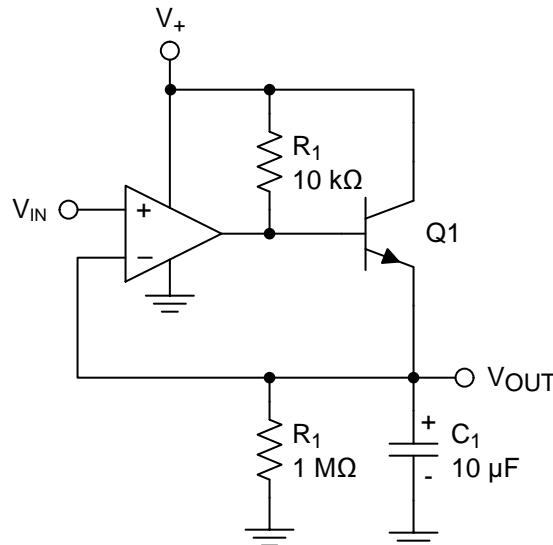


Figure 29. Square Wave Oscillator Output Waveforms

## Typical Applications (continued)

### 8.2.2 Positive Peak Detector

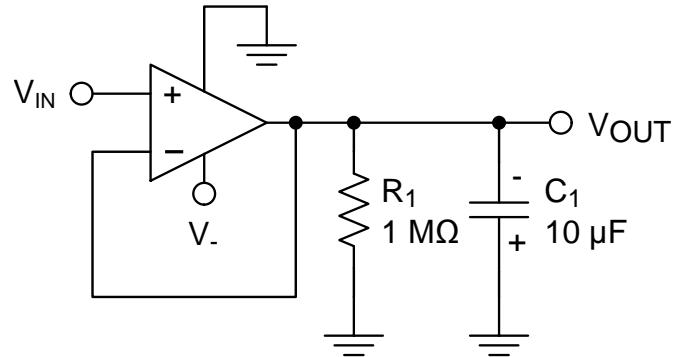


**Figure 30. Positive Peak Detector**

The positive peak detector is basically the comparator operated as a unity gain follower with a large holding capacitor from the output to ground. A transistor is added to the output to provide a low impedance current source. The upper output swing is limited by the emitter-base forward voltage. This allows capture of the most positive input signal between 0 V and  $(V_+) - 0.7V$ .

When the output of the comparator goes high, current is passed through the transistor to charge up the capacitor. The only discharge path will be the 1-MΩ resistor shunting C1 and any load that is connected to the output. The decay time can be altered simply by changing the 1-MΩ resistor.

### 8.2.3 Negative Peak Detector



**Figure 31. Negative Peak Detector for Negative Supply**

The Negative Peak Detector circuit will store the peak negative voltage below ground ( 0 V to  $V_-$ ). For the negative detector, the output transistor acts as a low-impedance current sink.

When  $V_{IN}$  is more negative than  $V_{OUT}$ , the output transistor will conduct and pull the output to  $-V_{CC}$ , charging C1. Charging stops when C1 reaches the same level as  $V_{IN}$ . Because there is no pull-up resistor, the only discharge path will be the 1-MΩ resistor and any load impedance applied. Therefore, the decay time is set by varying the 1-MΩ resistor. Be sure to observe the polarity of C1!

## Typical Applications (continued)

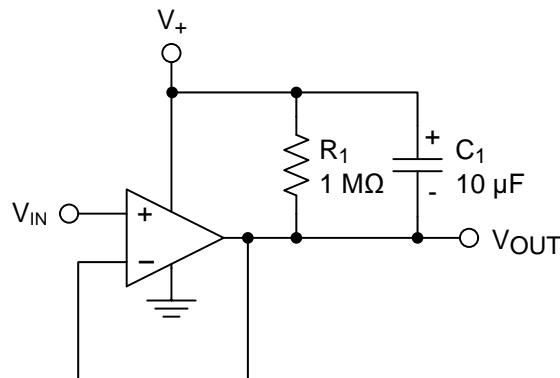


Figure 32. Negative Peak Detector for Positive Supply

An alternate positive supply version is shown in [Figure 32](#) that will capture the lowest applied  $V_{IN}$  value between  $V_+$  and ground ( $V_+$  to 0V).

The output of either version should be buffered by a high-impedance follower stage to prevent loading of the RC circuit.

### 8.2.4 Window Detector

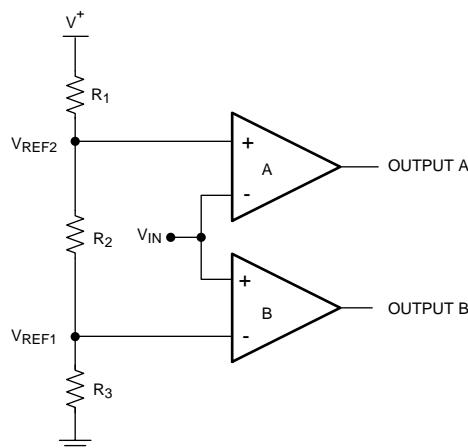
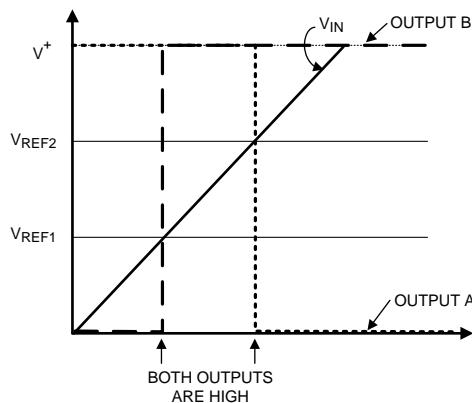


Figure 33. Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when  $V_{REF1} < V_{IN} < V_{REF2}$

## Typical Applications (continued)



**Figure 34. Window Detector Output Signal**

The comparator outputs A and B are high only when  $V_{REF1} < V_{IN} < V_{REF2}$ , or *within the window*, where these are defined as:

$$V_{REF1} = R_3 / (R_1 + R_2 + R_3) \times V_+ \quad (11)$$

$$V_{REF2} = (R_2 + R_3) / (R_1 + R_2 + R_3) \times V_+ \quad (12)$$

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

The outputs should be tied together and use a shared pull-up resistor for a common logic output. If individual limit outputs are needed, then each output will require its own pull-up resistor.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.

## 9 Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01- $\mu$ F ceramic capacitor in parallel with a 10- $\mu$ F capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to *ring* due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV7275-Q1 as a high-speed device. Keep the ground paths short and place small (low-ESR ceramic) bypass capacitors directly between the V+ and V- pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

## 10 Layout

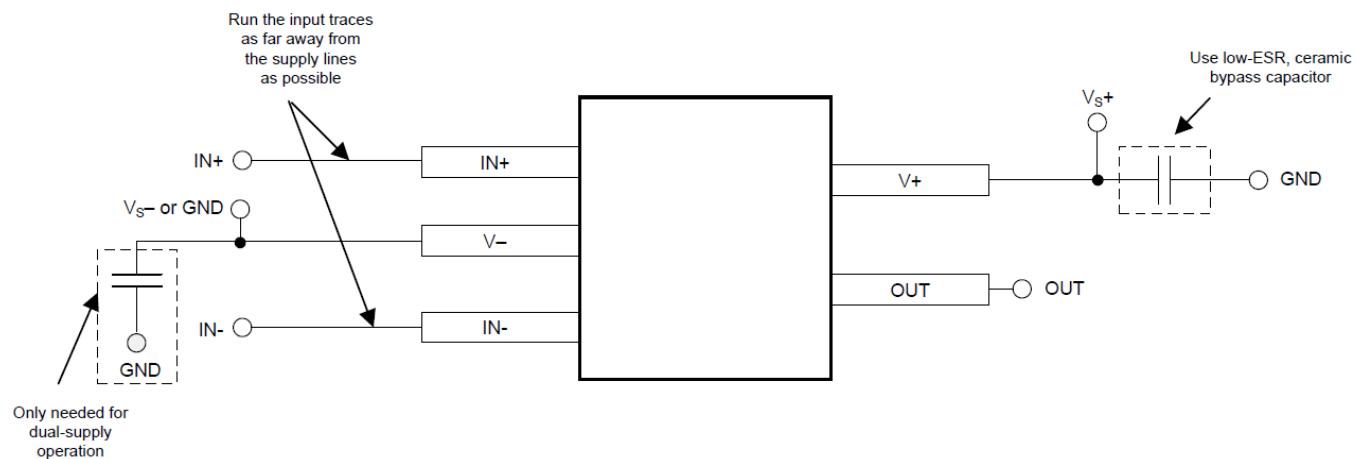
### 10.1 Layout Guidelines

#### 10.1.1 Circuit Techniques for Avoiding Oscillations in Comparator Applications

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and response time. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to malfunction. To avoid problems, a small bypass capacitor, such as 0.1- $\mu$ F ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8  $\mu$ F or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In a dual-supply application, a 0.1- $\mu$ F capacitor is recommended to be placed across V<sup>+</sup> and V<sup>-</sup> pins.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs through stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).
3. It is a good practice to use an unbroken ground plane on a printed-circuit-board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.
4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard. This can be achieved by running a topside ground plane between the output and inputs. A typical PCB layout is shown in [Figure 35](#).
5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.

## 10.2 Layout Example



**Figure 35. Typical PCB Layout**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

For developmental support, see the following:

- LMV7275 PSPICE Model, [SNOM555](#)
- TINA-TI SPICE-Based Analog Simulation Program, <http://www.ti.com/tool/tina-ti>
- DIP Adapter Evaluation Module, <http://www.ti.com/tool/dip-adapter-evm>
- TI Universal Operational Amplifier Evaluation Module, <http://www.ti.com/tool/opampevm>

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- AN-74 A Quad of Independently Functioning Comparators, [SNOA654](#)

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV7275IDCKRQ1	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	SKA
LMV7275IDCKRQ1.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	SKA

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

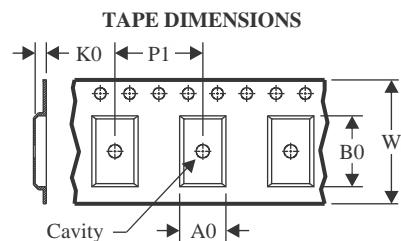
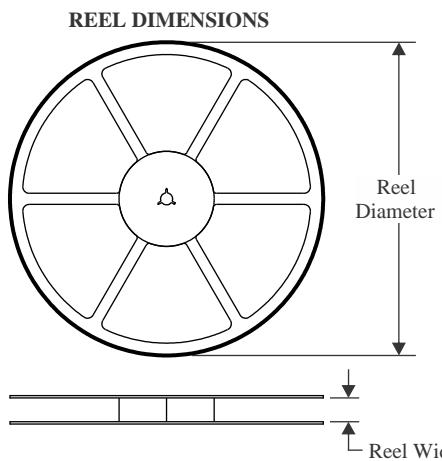
**OTHER QUALIFIED VERSIONS OF LMV7275-Q1 :**

- Catalog : [LMV7275](#)

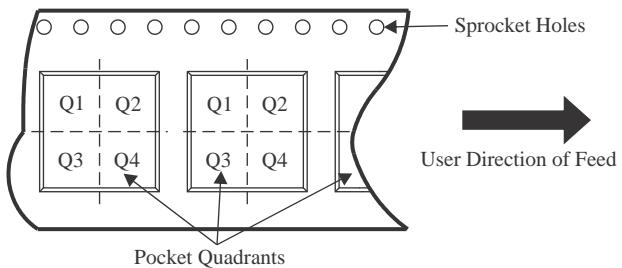
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NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

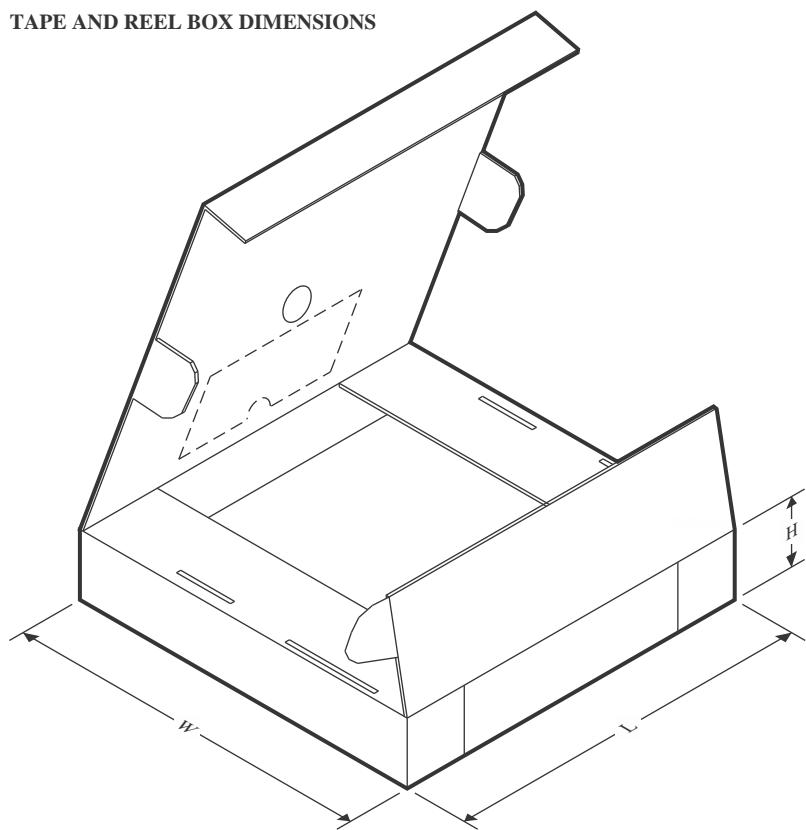
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7275IDCKRQ1	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7275IDCKRQ1	SC70	DCK	5	3000	208.0	191.0	35.0

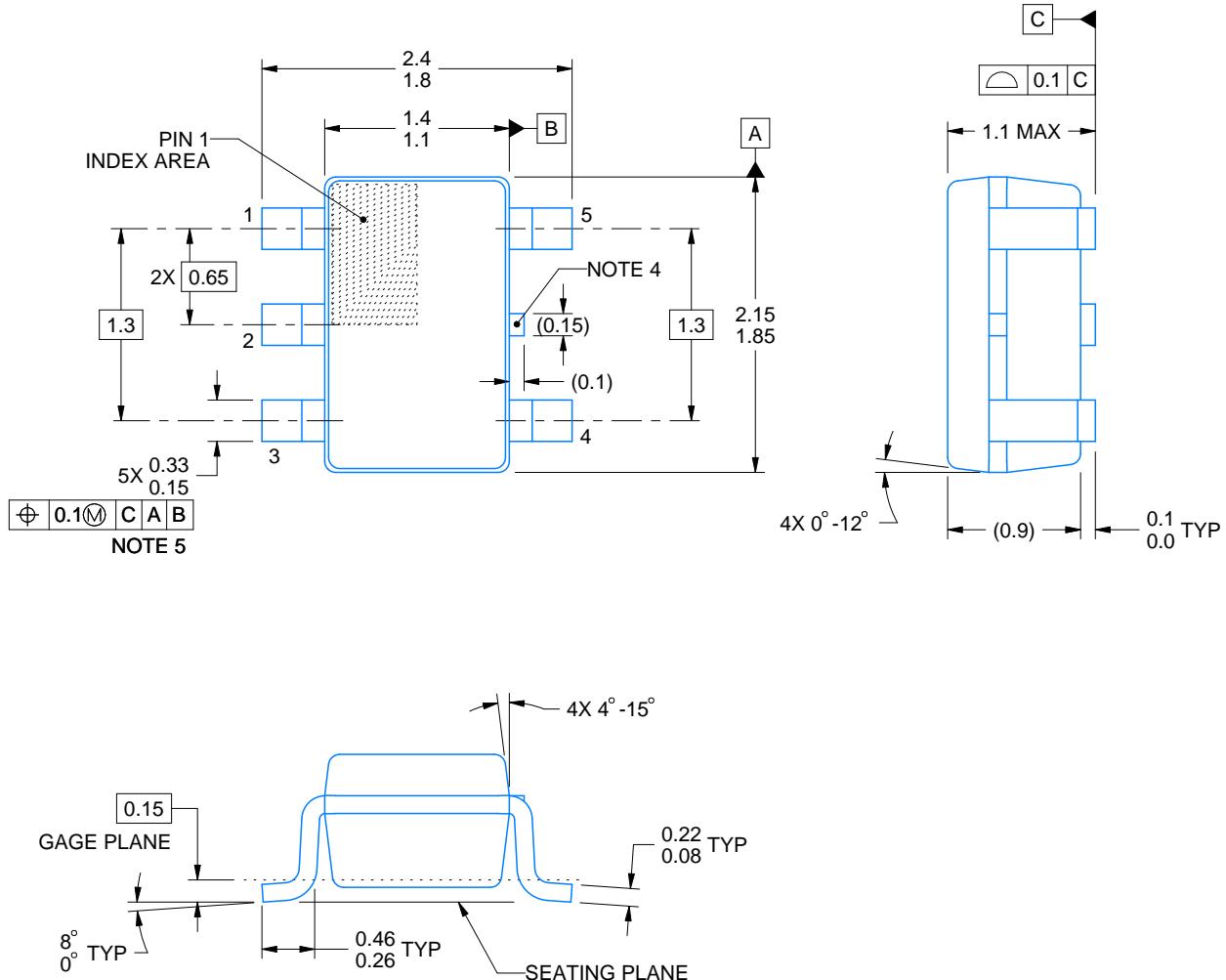
## PACKAGE OUTLINE

**DCK0005A**



## SOT - 1.1 max height

## SMALL OUTLINE TRANSISTOR



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## NOTES:

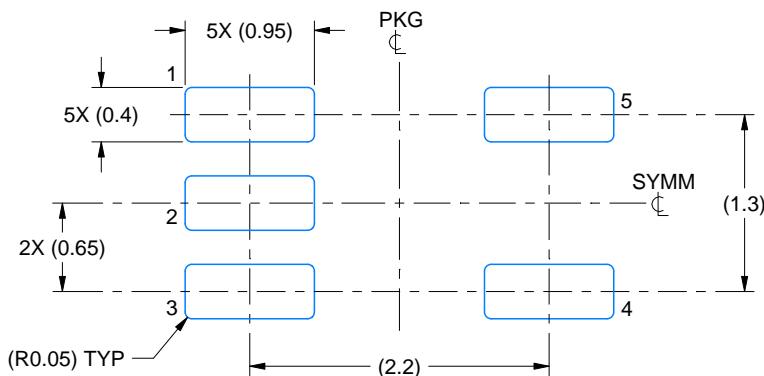
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

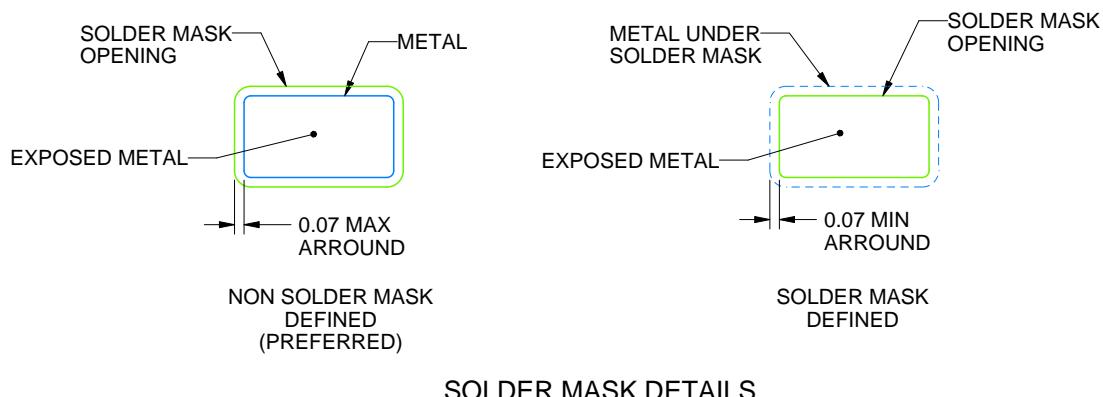
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



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NOTES: (continued)

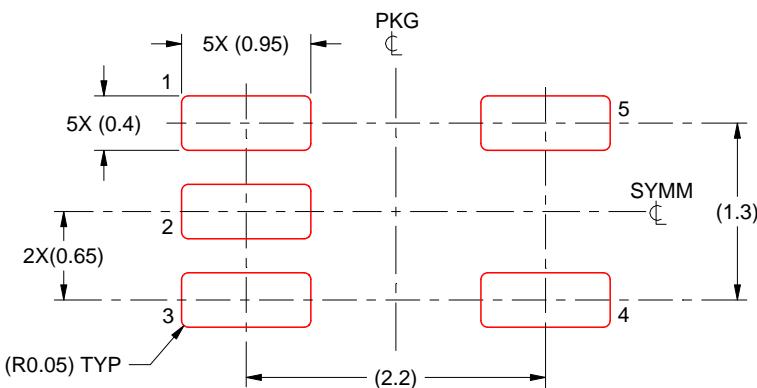
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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