LMX1860-SEP Low-Noise, High-Frequency JESD204B/C Buffer, Multiplier and Divider

1 Features

- VID #V62/24630
  - Total ionizing dose 30krad (ELDRS-free)
  - Single event latch-up (SEL) immune up to 43MeV - cm^2 /mg
  - Single event functional interrupt (SEFI) immune up to 43MeV - cm^2 /mg
- Clock buffer for 300MHz to 15GHz frequency
- Ultra-Low Noise
  - Noise floor of –159dBc/Hz at 6GHz output
  - 36-fs additive jitter (100Hz to f_{CLK}) at 6GHz output
  - 5fs additive jitter (100Hz - 100MHz)
- 4 high-frequency clocks with corresponding SYSREF outputs
  - Shared divide by 1 (Buffer), 2, 3, 4, 5, 6, 7, and 8
  - Shared programmable multiplier x2, x3, and x4
- Support pin mode options to configure the device without SPI
- LOGICLK output with corresponding SYSREF output
  - On separate divide bank
  - 1, 2, 4 pre-divider
  - 1 (bypass), 2, …, 1023 post divider
- 8 programmable output power levels
- Synchronized SYSREF clock outputs
  - 508 delay step adjustments of less than 2.5ps each at 12.8GHz
  - Generator and repeater modes
  - Windowing feature for SYSREFREQ pins to optimize timing
- SYNC feature to all divides and multiple devices
- 2.5V operating voltage
- –55ºC to 125ºC operating temperature
- High Reliability
  - Controlled Baseline
  - One Assembly/Test Site
  - One Fabrication Site
  - Extended Product Life Cycle
  - Product Traceability

2 Applications

- Radar imaging payload
- Communications payloads
- Command and data handling
- Data converter clocking
- Clock distribution/multiplication/division

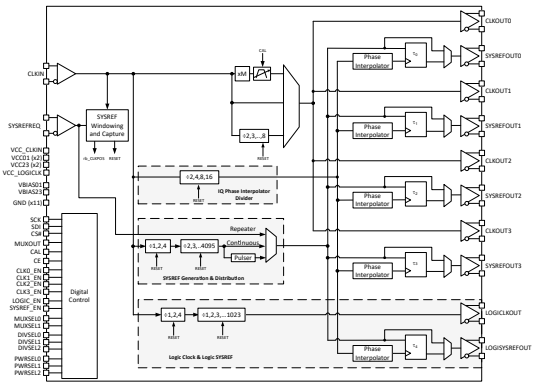
3 Description

The LMX1860-SEP is an buffer, divider and multiplier that features high frequency, ultra-low jitter, and SYSREF outputs. This device combined with an ultra-low noise reference clock source is an exemplary design for clocking data converters, especially when sampling above 3GHz. Each of the 4 high frequency clock outputs and additional LOGICLK output is paired with a SYSREF output clock signal. The SYSREF signal for JESD interfaces can either be internally generated or passed in as an input and re-clocked to the device clocks. This device can distribute the multichannel, low skew, ultra-low noise local oscillator signals to multiple mixers by disabling the SYSREF outputs.

Package Information

PART NUMBER	TYPE	PACKAGE(1)	PACKAGE SIZE(2)
LMX1860PAP/EM	Engineering Samples	PAP (HTQFP, 64)	10.00mm × 10.00mm
LMX1860MPAPSEP	Radiation Hardness Assured		

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

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4 Pin Configuration and Functions

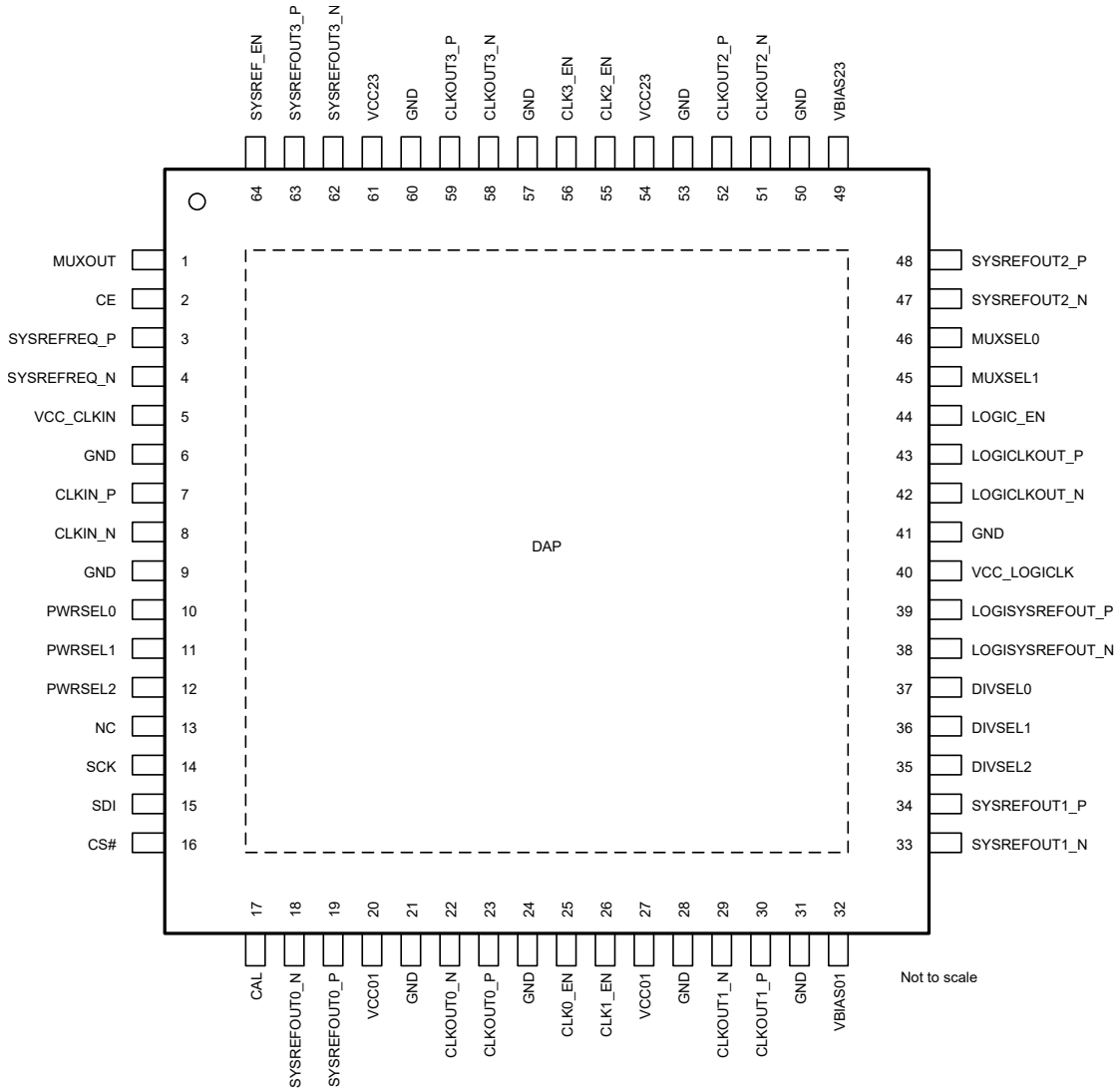


Figure 4-1. PAP0064E Package 64-Pin HTQFP Top View

Table 4-1. Pin Functions

NO.	NAME	TYPE[1]	DESCRIPTION
1	MUXOUT	O	Multiplexed pin serial data readback (SDO) and lock status of the multiplier.
2	CE	I	Chip Enable
3	SYSREFREQ_P	I	Differential SYSREF request input for JESD204B/C support. Internal 50Ω AC coupled to internal common-mode voltage or capacitor to GND. Supports AC and DC coupling which can directly accept a common mode voltage of 1.2V to 2V.

Table 4-1. Pin Functions (continued)

NO.	NAME	TYPE[1]	DESCRIPTION
4	SYSREFREQ_N	I	Differential SYSREF request input for JESD204B/C support. Internal 50Ω AC coupled to internal common-mode voltage or capacitor to GND. Supports AC and DC coupling which can directly accept a common mode voltage of 1.2V to 2V.
5	VCC_CLKIN	PWR	Connect to a 2.5V supply. Recommend a shunt RF wideband capacitor (typically 0.1µF or smaller) close to the pin in parallel with larger capacitors (typically 1µF and 10µF). Large capacitors can be placed further away from the pin.
6	GND	GND	Ground these pins.
7	CLKIN_P	I	Differential reference input clock. Internal 50Ω termination. AC-couple with a capacitor appropriate to the input frequency (typically 0.1µF or smaller). If using single-ended, terminate unused pin with 50Ω resistor AC-coupled to ground.
8	CLKIN_N		
9	GND	GND	Ground these pins.
10	PWRSEL0	I	Selects output power level in pin mode.
11	PWRSEL1	I	Selects output power level in pin mode.
12	PWRSEL2	I	Selects output power level in pin mode.
13	NC	NC	No connect pin (Connect to ground with 1kΩ resistor.)
14	SCK	I	SPI clock. High impedance CMOS input. Accepts up to 3.3V.
15	SDI	I	SPI data input. High impedance CMOS input. Accepts up to 3.3V.
16	CS#	I	SPI chip select. High impedance CMOS input. Accepts up to 3.3V.
17	CAL	I	Calibration pin used in multiplier mode.
18	SYSREFOUT0_N	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
19	SYSREFOUT0_P	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
20	VCC01	PWR	Connect to a 2.5V supply. Recommend a shunt RF wideband capacitor (typically 0.1µF or smaller) close to the pin in parallel with larger capacitors (typically 1µF and 10µF). Large capacitors can be placed bit further away from the pin.
21	GND	GND	Ground these pins.
22	CLKOUT0_N	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
23	CLKOUT0_P	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
24	GND	GND	Ground these pins.
25	CLK0_EN	I	Enable / Disable the individual output channel.
26	CLK1_EN	I	Enable / Disable the individual output channel.
27	VCC01	PWR	Connect to a 2.5V supply. Recommend a shunt RF wideband capacitor (typically 0.1µF or smaller) close to the pin in parallel with larger capacitors (typically 1µF and 10µF). Large capacitors can be placed bit further away from the pin.
28	GND	GND	Ground these pins.
29	CLKOUT1_N	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
30	CLKOUT1_P	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
31	GND	GND	Ground these pins.

Table 4-1. Pin Functions (continued)

NO.	NAME	TYPE[1]	DESCRIPTION
32	VBIAS01	BYP	Bypass this pin to GND with a 10nF capacitor for optimal noise performance in multiplier mode.
33	SYSREFOUT1_N	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
34	SYSREFOUT1_P	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
35	DIVSEL2	I	Select the divider value or multiplier value in divider or multiplier mode in pin configuration.
36	DIVSEL1	I	Select the divider value or multiplier value in divider or multiplier mode in pin configuration.
37	DIVSEL0	I	Select the divider value or multiplier value in divider or multiplier mode in pin configuration.
38	LOGISYSREFOUT_N	O	Differential clock output pair. Selectable CML, or LVDS format. Programmable common-mode voltage.
39	LOGISYSREFOUT_P	O	Differential clock output pair. Selectable CML, or LVDS format. Programmable common-mode voltage.
40	VCC_LOGICLK	PWR	Connect to a 2.5V supply. Recommend a shunt RF wideband capacitor (typically 0.1µF or smaller) close to the pin in parallel with larger capacitors (typically 1µF and 10µF). Large capacitors can be placed bit further away from the pin.
41	GND	GND	Ground these pins.
42	LOGICLKOUT_N	O	Differential clock output pair. Selectable CML, or LVDS format. Programmable common-mode voltage.
43	LOGICLKOUT_P	O	Differential clock output pair. Selectable CML, or LVDS format. Programmable common-mode voltage.
44	LOGIC_EN	I	Enable / disable the logic channel in pin mode.
45	MUXSEL1	I	Select the operating mode buffer, divider or multiplier in pin mode configuration.
46	MUXSEL0	I	Select the operating mode buffer, divider or multiplier in pin mode configuration.
47	SYSREFOUT2_N	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
48	SYSREFOUT2_P	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
49	VBIAS23	BYP	Bypass this pin to GND with a 10µF and 0.1µF capacitor for optimal noise performance in multiplier mode.
50	GND	GND	Ground these pins.
51	CLKOUT2_N	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
52	CLKOUT2_P	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
53	GND	GND	Ground these pins.
54	VCC23	PWR	Connect to a 2.5V supply. Recommend a shunt RF wideband capacitor (typically 0.1µF or smaller) close to the pin in parallel with larger capacitors (typically 1µF and 10µF). Large capacitors can be placed bit further away from the pin.
55	CLK2_EN	I	Enable / Disable the individual output channel.
56	CLK3_EN	I	Enable / Disable the individual output channel.

Table 4-1. Pin Functions (continued)

NO.	NAME	TYPE(1)	DESCRIPTION
57	GND	GND	Ground these pins.
58	CLKOUT3_N	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
59	CLKOUT3_P	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling required.
60	GND	GND	Ground these pins.
61	VCC23	PWR	Connect to a 2.5V supply. Recommend a shunt RF wideband capacitor (typically 0.1µF or smaller) close to the pin in parallel with larger capacitors (typically 1µF and 10µF). Large capacitors can be placed bit further away from the pin.
62	SYSREFOUT3_N	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
63	SYSREFOUT3_P	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.6V to 2V.
64	SYSREF_EN	I	Enable / disable the SYSREF section in pin mode configuration.
DAP	DAP	GND	Ground the pad.

(1) I = Input, O = Output, GND = Ground, PWR = Power, BYP = Bypass

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Power supply voltage	–0.3	2.75	V
V_{IN}	DC Input Voltage (SCK, SDI, CSB)	GND	3.6	V
V_{IN}	DC Input Voltage (SYSREFREQ)	GND	V_{DD} + 0.3	V
V_{IN}	AC Input Voltage (CLKIN)		2.1	Vpp
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2.4	2.5	2.6	V
T_C	Case Temperature	–55		125	°C

5.4 Thermal Information

SYMBOL	THERMAL MATRIC(1)	PAP (HTQFP)	UNIT
		64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

2.4V ≤ V_{DD} ≤ 2.6V, –55°C ≤ T_C ≤ +125°C. Typical values are at V_{DD} = 2.5V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Current Consumption							
I_{CC}	Supply Current (1)	Powered up, all outputs and SYSREF on			1050		mA
		Powered up, all outputs on, all SYSREF off			600		
		Powered up, all outputs and SYSREF off			265		
		Powered down(2)			11		
SYSREF							
f_{SYSREF}	SYSREF output frequency	Generator mode				200	MHz
		Repeater mode				100	MHz
Δt	SYSREF delay step size	f_{CLKIN} = 12.8GHz			3		ps
t_{RISE}	Rise time (20% to 80%)	SYSREFOUT			45		ps
		LOGISYSREFOUT	CML		120		ps
			LVDS		120		ps
t_{FALL}	Fall time (20% to 80%)	SYSREFOUT			45		ps
		LOGISYSREFOUT	CML		120		ps
			LVDS		120		ps
V_{OD}	Differential output voltage	SYSREFOUT			0.85		Vpp
		LOGISYSREFOUT	CML		0.4		Vp
			LVDS		0.4		Vp
$V_{SYSREFCM}$	Common mode voltage	SYSREFOUT	CML SYSREFOUTx_PWR=4 100Ω Differential Load		0.8		V
SYSREFREQ Pins							
$V_{SYSREFIN}$	Voltage input range	AC differential voltage		0.8		2	Vpp
V_{CM}	Input common mode	Differential 100Ω Termination, DC coupled Set externally		1.2	1.3	2	V
Clock Input							
f_{IN}	Input frequency	Buffer Mode Only		0.3		15(3)	GHz
P_{IN}	Input power	Single-ended power at CLKIN_P or CLKIN_N		0		10	dBm
Clock Outputs							
f_{OUT}	Output frequency	Divide-by-2		0.15		6.4	GHz
f_{OUT}	Output frequency	Buffer Mode		0.3		15(3)	
f_{OUT}	Output frequency	x2, x3, x4		3.2		6.4	
f_{OUT}	Output frequency	LOGICLK output		1		800	MHz
t_{CAL}	Calibration-time	Multiplier calibration time	f_{IN} = 3.2GHz; x2 f_{SMCLK} = 28MHz		750		µs
P_{OUT}	Output power	Single-Ended	$f_{CLKLOUT}$ = 6GHz OUTx_PWR = 7		6		dBm
			$f_{CLKLOUT}$ = 12.8GHz OUTx_PWR = 7		0		
			$f_{CLKLOUT}$ = 15GHz OUTx_PWR = 7		-3		
t_{RISE}	Rise time (20% to 80%)	f_{CLKOUT} = 300MHz			45		ps
t_{FALL}	Fall time (20% to 80%)	f_{CLKOUT} = 300MHz			45		ps
t_{MUTE}	Output mute time	Falling edge of OE pin				30	µs

2.4V ≤ V_{DD} ≤ 2.6V, –55°C ≤ T_C ≤ +125°C. Typical values are at V_{DD} = 2.5V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{UNMUTE}	Output unumte time	Rising edge of OE pin				30	µs
Propogation Delay and Skew							
$\lvert t_{SKEW} \rvert$	Magnitude of skew between outputs	T_A = -55ºC to +125ºC			2.5	10	ps
$\Delta t_{DLY}/\Delta T$	Propagation delay variation over temp	Buffer Mode		0.02	0.06	0.1	ps/C
t_{DLY}	Propagation delay	Buffer Mode	T_A = 25ºC		180		ps
		Divider Mode			182		
		Multiplier Mode			185		
Noise, Jitter, and Spurs							
J_{CKx}	Additive jitter	Additive Jitter. 12kHz to 100MHz integration bandwidth.	Buffer Mode		5		fs, rms
			x2 Multiplier		16		
			x3 Multiplier		21		
			x4 Multiplier		26		
Flicker	1/f flicker noise	Slew Rate > 8V/ns, f_{CLK}=6GHz	Buffer Mode		–155		dBc/Hz
NFL	Noise Floor	f_{OUT} = 6GHz; f_{Offset} = 100MHz	Buffer Mode		–159		dBc/Hz
NFL			Divide-by-2		–158.5		
NFL			Multiplier (x2,x3,x4)		–159.5		
NFL	Noise Floor	LOGICLK output, 300MHz	CML		–150.5		dBc/Hz
NFL			LVDS		–151.5		
H2	Second harmonic	f_{OUT} = 6GHz (differential), Buffer Mode			–25		dBc
		f_{OUT} = 6GHz (single-ended), Buffer Mode			–13		
		f_{OUT} = 6GHz, single-ended, Divide by 2			–16		
H1/2	Input clock leakage spur	f_{OUT} = 6GHz (single-ended)	x2 (f_{SPUR} = 3GHz)		–40		dBc
H1/3			x3 (f_{SPUR} = 2GHz)		–50		
H1/4			x4 (f_{SPUR} = 1.5GHz)		–54		dBc
I_{SPUR}	LOGICLK to CLKOUT	f_{SPUR} = 300MHz (differential)			–70		dBc
Digital Interface (SCK, SDI, CS#, MUXOUT,CLKx_EN,MUXSELx,PWRSELx,DIVSELx,LOGIC_EN,SYSREF_EN,CAL,CE)							
V_{IH}	High-level input voltage	SCK, SDI, CS#		1.4		3.3	V
	High-level input voltage	CLKx_EN,MUXSELx,PWRSELx,DIVSELx,LOGIC_EN,SYSREF_EN,CAL,CE		1.4		3.3	V
V_{IL}	Low-level input voltage	SCK, SDI, CS#		0		0.4	V
	Low-level input voltage	CLKx_EN,MUXSELx,PWRSELx,DIVSELx,LOGIC_EN,SYSREF_EN,CAL,CE		0		0.4	V
I_{IH}	High-level input current	SCK, SDI, CS#		–42		42	µA
	High-level input current	CLKx_EN,MUXSELx,PWRSELx,DIVSELx,LOGIC_EN,SYSREF_EN,CAL,CE		–42		42	µA
I_{IL}	Low-level input current	SCK, SDI, CS#		–25		25	µA
	Low-level input current	CLKx_EN,MUXSELx,PWRSELx,DIVSELx,LOGIC_EN,SYSREF_EN,CAL,CE		–25		25	µA
V_{OH}	High-level output voltage	MUXOUT	I_{OH} = 5mA	1.4		2.2	V
	High-level output voltage		I_{OH} = 0.1mA	2.2		2.5	V
V_{OL}	Low-level output voltage	MUXOUT	I_{OL} = 5mA			0.45	V

(1) Unless Otherwise Stated, f_{CLKIN}=6GHz, CLK_MUX=Buffer, All clocks on with OUTx_PWR=7, SYSREFREQ_MODE=1.
(2) For powered down mode.
(3) SYNC, divider, SYSREF and SYSREF windowing supported up to 12.8GHz frequency.

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Timing Requirements					
f_{SPI}	SPI Read/Write Speed			2	MHz
t_{CE}	Clock to enable low time	20			ns
t_{CS}	Clock to data wait time	20			ns
t_{CH}	Clock to data hold time	20			ns
t_{CWH}	Clock pulse width high	100			ns
t_{CWL}	Clock pulse width low	100			ns
t_{CES}	Enable to clock setup time	20			ns
t_{EWH}	Enable pulse width high	50			ns
t_{CD}	Falling clock edge to data wait time	0		100	ns

5.7 Timing Diagram

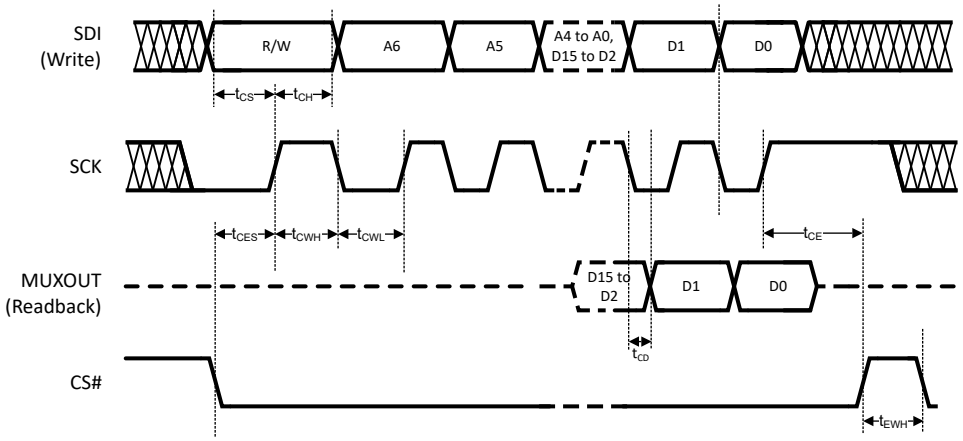


Figure 5-1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

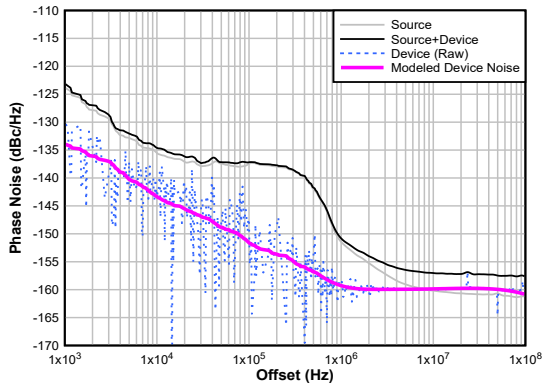
- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CS# must be held low for data to be clocked. The device ignores clock pulses if CS# is held high.
- Recommended SPI settings for this device are CPOL=0 and CPHA=0.
- When SCK and SDI lines are shared between devices, TI recommends to hold the CS# line high on the device that is not to be clocked.

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXOUT pin is always be low for the address portion of the transaction.
- The data on MUXOUT is clocked out at the falling edge of SCK. In other words, the readback data is available at the MUXOUT pin t_{CD} after the clock falling edge.
- The data portion of the transition on the SDI line is always ignored.
- The MUXOUT pin does not automatically tri-state after a readback transaction completes. When sharing the SPI bus readback pin with other devices, set MUXOUT_EN=0 after all readback transactions from device are complete to manually tri-state the MUXOUT pin, permitting other devices to control the readback line.
- The values read back, even for R/W bits are not always the value written but rather an internal device state that takes into account the programmed value as well as other factors, such as pin states.

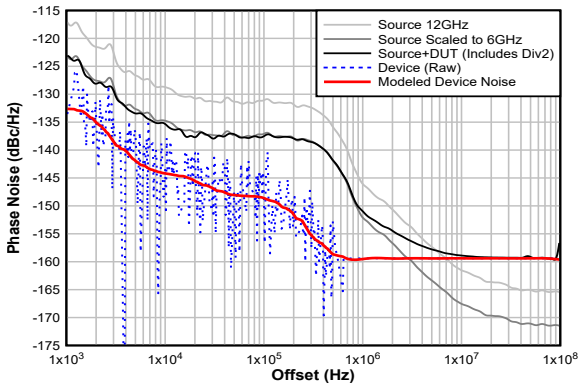
5.8 Typical Characteristics

If not otherwise, the following conditions can be assumed: Temperature = 25°C, V_{DD} = 2.5V, OUTx_PWR = 5, CLKIN driven differentially with 8dBm at each pin. Signal source used is Rohde & Schwarz® SMA100B with ultra-low noise option B711.



Noise Floor = -160dBc/Hz

Figure 5-2. Buffer Phase Noise Plot at 6GHz Output



Noise Floor = -159.8dBc/Hz

Figure 5-3. Divider Phase Noise Plot at 6GHz Output (Divide by 2)

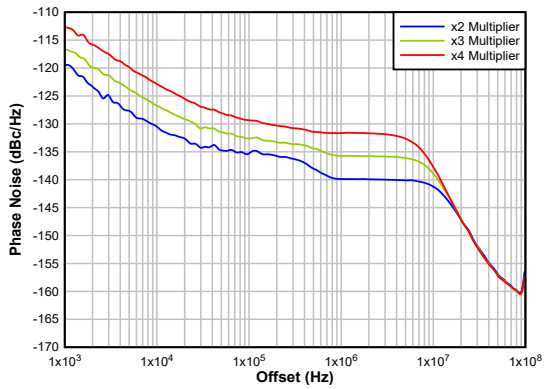
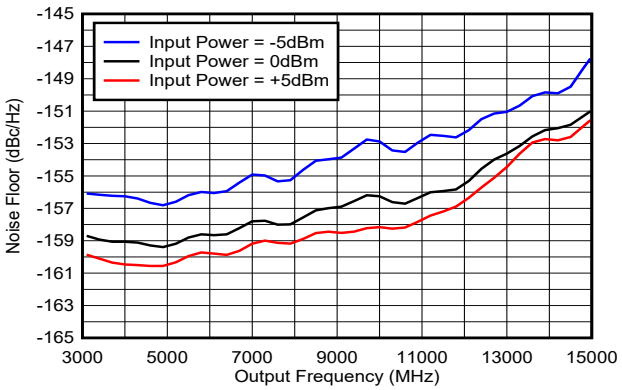


Figure 5-4. Multiplier Phase Noise Plot at 6GHz Output



Stated input power is applied at each pin

Figure 5-5. Noise Floor in Buffer Mode

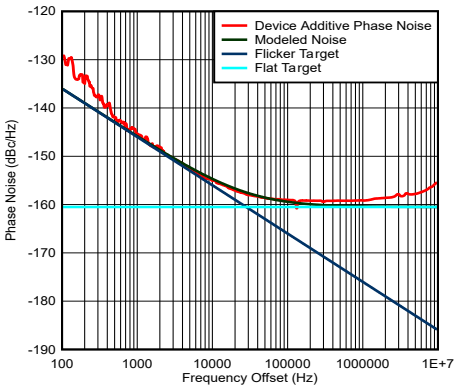


Figure 5-6. Flicker Noise

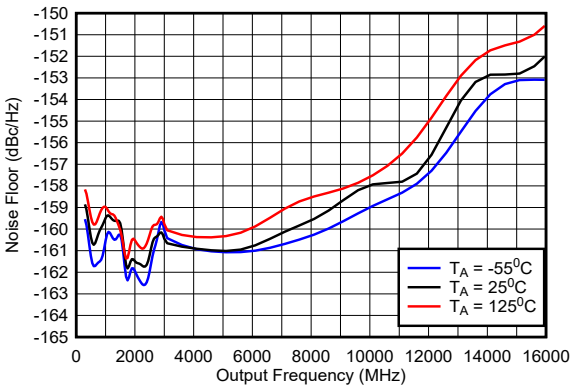
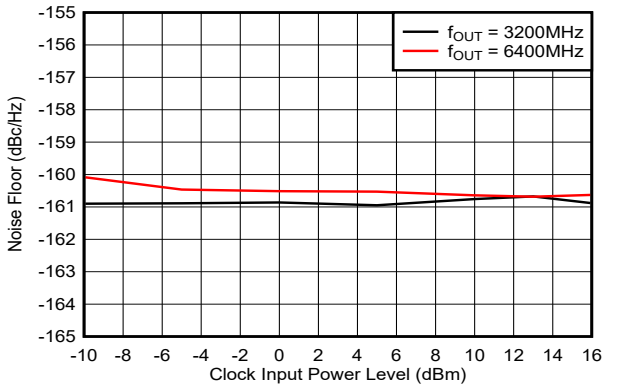


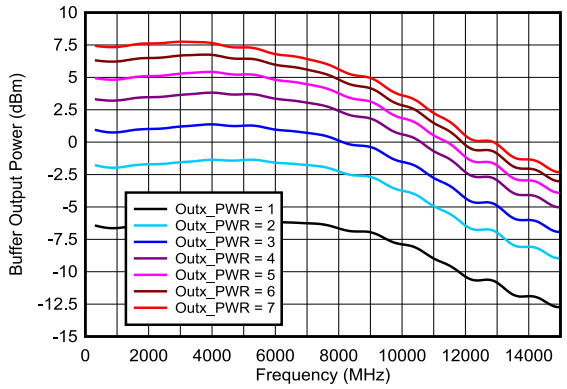
Figure 5-7. Noise Floor in Buffer Mode

5.8 Typical Characteristics (continued)



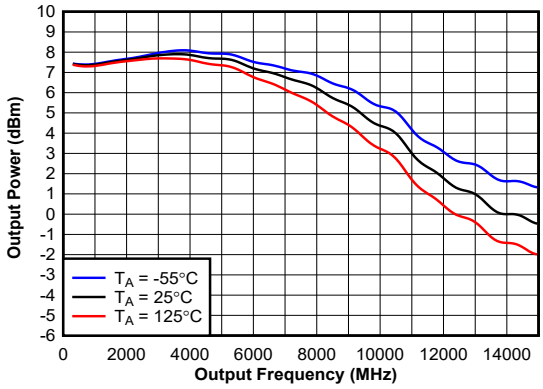
Input power is differential

Figure 5-8. Noise Floor in Multiply x2 Mode



Applies to all modes except divider mode with odd divide (which have slightly lower power).

Figure 5-9. Buffer Mode Single-Ended Output Power



CLKOUTx_PWR = 7

Figure 5-10. Buffer Mode Single-Ended Output Power

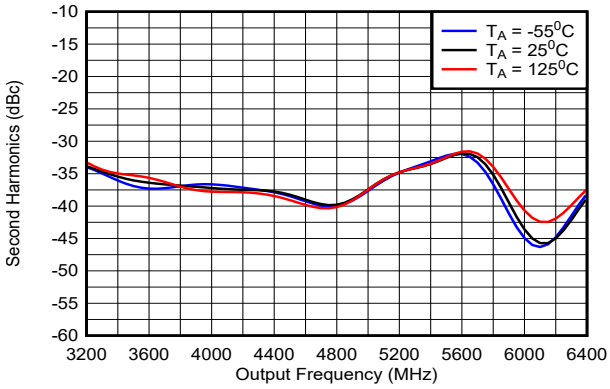


Figure 5-11. Second Harmonic in Multiply X2 Mode (Differential Output)

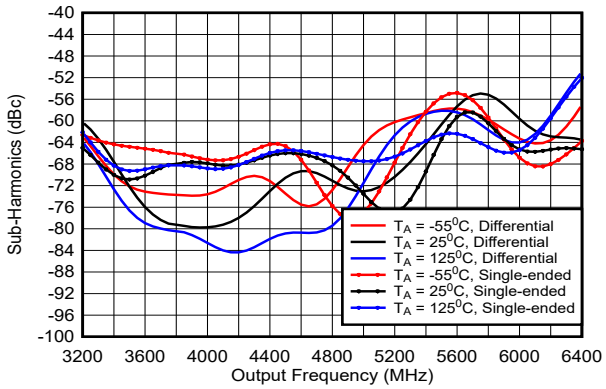


Figure 5-12. Multiplier 1/2 Sub-Harmonic in X2 Mode

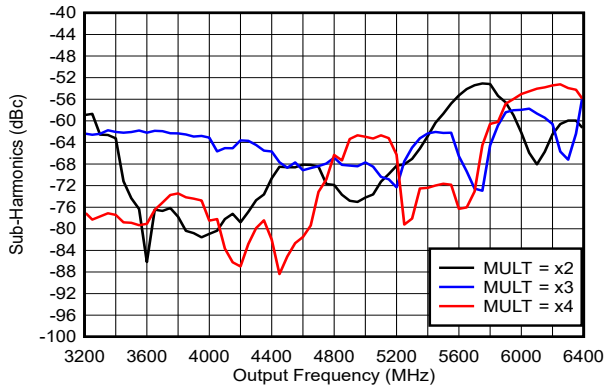


Figure 5-13. Multiplier Sub-Harmonics (Harmonic Frequency = Output Frequency / M)

5.8 Typical Characteristics (continued)

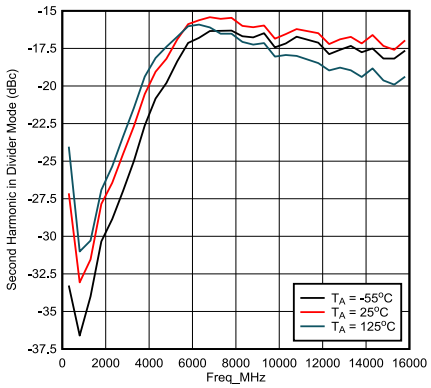


Figure 5-14. Second Harmonic on Divider Mode (Single-Ended Input)

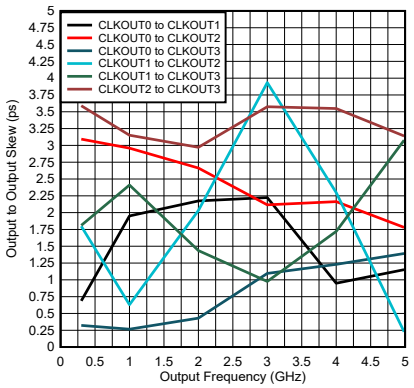


Figure 5-15. Output to Output Skew (ps)

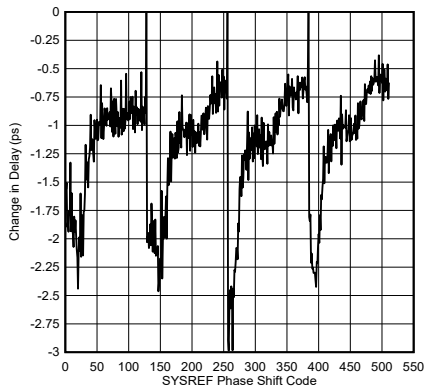
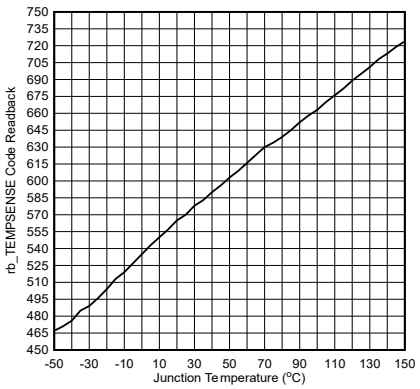


Figure 5-16. SYSREF Delta Delay vs. Code



Measured in power-down mode to make Junction Temperature = Ambient Temperature.

Figure 5-17. Temperature Sensor Readback

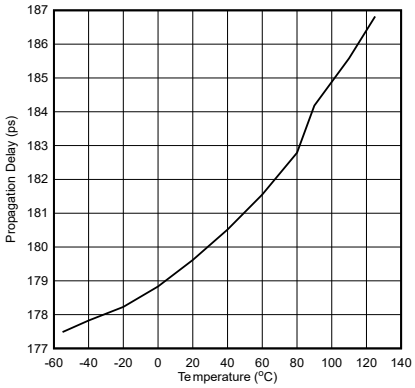


Figure 5-18. Propagation Delay

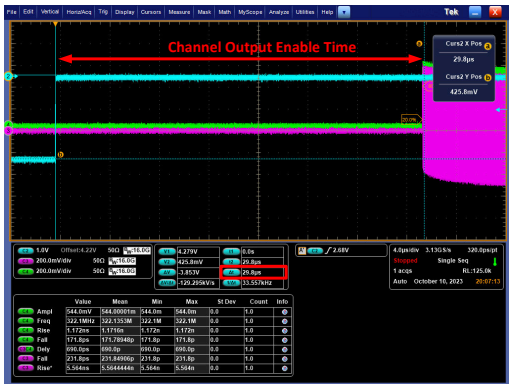


Figure 5-19. Channel Enable Setting Time

5.8 Typical Characteristics (continued)

Figure 5-20. Channel Disable Setting Time

6 Detailed Description

6.1 Overview

This device has four main clock outputs and another LOGICLK output. The main clock outputs are all the same frequency. This frequency can be the same, divided, or multiplied relative to the input clock. Each of these clock outputs has programmable power level. The LOGICLK output frequency is independent and typically lower frequency than the other four main clocks and has programmable output format (CML and LVDS) and power level.

The SYSREF can be generated by either repeating the input from the SYSREFREQ pins, or internally generated. There is an internal SYSREF windowing feature that allows the internal timing of the device to be adjusted to optimize setup and hold times of the SYSREFREQ input with respect to the CLKIN input. This feature assumes that the delay between the SYSREF edge and the next rising clock edge is consistent. Each of the five outputs has a corresponding SYSREF output that has individual delays and programmable common mode. For the LOGISYSREF output, the output format is programmable as CML or LVDS.

6.1.1 Range of Dividers and Multiplier

There are dividers that allow the main and LOGICLK outputs to be a divided value of the input clock. The main clock outputs also have a multiplier. In addition to this, dividers are used for SYSREF generation in generator mode as well as generation of the delay block.

Table 6-1. Range of Dividers and Multiplier

CATEGORY			RANGE	COMMENTS
Main Clocks	Buffer			
	Divider(1)		2, 3, 4, … 8	Odd divides (except 1) do not have 50% duty cycle
	Multiplier		2, 3, 4	
LOGICLK	Divide	PreDivide	1, 2, 4	TotalDivide = PreDivide × Divide Odd divides (except 1) do not have 50% duty cycle
		Divide	1, 2, 3, … 1023	
SYSREF	Divide for frequency generation	PreDivide	1,2, 4	Pre-divides clock for SYSREF generation. TotalDivide = PreDivide×Divide Odd divides do not have 50% duty cycle
		Divide	2, 3, 4,… 4095	
	Divide for delay generation	Divide	2, 4, 8, 16	This divide is for phase interpolator and set according to the input frequency.

(1) Divide /6 and /8 does not support SEFI compliant

6.2 Functional Block Diagram

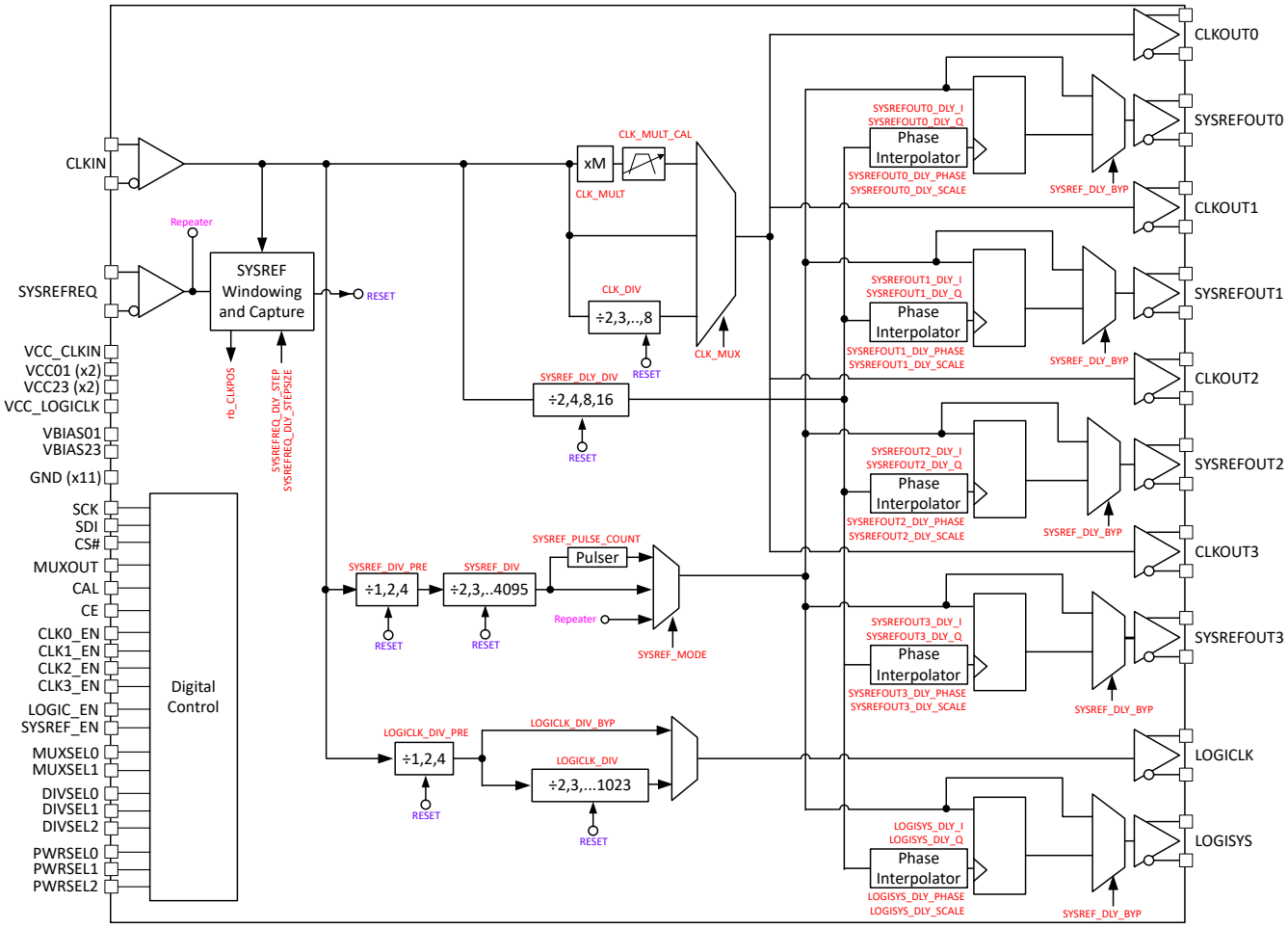


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Power On Reset

When the device is powered up, the power-on reset (POR) resets all registers to a default state as well as resets all state machines and dividers. For the power on reset state, all SYSREF outputs are disabled and all the dividers are bypassed and the device performs as a 4-output buffer. Wait approximately 100µs after the power supply rails before programming other registers to verify that this reset is finished. The device functions properly if the power-on reset happens when no device clock is present, but the current changes after an input clock is inserted.

Performing a software power on reset by writing RESET = 1 in the SPI bus is possible and generally good practice. The RESET bit self-clears when the user writes to any other register. The SPI bus can be used to override these states to the desired settings.

Although the device does have an automatic power on reset, the can be impacted by different ramp rates on the different supply pins, especially in the presence of a strong input clock signal. TI therefore recommends to do a software reset after POR. This can be done by programming RESET = 1. The reset bit can be cleared by programming any other register or setting RESET back to 0. Even at the maximum allowed SPI bus speed, the software reset event always completes before the subsequent SPI write.

6.3.2 Temperature Sensor

The junction temperature can be read back for purposes such as characterization or to make adjustments based on temperature. Such adjustments can include adjusting CLKOUTx_PWR to make the output power more stable or using external or digital delays to compensate for changes in propagation delay over temperature.

The junction temperature is typically higher than the ambient temperature due to power dissipation from the outputs and other functions on the device. Equation 1 shows the relationship between the code read back and the junction temperature.

$$\text{Temperature} = 0.65 \times \text{Code} - 351 \quad (1)$$

Equation 1 is based on a best-fit line created from three devices from slow, nominal, and fast corner lots (nine parts total). The worst-case variation of the actual temperature from the temperature predicted by the best-fit line is 13°C, which works out to 20 codes.

6.3.3 Clock Outputs

This device has four main output clocks which share a common frequency. This does not include the additional lower frequency LOGICLK output.

6.3.3.1 Clock Output Buffers

The output buffers have a format that is open collector with an integrated pullup resistor, similar to CML.

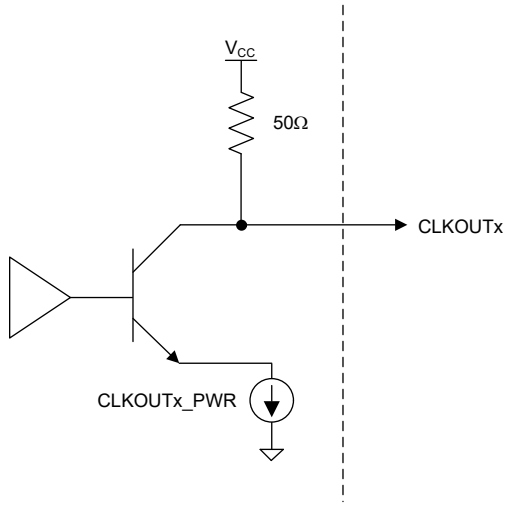


Figure 6-2. CLKOUT Output Buffer

The CLKOUTx_EN bits can enable the output buffers. The output power of the buffers can be individually set with CLKOUTx_PWR field. However, these fields only control the output buffer, not the internal channel path that drives this buffer. To power down the entire path, disable the CHx_EN bit.

Table 6-2. Clock Output Power

CHx_EN	INTERNAL CHANNEL PATH	CLKOUTx_EN	CLKOUTx_PWR	OUTPUT BUFFER
0	Powered Down	Don't Care	Don't Care	Powered Down
1	Powered Up	0	Don't Care	Powered Down
		1	0	Minimum
			1	
			...	
			7	Maximum

6.3.3.2 Clock MUX

The four main clocks must be the same frequency, but this frequency can be bypassed, multiplied, or divided. This is determined by the CLK_MUX word.

Table 6-3. Clock MUX

CLK_MUX	OPTION	VALUES SUPPORTED
0	Buffer Mode	÷1 (bypass)
1	Divider Mode	÷2, 3, 4, 5, 6, 7, and 8
2	Multiplier Mode	x2, x3, x4

6.3.3.3 Clock Divider

Set the CLK_MUX to Divided to a divide value by 2, 3, 4, 5, 6, 7, or 8. This is set by the CLK_DIV word. When using the clock divider, any change to the input frequency requires the CLK_DIV_RST bit to be toggled from 1 to 0.

Table 6-4. Clock Divider

CLK_DIV	DIVIDE	DUTY CYCLE
0	Reserved	n/a
1	2	50%
2	3	33%
3	4	50%

Table 6-4. Clock Divider (continued)

CLK_DIV	DIVIDE	DUTY CYCLE
4	5	40%
5	6	50%
6	7	43%
7	8	50%

6.3.3.4 Clock Multiplier

6.3.3.4.1 General Information about the Clock Multiplier

Use the clock multiplier to multiply up the input clock frequency by a factor of x2, x3, or x4. The multiply value is set by the CLK_MULT field. As the multiplier is PLL-based and includes an integrated VCO, the multiplier has a state machine clock, requires calibration, has a lock detect feature.

6.3.3.4.2 State Machine Clock for the Clock Multiplier

The state machine clock frequency (f_{SMCLK}) is derived by dividing down the input clock frequency by a programmed divider value. The state machine clock is also necessary for the multiplier calibration and lock detect. If there are concerns about the state machine clock creating spurs, then the state machine clock can be shut off, provided that the multiplier calibration is not running and the lock detect feature is not in use.

6.3.3.4.2.1 State Machine Clock

A valid state machine clock is required (SMCLK_EN=1 and signal present at CLKIN pins) in below circumstances:

1. Multiplier is being calibrated.
2. Lock Detect from the multiplier is being monitored.
3. Clock divide value is being changed to 6 or 8.
4. For the device to perform a proper power on reset.
    a. Note that SMCLK_EN=1 is enabled by the power on reset, but an input clock is also required to allow the power on reset before SMCLK_EN can be set to 0.

When the state machine clock is enabled, the clock needs to be less than 30MHz and the frequency is as follows:

$f_{SMCLK} = f_{CLKIN} / (SMCLK\_DIV\_PRE * SMCLK\_DIV)$

When the state machine clock is not required, the clock can be disabled by setting SMCLK_EN=0 to minimize crosstalk and spurs.

6.3.3.4.3 Calibration for the Clock Multiplier

For optimal phase noise, the VCO in the multiplier divides up the frequency range into many different bands and cores and has optimized amplitude settings for each band and core. For this reason, upon initial use or whenever the frequency is changed, the user must run a calibration routine to determine the correct core, frequency band, and amplitude setting. Program the R0 register with a valid input signal to perform a calibration. To provide reliable multiplier calibration, the state machine clock frequency must be at least twice the SPI write speed, but no more than 30MHz. Whenever the CLK_MUX mode is changed or the multiplier is calibrated for the first time, the calibration time is substantially longer, on the order of 5ms.

6.3.3.4.4 Lock Detect for the Clock Multiplier

The lock detect status of the multiplier can be read back through the rb_LD field or from the MUXOUT pin. The state machine clock must be running for the lock detect to work properly.

6.3.3.4.5 Watchdog Timer

The watchdog feature is used when radiation during VCO calibration causes the VCO calibration to fail in multiplier mode. The watchdog timer run during VCO calibration. If this timer runs out before the VCO calibration

is finished, then the VCO calibration is restarted. During the watchdog timer operation, state machine clock must be enabled.

6.3.4 Device Functional Modes Configurations

The device can configure in high frequency clock buffer mode, divider mode or multiplier mode. Each mode requires the below register configurations to function.

Table 6-5. Device Functional Modes Settings

REGISTER ADDRESS	BIT	FIELD	FUNCTION	BUFFER	DIVIDER	MULTIPLIER
R25	2:0	CLK_MUX	Select the mode	1	2	3
R25	5:3	CLK_DIV / CLK_MULT	Select the division or multiplication value	x	CLK_DIV 0x1 = ÷2 0x2 = ÷3 0x3 = ÷4 0x4 = ÷5 0x5 = ÷6 0x6 = ÷7 0x7 = ÷8	CLK_MULT 0x2 = ×2 0x3 = ×3 0x4 = ×4
R2	5	SMCLK_EN	Enables the state machine clock generator	x	x	1
R2	9:6	SMCLK_DIV_PRE	Sets pre-divider for state machine clock	x	x	Pre-clock divider for state machine clock 0x2 = ÷2 0x4 = ÷4 0x8 = ÷8
R3	2:0	SMCLK_DIV	Sets state machine clock divider	x	x	Additional SMCLK divider to keep output frequency must be ≤ 30MHz. 0x0 = ÷1 0x1 = ÷2 0x2 = ÷4 0x3 = ÷8 0x4 = ÷16 0x5 = ÷32 0x6 = ÷64 0x7 = ÷128
R0	All	Calibrate Multiplier	Calibrate the PLL based multiplier	x	x	Write R0 for calibrate multiplier

6.3.5 LOGICLK Output

The LOGICLK output can be used to drive devices using lower frequency clocks, such as FPGAs. The LOGICLK output has a programmable output format and a corresponding SYSREF output.

6.3.5.1 LOGICLK Output Format

The LOGICLK output format can be programmed to LVDS and CML modes. Depending on the format, the common mode can be programmable or external components can be required (see Table 6-6).

Table 6-6. LOGICLK Formats and Properties

LOGICLKOUT_FMT	FORMAT	EXTERNAL COMPONENTS REQUIRED	OUTPUT LEVEL	COMMON MODE
0	LVDS	None	Fixed	Programmable through LOGICLKOUT_VCM
2	CML	Pullup Resistors 50Ω to V_{CC}	Programmable through LOGICLKOUT_PWR	Not programmable

6.3.5.2 LOGICLK_DIV_PRE and LOGICLK_DIV Dividers

The LOGICLK_DIV_PRE divider and LOGICLK_DIV dividers are used for the LOGICLK output. The LOGICLK_DIV_PRE divider is necessary to divide the frequency down to verify that the input to the LOGICLK_DIV divider is 3.2GHz or less. When LOGICLK_DIV is not even and not bypassed, the duty cycle is not 50%. Both the LOGICLK dividers are synchronized by the SYNC feature, which allows synchronization across multiple devices. The dividers LOGICLK_DIV_PRE and LOGICLK_DIV has the default divide value of 4 and 32 respectively.

Table 6-7. Minimum N-Divider Restrictions

f_{CLKIN} (MHz)	LOGICLK_DIV_PRE	LOGICLK_DIV	TOTAL DIVIDE RANGE
$f_{CLKIN} \leq 3.2GHz$	÷1, 2, 4	÷1, 2, 3,…1023	[1, 2, ...1023] [2, 4, ... 2046] [4, 8, 4092]
$3.2GHz < f_{CLKIN} \leq 6.4GHz$	÷2, 4	÷1, 2, 3, …1023	[4, ... 2046] [4, 8, 4092]
$f_{CLKIN} > 6.4GHz$	÷4	1, 2, 3, …1023	[8, 4092]

6.3.6 SYSREF

SYSREF allows a low frequency JESD204B/C compliant signal to be produced that is reclocked to a main or LOGICLK output. The delays between the CLKOUT and SYSREF outputs are adjustable with software. The SYSREF output can be configured as a generator using the internal SYSREF divider, or as a repeater duplicating the signal on the SYSREFREQ pins. The SYSREF generator for both the main clocks and the LOGICLK output are the same.

Table 6-8. SYSREF Modes

SYSREF_MODE	DESCRIPTION
0	**Generator Mode** Internal generator creates a continuous stream of SYSREF pulses. The SYSREFREQ pins or the SYSREFREQ_FORCE bit can be used to gate the SYSREF divider from the channels for improved noise isolation without disrupting the synchronization of the SYSREF dividers. The SYSREFREQ pins or the SYSREFREQ_FORCE bit must be high for a SYSREF output to come out.
1	**Pulser** Internal generator generates a burst of 1 - 16 pulses that is set by SYSREF_PULSE_CNT that occurs after a rising edge on the SYSREFREQ pins or after changing SYSREFREQ_FORCE bit from 0 to 1 (assuming SYSREFREQ pins to be forced to a low state).
2	**Repeater Mode** SYSREFREQ pins input are reclocked to clock outputs and then delayed in accordance to the SYSREF_DLY_BYP field before sent to the SYSREFOUT output pins.

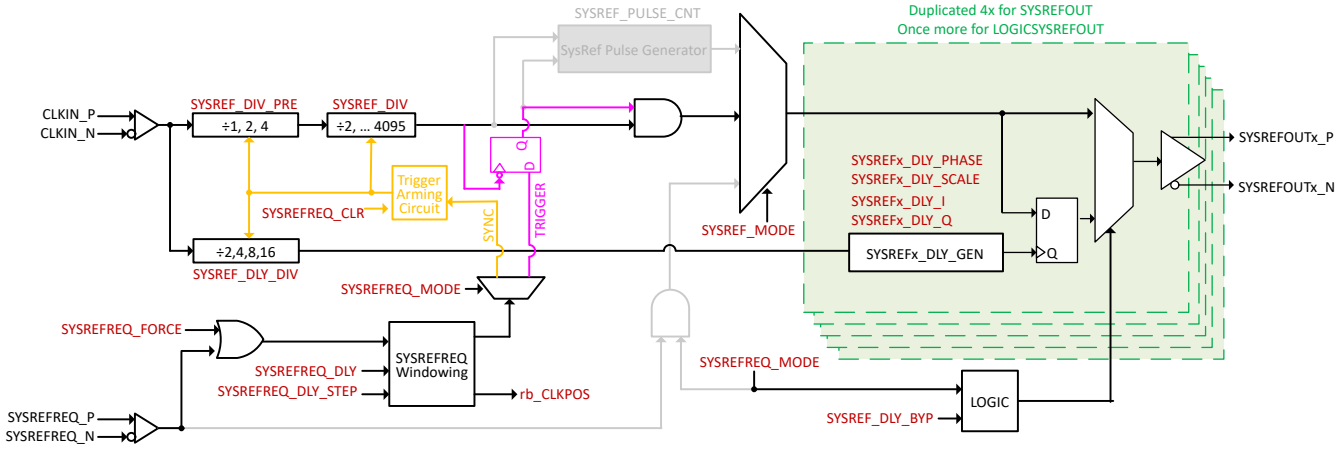


Figure 6-3. Functional Block Diagram of SYSREF Circuitry in Generator Mode

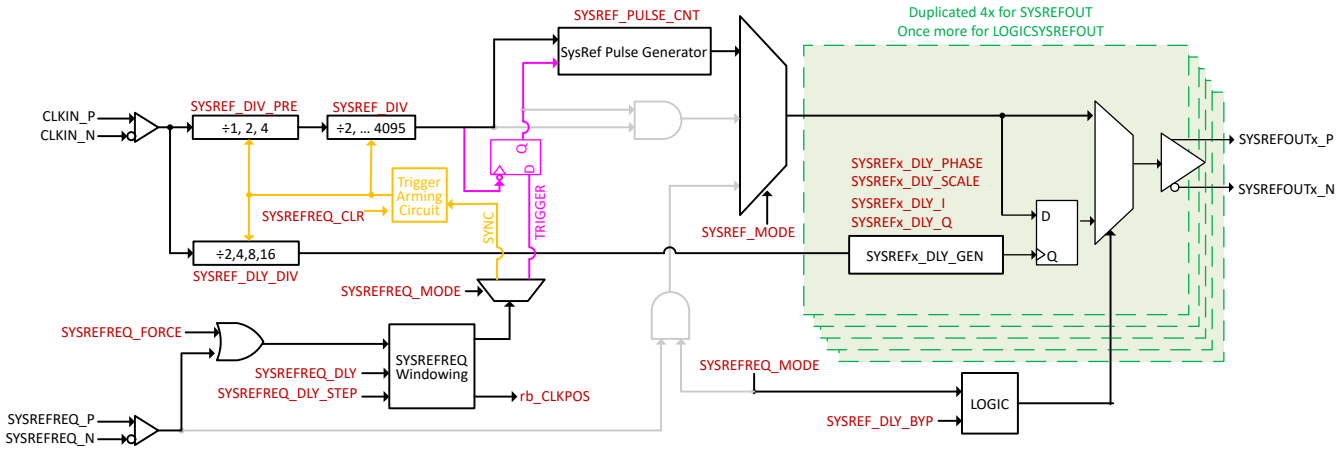


Figure 6-4. Functional Block Diagram of SYSREF Circuitry in Pulser Mode

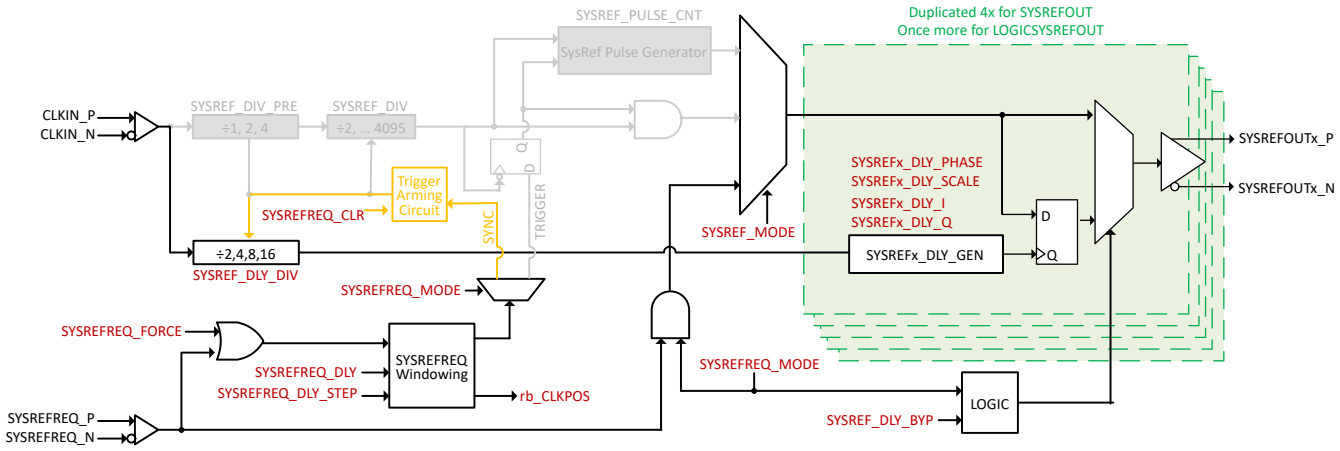


Figure 6-5. Functional Block Diagram of SYSREF Circuitry in Repeater Mode

To operate the SYSREFREQ_FORCE bit controlled SYSREF output (Pulser) and SYNC, set the SYSREFREQ pins to low logic state externally. For example, make sure the SYSREFREQ_N pin is at a higher level (400mV) than the SYSREFREQ_P pin and maintain the input common-mode voltage requirement.

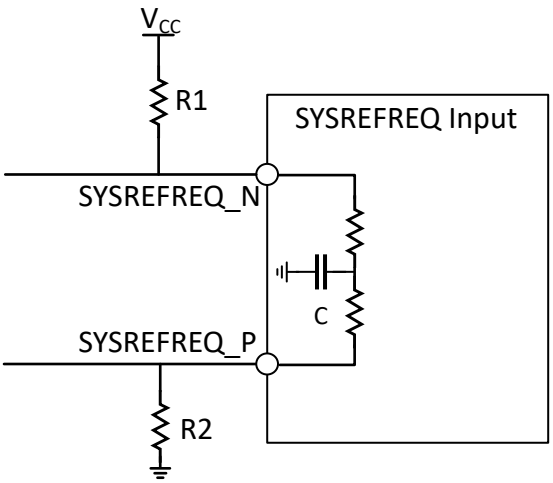


Figure 6-6. SYSREFREQ Pin Logic Low Setup

As an example, to maintain the minimum 400mV voltage difference for a VCC of 2.5V, the current draw through 100Ω is 4mA. In this example, keep the SYSREFREQ_P pin at 1.4V DC, set the R2 to 350Ω and the R1 to 175Ω with 1.8V at SYSREFREQ_N pin.

6.3.6.1 SYSREF Output Buffers

6.3.6.1.1 SYSREF Output Buffers for Main Clocks (SYSREFOUT)

The SYSREF outputs within the clock output channels have the same output buffer structure as the clock output buffer, with the addition of circuitry to adjust the common-mode voltage. The SYSREF outputs are CML outputs with a common-mode voltage that can be adjusted with the SYSREFOUTx_VCM field, and the output level that can be programmed with the SYSREFOUTx_PWR field. This design allows DC coupling. Note that the CLKOUT outputs do not have adjustable common-mode voltage and must be AC coupled for optimal noise performance.

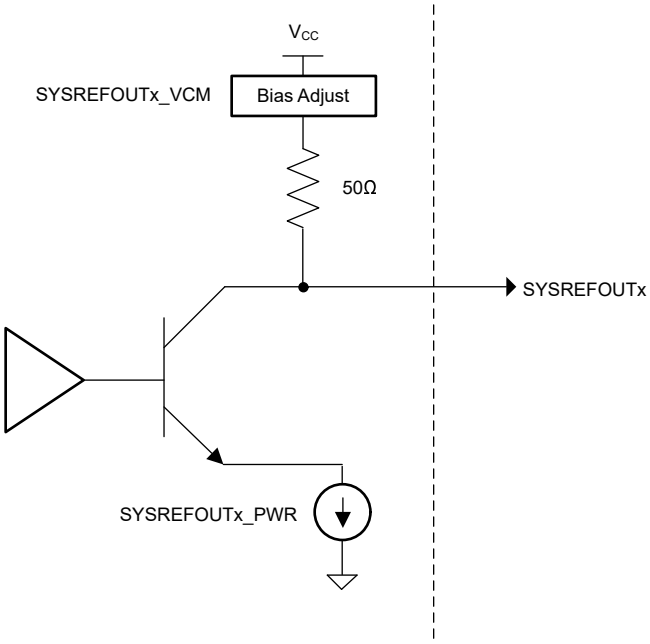


Figure 6-7. SYSREF Output Buffer

The common-mode voltage and output power are interrelated and can be simulated assuming a 100Ω differential load and no DC path to ground. The common mode voltage and output are interrelated as shown in Table 6-9. Note that for long-term reliability, $V_{CM} - V_{OD}/2 \geq 0.5V$ is required.

Table 6-9. Single-Ended Voltage (V_{OD}) and Common-Mode Voltage (V_{CM})

SYSREFOUT_PWR	Check: V_{CM} - V_{OL}/2 ≥ 0.5V?	SYSREFOUT_VCM	V_{OD}	V_{CM}
0	Valid State	0	0.27	1.09
		1	0.27	1.22
		2	0.28	1.37
		3	0.28	1.54
		4	0.29	1.69
		5	0.29	1.83
		6	0.29	2.00
		7	0.29	2.16
1		0	0.32	0.79
		1	0.33	0.95
		2	0.33	1.12
		3	0.34	1.33
		4	0.35	1.51
		5	0.35	1.69
		6	0.36	1.89
		7	0.37	2.08
2	Invalid State	0	0.37	0.52
		1	0.38	0.68
	Valid State	2	0.39	0.89
		3	0.40	1.12
		4	0.41	1.34
		5	0.42	1.54
		6	0.43	1.78
		7	0.44	2.01
3	Invalid State	0	0.39	0.43
		1	0.42	0.50
		2	0.45	0.66
	Valid State	3	0.46	0.93
		4	0.47	1.17
		5	0.48	1.41
		6	0.49	1.68
		7	0.51	1.93
4	Invalid State	0	0.40	0.40
		1	0.43	0.44
		2	0.48	0.52
		3	0.51	0.73
	Valid State	4	0.52	1.00
		5	0.54	1.27
		6	0.55	1.57
		7	0.57	1.86

Table 6-9. Single-Ended Voltage (V_{OD}) and Common-Mode Voltage (V_{CM}) (continued)

SYSREFOUT_PWR	Check: V_{CM} - V_{OL}/2 ≥ 0.5V?	SYSREFOUT_VCM	V_{OD}	V_{CM}
5	Invalid State	0	0.40	0.38
		1	0.44	0.42
		2	0.49	0.47
		3	0.55	0.59
	Valid State	4	0.58	0.85
		5	0.59	1.14
		6	0.62	1.48
		7	0.63	1.79
6	Invalid State	0	0.40	0.36
		1	0.44	0.39
		2	0.49	0.45
		3	0.57	0.54
		4	0.63	0.70
	Valid State	5	0.65	1.01
		6	0.67	1.38
		7	0.70	1.73
7	Invalid State	0	0.40	0.35
		1	0.44	0.38
		2	0.50	0.43
		3	0.58	0.51
		4	0.66	0.62
	Valid State	5	0.70	0.89
		6	0.73	1.29
		7	0.76	1.66

6.3.6.1.2 SYSREF Output Buffer for LOGICLK

The LOGISYSREFOUT output supports the two formats of LVDS and CML. The LOGISYSREFOUT_EN enables the output buffer and LOGISYSREF_FMT sets the format. LVDS mode allows programmable common mode, CML require external components, and CML allows programmable output power (see Table 6-10).

Table 6-10. LOGISYSREFOUT Output Buffer Configuration

LOGISYSREFOUT_EN	LOGISYSREF_FMT	LOGISYSREF FORMAT	EXTERNAL TERMINIATION REQUIRED	OUTPUT POWER	OUTPUT COMMON MODE
0	Powered Down				
1	0	LVDS	None	Fixed	Programmable with LOGISYSREF_VCM
	1	Reserved			
	2	CML	Pullup resistors 50Ω to V_{CC}	Controlled by LOGISYSREF_PWR	LOGISYSREF_VCM has no impact, but this changes with LOGISYSREF_PWR.
	3	Reserved			

6.3.6.2 SYSREF Frequency and Delay Generation

For the frequency of the SYSREF output in generator mode, the SYSREF_DIV_PRE divider is necessary to verify that the input of the SYSREF_DIV divider is not more than 3.2GHz.

Table 6-11. SYSREF_DIV_PRE Setup

f_{CLKIN}	SYSREF_DIV_PRE	TOTAL SYSREF DIVIDE RANGE
3.2GHz or Less	÷1, 2, or 4	÷2, 3, 4, ...16380
3.2GHz < f_{CLKIN} ≤ 6.4GHz	÷2 or 4	÷4, 6, 8, … 16380
f_{CLKIN} > 6.4GHz	÷4	÷8, 12, 16, … 16380

For the delay, the input clock frequency is divided by SYSREF_DLY_DIV to generate $f_{INTERPOLATOR}$. This has a restricted range as shown in Table 6-12. Note also that when SYSREF_DLY_BYP = 0 or 2 (delaygen engaged for generator mode), and SYSREF_MODE = 0 or 1 (a generator mode) the SYSREF output frequency must be a multiple of the phase interpolator frequency.

$f_{INTERPOLATOR}$ % f_{SYSREF} = 0.

Table 6-12. SYSREF Delay Setup

f_{CLKIN}	SYSREF_DLY_DIV	SYSREFx_DLY_SCALE	$f_{INTERPOLATOR}$
6.4GHz < f_{CLKIN} ≤ 12.8GHz	16	0	0.4GHz to 0.8GHz
3.2GHz < f_{CLKIN} ≤ 6.4GHz	8	0	0.4GHz to 0.8GHz
1.6GHz < f_{CLKIN} ≤ 3.2GHz	4	0	0.4GHz to 0.8GHz
0.8GHz < f_{CLKIN} ≤ 1.6GHz	2	0	0.4GHz to 0.8GHz
0.4GHz < f_{CLKIN} ≤ 0.8GHz	2	1	0.2GHz to 0.4GHz
0.3GHz < f_{CLKIN} ≤ 0.4GHz	2	2	0.15GHz to 0.2GHz

The maximum delay is equal to the phase interpolator period and there are 4 × 127 = 508 different delay steps. Use Equation 2 to calculate the size of each step.

$$\text{DelayStepSize} = 1 / (f_{INTERPOLATOR} \times 508) = \text{SYSREF\_DLY\_DIV} / (f_{CLKIN} \times 508) \quad (2)$$

Use Equation 3 to calculate the total delay.

$$\text{TotalDelay} = \text{DelayStepSize} \times \text{StepNumber} \quad (3)$$

Table 6-13 shows the number of steps for each delay.

Table 6-13. Calculation of StepNumber

SYSREFx_DLY_PHASE	STEPNUMBER
3	127 - SYSREFx_DLY_I
2	254 - SYSREFx_DLY_Q
0	381 - SYSREFx_DLY_I
1	508 - SYSREFx_DLY_Q

The SYSREF_DLY_BYP field selects the delay path in SYSREF generation output and or the repeater mode bypass signal. When SYSREF_MODE is set to continuous or pulser mode, TI recommends to set SYSREF_DLY_BYP to generator mode. If SYSREF_MODE is set to repeater mode, TI recommends to set SYSREF_DLY_BYP to bypass mode.

6.3.6.3 SYSREFREQ Pins and SYSREFREQ_FORCE Field

The SYSREFREQ pins are multipurpose and can be used for SYNC, SYSREF requests, and SYSREF windowing. These pins can be DC or AC coupled and have individual 50Ω, single-ended termination with programmable common-mode support.

In addition to these pins, the SYSREFREQ_FORCE field can be set to 1 to emulate the same effect as forcing these pins high, simplifying hardware in some cases.

6.3.6.3.1 SYSREFREQ Pins Common-Mode Voltage

The SYSREFREQ_P and SYSREFREQ_N pins can be driven either AC or DC coupled. When driven AC coupled, the common-mode voltage can be adjusted with the SYSREFREQ_VCM bit.

Table 6-14. SYSREFREQ Pin Common-Mode Voltage

SYSREFREQ_VCM	COMMON-MODE VOLTAGE
0	1.3V AC-coupled
1	1.1V AC-coupled
2	1.5V AC-coupled
3	No Bias (DC Coupled)

6.3.6.3.2 SYSREFREQ Windowing Feature

Use SYSREF windowing to internally calibrate the timing between the SYSREFREQ and CLKIN pins to optimize the setup and hold timing. SYSREF windowing can also trim out any mismatches between SYSREFREQ and CLKIN path. This feature requires that the timing from the SYSREFREQ rising edge to the CLKIN rising edge is consistent. The timing from the SYSREFREQ rising edge to the CLKIN rising edges can be tracked with the rb_CLKPOS field. Once the timing to the rising edge of the CLKIN pin is found, the SYSREFREQ rising edge can be internally adjusted with the SYSREFREQ_DLY and SYSREF_DLY_STEP fields to optimize setup and hold timing.

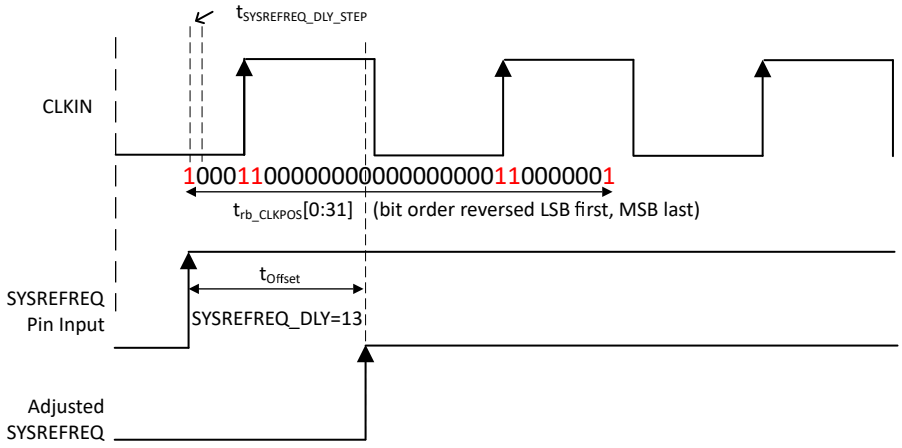


Figure 6-8. SYSREFREQ Internal Timing Adjustment

6.3.6.3.2.1 General Procedure Flowchart for SYSREF Windowing Operation

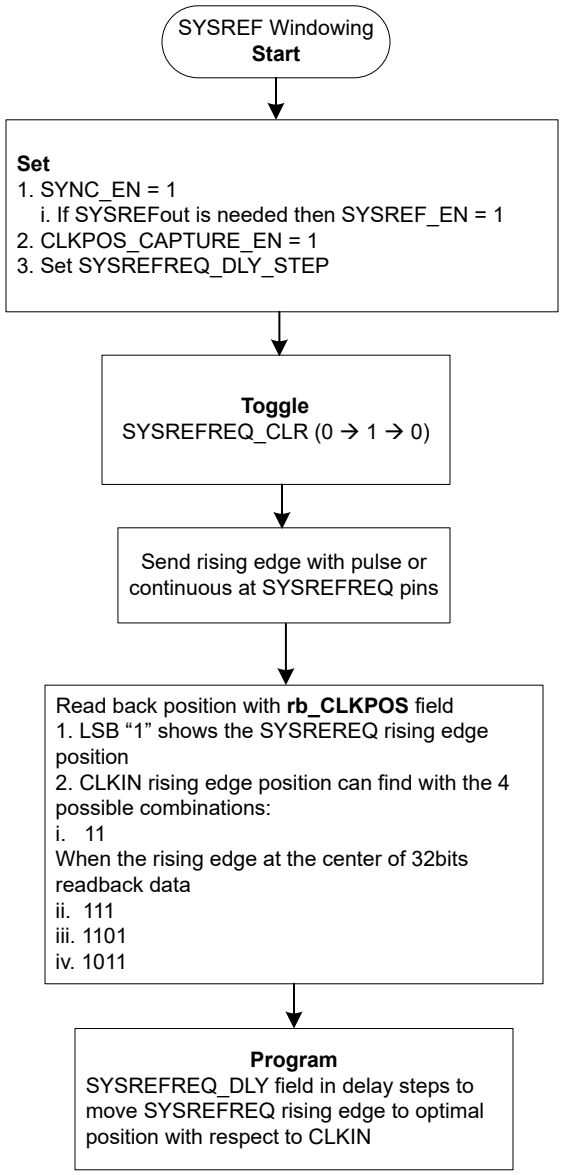


Figure 6-9. Flowchart for SYSREF Windowing Operation

Table 6-15. SYSREFREQ_DLY_STEP

INPUT FREQUENCY	RECOMMENDED SYSREFREQ_DLY_STEP	DELAY(ps)
1.4GHz < f_{CLKIN} ≤ 2.7GHz	0	22.25
2.4GHz < f_{CLKIN} ≤ 4.7GHz	1	13
3.1GHz < f_{CLKIN} ≤ 5.7GHz	2	10.5
f_{CLKIN} ≥ 4.5GHz	3	7.75

6.3.6.3.2.2 SYSREFREQ Repeater Mode With Delay Generation (Retime)

SYSREF repeater mode with delay enabled is possible with LMX to LMX fanout devices by retiming the SYSREFout at different edge of IQ generation. This retiming can have the delay margin between CLKIN and SYSREFREQ inputs based on SYSREF_DLY_DIV value.

Table 6-16 shows how the total delay margin for the SYSREF windowing relates the various SYSREF settings.

Table 6-16. SYSREF Phase Adjust Settings for Retime in Repeater Mode

SYSREF_DLY_DIV	POSITION CODE SELECTED DURING SYNC	EDGE FOR MAX MARGIN	TOTAL MARGIN IN CLKIN CYCLE	SYSREFx_DLY_PHASE	SYSREFx_DLY_Q	SYSREFx_DLY_I
/2	Before 1st edge	I	-1, +1	"11"	0	127
	After 1st edge	Qz	-1, +1	"01"	127	0
	After 2nd edge	Iz	-1, +1	"00"	0	127
/4	Before 1st edge	Qz	-2, +2	"01"	127	0
	After 1st edge	Iz	-2, +2	"00"	0	127
	After 2nd edge	Q	-2, +2	"10"	127	0
/8	Before 1st edge	Qz	-5, +3	"01"	127	0
	After 1st edge	Qz	-4, +4	"01"	127	0
	After 2nd edge	Qz	-3, +5	"01"	127	0
/16	Before 1st edge	I	-9, +7	"11"	0	127
	After 1st edge	I	-8, +8	"11"	0	127
	After 2nd edge	I	-7, +9	"11"	0	127

Repeater retime mode is required to perform the SYSREF windowing in the initial phase to synchronize the SYSREF_DLY_DIV in multiple devices. The user can later choose the SYSREFx_DLY_PHASE, SYSREF_DLY_Q and SYSREFx_DLY_I settings for the selected edge for the SYNC.

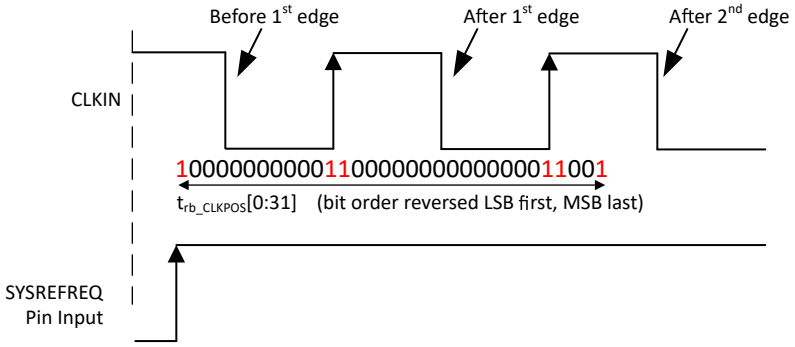


Figure 6-10. SYSREF Windowing to Select the Edge Position for SYNC

This configuration must set the device in **SYSREF_MODE** R17[1:0] value "2" (Repeater mode) and **SYSREF_DLY_BPY** R72[1:0] value "2" (Delay gen engaged in all modes).

6.3.6.3.2.3 Other Guidance For SYSREF Windowing

- The SYSREFREQ pins must be held high for a minimum time of $3/f_{CLKIN}$ + 1.6ns and only after this time rb_CLKPOS field is valid.
- If the user infers multiple valid SYSREFREQ_DLY values from rb_CLKPOS registers to avoid setup and hold time violations. TI recommends to choose the lowest valid SYSREFREQ_DLY to minimize variation over temperature.
- The programmed SYSREFREQ_DLY for optimized setup and hold time after SYSREF windowing adjusts the internal SYSREFREQ, but the SYSREFREQ_DLY does not show the movement in SYSREF windowing readback code. SYSREF windowing always evaluates the signals at the pins.

6.3.6.3.2.4 For Glitch-Free Output

- Keep the same state for the SYSREFREQ pin when switching from request mode to windowing mode and back to request mode. For example, if the SYSREFREQ pin is high (or low) when windowing mode starts, make sure the pin state is high (or low) again after windowing mode ends before programing CLKPOS_CAPTURE_EN.
- The SYSREFREQ pin must be set low when switching from or to SYNC mode.

6.3.6.3.2.5 If Using SYNC Feature

- Only one SYSREFREQ pin rising edge is permitted per 75 input clock cycles
- SYSREFREQ has to stay high for more than 6 clock cycles

6.3.6.3.3 SYNC Feature

The SYNC feature allows the user to synchronize the CLK_DIV, LOGICLK_DIV, LOGICLK_DIV_PRE, SYSREF_DIV, SYSREF_DIV_PRE, and SYSREF_DLY_DIV dividers so that the phase offset can be made consistent between power cycles. This allows users to synchronize multiple devices. This synchronization dividers can only be done through the SYSREFREQ pin, not the software.

6.3.7 Pin Mode Control

Device supports pin mode that can be used to program the device mode selection, divider and multiplier value selection, output power control, and channel output control (ON/OFF). The state machine (SM) clock must be enabled to take any logic state changed at the pin during pin mode operation.

6.3.7.1 Chip Enable (CE)

The chip enable pin is used to enable and disable the device. The chip enable can be controlled through SPI, when CE pin is high (1).

Table 6-17. Chip Enable Control

CE LOGIC	DEVICE STATUS	SPI OVERRIDE CONTROL
0	Disable	No
1	Enable	Yes

6.3.7.2 Output Channel Control

Each channel outputs control through the CLKx_EN pin. This pin enables or disable the CLKOUT and SYSREFOUT of particular channel outputs.

Table 6-18. Output Channel Control Selection

CLKx_EN	CHANNEL OUTPUT STATE	SPI OVERRIDE CONTROL
0	Disable channel output	No
1	Enable channel output	Yes

6.3.7.3 Logic Output Control

The logic output pin can enable and disable the logic clock and logic SYSREF outputs.

Table 6-19. Logic Output Enable

LOGIC_EN	LOGIC OUTPUT STATE	SPI OVERRIDE CONTROL
0	Disable logic output	No
1	Enable logic output	Yes

6.3.7.4 SYSREF Output Control

The SYSREF_EN pin can enable and disable the SYSREF section.

Table 6-20. SYSREF Circuitry Enable

SYSREF_EN	SYSREF CIRCUITRY	SPI OVERRIDE CONTROL
0	Disable	No
1	Enable	Yes

6.3.7.5 Device Mode Selection

The device functions like buffer mode, divider mode or multiplier mode are selected by the MUXSELx pin setting.

Table 6-21. Device Operating Mode Selection

MUXSEL1	MUXSEL0	MODE SELECTION
0	0	SPI control
0	1	Buffer mode
1	0	Divider mode
1	1	Multiplier mode

6.3.7.6 Divider or Multiplier Value Selection

After the operating mode (divider mode or multiplier mode) is selected by MUXSELx pin logic, the divider values or multiplier values are selected by DIVSELx pin logic.

Table 6-22. Divider or Multiplier Value Selection

DIVSEL2	DIVSEL1	DIVSEL0	DIVIDER VALUE	MULTIPLIER VALUE
0	0	0	SPI control	SPI control
0	0	1	2	x
0	1	0	3	2
0	1	1	4	3
1	0	0	5	4
1	0	1	6	x
1	1	0	7	x
1	1	1	8	x

6.3.7.7 Calibration Control Pin

While operating in multiplier mode, the PLL based multiplier required the calibration for frequency lock and the CAL pin transition from low to high initiates the calibration.

Table 6-23. CAL Pin Logic

CAL	CALIBRATION STATE
0	SPI controlled calibration
0 → 1	Initiate calibration

6.3.7.8 Output Power Control

The output power of the all channels control through PWRSELx pins.

Table 6-24. Channel Output Power Control

PWRSEL2	PWRSEL1	PWRSEL0	OUTPUT POWER
0	0	0	SPI Control
0	0	1	Lowest output power
0	1	0	-

Table 6-24. Channel Output Power Control (continued)

PWRSEL2	PWRSEL1	PWRSEL0	OUTPUT POWER
0	1	1	-
1	0	0	-
1	0	1	-
1	1	0	-
1	1	1	Highest output power

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 SYSREFREQ Input Configuration

The SYSREFREQ pins support single-ended or differential input in AC or DC coupling mode. The SYSREFREQ pins have an internal 50Ω termination with capacitive ground, which acts as 100Ω differential.

Figure 7-1 shows the generic SYSREFREQ input circuit recommendation to support all AC/DC, single-ended or differential inputs. Some of the discrete components in Figure 7-1 are just placeholder for individual input signal (single-ended or differential input) and AC or DC coupled input.

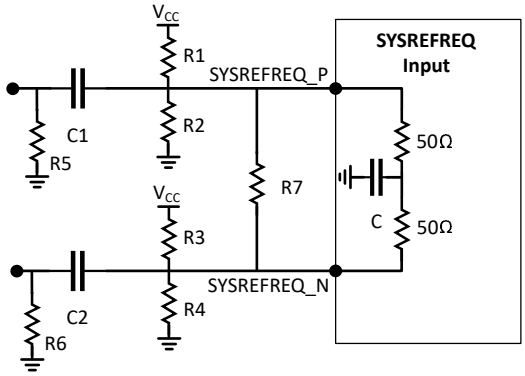


Figure 7-1. SYSREFREQ Input Circuit Recommendations

The following figures show the individual circuit diagram for each configurations:

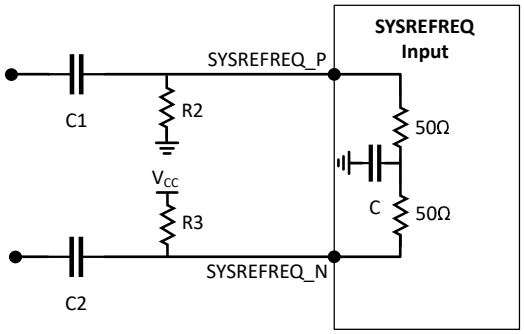


Figure 7-2. AC-Coupled Differential Input

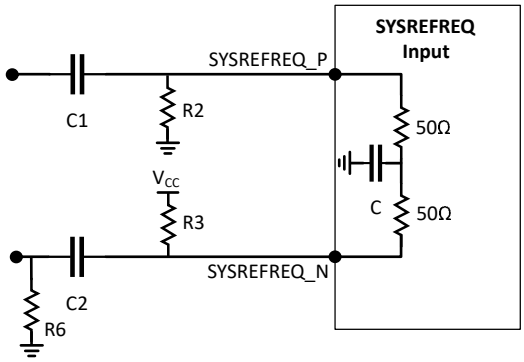


Figure 7-3. AC-Coupled, Single-Ended Input

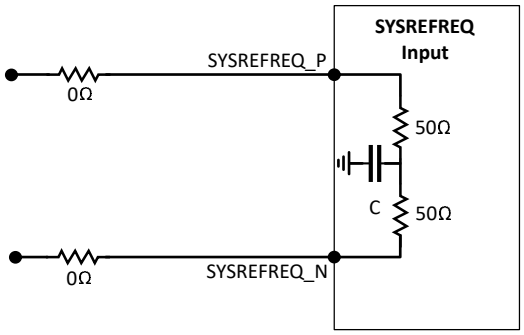


Figure 7-4. DC-Coupled Differential Input

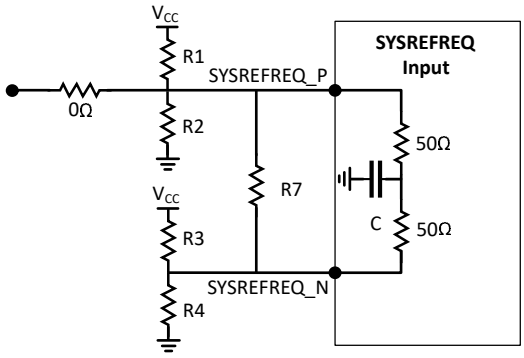


Figure 7-5. DC-Coupled, Single-Ended Input

1. AC coupled differential and single-ended input configurations required the resistor terminations (R2 and R3) to create the VCM at each pin and resistor values must select to maintain greater than 150mV potential difference between pin P and pin N.
   a. As an example, to create the VCM of 1.5V at pin P and 1.65V at pin N, with the 2.5V VCC, set R3 = 550Ω and R2 = 1kΩ
   b. For single-ended input configuration, place R6 = 50Ω to avoid any reflection at complementary input pin.
2. DC coupled differential and single-ended input configuration required to have the source common-mode voltage matched with the device input common mode specifications.
   a. For single-ended input configuration, keep the R1, R2, R3 and R4 resistors. This method creates the same common-mode voltage at both pins, and the resistive dividers create 75Ω at pin P and 50Ω Thevenin's equivalent at pin N.
   b. As an example, to have the common-mode voltage of 1.35V at each pin, set the resistive divider components values to R1 = 130Ω, R2 = 165Ω, R3 = 86.6Ω and R4 = 110Ω with the 2.5V VCC.

7.1.2 Treatment of Unused Pins

In many cases, not all pins are used. Table 7-1 lists the recommendation on how to handle these unused pins.

Table 7-1. Treatment of Unused or Partially Used Pins

PIN(S)	TREATMENT
All VCC Pins	These pins must always be connected to the power supply. If the block that powers by these VCC pins (as implied by the pin name) is not used, then the bypassing can be minimized or eliminated.
SYSREFREQ	1. If driving single-ended input, the complementary input pin terminates based on Section 7.1.1. 2. If the SYSREFREQ pins are unused, tie the pins to the VCC with a 1kΩ resistor.
CLKIN Complementary Input	If driving single-ended input, the complementary pin terminate with 50Ω resistor AC-coupled to ground.
VBIAS01 and VBIAS23	If multiplier is not used, connect these pins capacitor (1µF) to ground.

Table 7-1. Treatment of Unused or Partially Used Pins (continued)

PIN(S)	TREATMENT
CLKOUT SYSREFOUT LOGICLKOUT LOGISYSREFOUT	If not used, connect a AC-coupling capacitor and 50Ω to ground.
CE, CLKx_EN, LOGIC_EN, SYSREF_EN	1. If operating device in SPI controlled mode, these pins must tied to VCC with 1kΩ resistor. 2. If not operating in both SPI and pin mode, these pins must connect to ground with 1kΩ resistor.
CAL, MUXSELx, DIVSELx, PWRSELx	1. If these pins are unused, connect these pins to ground with a 1kΩ resistor.

7.1.3 Current Consumption

The current consumption varies as a function of the setup condition. By adding up all the block currents shown in Table 7-2, users can obtain reasonable estimate of the current for any setup condition.

Table 7-2. Current Consumption per Block

BLOCK		CONDITIONS		CURRENT (mA)
Device Core		CLK_MUX = Buffer Mode		294
		CLK_MUX = Divide Mode		260
		CLK_MUX = Multiply Mode	SMCLK_EN=0	540
			SMCLK_EN=1	560
SYSREF SYNC Windowing	Core	SYSREF_EN=1		80
	Delay Generator	Generator Mode (SYSREF_MODE=0,1)		53
		Repeater Mode (SYSREF_MODE=2)		40
	Windowing Circuitry	Windowing Circuitry (CLKPOS_CAPTURE_EN=1)	SYSREF_MODE=0,1	113
			SYSREF_MODE=2	0
	SYSREF Pulser	SYSREF_MODE=1		7
CLKOUT (Per active clock channel)	Core	SYSREF_EN=0		25
		SYSREF_EN = 1	Delay Not Used	30
			Delay Used	40
	Output Buffer	CHx_EN = CLKOUTx_EN=1		4+6*CLKOUTx_PWR
SYSREFOUT	Core	SYSREFOUT_EN = CHx_EN = 1		74 + SYSREFOUTx_PWR*5
	Output Buffer	SYSREFOUT_EN = CHx_EN = 1 (SYSREFOUTx_PWR and SYSREFOUTx_VCM can interact which makes the output buffer current lower than the formula predicts in some cases)		2*SYSREFOUTx_PWR + 2*SYSREFOUTx_VCM
LOGICLKOUT	Core	LOGIC_EN=1 LOGICLKOUT_EN=1	SYSREF_EN=0	49
			SYSREF_EN=1	59
	Output Buffer		CML(R_P=50Ω)	16+1*LOGICLKOUT_PWR
			LVDS	12
LOGISYSREFOUT	Core	LOGIC_EN=1 LOGISYSREFOUT_EN=1	SYSREF_EN=0	0
			SYSREF_EN=1	55
	Output Buffer	LOGIC_EN=1 LOGISYSREFOUT_EN=1	CML(R_P=50Ω)	16+1*LOGICLKOUT_PWR
			LVDS	12

7.2 Typical Applications

7.2.1 Local Oscillator Distribution Application

For this application, the additive noise impact of using the LMX1860-SEP as a x2 multiplier is exported when added to the LMX2694-SEP 3GHz output clock. This particular setup used a single-ended clock to drive the LMX1860-SEP for the sake of simplicity of hooking up two EVMs together, but driving the device differentially is generally recommended.

Figure 7-6. Typical Application Schematic

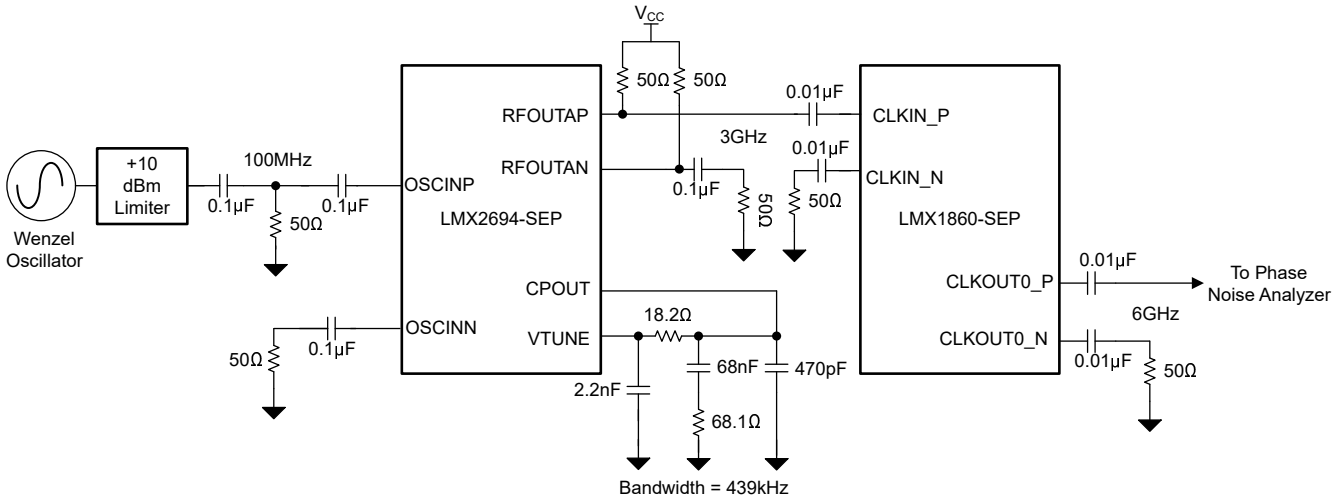


Figure 7-7. Typical Application Schematic

7.2.1.1 Design Requirements

Table 7-3 shows the design parameters for this example.

If not all outputs or SYSREF are used, TI recommends to compress the layout to minimize trace lengths, especially that of the input trace.

Table 7-3. Design Parameters

PARAMETERS	VALUE
LMX2694-SEP Input Frequency	100MHz
LMX2694-SEP Output Frequency	3GHz
LMX1860-SEP Clock Input Frequency	3GHz
LMX1860-SEP Clock Output Frequency	6GHz
LMX1860-SEP Multiplier Value	x2

7.2.1.2 Detailed Design Procedure

In this example, a 3GHz input clock is being multiplied up to a 6GHz input clock. The external components do not change that much based on internal configuration. The TICS Pro software is very useful in calculating the necessary register values and configuring the device.

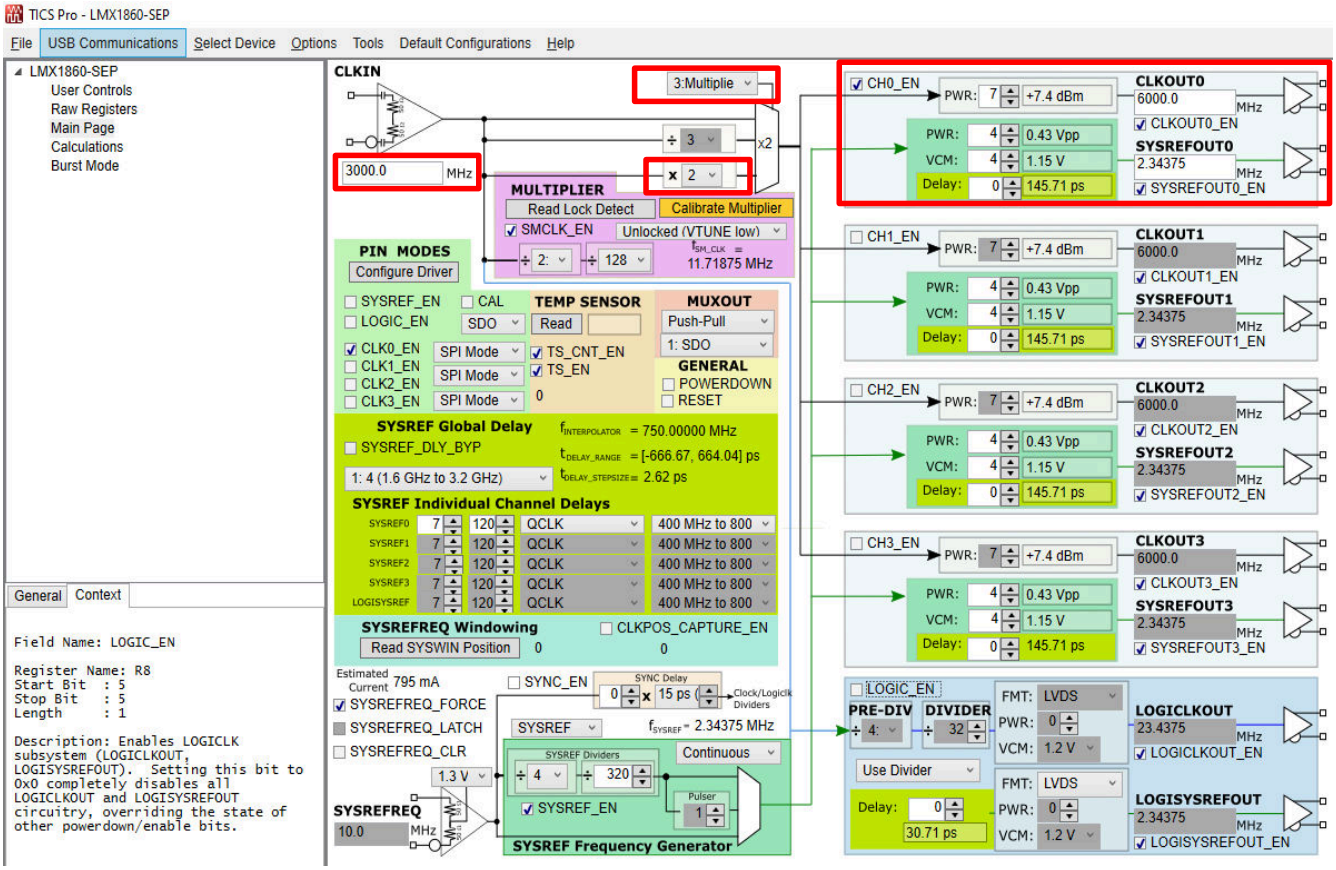


Figure 7-8. LMX1860-SEP TICS Pro Setup

7.2.1.3 Application Plot

LMX1860-SEP Multiplier Output the total plot is the sum of the noise of the LMX1860-SEP multiplier noise and the LMX2615-SP 3GHz output (scaled to 6GHz by adding 6dB). Note that the LMX1860-SEP does increase the phase noise in the 1MHz to 20MHz range, but beyond 20MHz, the input multiplier actually filters the output noise floor.

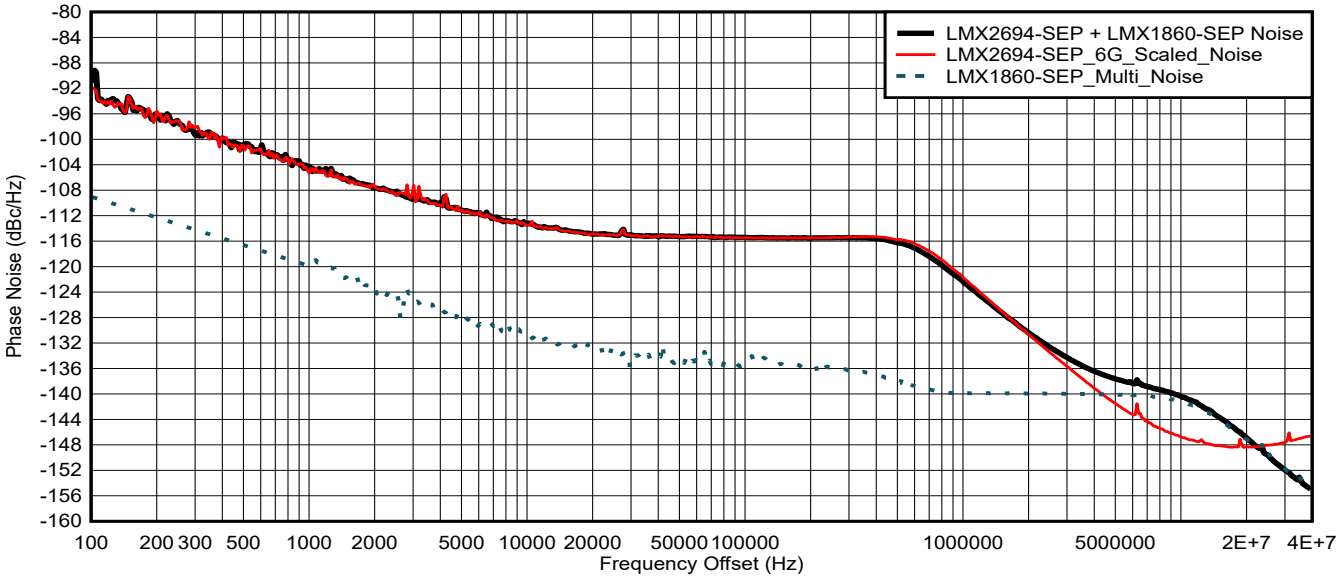


Figure 7-9. LMX1860-SEP Multiplier Output

7.2.2 JESD204B/C Clock Distribution Application

This application shows the JESD204B/C clock distribution circuit using the LMX1860-SEP, which can take the high frequency input from LMX2694-SEP and generate 4 pairs of JESD clocks to data converters along with clocks for FPGA.

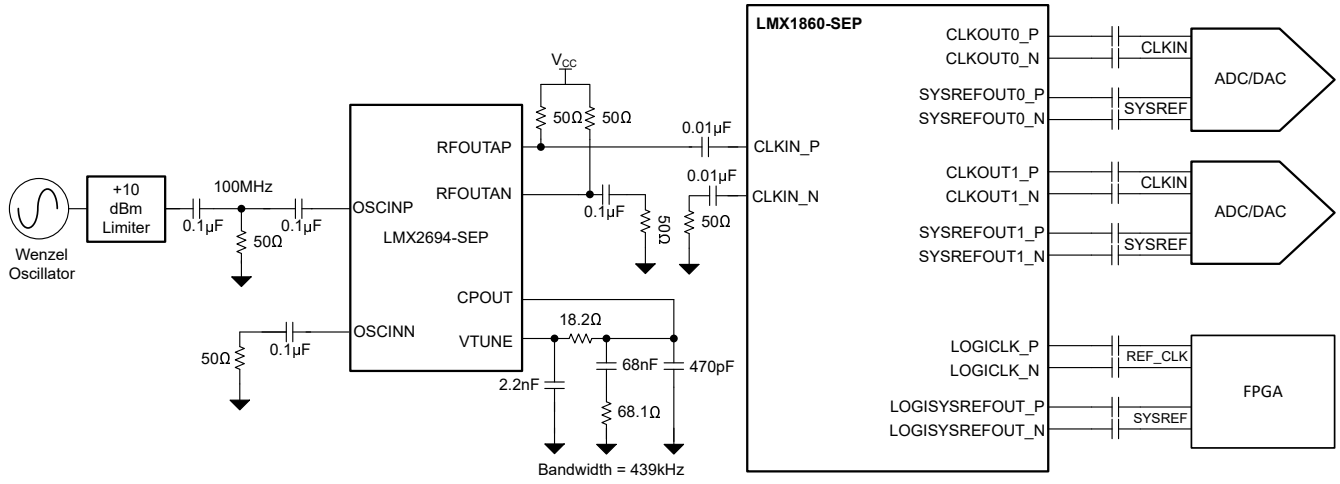


Figure 7-10. Typical JESD Clocks Block Diagram

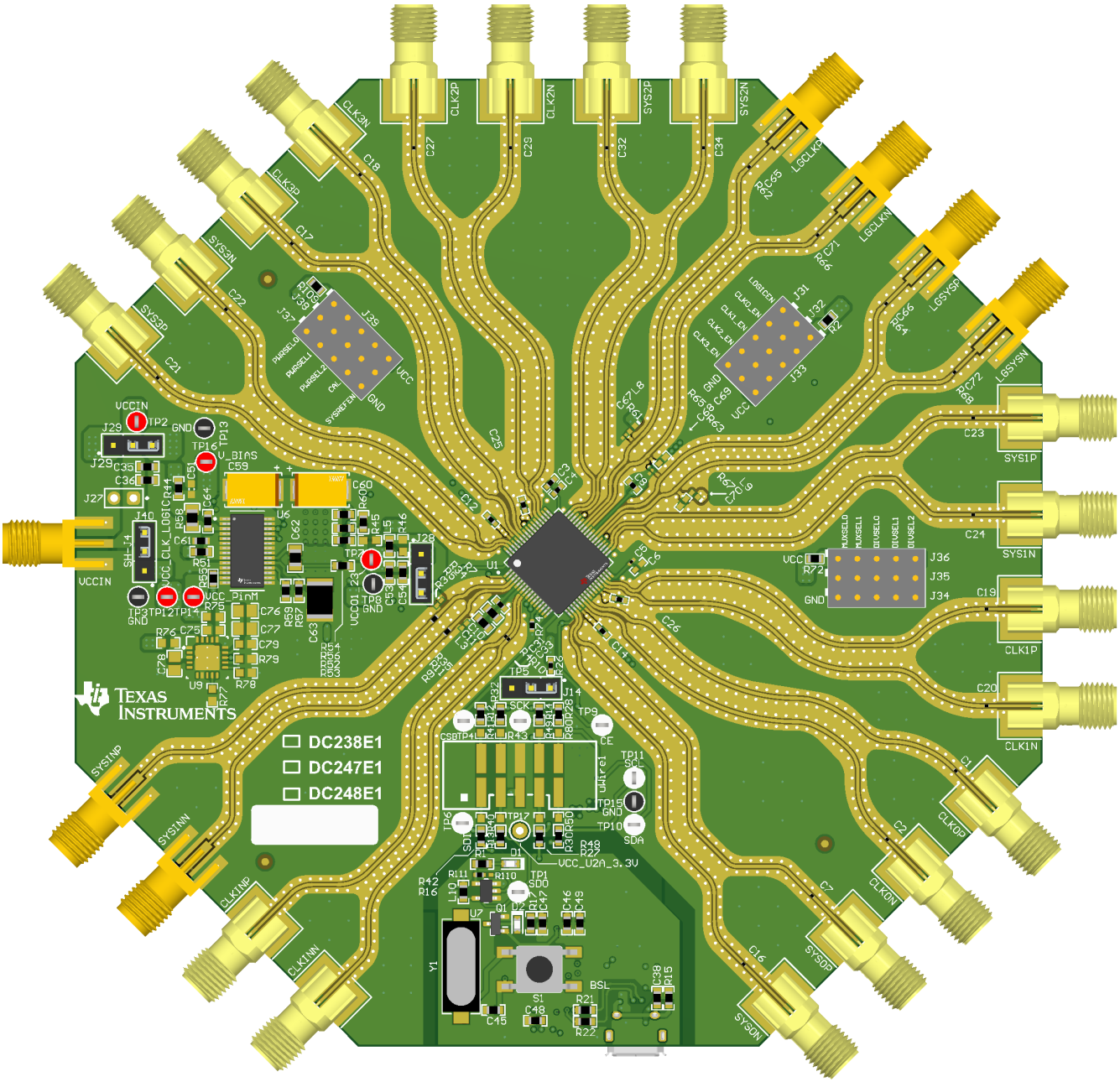
7.3 Layout

7.3.1 Layout Guidelines

- If using a single-ended output, terminate the complementary side with 50Ω so that the impedance for the signal output is same as complementary pin side.
- GND pins on the outer perimeter of the package can be routed on the package back to the DAP.
- Minimize the length of the CLKIN trace for optimal phase noise. Poor matching can degrade the noise floor.
- Verify that the DAP on the device is well-grounded with many vias.
- Use a low loss dielectric material, such as Rogers 4003C, for optimal output power.
- Be aware that if all the outputs and SYSREF are operating, the current consumption can be high enough to exceed the recommended internal junction temperature of 125°C; a heat sink can be necessary.

7.3.2 Layout Example

Layout Example



7.4 Power Supply Recommendations

This device uses a 2.5V supply for the whole device. A direct connection to a switching power supply can result in unwanted spurs at the output. Bypassing can be done individually at all the power pins. TI recommends placing smaller capacitors with higher frequency of minimum impedance on the same layer as the device, as close to the pins as possible. Since the frequencies of nearly all signals in the device are 100MHz or greater, therefore larger value bypass capacitors with low frequency of minimum impedance are only used for internal LDO stability, and the distance to the device (and the loop inductance of the bypass path) can be larger. Isolate the supply pins for the clocks and the LOGICLK with a small resistor or ferrite bead if both are being used simultaneously. See the *Pin Configuration and Functions* section for additional recommendations for each pin.

Note

This device has minimal PSRR due to the low operating voltage and internal filtering by LDOs. Connecting this device to a low noise supply that does not have excessive spurious noise is important.

7.4.1 Power-Up Timing

To power up the device, some power sequencing is required.

1. Apply power to the device and verify that the VCC pins reach proper levels.
2. Although the power-on reset happens automatically, the user can do a software reset by toggling the RESET bit from 1 to 0. Verify that the time between programming these two commands is at least 1µs.
3. Program the registers as desired.

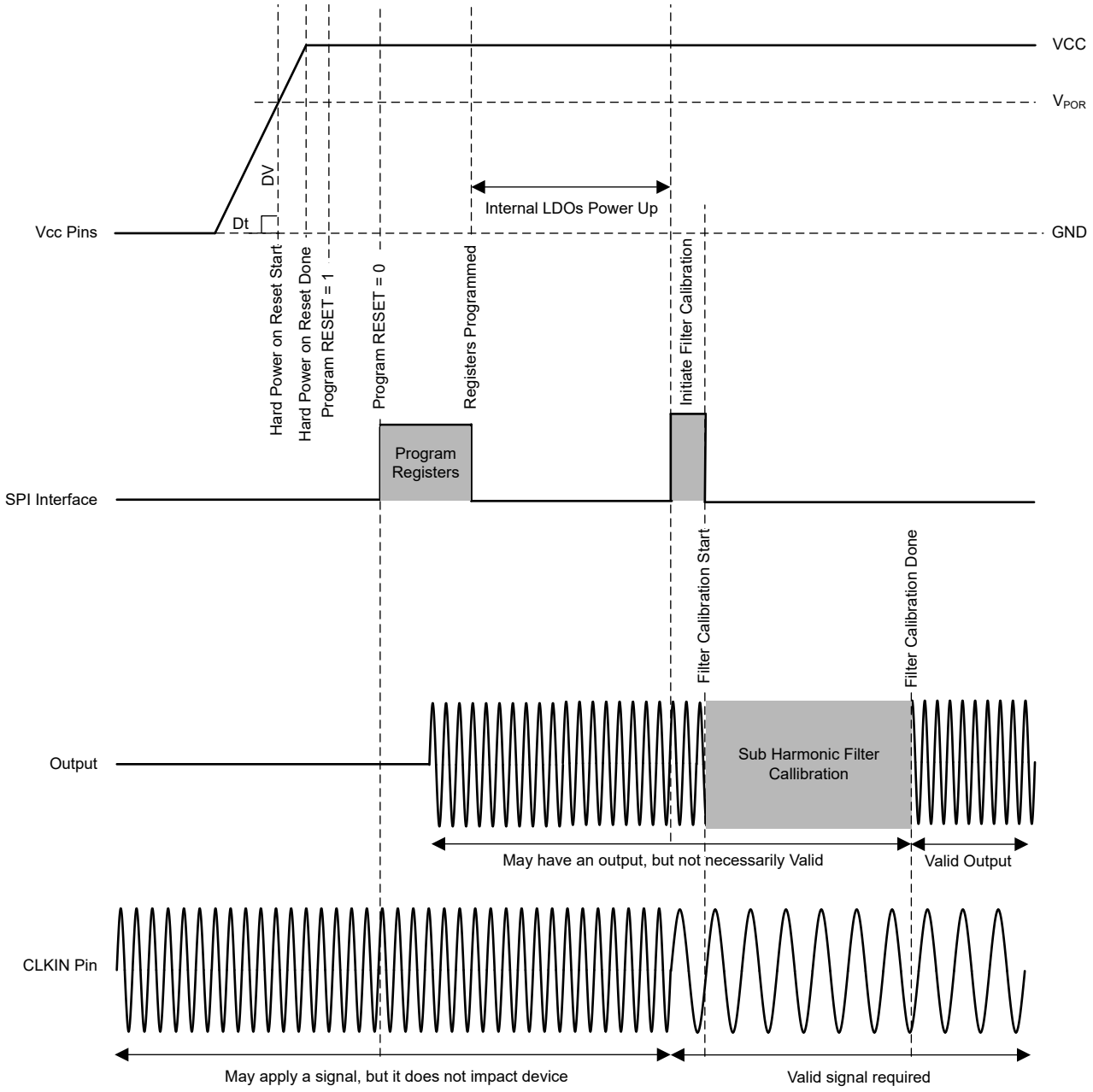


Figure 7-11. Power-Up Timing

7.5 Register Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	0	0	0	0	0	POWERDOWN	0	RESET
R2	0	0	0	0	0	0	SMCLK_DIV_PRE				SMCLK_EN	0	0	0	1	1
R3	CH3_EN	CH2_EN	CH1_EN	CH0_EN	LOGICLK_MUTE_CAL	CH3_MUTE_CAL	CH2_MUTE_CAL	CH1_MUTE_CAL	CH0_MUTE_CAL	0	0	0	0	SMCLK_DIV		
R4	0	0	CLKOUT1_PWR			CLKOUT0_PWR			SYSREFOUT3_EN	SYSREFOUT2_EN	SYSREFOUT1_EN	SYSREFOUT0_EN	CLKOUT3_EN	CLKOUT2_EN	CLKOUT1_EN	CLKOUT0_EN
R5	0	SYSREFOUT2_PWR			SYSREFOUT1_PWR			SYSREFOUT0_PWR			CLKOUT3_PWR			CLKOUT2_PWR		
R6	LOGICLKOUT_EN	SYSREFOUT3_VCM			SYSREFOUT2_VCM			SYSREFOUT1_VCM			SYSREFOUT0_VCM			SYSREFOUT3_PWR		
R7	0	LOGISYSREFOUT_VCM		LOGICLKOUT_VCM		LOGISYSREF_DIV_PWR_PRE		LOGICLK_DIV_PWR_PRE		LOGISYSREFOUT_PWR			LOGICLKOUT_PWR			LOGISYSREFOUT_EN
R8	0	0	0	0	0	0	0	LOGICLK_DIV_PRE			LOGIC_EN	0	LOGISYSREFOUT_FMT		LOGICLKOUT_FMT	
R9	SYSREFREQ_VCM		SYNC_EN	LOGICLK_DIV_PD	LOGICLK_DIV_BYP	0	LOGICLK_DIV									
R11	rb_CLKPOS															
R12	rb_CLKPOS[31:16]															
R13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SYSREFREQ_DLY_STEP	
R14	0	0	0	0	0	0	0	SYNC_MUTE_PD	0	0	0	0	0	CLKPOS_CAPTURE_EN	SYSREFREQ_MODE	SYSREFREQ_LATCH
R15	0	0	0	0	SYSREF_DIV_PRE		1	SYSREF_EN	0	SYSREFREQ_DLY						SYSREFREQ_CLR
R16	SYSREF_PULSE_CNT				SYSREF_DIV											
R17	0	0	0	0	0	SYSREF0_DLY_I							SYSREF0_DLY_PHASE	SYSREF_MODE		
R18	SYSREF1_DLY_I							SYSREF1_DLY_PHASE	SYSREF0_DLY_Q							
R19	SYSREF2_DLY_I							SYSREF2_DLY_PHASE	SYSREF1_DLY_Q							
R20	SYSREF3_DLY_I							SYSREF3_DLY_PHASE	SYSREF2_DLY_Q							
R21	LOGISYSREF_DLY_I							LOGISYSREF_DLY_PHASE	SYSREF3_DLY_Q							
R22	SYSREF1_DLY_SCALE		SYSREF0_DLY_SCALE		SYSREF_DLY_DIV			0	0	LOGISYSREF_DLY_Q						
R23	TS_EN	1	MUXOUT_EN	0	0	0	0	0	0	MUXOUT_SEL	LOGISYSREF_DLY_SCALE		SYSREF3_DLY_SCALE		SYSREF2_DLY_SCALE	
R24	0	0	0	0	rb_TS											TS_CNT_EN
R25	0	0	0	0	0	0	1	0	0	CLK_DIV_RST	CLK_DIV			CLK_MUX		
R28	0	0	0	VCO_CORE_FORCE	VCO_CORE			0	0	0	0	0	1	0	0	0
R29	0	0	0	0	0	1	0	1	VCO_CAPCTRL							

R33	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0
R34	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R65	0	1	1	0	0	1	0	rb_VCO_CORE					0	0	0	0
R67	0	1	0	1	0	0	0	1	1	1	0	0	1	0	1	1
R72	0	0	0	0	0	0	0	0	0	0	0	0	0	SYSREFREQ_FORCE	SYSREF_DLY_BYP	
R73	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R75	rb_CLK2_EN	rb_CLK1_EN	rb_CLK0_EN	rb_MUXSEL1	rb_MUXSEL0	rb_LOGIC_EN	rb_LD		rb_DIVSEL2	rb_DIVSEL1	rb_DIVSEL0	rb_CE	0	0	1	1
R76	0	0	0	0	0	0	0	0	0	0	0	0	rb_PWRSEL2	rb_PWRSEL1	rb_PWRSEL0	rb_CLK3_EN
R79	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R86	0	0	0	0	0	0	0	0	0	0	0	0	0	MUXOUT_EN_OVRD	0	0
R90	0	0	0	0	0	0	0	0	0	LOGICLK_DIV_BYP3	LOGICLK_DIV_BYP2	0	0	0	0	0

Registers not listed in this table must NOT be programmed as doing so can adversely impact performance or functionality of the device.

The following registers must NOT be programmed to avoid adversely impacting the performance of the device: R1, R10, R26, R27, R30-R32,

The following registers do NOT require programming if clock output multiplier is NOT used: R29, R33, R34, R65, R67, R73

The following registers do NOT require programming if LOGICLK is NOT used: R79, R90

7.5.1 Device Registers

Table 7-4 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 7-4 must be considered as reserved locations and the register contents must not be modified.

Table 7-4. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	R0	Powerdown, Reset, Multiplier Mode Calibration	Section 7.5.1.1
2h	R2	Multiplier Mode (State Machine Clock)	Section 7.5.1.2
3h	R3	Multiplier Mode (State Machine Clock), Output Enables	Section 7.5.1.3
4h	R4	Output Enables, CLKOUT Power	Section 7.5.1.4
5h	R5	CLKOUT Power, SYSREFOUT Power	Section 7.5.1.5
6h	R6	LOGICLK Enable, SYSREFOUT Power/VCM	Section 7.5.1.6
7h	R7	LOGICLK and LOGISYSREF	Section 7.5.1.7
8h	R8	LOGICLK and LOGISYSREF	Section 7.5.1.8
9h	R9	LOGICLK Divider, SYNC, SYSREFREQ	Section 7.5.1.9
Bh	R11	SYSREFREQ Windowing (readback)	Section 7.5.1.10
Ch	R12	SYSREFREQ Windowing (readback)	Section 7.5.1.11
Dh	R13	SYSREFREQ Windowing	Section 7.5.1.12
Eh	R14	SYSREFREQ Windowing, SYNC, SYSREF	Section 7.5.1.13
Fh	R15	SYSREFREQ Windowing, SYNC, SYSREF	Section 7.5.1.14
10h	R16	SYSREF	Section 7.5.1.15
11h	R17	SYSREF, SYSREFOUT Delay	Section 7.5.1.16
12h	R18	SYSREFOUT Delay	Section 7.5.1.17
13h	R19	SYSREFOUT Delay	Section 7.5.1.18
14h	R20	SYSREFOUT Delay	Section 7.5.1.19
15h	R21	SYSREFOUT Delay	Section 7.5.1.20
16h	R22	SYSREFOUT Delay	Section 7.5.1.21
17h	R23	Temperature Sensor, MUXOUT, SYSREFOUT Delay	Section 7.5.1.22
18h	R24	Temperature Sensor	Section 7.5.1.23
19h	R25	Multiplier Mode, Divider Mode	Section 7.5.1.24
1Ch	R28	Multiplier Mode (optional, partial assist calibration)	Section 7.5.1.25
1Dh	R29	Multiplier Mode (optional, partial assist calibration)	Section 7.5.1.26
21h	R33	Multiplier Mode (RESERVED, must write in multiplier mode)	
22h	R34	Multiplier Mode (RESERVED, must write in multiplier mode)	
41h	R65	Multiplier Mode (read-only, optional, for partial assist calibration)	Section 7.5.1.29
43h	R67	Multiplier Mode (read-only, optional, for partial assist calibration)	Section 7.5.1.30
48h	R72	SYSREF	Section 7.5.1.31
49h	R73	Reserved	
4Bh	R75	Multiplier Mode (read-only, optional, lock detect)	Section 7.5.1.33
4Ch	R76	Read-only	Section 7.5.1.34
56h	R86	MUXOUT (RESERVED, optional, for tri-state)	
5Ah	R90	LOGICLK Divider (RESERVED, optional, for divider bypass)	

Complex bit access types are encoded to fit into small table cells. Table 7-5 shows the codes that are used for access types in this section.

Table 7-5. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1.1 R0 Register (Offset = 0h) [Reset = 0000h]

R0 is shown in Table 7-6.

Return to the Table 7-4.

Table 7-6. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	UNDISCLOSED	R/W	0h	Program this field to 0x0.
2	POWERDOWN	R/W	0h	Sets the device in a low-power state. The states of other registers are maintained.
1	UNDISCLOSED	R/W	0h	Program this field to 0x0.
0	RESET	R/W	0h	Soft Reset. Resets the entirie logic and reigsters (equivalent to power-on reset). Self-clearing on next register write.

7.5.1.2 R2 Register (Offset = 2h) [Reset = 0223h]

R2 is shown in Table 7-7.

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Table 7-7. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R	0h	Program this field to 0x0.
10	UNDISCLOSED	R/W	0h	Program this field to 0x0.
9-6	SMCLK_DIV_PRE	R/W	8h	Pre-divider for State Machine clock (one hot divider).The state machine clock is divided from the input clock. The output of the pre-divider should be ≤1600MHz. Values other than those listed are reserved. 2h = /2 4h = /4 8h = /8
5	SMCLK_EN	R/W	1h	Enables the state machine clock generator. Only required to calibrate the multiplier, and for multiplier lock detect (including on MUXOUT pin). If the multiplier is not used, or if the multiplier lock detect feature is not used, the state machine clock generator can be disabled to minimize crosstalk.
4-0	UNDISCLOSED	R/W	3h	Program this field to 0x3.

7.5.1.3 R3 Register (Offset = 3h) [Reset = FF86h]

R3 is shown in Table 7-8.

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Table 7-8. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CH3_EN	R/W	1h	Enables CH3 (CLKOUT3, SYSOUT3). Setting this bit to 0 will completely disable CH3, overriding the state of other powerdown/ enable bits.
14	CH2_EN	R/W	1h	Enables CH2 (CLKOUT2, SYSOUT2). Setting this bit to 0 will completely disable CH2, overriding the state of other powerdown/ enable bits.
13	CH1_EN	R/W	1h	Enables CH1 (CLKOUT1, SYSOUT1). Setting this bit to 0 will completely disable CH1, overriding the state of other powerdown/ enable bits.
12	CH0_EN	R/W	1h	Enables CH0 (CLKOUT0, SYSOUT0). Setting this bit to 0 will completely disable CH0, overriding the state of other powerdown/ enable bits.
11	LOGICLK_MUTE_CAL	R/W	1h	Mutes LOGIC outputs (LOGICLK/LOGISYS) during multiplier calibration.
10	CH3_MUTE_CAL	R/W	1h	Mutes CH3 (CLKOUT3/SYSOUT3) during multiplier calibration.
9	CH2_MUTE_CAL	R/W	1h	Mutes CH2 (CLKOUT2/SYSOUT2) during multiplier calibration.
8	CH1_MUTE_CAL	R/W	1h	Mutes CH1 (CLKOUT1/SYSOUT1) during multiplier calibration.
7	CH0_MUTE_CAL	R/W	1h	Mutes CH0 (CLKOUT0/SYSOUT0) during multiplier calibration.
6-3	UNDISCLOSED	R	0h	Program this field to 0x0.
2-0	SMCLK_DIV	R/W	6h	Sets state machine clock divider. Further divides the output of the state machine clock pre-divider. Input frequency from SMCLK_DIV_PRE must be ≤ 1600 MHz. Output frequency must be ≤ 30 MHz. Divide value is 2^{SMCLK_DIV}. 0h = /1 1h = /2 2h = /4 3h = /8 4h = /16 5h = /32 6h = /64 7h = /128

7.5.1.4 R4 Register (Offset = 4h) [Reset = 36FFh]

R4 is shown in Table 7-9.

Return to the Table 7-4.

Table 7-9. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	UNDISCLOSED	R	0h	Program this field to 0x0.
13-11	CLKOUT1_PWR	R/W	6h	Sets the output power of CLKOUT1. Larger values correspond to higher output power.
10-8	CLKOUT0_PWR	R/W	6h	Sets the output power of CLKOUT0. Larger values correspond to higher output power.
7	SYSREFOUT3_EN	R/W	1h	Enables SYSREFOUT3 output buffer.
6	SYSREFOUT2_EN	R/W	1h	Enables SYSREFOUT2 output buffer.
5	SYSREFOUT1_EN	R/W	1h	Enables SYSREFOUT1 output buffer.
4	SYSREFOUT0_EN	R/W	1h	Enables SYSREFOUT0 output buffer.
3	CLKOUT3_EN	R/W	1h	Enables CLKOUT3 output buffer.
2	CLKOUT2_EN	R/W	1h	Enables CLKOUT2 output buffer.
1	CLKOUT1_EN	R/W	1h	Enables CLKOUT1 output buffer.
0	CLKOUT0_EN	R/W	1h	Enables CLKOUT0 output buffer.

7.5.1.5 R5 Register (Offset = 5h) [Reset = 4936h]

R5 is shown in Table 7-10.

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Table 7-10. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14-12	SYSREFOUT2_PWR	R/W	4h	Sets the output power of SYSREFOUT2. Larger values corespond to higher output power. SYSREFOUT2_VCM must be set properly to bring the output common mode voltage within permissible limits.
11-9	SYSREFOUT1_PWR	R/W	4h	Sets the output power of SYSREFOUT1. Larger values corespond to higher output power. SYSREFOUT1_VCM must be set properly to bring the output common mode voltage within permissible limits.
8-6	SYSREFOUT0_PWR	R/W	4h	Sets the output power of SYSREFOUT0. Larger values corespond to higher output power. SYSREFOUT0_VCM must be set properly to bring the output common mode voltage within permissible limits.
5-3	CLKOUT3_PWR	R/W	6h	Sets the output power of CLKOUT3. Larger values correspond to higher output power.
2-0	CLKOUT2_PWR	R/W	6h	Sets the output power of CLKOUT2. Larger values correspond to higher output power.

7.5.1.6 R6 Register (Offset = 6h) [Reset = B6DCh]

R6 is shown in Table 7-11.

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Table 7-11. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOGICLKOUT_EN	R/W	1h	Enables the logic clock output buffer.
14-12	SYSREFOUT3_VCM	R/W	3h	Sets the output common mode of SYSREFOUT3. SYSREFOUT3_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
11-9	SYSREFOUT2_VCM	R/W	3h	Sets the output common mode of SYSREFOUT2. SYSREFOUT2_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
8-6	SYSREFOUT1_VCM	R/W	3h	Sets the output common mode of SYSREFOUT1. SYSREFOUT1_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
5-3	SYSREFOUT0_VCM	R/W	3h	Sets the output common mode of SYSREFOUT0. SYSREFOUT0_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
2-0	SYSREFOUT3_PWR	R/W	4h	Sets the output power of SYSREFOUT3. Larger values corespond to higher output power. SYSREFOUT3_VCM must be set properly to bring the output common mode voltage within permissible limits.

7.5.1.7 R7 Register (Offset = 7h) [Reset = 0001h]

R7 is shown in Table 7-12.

Return to the Table 7-4.

Table 7-12. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.

Table 7-12. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-13	LOGISYSREFOUT_VCM	R/W	0h	In LVDS mode, sets the output common mode of the logic SYSREF output. Other output formats ignore this field. 0h = 1.2V 1h = 1.1V 2h = 1.0V 3h = 0.9V
12-11	LOGICLKOUT_VCM	R/W	0h	In LVDS mode, sets the output common mode of the logic clock output. Other output formats ignore this field. 0h = 1.2V 1h = 1.1V 2h = 1.0V 3h = 0.9V
10-9	LOGISYSREF_DIV_PWR_PRE	R/W	0h	Sets the output power of the logic SYSREF pre-driver. Larger values correspond to higher output power.
8-7	LOGICLK_DIV_PWR_PRE	R/W	0h	Sets the output power of the logic clock pre-driver. Larger values correspond to higher output power.
6-4	LOGISYSREFOUT_PWR	R/W	0h	Sets the output power of LOGISYSREFOUT for CML format only (other output formats ignore this field). Larger values correspond to higher output power.
3-1	LOGICLKOUT_PWR	R/W	0h	Sets the output power of LOGICLKOUT for CML format only (other output formats ignore this field). Larger values correspond to higher output power.
0	LOGISYSREFOUT_EN	R/W	1h	Enables the logic SYSREF output buffer.

7.5.1.8 R8 Register (Offset = 8h) [Reset = 0120h]

R8 is shown in Table 7-13.

Return to the Table 7-4.

Table 7-13. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R	0h	Program this field to 0x0.
8-6	LOGICLK_DIV_PRE	R/W	4h	Sets pre-divider value for logic clock divider. Output of the pre-divider must be less than or equal to 3.2 GHz. When LOGICLK_DIV_PRE=1, it is also required register R79 is programmed to a value of 0x0005 and R90 to 0x0060 (LOGICLK_DIV_BYP2=1, LOGICLK_DIV_BYP3=1). Values for LOGICLK_DIV_PRE other than those listed below are reserved. 1h = /1 2h = /2 4h = /4
5	LOGIC_EN	R/W	1h	Enables LOGICLK subsystem (LOGICLKOUT, LOGISYSREFOUT). Setting this bit to 0x0 completely disables all LOGICLKOUT and LOGISYSREFOUT circuitry, overriding the state of other powerdown/enable bits.
4	UNDISCLOSED	R/W	0h	Program this field to 0x0.
3-2	LOGISYSREFOUT_FMT	R/W	0h	Selects the output driver format of the LOGISYSREFOUT output. 0h = LVDS 1h = Reserved 2h = CML 3h = Reserved
1-0	LOGICLKOUT_FMT	R/W	0h	Selects the output driver format of the LOGICLKOUT output. 0h = LVDS 1h = Reserved 2h = CML 3h = Reserved

7.5.1.9 R9 Register (Offset = 9h) [Reset = 0020h]

R9 is shown in Table 7-14.

Return to the Table 7-4.

Table 7-14. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SYSREFREQ_VCM	R/W	0h	Sets the internal DC Bias for the SYSREFREQ pins. Bias must be enabled for AC-coupled inputs; but can be enabled and overdriven, or disabled, for DC-coupled inputs. SYSREFREQ DC pin voltage must be in the range of 0.7 V to VCC, including minimum and maximum signal swing. 0h = 1.3V 1h = 1.1V 2h = 1.5V 3h = Disabled
13	SYNC_EN	R/W	0h	Enables synchronization path for the dividers and allows the clock position capture circuitry to be enabled. Used for multi-device synchronization. Redundant if SYSREF_EN = 0x1.
12	LOGICLK_DIV_PD	R/W	0h	Disables the LOGICLK divider. LOGICLK pre-divider remains enabled. Used to reduce current consumption when bypassing the LOGICLK divider.
11	LOGICLK_DIV_BYP	R/W	0h	Bypasses the LOGICLK_DIV divider in order to derive the LOGICLK output directly from the LOGICLK_DIV_PRE divider. Should only be used when LOGICLK_DIV_PRE=1 as one of the steps to achieve a total divide of 1 for the LOGICLK. In order to aciheve a divde by 1, the following steps are required. 1. Set LOGICLK_DIV_PRE=1 2. Ensure that register R79 is programmed to a value of 0x0005 3. Program R90 to 0x0060 (LOGICLK_DIV23=1, LOGICLK_DIV_DCC=1) 4. Set LOGICLK_DIV_BYP=1 When not wanting a total divide of 1 for the LOGICLK, this bit should be set to 0. 0h = Engage LOGICLK divider 1h = Bypass LOGICLK divider
10	UNDISCLOSED	R/W	0h	Program this field to 0x0.
9-0	LOGICLK_DIV	R/W	20h	Sets LOGICLK divider value. Maximum input frequency from LOGICLK_DIV_PRE must be ≤ 3200 MHz. The maximum LOGICLKOUT frequency must be ≤ 800 MHz to avoid amplitude degradation. 0h = Reserved 1h = Reserved 2h = /2 3h = /3 3FFh = /1023

7.5.1.10 R11 Register (Offset = Bh) [Reset = 0000h]

R11 is shown in Table 7-15.

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Table 7-15. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_CLKPOS	R	0h	Stores a snapshot of the CLKIN signal rising edge positions relative to a SYSREFREQ rising edge, with the snapshot starting from the LSB and ending at the MSB. Each bit represents a sample of the CLKIN signal, separated by a delay determined by the SYSREFREQ_DLY_STEP field. The first and last bits of rb_CLKPOS are always set, indicating uncertainty at the capture window boundary conditions. CLKIN rising edges are represented by every sequence of two set bits from LSB to MSB, including bits at the boundary conditions. The position of the CLKIN rising edges in the snapshot, along with the CLKIN signal period and the delay step size, can be used to compute the value of SYSREFREQ_DLY which maximizes setup and hold times for SYNC signals on the SYSREFREQ pins.

7.5.1.11 R12 Register (Offset = Ch) [Reset = 0000h]

R12 is shown in Table 7-16.

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Table 7-16. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_CLKPOS[31:16]	R	0h	MSB of rb_CLKPOS field.

7.5.1.12 R13 Register (Offset = Dh) [Reset = 0003h]

R13 is shown in Table 7-17.

Return to the Table 7-4.

Table 7-17. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	UNDISCLOSED	R	0h	Program this field to 0x0.
1-0	SYSREFREQ_DLY_STEP	R/W	3h	Sets the step size of the delay element used in the SYSREFREQ path, both for SYSREFREQ input delay and for clock position captures. The recommended frequency range for each step size creates the maximum number of usable steps for a given CLKIN frequency. The ranges include some overlap to account for process and temperature variations. If the CLKIN frequency is covered by an overlapping span, larger delay step sizes improve the likelihood of detecting a CLKIN rising edge during a clock position capture. However, since larger values include more delay steps, larger step sizes have greater total delay variation across PVT relative to smaller step sizes. 0h = 28 ps (1.4GHz to 2.7GHz) 1h = 15 ps (2.4GHz to 4.7GHz) 2h = 11 ps (3.1GHz to 5.7GHz) 3h = 8 ps (4.5GHz to 12.8GHz)

7.5.1.13 R14 Register (Offset = Eh) [Reset = 0002h]

R14 is shown in Table 7-18.

Return to the Table 7-4.

Table 7-18. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.

Table 7-18. R14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SYNC_MUTE_PD	R/W	0h	Removes the mute condition on the SYSREFOUT and LOGISYSREFOUT pins during SYNC mode (SYSREFREQ_MODE = 0x0). Since the SYNC operation also resets the SYSREF dividers, the mute condition is usually desirable, and this bit can be left at the default value.
7-3	UNDISCLOSED	R/W	0h	Program this field to 0x0.
2	CLKPOS_CAPTURE_EN	R/W	0h	Enables the windowing circuit which captures the clock position in the rb_CLKPOS registers with respect to a SYSREF edge. The windowing circuit must be cleared by toggling SYSREFREQ_CLR high then low before a clock position capture. The first rising edge on the SYSREFREQ pins after clearing the windowing circuit triggers the capture. The capture circuitry greatly increases supply current, and does not need to be enabled to delay the SYSREFREQ signal in SYNC or SYSREF modes. Once the desired value of SYSREFREQ_DLY is determined, set this bit to 0x0 to minimize current consumption. If SYNC_EN = 0 and SYSREF_EN = 0, the value of this bit is ignored, and the windowing circuit is disabled.
1	SYSREFREQ_MODE	R/W	1h	Selects the function of the SYSREFREQ pins 0h = SYNC pin 1h = SYSREFREQ pin
0	SYSREFREQ_LATCH	R/W	0h	Latches the internal SYSREFREQ state to logic high on the first rising edge of the SYSREFREQ pins. This latch can be cleared by setting SYSREFREQ_CLR=1.

7.5.1.14 R15 Register (Offset = Fh) [Reset = 0B01h]

R15 is shown in Table 7-19.

Return to the Table 7-4.

Table 7-19. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R	0h	Program this field to 0x0.
11-10	SYSREF_DIV_PRE	R/W	2h	Sets the SYSREF pre-divider. Maximum output frequency must be ≤ 3.2GHz. 0h = /1 1h = /2 2h = /4 3h = Reserved
9	UNDISCLOSED	R/W	1h	Program this field to 0x1.
8	SYSREF_EN	R/W	1h	Enables SYSREF subsystem (and SYNC subsystem when SYSREFREQ_MODE = 0x0). Setting this bit to 0x0 completely disables all SYNC, SYSREF, and clock position capture circuitry, overriding the state of other powerdown/enable bits except SYNC_EN. If SYNC_EN = 0x1, the SYNC path and clock position capture circuitry are still enabled, regardless of the state of SYSREF_EN.
7	UNDISCLOSED	R/W	0h	Program this field to 0x0.

Table 7-19. R15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-1	SYSREFREQ_DLY	R/W	0h	Sets the delay line step for the external SYSREFREQ signal. Each delay line step delays the SYSREFREQ signal by an amount equal to SYSREFREQ_DELAY_STEP x SYSREFREQ_DLY_STEP. In SYNC mode, the value for this field can be determined based on the rb_CLKPOS value to satisfy the internal setup and hold time of the SYNC signal with respect to the CLKIN signal. In SYSREF Repeater Mode, the value for this field can be used as a coarse global delay. Values greater than 0x3F are invalid. Since larger values include more delay steps, larger values have greater total step size variation across PVT relative to smaller values. Refer to the data sheet or the device TICS Pro profile for detailed description of the delay step computation procedure.
0	SYSREFREQ_CLR	R/W	1h	Clears SYSREFREQ_LATCH and resets synchronization path timing for SYSREFREQ signal. Holding this bit high keeps internal SYSREFREQ signal low in all modes except SYSREF repeater mode, overriding the state of SYSREFREQ_FORCE. This bit must be set and cleared once before the SYNC or clock position capture operations are performed.

7.5.1.15 R16 Register (Offset = 10h) [Reset = 1005h]

R16 is shown in Table 7-20.

Return to the Table 7-4.

Table 7-20. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	SYSREF_PULSE_CNT	R/W	1h	Programs the number of pulses generated in pulser mode. The pulser is a counter gating the SYSREF divider; consequently, the pulse duration and frequency are equal to the duty cycle and frequency of the SYSREF divider output, respectively. 0h = Reserved 1h = 1 pulse 2h = 2 pulses Fh = 15 pulses
11-0	SYSREF_DIV	R/W	5h	Sets the SYSREF divider. Maximum input frequency from SYSREF_DIV_PRE must be ≤ 3200 MHz. Maximum output frequency must be ≤ 100 MHz. Odd divides (with duty cycle < 50%) are only allowed when the delay generators are bypassed. 0h = Reserved 1h = Reserved 2h = /2 3h = /3 FFFh = /4095

7.5.1.16 R17 Register (Offset = 11h) [Reset = 07F0h]

R17 is shown in Table 7-21.

Return to the Table 7-4.

Table 7-21. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R	0h	Program this field to 0x0.
10-4	SYSREF0_DLY_I	R/W	7Fh	Sets the delay step for the SYSREFOUT0 delay generator. Must satisfy SYSREFOUT0_DLY_I + SYSREFOUT0_DLY_Q = 127

Table 7-21. R17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	SYSREF0_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT0 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = ICLK 3h = QCLK
1-0	SYSREF_MODE	R/W	0h	Controls how the SYSREF signal is generated and is also impacted by the SYSREF_DLY_BYP field. Continuous mode generates a continuous SYSREF clock that is derived from the SYSREF divdier and delay. In pulser mode, a pulse at the SYSREFREQ pin causes a specifc number (determined by SYSREF_PULSE_CNT) of pulses to be generated for the SYSREF outputs. In Repeater mode, a pulse at the SYSREFREQ pins will generate a single pulse at the SYSREF outputs and only the propagation delay through the device is added. 0h = Continuous 1h = Pulser 2h = Repeater 3h = Reserved

7.5.1.17 R18 Register (Offset = 12h) [Reset = FE00h]

R18 is shown in Table 7-22.

Return to the Table 7-4.

Table 7-22. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	SYSREF1_DLY_I	R/W	7Fh	Sets the delay step for the SYSREFOUT0 delay generator. Must satisfy SYSREFOUT0_DLY_I + SYSREFOUT0_DLY_Q = 127
8-7	SYSREF1_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT1 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK
6-0	SYSREF0_DLY_Q	R/W	0h	Determines the strength of QCLK for delay generation. Must satisfy SYSREF0_DLY_I + SYSREF0_DLY_Q = 127

7.5.1.18 R19 Register (Offset = 13h) [Reset = FE00h]

R19 is shown in Table 7-23.

Return to the Table 7-4.

Table 7-23. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	SYSREF2_DLY_I	R/W	7Fh	Determines the strength of ICLK for delay generation. Must satisfy SYSREF2_DLY_I + SYSREF2_DLY_Q = 127
8-7	SYSREF2_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT2 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK
6-0	SYSREF1_DLY_Q	R/W	0h	Determines the strength of QCLK for delay generation. Must satisfy SYSREF1_DLY_I + SYSREF1_DLY_Q = 127

7.5.1.19 R20 Register (Offset = 14h) [Reset = FE00h]

R20 is shown in Table 7-24.

Return to the Table 7-4.

Table 7-24. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	SYSREF3_DLY_I	R/W	7Fh	Sets the delay step for the SYSREFOUT1 delay generator. Must satisfy SYSREFOUT1_DLY_I + SYSREFOUT1_DLY_Q = 127
8-7	SYSREF3_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT3 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK
6-0	SYSREF2_DLY_Q	R/W	0h	Determines the strength of QCLK for delay generation. Must satisfy SYSREF3_DLY_I + SYSREF3_DLY_Q = 127

7.5.1.20 R21 Register (Offset = 15h) [Reset = FE00h]

R21 is shown in Table 7-25.

Return to the Table 7-4.

Table 7-25. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	LOGISYSREF_DLY_I	R/W	7Fh	Determines the strength of logic ICLK for delay generation. Must satisfy LOGISYSREF_DLY_I+LOGISYSREF_DLY_Q = 127
8-7	LOGISYSREF_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the LOGISYSREFOUT delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK
6-0	SYSREF3_DLY_Q	R/W	0h	Determines the strength of QCLK for delay generation. Must satisfy SYSREFx_DLY_I + SYSREFx_DLY_Q = 127

7.5.1.21 R22 Register (Offset = 16h) [Reset = 0800h]

R22 is shown in Table 7-26.

Return to the Table 7-4.

Table 7-26. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SYSREF1_DLY_SCALE	R/W	0h	Sets the frequency range of the SYSREFOUT1 delay generator. Set according to phase interpolator frequency. 0h = 400MHz to 800MHz 1h = 200MHz to 400MHz 2h = 150MHz to 200MHz 3h = Reserved
13-12	SYSREF0_DLY_SCALE	R/W	0h	Sets the frequency range of the SYSREFOUT0 delay generator. Set according to phase interpolator frequency. 0h = 400MHz to 800MHz 1h = 200MHz to 400MHz 2h = 150MHz to 200MHz 3h = Reserved

Table 7-26. R22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	SYSREF_DLY_DIV	R/W	4h	Sets the delay generator clock division, determining the phase interpolator frequency and the delay generator resolution. Values other than those listed below are reserved. 0h = /1 (Up to 1.6GHz) 1h = /2 (1.6GHz to 3.2GHz) 2h = /4 (3.2GHz to 6.4GHz) 4h = /8 (6.4GHz to 12.8GHz)
8-7	UNDISCLOSED	R/W	0h	Program this field to 0x0.
6-0	LOGISYSREF_DLY_Q	R/W	0h	Sets the delay step for the LOGISYSREFOUT delay generator. Must satisfy LOGISYSREFOUT_DLY_I + LOGISYSREFOUT_DLY_Q = 127.

7.5.1.22 R23 Register (Offset = 17h) [Reset = 4000h]

R23 is shown in Table 7-27.

Return to the Table 7-4.

Table 7-27. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TS_EN	R/W	0h	Enables the on-die temperature sensor. Temperature sensor counter (TS_CNT_EN) must also be enabled for readback.
14	UNDISCLOSED	R/W	1h	Program this field to 0x1.
13	MUXOUT_EN	R/W	0h	Enables or tri-states the MUXOUT pin driver. 0h = Tri-States 1h = Push-Pull
12-7	UNDISCLOSED	R/W	0h	Program this field to 0x0.
6	MUXOUT_SEL	R/W	0h	Selects MUXOUT pin function. 0h = Lock Detect 1h = Readback
5-4	LOGISYSREF_DLY_SCALE	R/W	0h	Sets the frequency range of the LOGISYSREFOUT delay generator. Set according to phase interpolator frequency. 0h = 400MHz to 800MHz 1h = 200MHz to 400MHz 2h = 150MHz to 200MHz 3h = Reserved
3-2	SYSREF3_DLY_SCALE	R/W	0h	Sets the frequency range of the SYSREFOUT3 delay generator. Set according to phase interpolator frequency. 0h = 400MHz to 800MHz 1h = 200MHz to 400MHz 2h = 150MHz to 200MHz 3h = Reserved
1-0	SYSREF2_DLY_SCALE	R/W	0h	Sets the frequency range of the SYSREFOUT2 delay generator. Set according to phase interpolator frequency. 0h = 400MHz to 800MHz 1h = 200MHz to 400MHz 2h = 150MHz to 200MHz 3h = Reserved

7.5.1.23 R24 Register (Offset = 18h) [Reset = 0000h]

R24 is shown in Table 7-28.

Return to the Table 7-4.

Table 7-28. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	UNDISCLOSED	R	0h	Program this field to 0x0.
13-12	UNDISCLOSED	R/W	0h	Program this field to 0x0.
11-1	rb_TS	R	0h	Readback value of on-die temperature sensor.
0	TS_CNT_EN	R/W	0h	Enables temperature sensor counter. Temperature sensor (EN_TS) must be enabled for accurate data.

7.5.1.24 R25 Register (Offset = 19h) [Reset = 0211h]

R25 is shown in Table 7-29.

Return to the Table 7-4.

Table 7-29. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	UNDISCLOSED	R/W	4h	Program this field to 0x4.
6	CLK_DIV_RST	R/W	0h	Resets the main clock divider. If the clock divider value is changed during operation, set this bit high then low after setting the new divider value. Synchronizing the device with the SYSREFREQ pins in SYSREFREQ_MODE = 0x0 and SYNC_EN = 0x1 also resets the main clock divider. This bit has no effect when outside of Divider Mode.
5-3	CLK_DIV	R/W	2h	CLK_DIV and CLK_MULT are aliases for the same field. When CLK_MUX=1 (Buffer Mode), this field is ignored. When CLK_MUX = 2 (Divider Mode), the clock divider is CLK_DIV + 1. Valid range for CLK_DIV is 1 to 7. Setting this to 0 disables the main clock divider and reverts to buffer mode. When CLK_MUX = 3 (Multiplier Mode), CLK_MULT the multiplier vaue is CLK_MULT. Valid range is 1 to 4. Setting outside this range disables multiplier mode and reverts to buffer mode. Valid range is 0x1 to 0x4.
2-0	CLK_MUX	R/W	1h	Selects the function for the main clock outputs 0h = Reserved 1h = Buffer 2h = Dividers 3h = Multiplier

7.5.1.25 R28 Register (Offset = 1Ch) [Reset = 0A08h]

R28 is shown in Table 7-30.

Return to the Table 7-4.

Table 7-30. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	UNDISCLOSED	R	0h	Program this field to 0x0.
12	VCO_CORE_FORCE	R/W	0h	Forces the multiplier PLL's VCO to the value selected by VCO_CORE. Not required for Multiplier Mode programming, but can optionally be used to reduce calibration time.
11-9	VCO_CORE	R/W	5h	When VCO_CORE_FORCE=0, specifies start VCO for multiplier calibration. When VCO_CORE_FORCE=1, this VCO core is forced. Programming of this field is not required for Multiplier Mode programming, but can be used to debugging purposes or to reduce calibration time.
8-0	UNDISCLOSED	R/W	8h	Program this field to 0x8.

7.5.1.26 R29 Register (Offset = 1Dh) [Reset = 05FFh]

R29 is shown in Table 7-31.

Return to the Table 7-4.

Table 7-31. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	UNDISCLOSED	R	0h	Program this field to 0x0.
12-8	UNDISCLOSED	R/W	5h	Program this field to 0x5.
7-0	VCO_CAPCTRL	R/W	FFh	Sets the starting value for the VCO tuning capacitance during multiplier calibration. Not required for Multiplier Mode programming, but can be used to reduce calibration time.

7.5.1.27 R33 Register (Offset = 21h) [Reset = 7777h]

R33 is shown in Table 7-32.

Return to the Table 7-4.

Table 7-32. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UNDISCLOSED	R/W	7777h	Program this field to 0x6666. Note that this is different than the reset value.

7.5.1.28 R34 Register (Offset = 22h) [Reset = 0007h]

R34 is shown in Table 7-33.

Return to the Table 7-4.

Table 7-33. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	UNDISCLOSED	R	0h	Program this field to 0x0.
13-0	UNDISCLOSED	R/W	7h	Program this field to 0x5. Note that this is different than the reset value.

7.5.1.29 R65 Register (Offset = 41h) [Reset = 65F0h]

R65 is shown in Table 7-34.

Return to the Table 7-4.

Table 7-34. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	32h	Program this field to 0x32.
8-4	rb_VCO_CORE	R	1Fh	Readback for the multiplier VCO Core. There are only valid values and the VCO is determined by the bit that is low. Fh = VCO1 17h = VCO2 1Bh = VCO3 1Dh = VCO4 1Eh = VCO5
3-0	UNDISCLOSED	R/W	0h	Program this field to 0x0.

7.5.1.30 R67 Register (Offset = 43h) [Reset = 50C8h]

R67 is shown in Table 7-35.

Return to the Table 7-4.

Table 7-35. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UNDISCLOSED	R/W	50C8h	Program this field to 0x51CB. Note that this is different than the reset value.

7.5.1.31 R72 Register (Offset = 48h) [Reset = 0000h]

R72 is shown in Table 7-36.

Return to the Table 7-4.

Table 7-36. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14-3	UNDISCLOSED	R/W	0h	Program this field to 0x0.
2	SYSREFREQ_FORCE	R/W	0h	Setting this bit emulates the behavior of a logic HIGH at SYSREFREQ pins and causes external signals on SYSREFREQ pins to be ignored.
1-0	SYSREF_DLY_BYP	R/W	0h	Option to bypass delay generator retiming. Under normal circumstances (SYSREF_DLY_BYP = 0) the delay generator is engaged for continuous or pulser modes (Generator Modes), and bypassed in Repeater Mode. Generally this ctypically utilize a different delay mechanism. In certain cases, bypassing the delay generator retiming in Generator Mode by setting SYSREF_DLY_BYP = 1 can substantially reduce the device current consumption if the SYSREF delay can be compensated at the JESD receiver. In other cases, retiming the SYSREFREQ signal to the delay generators by setting SYSREF_DLY_BYP = 2 can improve the accuracy of the SYSREF output phase with respect to the CLKIN phase, or can vary the delay of individual outputs independently, as long as coherent phase relationship exists between the interpolator divider phase and the SYSREFREQ phase. 0h = Engage in Generator Mode, Bypass in Repeater Mode 1h = Bypass in All Modes 2h = Engage in All Modes 3h = Reserved

7.5.1.32 R73 Register (Offset = 49h) [Reset = 0000h]

R73 is shown in Table 7-37.

Return to the Table 7-4.

Table 7-37. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	UNDISCLOSED	R	0h	Program this field to 0x0.
12-0	UNDISCLOSED	R/W	0h	Program this field to 0x1000. Note that this is different than the reset value.

7.5.1.33 R75 Register (Offset = 4Bh) [Reset = 0006h]

R75 is shown in Table 7-38.

Return to the Table 7-4.

Table 7-38. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	rb_CLK2_EN	R	0h	Readback Pin Status
14	rb_CLK1_EN	R	0h	Readback Pin Status
13	rb_CLK0_EN	R	0h	Readback Pin Status
12	rb_MUXSEL1	R	0h	Readback Pin Status
11	rb_MUXSEL0	R	0h	Readback Pin Status
10	rb_LOGIC_EN	R	0h	Readback Pin Status
9-8	rb_LD	R	0h	Readback for Multiplier PLL lock detect. 0h = Unlocked (VTUNE low) 1h = Reserved 2h = Locked 3h = Unlocked (VTUNE high)
7	rb_DIVSEL2	R	0h	Readback Pin Status
6	rb_DIVSEL1	R	0h	Readback Pin Status
5	rb_DIVSEL0	R	0h	Readback Pin Status
4	rb_CE	R	0h	Readback Pin Status
3-0	UNDISCLOSED	R/W	6h	Program this field to 0x3. Note that this is different than the reset value.

7.5.1.34 R76 Register (Offset = 4Ch) [Reset = 0000h]

R76 is shown in Table 7-39.

Return to the Table 7-4.

Table 7-39. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	UNDISCLOSED	R/W	0h	Program this field to 0x0.
3	rb_PWRSEL2	R	0h	Readback Pin Status
2	rb_PWRSEL1	R	0h	Readback Pin Status
1	rb_PWRSEL0	R	0h	Readback Pin Status
0	rb_CLK3_EN	R	0h	Readback Pin Status

7.5.1.35 R86 Register (Offset = 56h) [Reset = 0000h]

R86 is shown in Table 7-40.

Return to the Table 7-4.

Table 7-40. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	UNDISCLOSED	R/W	0h	Program this field to 0x0.
2	MUXOUT_EN_OVRD	R/W	0h	No description
1-0	UNDISCLOSED	R/W	0h	Program this field to 0x0.

7.5.1.36 R90 Register (Offset = 5Ah) [Reset = 0000h]

R90 is shown in Table 7-41.

Return to the Table 7-4.

Table 7-41. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	UNDISCLOSED	R	0h	Program this field to 0x0.
7	UNDISCLOSED	R/W	0h	Program this field to 0x0.
6	LOGICLK_DIV_BYP3	R/W	0h	This bit should be set to 1 if LOGICLK_DIV_BYP=1, 0 otherwise.
5	LOGICLK_DIV_BYP2	R/W	0h	This bit should be set to 1 if LOGICLK_DIV_BYP=1, 0 otherwise.
4-0	UNDISCLOSED	R/W	0h	Program this field to 0x0.

8 Device and Documentation Support

8.1 Device Support

TI offers an extensive line of development tools and software to simulate the device performance and program the device.

Table 8-1. Development Tools and Software

TOOL	TYPE	DESCRIPTION
PLLatinum™ Sim	Software	Simulates phase noise in all modes
TICS Pro	Software	Programs the device with a user-friendly GUI with interactive feedback and hex register export.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *LMX1860-SEP Evaluation Module* , EVM user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

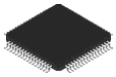
DATE	REVISION	NOTES
June 2024	*	Initial release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

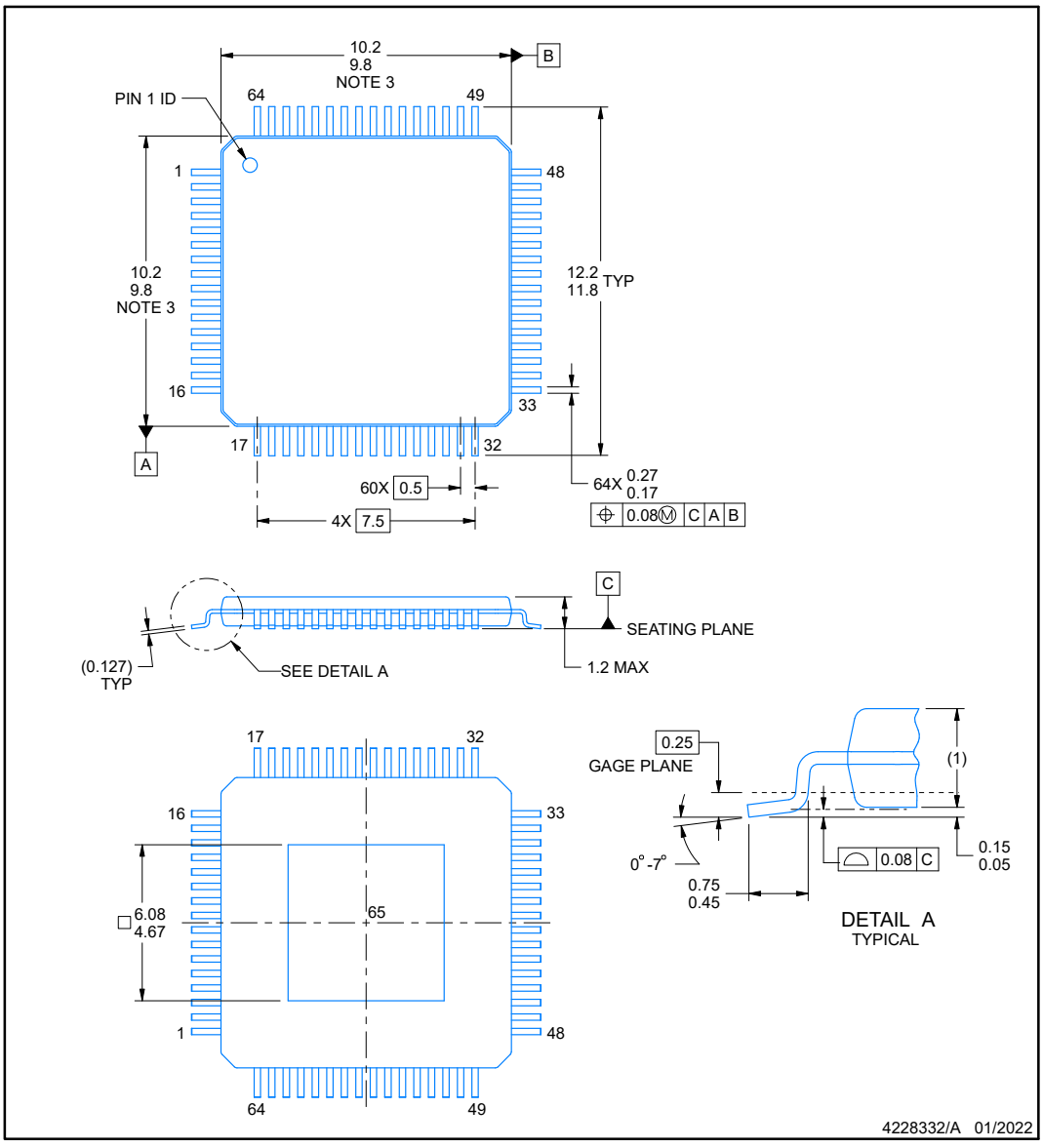
PACKAGE OUTLINE

PAP0064E



PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES:

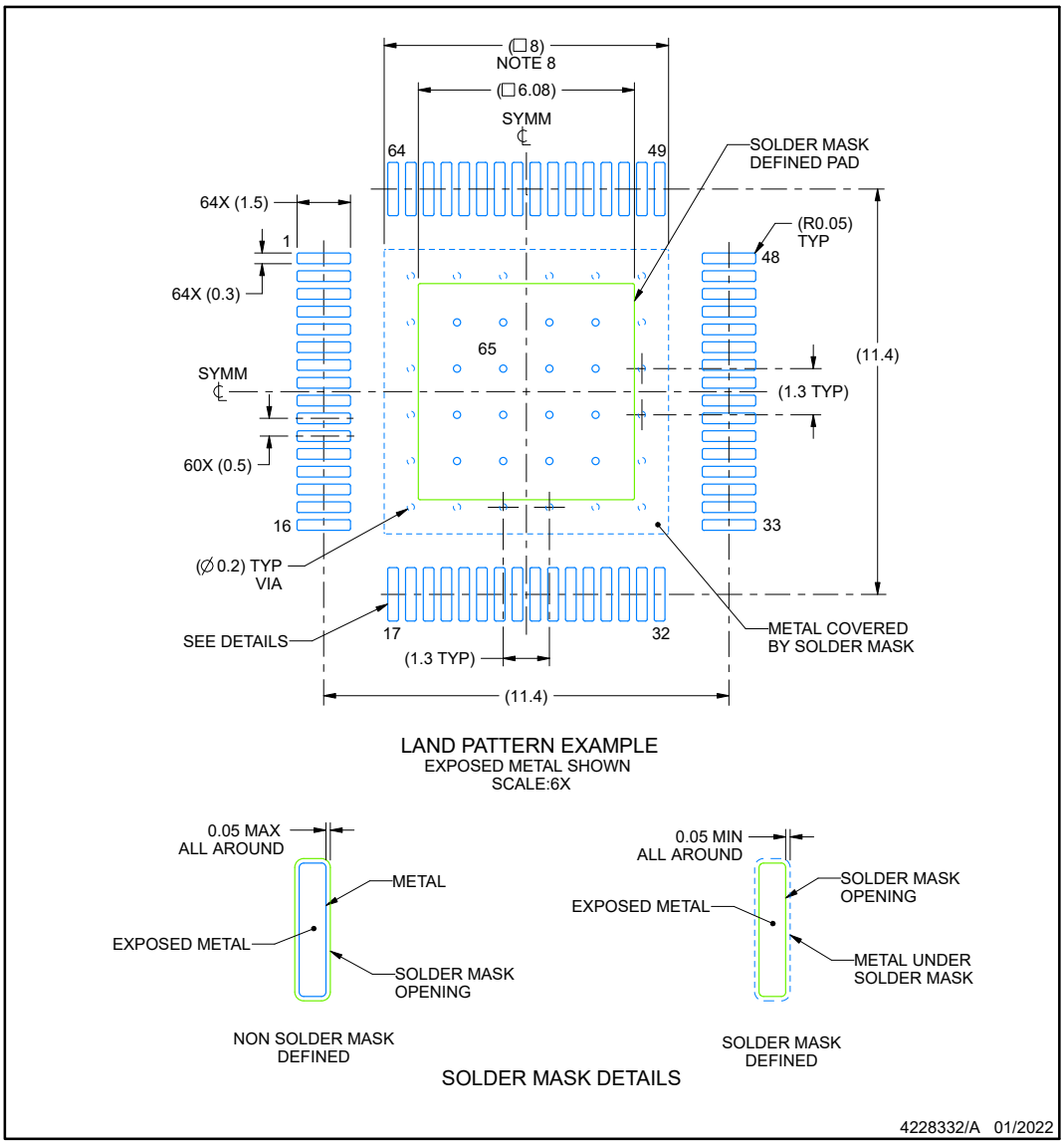
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PAP0064E — **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



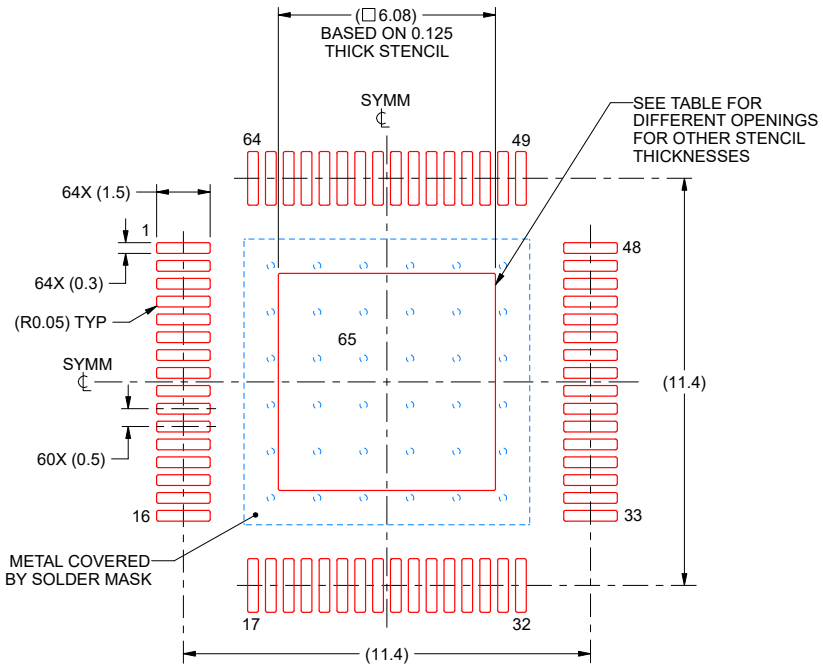
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PAP0064E — **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.80 X 6.80
0.125	6.08 X 6.08 (SHOWN)
0.15	5.55 X 5.55
0.175	5.14 X 5.14

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX1860MPAPSEP	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	LMX1860 (MPAPSEP, PAPSEP)	Samples
LMX1860PAP/EM	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	LMX1860 PAP/EM	Samples
V62/24630-01XE	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	LMX1860 (MPAPSEP, PAPSEP)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

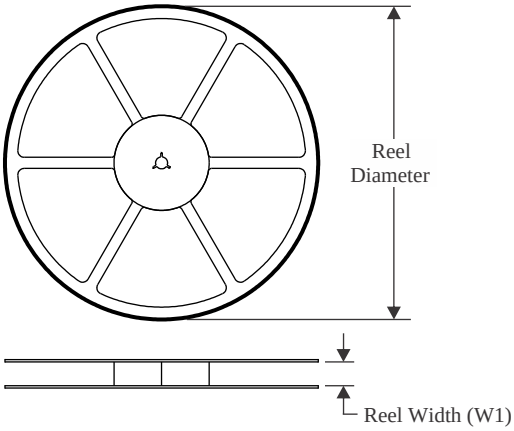
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

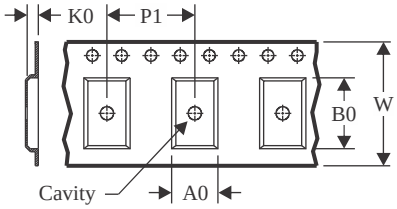
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

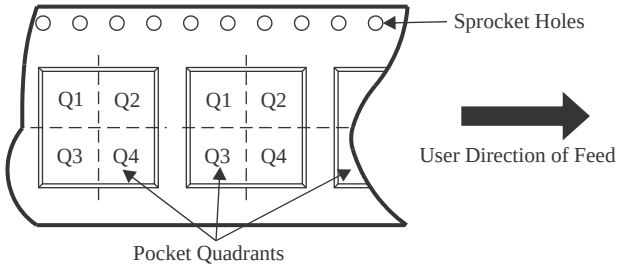


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

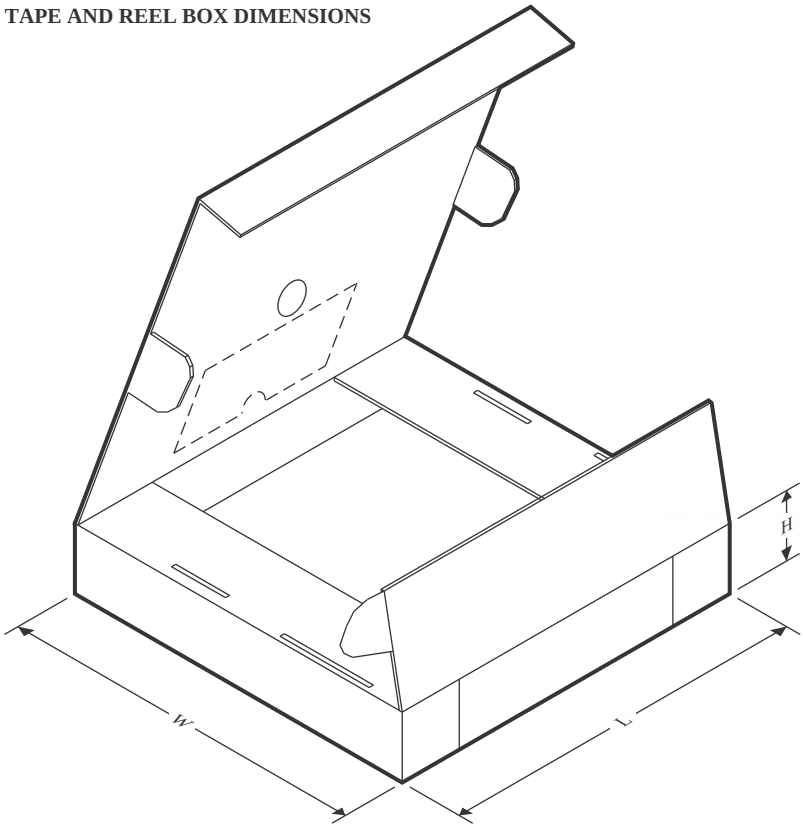
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

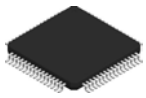
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX1860PAP/EM	HTQFP	PAP	64	250	178.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX1860PAP/EM	HTQFP	PAP	64	250	213.0	191.0	55.0

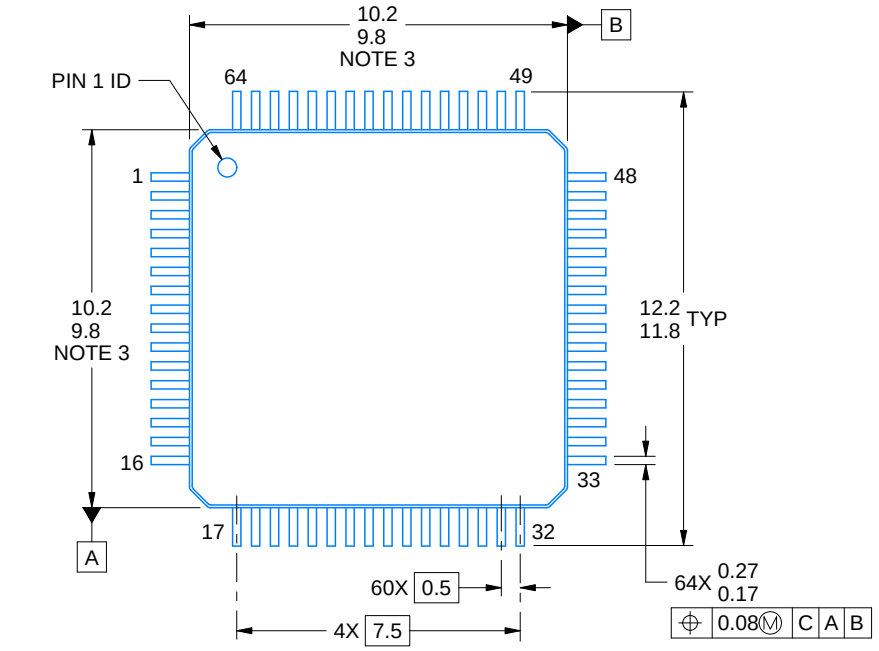


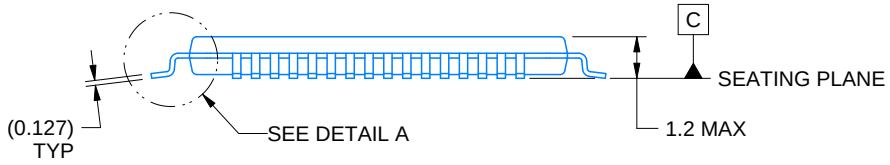
PACKAGE OUTLINE

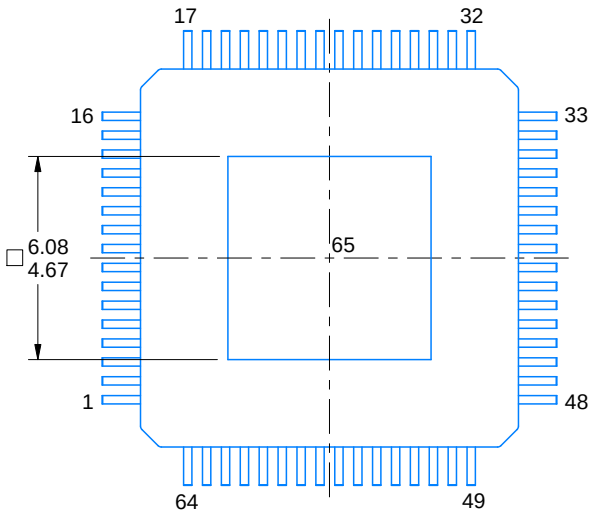
PAP0064E

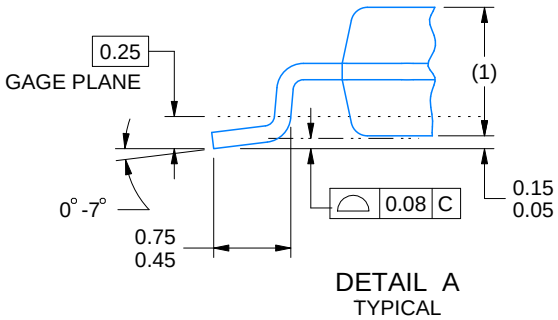
PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK









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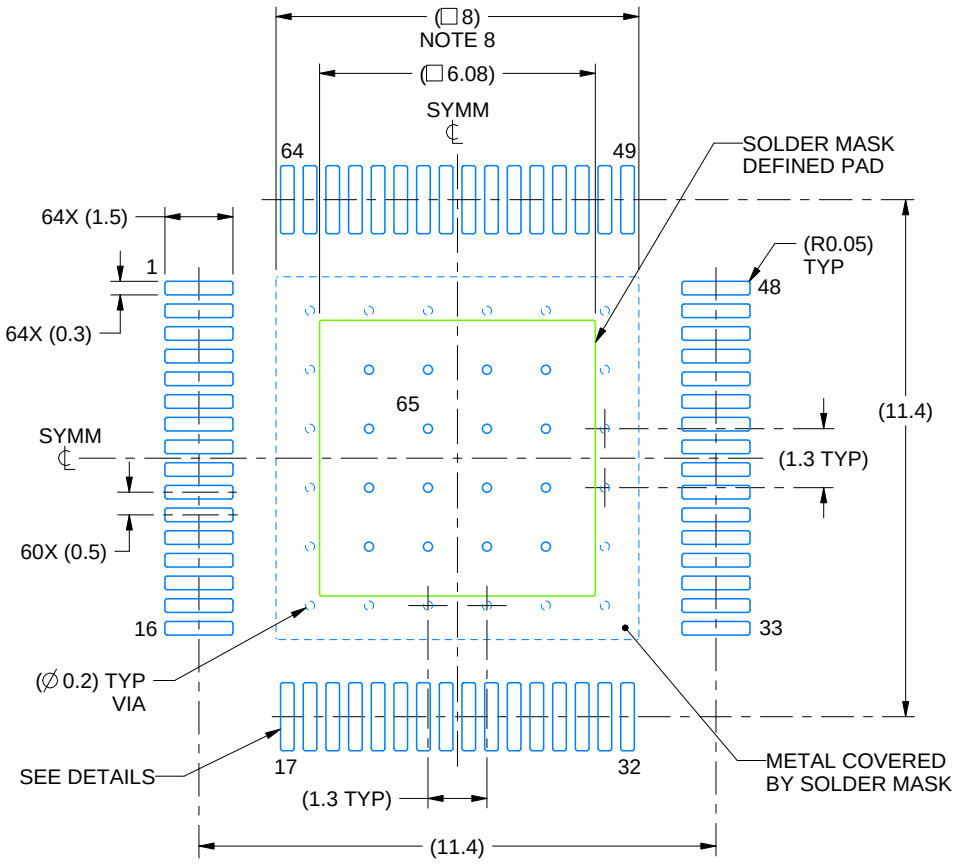
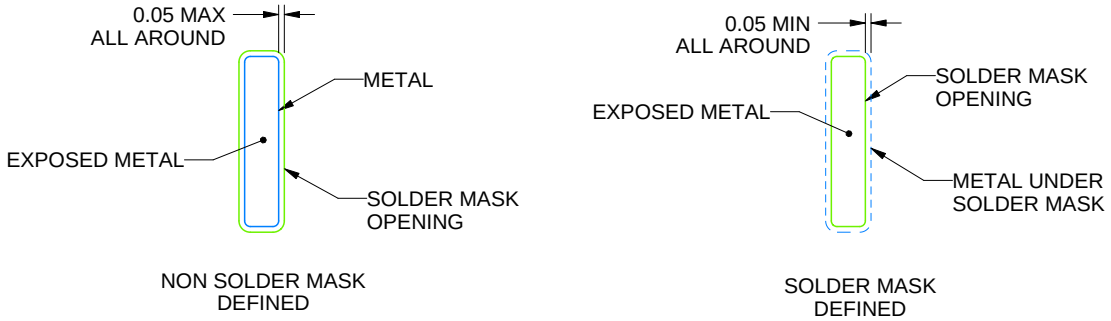
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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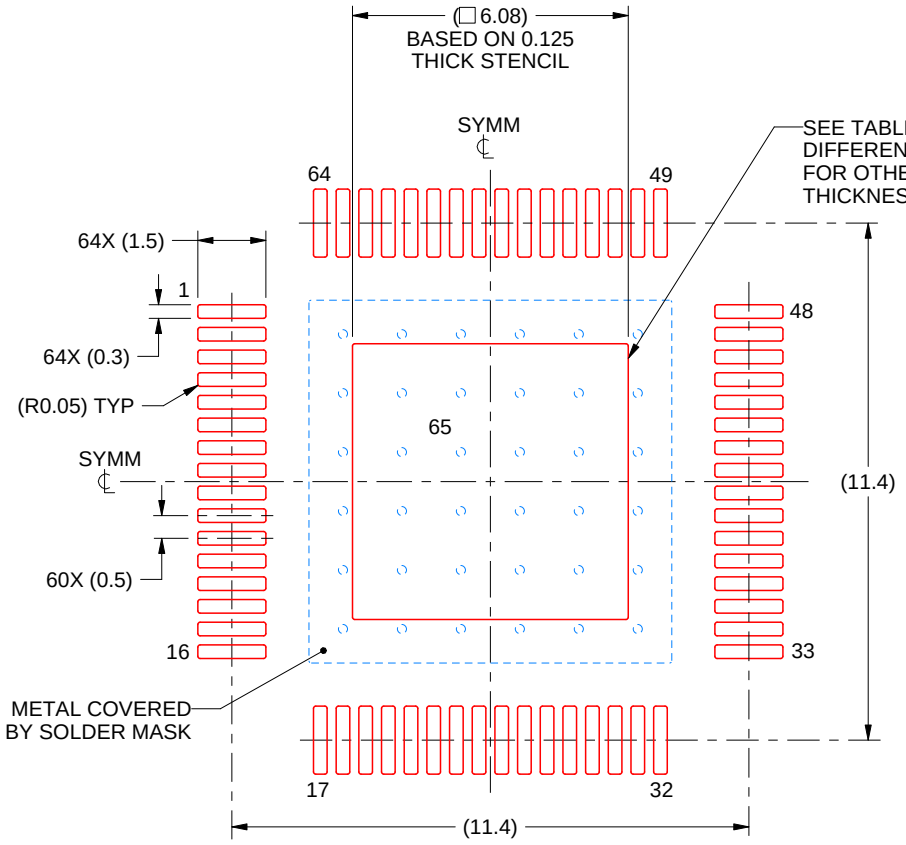
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.80 X 6.80
0.125	6.08 X 6.08 (SHOWN)
0.15	5.55 X 5.55
0.175	5.14 X 5.14

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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