MSPM0C1105-Q1, MSPM0C1106-Q1 Automotive Mixed-Signal Microcontrollers

1 Features

- AEC-Q100 Grade 1 qualified for automotive applications
- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU with memory protection unit, frequency up to 32MHz
- **Operating characteristics**
  - Extended temperature: –40°C up to 125°C
  - Wide supply voltage range: 1.62V to 3.6V
- **Memories**
  - Up to 64KB of flash memory
  - 8KB of SRAM
- **High-performance analog peripherals**
  - 12-bit 1.6 Msps analog-to-digital converter (ADC), up to 27 external channels
  - Configurable 1.4V or 2.5V internal shared voltage reference (VREF)
  - Comparator (COMP) with 8-bit reference DAC
  - Integrated temperature sensor
- **Optimized low-power modes**
  - RUN: 93µA/MHz (CoreMark)
  - STANDBY 2µA and SRAM and registers fully retained
  - SHUTDOWN: 63nA with I/O wake-up
- **Intelligent digital peripherals**
  - 3-channel DMA controller
  - 7-channel event fabric signaling system
  - Five timers supporting up to 18 PWM outputs, all operational down to STANDBY mode
    - One 16-bit advanced timer with deadband and the timer frequency up to 64Mhz
    - One 16-bit general purpose timer with 4 capture/compares
    - Three 16-bit general-purpose timers with 2 capture/compares
  - Window-watchdog timer (WWDT)
  - Independent watchdog timer (IWDT)
  - RTC with alarm and calendar mode
  - BEEPER generating 1/2/4/8kHz square wave to drive an external beeper
- **Communication interfaces**
  - Three UART modules, with one supporting LIN, IrDA, DALI, smart card, Manchester
  - Two I^2C modules supporting SMBus/PMBus and wakeup from STOP mode, supporting up to FM+ (1Mbps)
  - One SPI module supporting up to 16Mbps
- **Clock system**
  - Internal 32MHz oscillator with -2.1% to 1.6% accuracy (SYSOSC)
  - Internal 32kHz oscillator (LFOSC) with ±3% accuracy
  - External 4MHz to 32MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator (LFXT)
  - External Low Frequency (LF) and High Frequency (HF) digital clock inputs
  - Digital clock output
- **Data integrity and encryption**
  - Cyclic redundancy checker (CRC-16)
- **Flexible I/O features**
  - Up to 45 total GPIOs
  - Two 5V-tolerant open-drain IOs
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options** [1]
  - 48-pin LQFP (PT), VQFN (RGZ)
  - 32-pin VQFN (RHB), VSSOP (DGS32)
  - 28-pin VSSOP (DGS28)
  - 24-pin VQFN (RGE)
  - 20-pin WQFN (RUK), VSSOP (DGS20)
- **Family members** (also see *Device Comparison*)
  - MSPM0C1106-Q1: 64KB of flash, 8KB of RAM
  - MSPM0C1105-Q1: 32KB of flash, 8KB of RAM
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0C1106 LaunchPad™ development kit
  - MSP Software Development Kit (SDK)

2 Applications

- Automotive body electronics and Lighting
- Automotive Gateway
- Steering Wheel Systems
- Automotive Motor Control
- DC to AC Inverters
- Automotive Interior Lighting
- Door handle modules
- Kick to open modules
- Vehicle Occupancy Detection
- Seat Comfort Module

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[1] QFN packages have wettable flanks.

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3 Description

MSPM0C1105/6 microcontrollers (MCUs) are part of MSP's highly integrated, ultra-low-power 32-bit MSPM0 MCU family based on the Arm® Cortex®-M0+ 32-bit core platform, operating at up to 32MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 1.62V to 3.6V.

The MSPM0C1105/6 devices provide up to 64KB embedded flash program memory with 8KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy from -2.1% to +1.6%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.6 Msps ADC with VDD as the voltage reference, a comparator with 8-bit reference DAC and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as one 16-bit advanced timer with deadband and timer frequency up to 64MHz, four 16-bit general purpose timer, one windowed watchdog timer, and a variety of communication peripherals including three UART, one SPI, and two I2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers to find the MCU that meets the project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0C1105/6 MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

Table 3-1. Package Information

DEVICE NAME	PACKAGE(1)	PACKAGE SIZE(2)
M0C1106QPTRQ1	48 LQFP	9mm × 9mm
M0C1105QPTRQ1	48 LQFP	9mm × 9mm
M0C1106QRGZRQ1	48 VQFN	7mm × 7mm
M0C1105QRGZRQ1	48 VQFN	7mm × 7mm
M0C1106QRHBRQ1	32 VQFN	5mm × 5mm
M0C1105QRHBRQ1	32 VQFN	5mm × 5mm
M0C1106QDGS32RQ1	32 VSSOP	8.1mm × 4.9mm
M0C1105QDGS32RQ1	32 VSSOP	8.1mm × 4.9mm
M0C1106QDGS28RQ1	28 VSSOP	7.1mm × 4.9mm
M0C1105QDGS28RQ1	28 VSSOP	7.1mm × 4.9mm
M0C1106QRGERQ1	24 VQFN	4mm × 4mm
M0C1105QRGERQ1	24 VQFN	4mm × 4mm
M0C1106QDGS20RQ1	20 VSSOP	5.1mm × 4.9mm
M0C1105QDGS20RQ1	20 VSSOP	5.1mm × 4.9mm
M0C1106QRUKRQ1	20 WQFN	3mm × 3mm
M0C1105QRUKRQ1	20 WQFN	3mm × 3mm

(1) For more information, see Mechanical, Packaging, and Orderable Information
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM0 MCUs.

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4 Functional Block Diagram

Figure 4-1 shows the functional block diagram.

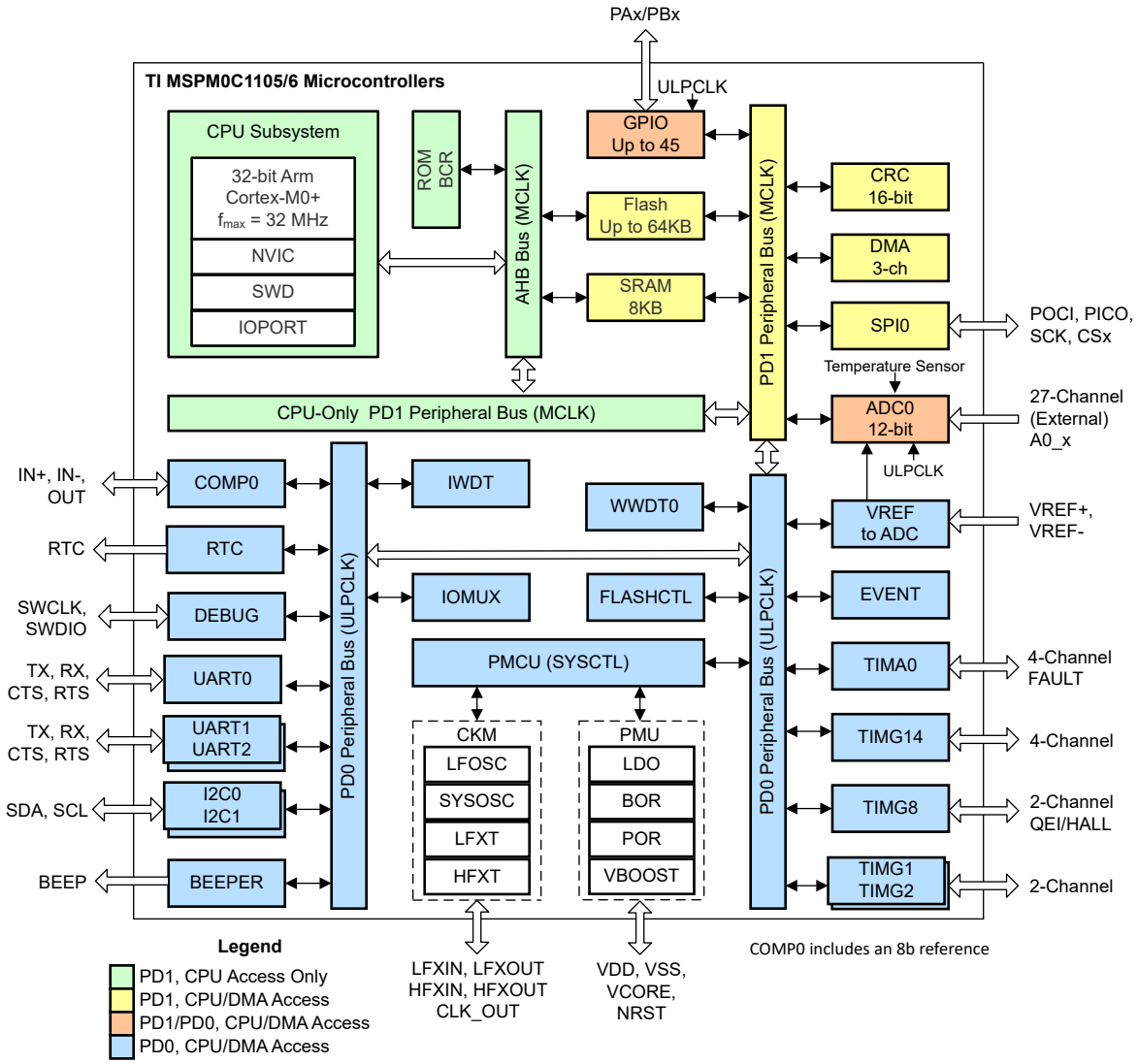

Figure 4-1. MSPM0C1105/6 Functional Block Diagram

5 Device Comparison

Table 5-1. Device Comparison Table

DEVICE NAME	FLASH / SRAM (KB)	ADC CHANNEL	UART / I2C / SPI	TIMG	TIMA	GPIO	COMP	PACKAGE
M0C1106QPTRQ1	64 / 8	27	3 /2 / 1	4	1	45	1	48 LQFP (9mm × 9mm)
M0C1105QPTRQ1	32 / 8							
M0C1106QRGZRQ1	64 / 8	27	3 /2 / 1	4	1	45	1	48 VQFN (7mm × 7mm)
M0C1105QRGZRQ1	32 / 8							
M0C1106QRHBRQ1	64 / 8	18	3 /2 / 1	4	1	29	1	32 VQFN (5mm × 5mm)
M0C1105QRHBRQ1	32 / 8							
M0C1106QDGS32RQ1	64 / 8	18	3 /2 / 1	4	1	29	1	32 VSSOP (8.1mm × 4.9mm)
M0C1105QDGS32RQ1	32 / 8							
M0C1106QDGS28RQ1	64 / 8	15	3 /2 / 1	4	1	25	1	28 VSSOP (7.1mm × 4.9mm)
M0C1105QDGS28RQ1	32 / 8							
M0C1106QRGERQ1	64 / 8	13	3 /2 / 1	4	1	21	1	24 VQFN (4mm × 4mm)
M0C1105QRGERQ1	32 / 8							
M0C1106QDGS20RQ1	64 / 8	12	3 /2 / 1	4	1	17	1	20 VSSOP (5.1mm × 4.9mm)
M0C1105QDGS20RQ1	32 / 8							
M0C1106QRUKRQ1	64 / 8	12	3 /2 / 1	4	1	17	1	20 WQFN (3mm × 3mm)
M0C1105QRUKRQ1	32 / 8							

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6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The pin diagrams shown in the data sheet show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout.

For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

Note

For full pin configuration and functions for each package option, refer to Pin Attributes and Signal Descriptions.

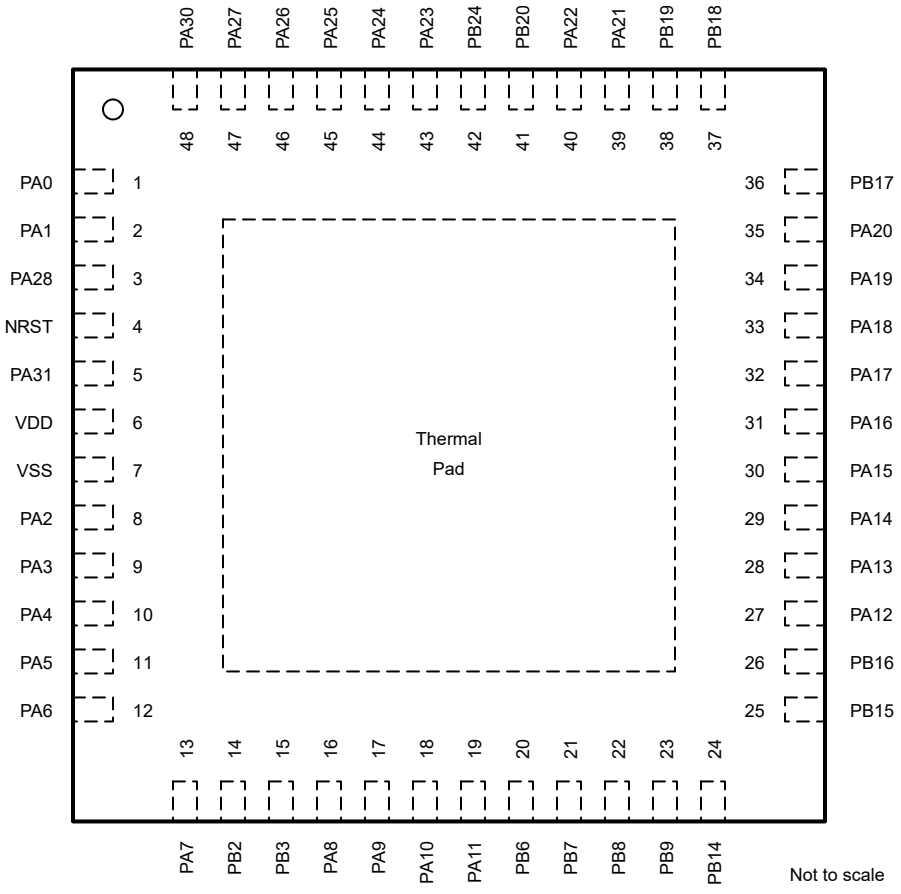

Figure 6-1. 48-pin RGZ (VQFN) Package

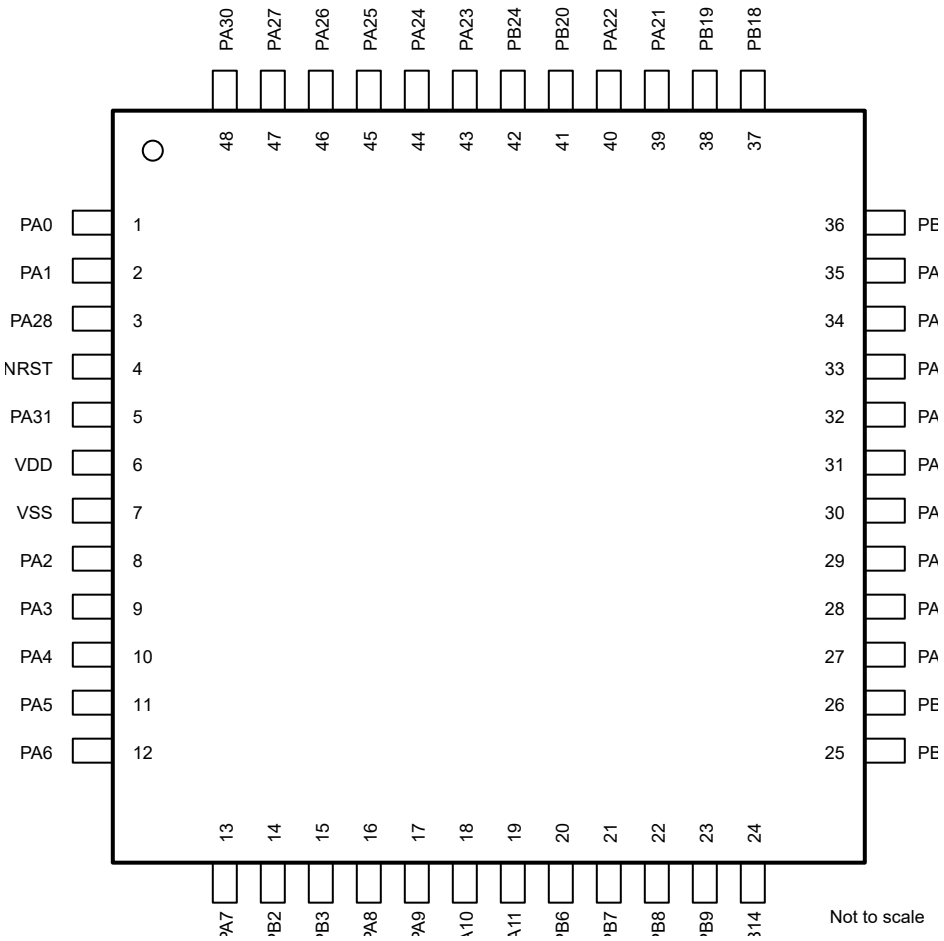

Figure 6-2. 48-pin PT (LQFP) Package

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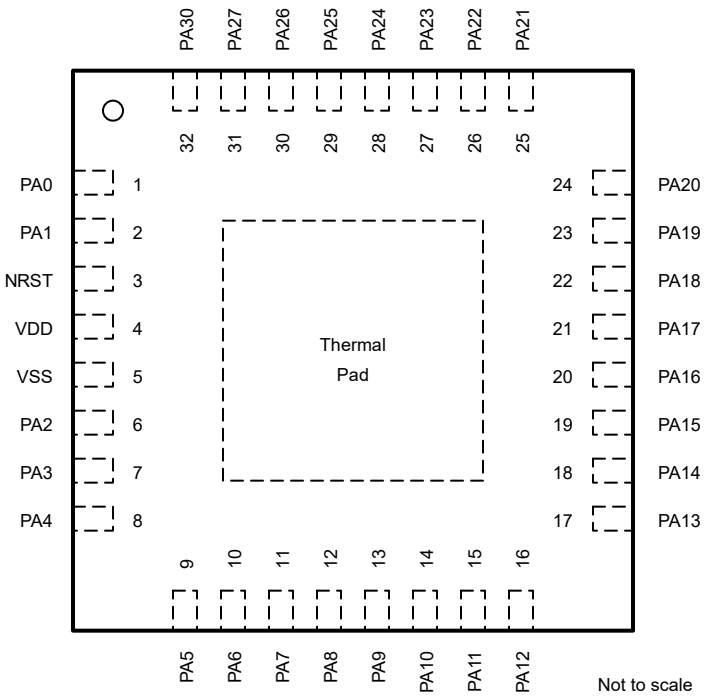

Figure 6-3. 32-pin RHB (VQFN) Package

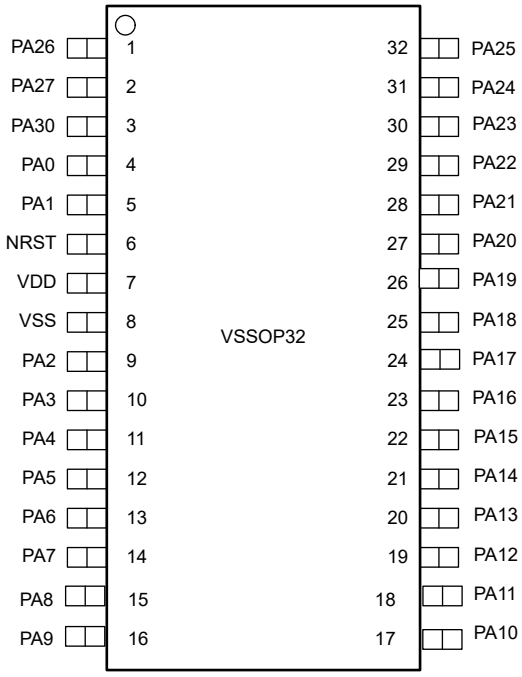

Figure 6-4. 32-pin DGS32 (VSSOP)

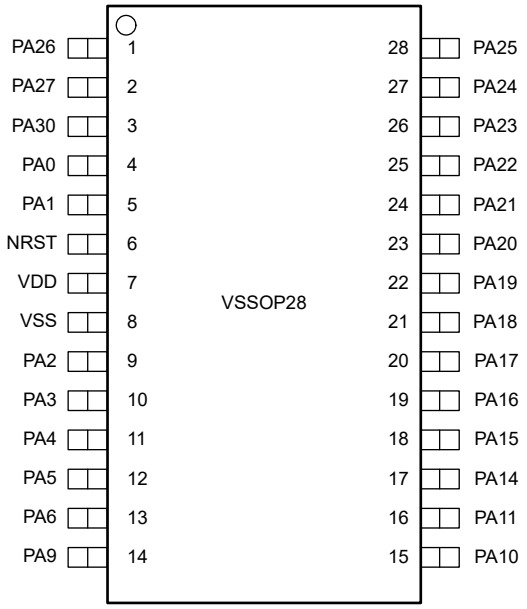

Figure 6-5. 28-pin DGS28 (VSSOP)

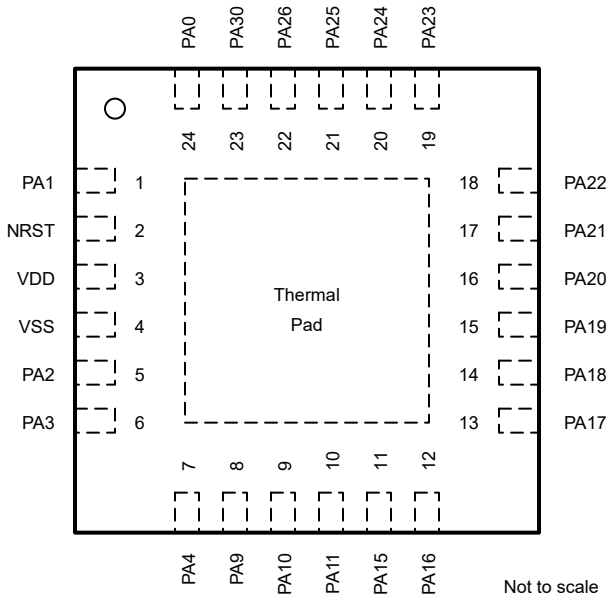

Figure 6-6. 24-pin RGE (VQFN) Package

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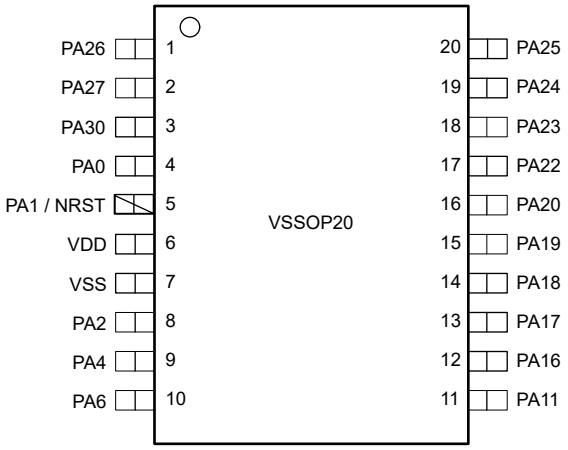

Figure 6-7. 20-pin DGS20 (VSSOP)

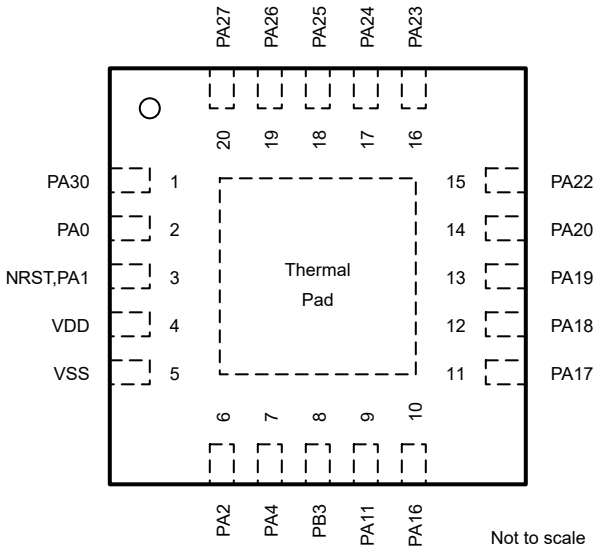

Figure 6-8. 20-pin RUK (WQFN)

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
SDIO (standard drive)	Y			Y	Y	
SDIO (standard drive) with wake1	Y			Y	Y	Y
ODIO (5V-tolerant open drain)	Y		Y		Y	Y

1. Standard with Wake allows the I/O to wake up the device from the lowest low-power mode of SHUTDOWN. All I/O can be configured to wakeup the MCU from higher low-power modes. See section *GPIO FastWake* in the MSPM0 C-Series Microcontrollers Technical Reference Manual for details.

Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
4	4	3	6	6	2	5	3	NRST	NRST	(Non-IOMUX 1) 0	RESET	RESET
1	1	1	4	4	24	4	2	PA0 PINCM1 0x40428000	PA0	1	IO	ODIO (5V-tol)with wake
									UART0_TX	2	O	
									I2C0_SDA	3	IOD	
									TIMA0_C0	4	IO	
									TIMA_FAL1	5	I	
									FCC_IN	6	I	
									TIMG8_C1	7	IO	
									BEEP	8	O	
									TIMG14_C0	9	IO	
									SPI0_CS1_MISO 1	10	IO	
									RTC_OUT	12	O	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
2	2	2	5	5	1	5	3	PA1 PINCM2 0x40428004	PA1	1	IO	ODIO (5V-tol)with wake
									UART0_RX	2	IO	
									I2C0_SCL	3	IOD	
									TIMA0_C1	4	IO	
									TIMA_FAL2	5	I	
									TIMG8_IDX	6	I	
									TIMG8_C0	7	IO	
									TIMG14_C1	9	IO	
									SPI0_CS3_CD_MISO3	10	IO	
									HFCLKIN	11	I	
									UART0_TX	12	O	
									UART1_RTS	13	O	
									I2C0_SDA	14	IOD	
8	8	6	9	9	5	8	6	PA2 PINCM5 0x40428010	PA2	1	IO	SDIO (standard)
									TIMG8_C1	2	IO	
									SPI0_CS0	3	IO	
									TIMG2_C1	4	IO	
									TIMG8_IDX	5	I	
									TIMA0_C3N	6	O	
									TIMA0_C2N	7	O	
									TIMA_FAL0	8	I	
									TIMA_FAL1	9	I	
									TIMA0_C0	11	IO	
									I2C0_SCL	12	IOD	
9	9	7	10	10	6			PA3 PINCM6 0x40428014	PA3	1	IO	SDIO (standard)
									TIMG8_C0	2	IO	
									SPI0_CS1_MISO1	3	IO	
									I2C1_SDA	4	IOD	
									TIMA0_C1	5	IO	
									TIMG2_C0	7	IO	
									TIMA0_C2	8	IO	
									UART2_CTS	9	I	
									UART1_TX	10	O	
									SPI0_CS3_CD_MISO3	11	IO	
									I2C0_SDA	12	IOD	
									COMP0_OUT	14	O	
									LFXIN	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
10	10	8	11	11	7	9	7	PA4 PINCM7 0x40428018	PA4	1	IO	SDIO (standard)
									TIMG8_C1	2	IO	
									SPI0_POCI	3	IO	
									I2C1_SCL	4	IOD	
									TIMA0_C1N	5	O	
									LFCLKIN	6	I	
									TIMG2_C1	7	IO	
									TIMA0_C3	8	IO	
									UART2_RTS	9	O	
									UART1_RX	10	I	
									SPI0_CS0	11	IO	
									TIMA0_C0N	12	O	
									HFCLKIN	13	I	
									LFXOUT	(Non-IOMUX 1) 0	A	
11	11	9	12	12				PA5 PINCM8 0x4042801c	PA5	1	IO	SDIO (standard)
									TIMG8_C0	2	IO	
									SPI0_PICO	3	IO	
									I2C1_SDA	4	IOD	
									TIMG14_C0	5	IO	
									FCC_IN	6	I	
									TIMG1_C0	7	IO	
									TIMA_FAL1	8	I	
									UART0_CTS	9	I	
									UART1_TX	11	O	
									TIMA0_C1	12	IO	
									HFXIN	(Non-IOMUX 1) 0	A	
12	12	10	13	13		10		PA6 PINCM9 0x40428020	PA6	1	IO	SDIO (standard)
									TIMG8_C1	2	IO	
									SPI0_SCLK	3	IOD	
									I2C1_SCL	4	IOD	
									TIMG14_C1	5	IO	
									HFCLKIN	6	I	
									TIMG1_C1	7	IO	
									TIMA_FAL0	8	I	
									UART0_RTS	9	O	
									TIMA0_C2N	10	O	
									UART1_RX	11	I	
									TIMA0_C2	12	IO	
									I2C0_SDA	13	IOD	
									BEEP	14	O	
									HFXOUT	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
13	13	11	14					PA7 PINCM10 0x40428024	PA7	1	IO	SDIO (standard)
									CLK_OUT	2	O	
									TIMG8_C0	3	IO	
									TIMA0_C2	4	IO	
									TIMG8_IDX	5	I	
									TIMG2_C1	6	IO	
									TIMA0_C1	7	IO	
									SPI0_CS2_MISO 2	8	IO	
									FCC_IN	9	I	
									SPI0_POCI	10	IO	
									SPI0_PICO	11	IO	
									UART1_TX	12	O	
									TIMG1_C0	13	IO	
									COMP0_OUT	14	O	
16	16	12	15					PA8 PINCM13 0x40428030	PA8	1	IO	SDIO (standard)
									UART1_TX	2	O	
									SPI0_CS0	3	IO	
									I2C0_SDA	4	IOD	
									TIMA0_C0	5	IO	
									TIMA_FAL2	6	I	
									TIMA_FAL0	7	I	
									SPI0_CS3_CD_ MISO3	8	IO	
									TIMG2_C1	9	IO	
									HFCLKIN	10	I	
									UART0_RTS	11	O	
									SPI0_SCLK	12	IOD	
									UART1_RX	13	I	
									TIMA0_C3N	14	O	
17	17	13	16	14	8			PA9 PINCM14 0x40428034	PA9	1	IO	SDIO (standard)
									UART1_RX	2	I	
									SPI0_PICO	3	IO	
									I2C0_SCL	4	IOD	
									TIMA0_C0N	5	O	
									CLK_OUT	6	O	
									TIMA0_C1	7	IO	
									RTC_OUT	8	O	
									TIMG2_C0	9	IO	
									SPI0_POCI	10	IO	
									UART0_CTS	11	I	
									TIMA_FAL1	12	I	
									TIMG1_C1	13	IO	

Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
18	18	14	17	15	9			PA10 PINCM15 0x40428038	PA10	1	IO	SDIO (standard)with wake
									UART0_TX	2	O	
									SPI0_POCI	3	IO	
									I2C0_SDA	4	IOD	
									TIMA0_C2	5	IO	
									CLK_OUT	6	O	
									TIMG14_C0	7	IO	
									I2C1_SDA	8	IOD	
									TIMA_FAL1	10	I	
									TIMG2_C1	11	IO	
									TIMA0_C1N	12	O	
									TIMG8_C1	13	IO	
									SPI0_PICO	14	IO	
19	19	15	18	16	10	11	9	PA11 PINCM16 0x4042803c	PA11	1	IO	SDIO (standard)with wake
									UART0_RX	2	IO	
									SPI0_SCLK	3	IOD	
									I2C0_SCL	4	IOD	
									TIMA0_C2N	5	O	
									UART1_RX	6	I	
									TIMG14_C1	7	IO	
									I2C1_SCL	8	IOD	
									TIMA_FAL0	10	I	
									SPI0_CS0	12	IO	
									COMP0_OUT	14	O	
									ADC0_25	(Non-IOMUX 1) 0	A	
									COMP0_DAC_OUT	(Non-IOMUX 2) 0	A	
27	27	16	19					PA12 PINCM24 0x4042805c	PA12	1	IO	SDIO (standard)
									SPI0_SCLK	2	IOD	
									TIMA0_C3	4	IO	
									FCC_IN	5	I	
									TIMG14_C0	6	IO	
									SPI0_CS1_MISO1	8	IO	
									UART2_CTS	9	I	
									UART1_CTS	10	I	
									TIMA0_C3N	11	O	
									I2C1_SCL	12	IOD	
									TIMG2_C1	13	IO	
									COMP0_OUT	14	O	
									ADC0_18	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
28	28	17	20					PA13 PINCM25 0x40428060	PA13	1	IO	SDIO (standard)
									UART0_RX	2	IO	
									SPI0_POCI	3	IO	
									TIMA0_C2N	4	O	
									TIMA0_C3N	5	O	
									RTC_OUT	6	O	
									TIMG14_C1	7	IO	
									TIMG14_C3	8	IO	
									SPI0_CS3_CD_MISO3	9	IO	
									UART2_TX	10	O	
									UART1_RTS	11	O	
									SPI0_CS0	12	IO	
									TIMG8_C1	13	IO	
									TIMA0_C1	14	IO	
									ADC0_17	(Non-IOMUX 1) 0	A	
									COMP0_IN2-	(Non-IOMUX 2) 0	A	
29	29	18	21	17				PA14 PINCM26 0x40428064	PA14	1	IO	SDIO (standard)
									UART0_CTS	2	I	
									SPI0_PICO	3	IO	
									TIMG1_C0	4	IO	
									CLK_OUT	6	O	
									SPI0_CS2_MISO2	9	IO	
									UART2_RX	10	I	
									I2C0_SCL	12	IOD	
									UART0_TX	13	O	
									TIMA0_C2	14	IO	
									ADC0_16	(Non-IOMUX 1) 0	A	
									COMP0_IN2+	(Non-IOMUX 2) 0	A	
30	30	19	22	18	11			PA15 PINCM27 0x40428068	PA15	1	IO	SDIO (standard)
									UART0_RTS	2	O	
									SPI0_CS2_MISO2	3	IO	
									I2C1_SCL	4	IOD	
									TIMA0_C2	5	IO	
									TIMG8_IDX	7	I	
									UART2_RTS	10	O	
									TIMG14_C1	12	IO	
									ADC0_15	(Non-IOMUX 1) 0	A	
									COMP0_IN3+	(Non-IOMUX 2) 0	A	

Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
31	31	20	23	19	12	12	10	PA16 PINCM28 0x4042806c	PA16	1	IO	SDIO (standard)
									SPI0_POCI	3	IO	
									I2C1_SDA	4	IOD	
									TIMA0_C2N	5	O	
									FCC_IN	7	I	
									UART2_CTS	10	I	
									TIMG14_C2	12	IO	
									COMP0_OUT	14	O	
									ADC0_14	(Non-IOMUX 1) 0	A	
32	32	21	24	20	13	13	11	PA17 PINCM29 0x40428070	PA17	1	IO	SDIO (standard)
									UART1_TX	2	O	
									TIMA0_C2	3	IO	
									I2C1_SCL	4	IOD	
									TIMA0_C3	5	IO	
									TIMG2_C0	6	IO	
									TIMG8_C0	7	IO	
									TIMA0_C0N	8	O	
									SPI0_CS1_MISO 1	9	IO	
									SPI0_SCLK	10	IOD	
									I2C0_SDA	11	IOD	
									UART0_RX	12	IO	
									ADC0_13	(Non-IOMUX 1) 0	A	
									COMP0_IN1-	(Non-IOMUX 2) 0	A	
33	33	22	25	21	14	14	12	PA18 PINCM30 0x40428074	PA18	1	IO	SDIO (standard)
									UART1_RX	2	I	
									UART1_RTS	3	O	
									I2C1_SDA	4	IOD	
									TIMA0_C3N	5	O	
									TIMG2_C1	6	IO	
									TIMG8_C1	7	IO	
									SPI0_PICO	8	IO	
									SPI0_CS0	9	IO	
									TIMA0_C1N	10	O	
									TIMA0_C0	11	IO	
									SPI0_POCI	12	IO	
									TIMA_FAL2	13	I	
									CLK_OUT	14	O	
									ADC0_12	(Non-IOMUX 1) 0	A	
									COMP0_IN1+	(Non-IOMUX 2) 0	A	
									BSL_invoke (Flash)	(Non-IOMUX 3) 0	I	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
34	34	23	26	22	15	15	13	PA19 PINCM32 0x4042807c	PA19	1	IO	SDIO (standard)
									SWDIO	2	IO	
									SPI0_SCLK	3	IOD	
									I2C1_SDA	4	IOD	
									TIMA0_C2	5	IO	
									TIMG14_C0	6	IO	
									SPI0_POCI	7	IO	
									UART0_CTS	8	I	
									UART1_RX	11	I	
									SPI0_PICO	13	IO	
									ADC0_22	(Non-IOMUX 1) 0	A	
35	35	24	27	23	16	16	14	PA20 PINCM33 0x40428080	PA20	1	IO	SDIO (standard)
									SWCLK	2	I	
									TIMA_FAL1	3	I	
									I2C1_SCL	4	IOD	
									TIMA0_C2N	5	O	
									TIMG14_C1	6	IO	
									SPI0_PICO	7	IO	
									TIMA0_C0	8	IO	
									UART0_RTS	10	O	
									UART1_TX	11	O	
									SPI0_CS0	12	IO	
									UART1_RX	13	I	
									ADC0_4	(Non-IOMUX 1) 0	A	
39	39	25	28	24	17			PA21 PINCM37 0x40428090	PA21	1	IO	SDIO (standard)
									UART2_TX	2	O	
									SPI0_CS3_CD_ MISO3	3	IO	
									UART1_CTS	4	I	
									TIMA0_C0	5	IO	
									TIMG1_C0	6	IO	
									UART2_CTS	8	I	
									TIMG8_C0	10	IO	
									TIMA0_C0N	12	O	
									UART2_RX	13	I	
									ADC0_8	(Non-IOMUX 1) 0	A	
									ADC0_VREF-	(Non-IOMUX 2) 0	A	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
40	40	26	29	25	18	17	15	PA22 PINCM38 0x40428094	PA22	1	IO	SDIO (standard)
									UART2_RX	2	I	
									SPI0_CS2_MISO 2	3	IO	
									UART1_RTS	4	O	
									TIMA0_C0N	5	O	
									TIMG1_C1	6	IO	
									TIMA0_C1	7	IO	
									CLK_OUT	8	O	
									I2C0_SCL	9	IOD	
									TIMG8_C1	10	IO	
									UART1_RX	11	I	
									SPI0_POCI	12	IO	
									UART2_TX	13	O	
									ADC0_7	(Non-IOMUX 1) 0	A	
43	43	27	30	26	19	18	16	PA23 PINCM41 0x404280a0	PA23	1	IO	SDIO (standard)
									UART2_TX	2	O	
									SPI0_CS3_CD_ MISO3	3	IO	
									TIMA0_C3	5	IO	
									TIMG8_C0	6	IO	
									TIMG2_C0	7	IO	
									UART0_TX	8	O	
									TIMG14_C0	9	IO	
									SPI0_POCI	12	IO	
									UART0_CTS	13	I	
									ADC0_26	(Non-IOMUX 1) 0	A	
									ADC0_VREF+	(Non-IOMUX 2) 0	A	
44	44	28	31	27	20	19	17	PA24 PINCM42 0x404280a4	PA24	1	IO	SDIO (standard)
									UART2_RX	2	I	
									SPI0_CS2_MISO 2	3	IO	
									UART0_RTS	4	O	
									TIMA0_C3N	5	O	
									TIMG8_C1	6	IO	
									TIMG2_C1	7	IO	
									UART1_RX	8	I	
									TIMG14_C1	9	IO	
									SPI0_PICO	12	IO	
									I2C0_SDA	13	IOD	
									ADC0_3	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
45	45	29	32	28	21	20	18	PA25 PINCM43 0x404280a8	PA25	1	IO	SDIO (standard)
									SPI0_PICO	2	IO	
									SPI0_POCI	3	IO	
									SPI0_SCLK	4	IOD	
									TIMA0_C3	5	IO	
									TIMA0_C1N	6	O	
									TIMA0_C2	7	IO	
									UART2_CTS	8	I	
									TIMG14_C0	9	IO	
									TIMG1_C0	10	IO	
									I2C0_SDA	11	IOD	
									UART0_TX	12	O	
									TIMA_FAL2	13	I	
									I2C0_SCL	14	IOD	
									ADC0_2	(Non-IOMUX 1) 0	A	
46	46	30	1	1	22	1	19	PA26 PINCM44 0x404280ac	PA26	1	IO	SDIO (standard)
									BEEP	2	O	
									SPI0_POCI	3	IO	
									TIMG8_C0	4	IO	
									TIMA_FAL0	5	I	
									TIMA0_C3N	6	O	
									TIMG2_C0	7	IO	
									UART2_RTS	8	O	
									I2C0_SCL	9	IOD	
									TIMG1_C1	10	IO	
									UART0_RX	11	IO	
									TIMA0_C0	12	IO	
									I2C0_SDA	13	IOD	
									UART1_CTS	14	I	
									ADC0_1	(Non-IOMUX 1) 0	A	
									COMP0_IN0+	(Non-IOMUX 2) 0	A	
47	47	31	2	2		2	20	PA27 PINCM45 0x404280b0	PA27	1	IO	SDIO (standard)
									SPI0_CS3_CD_ MISO3	2	IO	
									TIMA0_C0N	3	O	
									TIMG8_C1	4	IO	
									TIMA_FAL2	5	I	
									CLK_OUT	6	O	
									TIMG2_C1	7	IO	
									RTC_OUT	8	O	
									UART1_CTS	9	I	
									I2C0_SCL	10	IOD	
									UART0_TX	11	O	
									SPI0_POCI	12	IO	
									COMP0_OUT	14	O	
									ADC0_0	(Non-IOMUX 1) 0	A	
									COMP0_IN0-	(Non-IOMUX 2) 0	A	

Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
3	3							PA28 PINCM3 0x40428008	PA28	1	IO	SDIO (standard)
									UART0_TX	2	O	
									I2C0_SDA	3	IOD	
									TIMA0_C3	4	IO	
									TIMA_FAL0	5	I	
									TIMG2_C0	6	IO	
									TIMA0_C1	7	IO	
48	48	32	3	3	23	3	1	PA30 PINCM46 0x404280b4	PA30	1	IO	SDIO (standard)
									UART0_RX	4	IO	
									TIMG8_IDX	5	I	
									TIMA0_C0	6	IO	
									UART1_RTS	9	O	
									TIMG2_C1	10	IO	
									TIMG14_C2	11	IO	
									I2C0_SDA	12	IOD	
5	5							PA31 PINCM4 0x4042800c	PA31	1	IO	SDIO (standard)
									UART0_RX	2	IO	
									I2C0_SCL	3	IOD	
									TIMA0_C3N	4	O	
									CLK_OUT	6	O	
14	14							PB2 PINCM11 0x40428028	PB2	1	IO	SDIO (standard)
									UART2_CTS	3	I	
									I2C1_SCL	4	IOD	
									TIMA0_C3	5	IO	
									UART1_CTS	6	I	
									TIMG1_C0	7	IO	
									UART2_TX	8	O	
									HFCLKIN	10	I	
									SPI0_PICO	11	IO	
									UART1_RX	12	I	
									TIMA0_C1N	13	O	
15	15						8	PB3 PINCM12 0x4042802c	PB3	1	IO	SDIO (standard)
									TIMA_FAL0	2	I	
									UART2_RTS	3	O	
									I2C1_SDA	4	IOD	
									TIMA0_C3N	5	O	
									UART1_RTS	6	O	
									TIMG1_C1	7	IO	
									UART2_RX	8	I	
									TIMG2_C1	9	IO	
									TIMA0_C0	10	IO	
									SPI0_SCLK	11	IOD	
									SPI0_CS0	12	IO	
									UART1_TX	13	O	
									RTC_OUT	14	O	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
20	20							PB6 PINCM17 0x40428040	PB6	1	IO	SDIO (standard)
									UART1_TX	2	O	
									TIMG8_C0	5	IO	
									UART2_CTS	6	I	
									TIMG1_C0	7	IO	
									TIMA_FAL2	8	I	
									SPI0_CS1_MISO 1	9	IO	
									TIMA0_C3N	11	O	
									TIMG8_C1	12	IO	
									TIMA0_C2N	13	O	
									UART0_TX	14	O	
									ADC0_24	(Non-IOMUX 1) 0	A	
21	21							PB7 PINCM18 0x40428044	PB7	1	IO	SDIO (standard)
									UART1_RX	2	I	
									TIMG8_C1	5	IO	
									UART2_RTS	6	O	
									TIMG1_C1	7	IO	
									SPI0_CS2_MISO 2	9	IO	
									BEEP	12	O	
									SPI0_SCLK	13	IOD	
									UART0_RX	14	IO	
									ADC0_23	(Non-IOMUX 1) 0	A	
22	22							PB8 PINCM19 0x40428048	PB8	1	IO	SDIO (standard)
									UART1_CTS	2	I	
									TIMA0_C0	3	IO	
									TIMG1_C0	5	IO	
									SPI0_SCLK	7	IOD	
									BEEP	8	O	
									TIMG8_C0	9	IO	
									UART0_RX	10	IO	
									SPI0_POCI	11	IO	
									I2C0_SCL	12	IOD	
									COMP0_OUT	14	O	
23	23							PB9 PINCM20 0x4042804c	PB9	1	IO	SDIO (standard)
									UART1_RTS	2	O	
									TIMA0_C0N	5	O	
									TIMA0_C1	6	IO	
									TIMG1_C1	7	IO	
									TIMG2_C0	8	IO	
									SPI0_POCI	10	IO	
									UART0_RX	11	IO	
									I2C0_SCL	12	IOD	
									UART0_TX	13	O	
									I2C0_SDA	14	IOD	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
24	24							PB14 PINCM21 0x40428050	PB14	1	IO	SDIO (standard)
									TIMA0_C0	5	IO	
									TIMG8_IDX	6	I	
									SPI0_CS3_CD_MISO3	7	IO	
									TIMG2_C1	8	IO	
									I2C0_SDA	9	IOD	
									SPI0_PICO	10	IO	
									UART0_TX	11	O	
									TIMA_FAL2	12	I	
									TIMA_FAL0	13	I	
									TIMG14_C2	14	IO	
									ADC0_21	(Non-IOMUX 1) 0	A	
25	25							PB15 PINCM22 0x40428054	PB15	1	IO	SDIO (standard)
									UART2_TX	2	O	
									TIMG8_C0	5	IO	
									TIMG2_C0	6	IO	
									TIMA0_C1N	12	O	
									UART1_TX	13	O	
									TIMG2_C1	14	IO	
									ADC0_20	(Non-IOMUX 1) 0	A	
26	26							PB16 PINCM23 0x40428058	PB16	1	IO	SDIO (standard)
									UART2_RX	2	I	
									TIMG8_C1	5	IO	
									TIMG2_C1	6	IO	
									TIMA0_C2N	12	O	
									UART1_RX	13	I	
									I2C1_SDA	14	IOD	
									ADC0_19	(Non-IOMUX 1) 0	A	
36	36							PB17 PINCM34 0x40428084	PB17	1	IO	SDIO (standard)
									UART2_TX	2	O	
									SPI0_PICO	3	IO	
									I2C0_SCL	4	IOD	
									TIMA0_C2	5	IO	
									TIMG14_C0	6	IO	
									TIMG1_C0	9	IO	
									SPI0_CS0	10	IO	
									ADC0_11	(Non-IOMUX 1) 0	A	
37	37							PB18 PINCM35 0x40428088	PB18	1	IO	SDIO (standard)
									UART2_RX	2	I	
									SPI0_SCLK	3	IOD	
									I2C0_SDA	4	IOD	
									TIMA0_C2N	5	O	
									TIMG14_C1	6	IO	
									SPI0_CS0	7	IO	
									TIMG1_C1	9	IO	
									TIMA0_C1	12	IO	
									UART0_RTS	13	O	
									ADC0_10	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RGZ, RHB, DGS32, DGS28, RGE, DGS20, RUK Packages) (continued)

PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
38	38							PB19 PINCM36 0x4042808c	PB19	1	IO	SDIO (standard)
									SPI0_POCI	3	IO	
									TIMG8_C1	4	IO	
									UART0_CTS	5	I	
									TIMG2_C1	6	IO	
									TIMG8_IDX	7	I	
									UART2_CTS	8	I	
									TIMA0_C1N	12	O	
									UART2_RX	13	I	
									COMP0_OUT	14	O	
									ADC0_9	(Non-IOMUX 1) 0	A	
41	41							PB20 PINCM39 0x40428098	PB20	1	IO	SDIO (standard)
									SPI0_CS2_MISO 2	2	IO	
									TIMA0_C2	5	IO	
									TIMA_FAL1	6	I	
									TIMA0_C1	7	IO	
									UART2_RTS	8	O	
									I2C0_SDA	9	IOD	
									UART1_CTS	12	I	
									TIMA0_C2N	13	O	
									TIMG8_C1	14	IO	
									ADC0_6	(Non-IOMUX 1) 0	A	
42	42							PB24 PINCM40 0x4042809c	PB24	1	IO	SDIO (standard)
									SPI0_CS3_CD_ MISO3	2	IO	
									SPI0_CS1_MISO 1	3	IO	
									TIMA0_C3	5	IO	
									TIMA0_C1N	6	O	
									UART2_RTS	8	O	
									SPI0_SCLK	12	IOD	
									TIMG14_C2	13	IO	
									UART0_RTS	14	O	
									ADC0_5	(Non-IOMUX 1) 0	A	
6	6	4	7	7	3	6	4	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
7	7	5	8	8	4	7	5	VSS	VSS	(Non-IOMUX 1) 0	PWR	PWR

6.3 Signal Descriptions

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
ADC0_VREF+	A	ADC0 voltage reference (VREF) power supply	43	43	27	30	26	19	18	16
ADC0_VREF-	A	ADC0 voltage reference (VREF) ground supply	39	39	25	28	24	17		
ADC0_0	A	ADC0 analog input channel 0	47	47	31	2	2		2	20
ADC0_1	A	ADC0 analog input channel 1	46	46	30	1	1	22	1	19
ADC0_2	A	ADC0 analog input channel 2	45	45	29	32	28	21	20	18

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
ADC0_3	A	ADC0 analog input channel 3	44	44	28	31	27	20	19	17
ADC0_4	A	ADC0 analog input channel 4	35	35	24	27	23	16	16	14
ADC0_5	A	ADC0 analog input channel 5	42	42						
ADC0_6	A	ADC0 analog input channel 6	41	41						
ADC0_7	A	ADC0 analog input channel 7	40	40	26	29	25	18	17	15
ADC0_8	A	ADC0 analog input channel 8	39	39	25	28	24	17		
ADC0_9	A	ADC0 analog input channel 9	38	38						
ADC0_10	A	ADC0 analog input channel 10	37	37						
ADC0_11	A	ADC0 analog input channel 11	36	36						
ADC0_12	A	ADC0 analog input channel 12	33	33	22	25	21	14	14	12
ADC0_13	A	ADC0 analog input channel 13	32	32	21	24	20	13	13	11
ADC0_14	A	ADC0 analog input channel 14	31	31	20	23	19	12	12	10
ADC0_15	A	ADC0 analog input channel 15	30	30	19	22	18	11		
ADC0_16	A	ADC0 analog input channel 16	29	29	18	21	17			
ADC0_17	A	ADC0 analog input channel 17	28	28	17	20				
ADC0_18	A	ADC0 analog input channel 18	27	27	16	19				
ADC0_19	A	ADC0 analog input channel 19	26	26						
ADC0_20	A	ADC0 analog input channel 20	25	25						
ADC0_21	A	ADC0 analog input channel 21	24	24						
ADC0_22	A	ADC0 analog input channel 22	34	34	23	26	22	15	15	13
ADC0_23	A	ADC0 analog input channel 23	21	21						
ADC0_24	A	ADC0 analog input channel 24	20	20						
ADC0_25	A	ADC0 analog input channel 25	19	19	15	18	16	10	11	9
ADC0_26	A	ADC0 analog input channel 26	43	43	27	30	26	19	18	16

Table 6-4. Flash Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
BSL_invoke (Flash)	I	Default Flash BSL invoke signal	33	33	22	25	21	14	14	12

Table 6-5. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
CLK_OUT	O	CLK_OUT digital clock output from the PMCU	13, 17, 18, 29, 33, 40, 47, 5	13, 17, 18, 29, 33, 40, 47, 5	11, 13, 14, 18, 22, 26, 31	14, 16, 17, 2, 21, 25, 29	14, 15, 17, 2, 21, 25	14, 18, 8, 9	14, 17, 2	12, 15, 20
FCC_IN	I	Frequency clock counter (FCC) input signal	1, 11, 13, 27, 31	1, 11, 13, 27, 31	1, 11, 16, 20, 9	12, 14, 19, 23, 4	12, 19, 4	12, 24	12, 4	10, 2
HFCLKIN	I	High frequency clock digital clock input signal	10, 12, 14, 16, 2	10, 12, 14, 16, 2	10, 12, 2, 8	11, 13, 15, 5	11, 13, 5	1, 7	10, 5, 9	3, 7
HFXIN	A	High frequency crystal oscillator (HFXT) signal	11	11	9	12	12			
HFXOUT	A	High frequency crystal oscillator (HFXT) signal	12	12	10	13	13		10	

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Table 6-5. Clock Module (CKM) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
LFCLKIN	I	Low frequency clock digital clock input signal	10	10	8	11	11	7	9	7
LFXIN	A	Low frequency crystal oscillator (LFXT) signal	9	9	7	10	10	6		
LFXOUT	A	Low frequency crystal oscillator (LFXT) signal	10	10	8	11	11	7	9	7

Table 6-6. Comparator (COMP) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
COMP0_DAC_OUT	A	COMP0 DAC output	19	19	15	18	16	10	11	9
COMP0_OUT	O	COMP0 output	13, 19, 22, 27, 31, 38, 47, 9	13, 19, 22, 27, 31, 38, 47, 9	11, 15, 16, 20, 31, 7	10, 14, 18, 19, 2, 23	10, 16, 19, 2	10, 12, 6	11, 12, 2	10, 20, 9
COMP0_IN0+	A	COMP0 non-inverting input 0	46	46	30	1	1	22	1	19
COMP0_IN0-	A	COMP0 inversting input 0	47	47	31	2	2		2	20
COMP0_IN1+	A	COMP0 non-inverting input 1	33	33	22	25	21	14	14	12
COMP0_IN1-	A	COMP0 inversting input 1	32	32	21	24	20	13	13	11
COMP0_IN2+	A	COMP0 non-inverting input 2	29	29	18	21	17			
COMP0_IN2-	A	COMP0 inversting input 2	28	28	17	20				
COMP0_IN3+	A	COMP0 non-inverting input 3	30	30	19	22	18	11		

Table 6-7. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
PA0	IO	GPIO port A input/output 0	1	1	1	4	4	24	4	2
PA1	IO	GPIO port A input/output 1	2	2	2	5	5	1	5	3
PA2	IO	GPIO port A input/output 2	8	8	6	9	9	5	8	6
PA3	IO	GPIO port A input/output 3	9	9	7	10	10	6		
PA4	IO	GPIO port A input/output 4	10	10	8	11	11	7	9	7
PA5	IO	GPIO port A input/output 5	11	11	9	12	12			
PA6	IO	GPIO port A input/output 6	12	12	10	13	13		10	
PA7	IO	GPIO port A input/output 7	13	13	11	14				
PA8	IO	GPIO port A input/output 8	16	16	12	15				
PA9	IO	GPIO port A input/output 9	17	17	13	16	14	8		
PA10	IO	GPIO port A input/output 10	18	18	14	17	15	9		
PA11	IO	GPIO port A input/output 11	19	19	15	18	16	10	11	9
PA12	IO	GPIO port A input/output 12	27	27	16	19				
PA13	IO	GPIO port A input/output 13	28	28	17	20				
PA14	IO	GPIO port A input/output 14	29	29	18	21	17			
PA15	IO	GPIO port A input/output 15	30	30	19	22	18	11		
PA16	IO	GPIO port A input/output 16	31	31	20	23	19	12	12	10
PA17	IO	GPIO port A input/output 17	32	32	21	24	20	13	13	11
PA18	IO	GPIO port A input/output 18	33	33	22	25	21	14	14	12
PA19	IO	GPIO port A input/output 19	34	34	23	26	22	15	15	13
PA20	IO	GPIO port A input/output 20	35	35	24	27	23	16	16	14

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Table 6-7. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
PA21	IO	GPIO port A input/output 21	39	39	25	28	24	17		
PA22	IO	GPIO port A input/output 22	40	40	26	29	25	18	17	15
PA23	IO	GPIO port A input/output 23	43	43	27	30	26	19	18	16
PA24	IO	GPIO port A input/output 24	44	44	28	31	27	20	19	17
PA25	IO	GPIO port A input/output 25	45	45	29	32	28	21	20	18
PA26	IO	GPIO port A input/output 26	46	46	30	1	1	22	1	19
PA27	IO	GPIO port A input/output 27	47	47	31	2	2		2	20
PA28	IO	GPIO port A input/output 28	3	3						
PA30	IO	GPIO port A input/output 30	48	48	32	3	3	23	3	1
PA31	IO	GPIO port A input/output 31	5	5						
PB2	IO	GPIO port B input/output 2	14	14						
PB3	IO	GPIO port B input/output 3	15	15						8
PB6	IO	GPIO port B input/output 6	20	20						
PB7	IO	GPIO port B input/output 7	21	21						
PB8	IO	GPIO port B input/output 8	22	22						
PB9	IO	GPIO port B input/output 9	23	23						
PB14	IO	GPIO port B input/output 14	24	24						
PB15	IO	GPIO port B input/output 15	25	25						
PB16	IO	GPIO port B input/output 16	26	26						
PB17	IO	GPIO port B input/output 17	36	36						
PB18	IO	GPIO port B input/output 18	37	37						
PB19	IO	GPIO port B input/output 19	38	38						
PB20	IO	GPIO port B input/output 20	41	41						
PB24	IO	GPIO port B input/output 24	42	42						

Table 6-8. I2C Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
I2C0_SCL	IOD	I2C0 serial clock signal (SCL)	17, 19, 2, 22, 23, 29, 36, 40, 45, 46, 47, 5, 8	17, 19, 2, 22, 23, 29, 36, 40, 45, 46, 47, 5, 8	13, 15, 18, 2, 26, 29, 30, 31, 6	1, 16, 18, 2, 21, 29, 32, 5, 9	1, 14, 16, 17, 2, 25, 28, 5, 9	1, 10, 18, 21, 22, 5, 8	1, 11, 17, 2, 20, 5, 8	15, 18, 19, 20, 3, 6, 9
I2C0_SDA	IOD	I2C0 serial data signal (SDA)	1, 12, 16, 18, 2, 23, 24, 3, 32, 37, 41, 44, 45, 46, 48, 9	1, 12, 16, 18, 2, 23, 24, 3, 32, 37, 41, 44, 45, 46, 48, 9	1, 10, 12, 14, 2, 21, 28, 29, 30, 32, 7	1, 10, 13, 15, 17, 24, 3, 31, 32, 4, 5	1, 10, 13, 15, 20, 27, 28, 3, 4, 5	1, 13, 20, 21, 22, 23, 24, 6, 9	1, 10, 13, 19, 20, 3, 4, 5	1, 11, 17, 18, 19, 2, 3
I2C1_SCL	IOD	I2C1 serial clock signal (SCL)	10, 12, 14, 19, 27, 30, 32, 35	10, 12, 14, 19, 27, 30, 32, 35	10, 15, 16, 19, 21, 24, 8	11, 13, 18, 19, 22, 24, 27	11, 13, 16, 18, 20, 23	10, 11, 13, 16, 7	10, 11, 13, 16, 9	11, 14, 7, 9

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Table 6-8. I2C Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
I2C1_SDA	IOD	I2C1 serial data signal (SDA)	11, 15, 18, 26, 31, 33, 34, 9	11, 15, 18, 26, 31, 33, 34, 9	14, 20, 22, 23, 7, 9	10, 12, 17, 23, 25, 26	10, 12, 15, 19, 21, 22	12, 14, 15, 6, 9	12, 14, 15	10, 12, 13, 8

Table 6-9. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
RTC_OUT	O	Real-time clock output signal	1, 15, 17, 28, 47	1, 15, 17, 28, 47	1, 13, 17, 31	16, 2, 20, 4	14, 2, 4	24, 8	2, 4	2, 20, 8

Table 6-10. Serial Peripheral Interface (SPI) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
SPI0_PICO	IO	SPI0 peripheral in controller out signal	11, 13, 14, 17, 18, 24, 29, 33, 34, 35, 36, 44, 45	11, 13, 14, 17, 18, 24, 29, 33, 34, 35, 36, 44, 45	11, 13, 14, 18, 22, 23, 24, 28, 29, 9	12, 14, 16, 17, 21, 25, 26, 27, 31, 32	12, 14, 15, 17, 21, 22, 23, 27, 28	14, 15, 16, 20, 21, 8, 9	14, 15, 16, 19, 20	12, 13, 14, 17, 18
SPI0_POCI	IO	SPI0 peripheral out controller in signal	10, 13, 17, 18, 22, 23, 28, 31, 33, 34, 38, 40, 43, 45, 46, 47	10, 13, 17, 18, 22, 23, 28, 31, 33, 34, 38, 40, 43, 45, 46, 47	11, 13, 14, 17, 20, 22, 23, 26, 27, 29, 30, 31, 8	1, 11, 14, 16, 17, 2, 20, 23, 25, 26, 29, 30, 32	1, 11, 14, 15, 19, 2, 21, 22, 25, 26, 28	12, 14, 15, 18, 19, 21, 22, 7, 8, 9	1, 12, 14, 15, 17, 18, 2, 20, 9	10, 12, 13, 15, 16, 18, 19, 20, 7
SPI0_SCLK	IOD	SPI0 serial clock	12, 15, 16, 19, 21, 22, 27, 32, 34, 37, 42, 45	12, 15, 16, 19, 21, 22, 27, 32, 34, 37, 42, 45	10, 12, 15, 16, 21, 23, 29	13, 15, 18, 19, 24, 26, 32	13, 16, 20, 22, 28	10, 13, 15, 21	10, 11, 13, 15, 20	11, 13, 18, 8, 9
SPI0_CS0	IO	SPI0 chip-select 0 signal	10, 15, 16, 19, 28, 33, 35, 36, 37, 8	10, 15, 16, 19, 28, 33, 35, 36, 37, 8	12, 15, 17, 22, 24, 6, 8	11, 15, 18, 20, 25, 27, 9	11, 16, 21, 23, 9	10, 14, 16, 5, 7	11, 14, 16, 8, 9	12, 14, 6, 7, 8, 9
SPI0_CS1_MISO1	IO		1, 20, 27, 32, 42, 9	1, 20, 27, 32, 42, 9	1, 16, 21, 7	10, 19, 24, 4	10, 20, 4	13, 24, 6	13, 4	11, 2
SPI0_CS2_MISO2	IO		13, 21, 29, 30, 40, 41, 44	13, 21, 29, 30, 40, 41, 44	11, 18, 19, 26, 28	14, 21, 22, 29, 31	17, 18, 25, 27	11, 18, 20	17, 19	15, 17
SPI0_CS3_CD_MISO3	IO		16, 2, 24, 28, 39, 42, 43, 47, 9	16, 2, 24, 28, 39, 42, 43, 47, 9	12, 17, 2, 25, 27, 31, 7	10, 15, 2, 20, 28, 30, 5	10, 2, 24, 26, 5	1, 17, 19, 6	18, 2, 5	16, 20, 3

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Table 6-11. Serial Wire Debug (SWD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
SWCLK	I	Serial wire debug interface clock input signal	35	35	24	27	23	16	16	14
SWDIO	IO	Serial wire debug interface data input/output signal	34	34	23	26	22	15	15	13

Table 6-12. System Controller (SYSCTL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
BEEP	O	Beep output	1, 12, 21, 22, 46	1, 12, 21, 22, 46	1, 10, 30	1, 13, 4	1, 13, 4	22, 24	1, 10, 4	19, 2
NRST	RESET	Active-low reset signal (must be logic high for the device to start)	4	4	3	6	6	2	5	3
VDD	PWR	VDD supply	6	6	4	7	7	3	6	4
VSS	PWR	VSS (ground)	7	7	5	8	8	4	7	5

Table 6-13. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
TIMA0_C0	IO	TIMA0 capture/compare 0 signal	1, 15, 16, 22, 24, 33, 35, 39, 46, 48, 8	1, 15, 16, 22, 24, 33, 35, 39, 46, 48, 8	1, 12, 22, 24, 25, 30, 32, 6	1, 15, 25, 27, 28, 3, 4, 9	1, 21, 23, 24, 3, 4, 9	14, 16, 17, 22, 23, 24, 5	1, 14, 16, 3, 4, 8	1, 12, 14, 19, 2, 6, 8
TIMA0_C1	IO	TIMA0 capture/compare 1 signal	11, 13, 17, 2, 23, 28, 3, 37, 40, 41, 9	11, 13, 17, 2, 23, 28, 3, 37, 40, 41, 9	11, 13, 17, 2, 26, 7, 9	10, 12, 14, 16, 20, 29, 5	10, 12, 14, 25, 5	1, 18, 6, 8	17, 5	15, 3
TIMA0_C2	IO	TIMA0 capture/compare 2 signal	12, 13, 18, 29, 30, 32, 34, 36, 41, 45, 9	12, 13, 18, 29, 30, 32, 34, 36, 41, 45, 9	10, 11, 14, 18, 19, 21, 23, 29, 7	10, 13, 14, 17, 21, 22, 24, 26, 32	10, 13, 15, 17, 18, 20, 22, 28	11, 13, 15, 21, 6, 9	10, 13, 15, 20	11, 13, 18
TIMA0_C3	IO	TIMA0 capture/compare 3 signal	10, 14, 27, 3, 32, 42, 43, 45	10, 14, 27, 3, 32, 42, 43, 45	16, 21, 27, 29, 8	11, 19, 24, 30, 32	11, 20, 26, 28	13, 19, 21, 7	13, 18, 20, 9	11, 16, 18, 7
TIMA0_C0N	O	TIMA0 capture/compare 0 complementary output	10, 17, 23, 32, 39, 40, 47	10, 17, 23, 32, 39, 40, 47	13, 21, 25, 26, 31, 8	11, 16, 2, 24, 28, 29	11, 14, 2, 20, 24, 25	13, 17, 18, 7, 8	13, 17, 2, 9	11, 15, 20, 7
TIMA0_C1N	O	TIMA0 capture/compare 1 complementary output	10, 14, 18, 25, 33, 38, 42, 45	10, 14, 18, 25, 33, 38, 42, 45	14, 22, 29, 8	11, 17, 25, 32	11, 15, 21, 28	14, 21, 7, 9	14, 20, 9	12, 18, 7
TIMA0_C2N	O	TIMA0 capture/compare 2 complementary output	12, 19, 20, 26, 28, 31, 35, 37, 41, 8	12, 19, 20, 26, 28, 31, 35, 37, 41, 8	10, 15, 17, 20, 24, 6	13, 18, 20, 23, 27, 9	13, 16, 19, 23, 9	10, 12, 16, 5	10, 11, 12, 16, 8	10, 14, 6, 9

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Table 6-13. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
TIMA0_C3N	O	TIMA0 capture/compare 3 complementary output	15, 16, 20, 27, 28, 33, 44, 46, 5, 8	15, 16, 20, 27, 28, 33, 44, 46, 5, 8	12, 16, 17, 22, 28, 30, 6	1, 15, 19, 20, 25, 31, 9	1, 21, 27, 9	14, 20, 22, 5	1, 14, 19, 8	12, 17, 19, 6, 8
TIMA_FAL0	I	TIMA fault input 0	12, 15, 16, 19, 24, 3, 46, 8	12, 15, 16, 19, 24, 3, 46, 8	10, 12, 15, 30, 6	1, 13, 15, 18, 9	1, 13, 16, 9	10, 22, 5	1, 10, 11, 8	19, 6, 8, 9
TIMA_FAL1	I	TIMA fault input 1	1, 11, 17, 18, 35, 41, 8	1, 11, 17, 18, 35, 41, 8	1, 13, 14, 24, 6, 9	12, 16, 17, 27, 4, 9	12, 14, 15, 23, 4, 9	16, 24, 5, 8, 9	16, 4, 8	14, 2, 6
TIMA_FAL2	I	TIMA fault input 2	16, 2, 20, 24, 33, 45, 47	16, 2, 20, 24, 33, 45, 47	12, 2, 22, 29, 31	15, 2, 25, 32, 5	2, 21, 28, 5	1, 14, 21	14, 2, 20, 5	12, 18, 20, 3
TIMG8_IDX	I	TIMG8 quadrature encoder index pulse signal	13, 2, 24, 30, 38, 48, 8	13, 2, 24, 30, 38, 48, 8	11, 19, 2, 32, 6	14, 22, 3, 5, 9	18, 3, 5, 9	1, 11, 23, 5	3, 5, 8	1, 3, 6
TIMG14_C0	IO	TIMG14 capture/compare 0 signal	1, 11, 18, 27, 34, 36, 43, 45	1, 11, 18, 27, 34, 36, 43, 45	1, 14, 16, 23, 27, 29, 9	12, 17, 19, 26, 30, 32, 4	12, 15, 22, 26, 28, 4	15, 19, 21, 24, 9	15, 18, 20, 4	13, 16, 18, 2
TIMG14_C1	IO	TIMG14 capture/compare 1 signal	12, 19, 2, 28, 30, 35, 37, 44	12, 19, 2, 28, 30, 35, 37, 44	10, 15, 17, 19, 2, 24, 28	13, 18, 20, 22, 27, 31, 5	13, 16, 18, 23, 27, 5	1, 10, 11, 16, 20	10, 11, 16, 19, 5	14, 17, 3, 9
TIMG14_C2	IO	TIMG14 capture/compare 2 signal	24, 31, 42, 48	24, 31, 42, 48	20, 32	23, 3	19, 3	12, 23	12, 3	1, 10
TIMG14_C3	IO	TIMG14 capture/compare 3 signal	28	28	17	20				
TIMG1_C0	IO	TIMG1 capture/compare 0 signal	11, 13, 14, 20, 22, 29, 36, 39, 45	11, 13, 14, 20, 22, 29, 36, 39, 45	11, 18, 25, 29, 9	12, 14, 21, 28, 32	12, 17, 24, 28	17, 21	20	18
TIMG1_C1	IO	TIMG1 capture/compare 1 signal	12, 15, 17, 21, 23, 37, 40, 46	12, 15, 17, 21, 23, 37, 40, 46	10, 13, 26, 30	1, 13, 16, 29	1, 13, 14, 25	18, 22, 8	1, 10, 17	15, 19, 8
TIMG2_C0	IO	TIMG2 capture/compare 0 signal	17, 23, 25, 3, 32, 43, 46, 9	17, 23, 25, 3, 32, 43, 46, 9	13, 21, 27, 30, 7	1, 10, 16, 24, 30	1, 10, 14, 20, 26	13, 19, 22, 6, 8	1, 13, 18	11, 16, 19
TIMG2_C1	IO	TIMG2 capture/compare 1 signal	10, 13, 15, 16, 18, 24, 25, 26, 27, 33, 38, 44, 47, 48, 8	10, 13, 15, 16, 18, 24, 25, 26, 27, 33, 38, 44, 47, 48, 8	11, 12, 14, 16, 22, 28, 31, 32, 6, 8	11, 14, 15, 17, 19, 2, 25, 3, 31, 9	11, 15, 2, 21, 27, 3, 9	14, 20, 23, 5, 7, 9	14, 19, 2, 3, 8, 9	1, 12, 17, 20, 6, 7, 8
TIMG8_C0	IO	TIMG8 capture/compare 0 signal	11, 13, 2, 20, 22, 25, 32, 39, 43, 46, 9	11, 13, 2, 20, 22, 25, 32, 39, 43, 46, 9	11, 2, 21, 25, 27, 30, 7, 9	1, 10, 12, 14, 24, 28, 30, 5	1, 10, 12, 20, 24, 26, 5	1, 13, 17, 19, 22, 6	1, 13, 18, 5	11, 16, 19, 3

Table 6-13. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
TIMG8_C1	IO	TIMG8 capture/compare 1 signal	1, 10, 12, 18, 20, 21, 26, 28, 33, 38, 40, 41, 44, 47, 8	1, 10, 12, 18, 20, 21, 26, 28, 33, 38, 40, 41, 44, 47, 8	1, 10, 14, 17, 22, 26, 28, 31, 6, 8	11, 13, 17, 2, 20, 25, 29, 31, 4, 9	11, 13, 15, 2, 21, 25, 27, 4, 9	14, 18, 20, 24, 5, 7, 9	10, 14, 17, 19, 2, 4, 8, 9	12, 15, 17, 2, 20, 6, 7

Table 6-14. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
UART0_CTS	I	UART0 clear to send signal	11, 17, 29, 34, 38, 43	11, 17, 29, 34, 38, 43	13, 18, 23, 27, 9	12, 16, 21, 26, 30	12, 14, 17, 22, 26	15, 19, 8	15, 18	13, 16
UART0_RTS	O	UART0 ready to send signal	12, 16, 30, 35, 37, 42, 44	12, 16, 30, 35, 37, 42, 44	10, 12, 19, 24, 28	13, 15, 22, 27, 31	13, 18, 23, 27	11, 16, 20	10, 16, 19	14, 17
UART0_RX	IO	UART0 receive signal (RXD)	19, 2, 21, 22, 23, 28, 32, 46, 48, 5	19, 2, 21, 22, 23, 28, 32, 46, 48, 5	15, 17, 2, 21, 30, 32	1, 18, 20, 24, 3, 5	1, 16, 20, 3, 5	1, 10, 13, 22, 23	1, 11, 13, 3, 5	1, 11, 19, 3, 9
UART0_TX	O	UART0 transmit signal (TXD)	1, 18, 2, 20, 23, 24, 29, 3, 43, 45, 47	1, 18, 2, 20, 23, 24, 29, 3, 43, 45, 47	1, 14, 18, 2, 27, 29, 31	17, 2, 21, 30, 32, 4, 5	15, 17, 2, 26, 28, 4, 5	1, 19, 21, 24, 9	18, 2, 20, 4, 5	16, 18, 2, 20, 3
UART1_CTS	I	UART1 clear to send signal	14, 22, 27, 39, 41, 46, 47	14, 22, 27, 39, 41, 46, 47	16, 25, 30, 31	1, 19, 2, 28	1, 2, 24	17, 22	1, 2	19, 20
UART1_RTS	O	UART1 ready to send signal	15, 2, 23, 28, 33, 40, 48	15, 2, 23, 28, 33, 40, 48	17, 2, 22, 26, 32	20, 25, 29, 3, 5	21, 25, 3, 5	1, 14, 18, 23	14, 17, 3, 5	1, 12, 15, 3, 8
UART1_RX	I	UART1 receive signal (RXD)	10, 12, 14, 16, 17, 19, 21, 26, 33, 34, 35, 40, 44	10, 12, 14, 16, 17, 19, 21, 26, 33, 34, 35, 40, 44	10, 12, 13, 15, 22, 23, 24, 26, 28, 8	11, 13, 15, 16, 18, 25, 26, 27, 29, 31	11, 13, 14, 16, 21, 22, 23, 25, 27	10, 14, 15, 16, 18, 20, 7, 8	10, 11, 14, 15, 16, 17, 19, 9	12, 13, 14, 15, 17, 7, 9
UART1_TX	O	UART1 transmit signal (TXD)	11, 13, 15, 16, 20, 25, 32, 35, 9	11, 13, 15, 16, 20, 25, 32, 35, 9	11, 12, 21, 24, 7, 9	10, 12, 14, 15, 24, 27	10, 12, 20, 23	13, 16, 6	13, 16	11, 14, 8
UART2_CTS	I	UART2 clear to send signal	14, 20, 27, 31, 38, 39, 45, 9	14, 20, 27, 31, 38, 39, 45, 9	16, 20, 25, 29, 7	10, 19, 23, 28, 32	10, 19, 24, 28	12, 17, 21, 6	12, 20	10, 18
UART2_RTS	O	UART2 ready to send signal	10, 15, 21, 30, 41, 42, 46	10, 15, 21, 30, 41, 42, 46	19, 30, 8	1, 11, 22	1, 11, 18	11, 22, 7	1, 9	19, 7, 8

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Table 6-14. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RGZ PIN	RHB PIN	DGS32 PIN	DGS28 PIN	RGE PIN	DGS20 PIN	RUK PIN
UART2_RX	I	UART2 receive signal (RXD)	15, 26, 29, 37, 38, 39, 40, 44	15, 26, 29, 37, 38, 39, 40, 44	18, 25, 26, 28	21, 28, 29, 31	17, 24, 25, 27	17, 18, 20	17, 19	15, 17, 8
UART2_TX	O	UART2 transmit signal (TXD)	14, 25, 28, 36, 39, 40, 43	14, 25, 28, 36, 39, 40, 43	17, 25, 26, 27	20, 28, 29, 30	24, 25, 26	17, 18, 19	17, 18	15, 16

6.4 Connections for Unused Pins

Table 6-15 lists the correct termination of unused pins.

Table 6-15. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx and PBx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup/ pulldown resistor.
NRST	VCC	NRST is an active-low reset signal; it must be pulled high to VCC or the device will not start, for more information refer to Section 9.1

(1) Any unused pin with a function that is shared with general-purpose I/O should follow the "PAx and PBx" unused pin connection guidelines.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin, with respect to VSS	–0.3	4.1	V
V_I	Input voltage	Applied to any 5-V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD} (3)	Current into VDD pin (source)	-40°C ≤ Tj ≤ 130°C		80	mA
		-40°C ≤ Tj ≤ 85°C		100	mA
I_{VSS} (3)	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 130°C		80	mA
		-40°C ≤ Tj ≤ 85°C		100	mA
I_{IO}	Current for SDIO pin	Current sunk or sourced by SDIO pin		6	mA
	Current for ODIO pin	Current sunk by ODIO pin		20	mA
I_D	Supported diode current	Diode current at any device pin		±2	mA
Tj	Junction temperature		-40	130	°C
T_{stg}	Storage temperature(2)		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Higher temperatures can be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(3) For applications operating at VDD=1.62V, I_VDD/I_VSS<=20mA is required to maintain device functionality

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC-Q100-011 , All pins	±500	V
		Charged device model (CDM), per AEC-Q100-011 , Corner pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage (3)	1.62(4)		3.6	V
C_{VDD}	Capacitor placed between VDD and VSS (1)		10		uF
T_A	Ambient temperature	–40		125	°C
T_J	Max junction temperature			130	°C
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state (2)			32	MHz
	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states (2)			24	

(1) Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}.
(2) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software.
(3) There is no dependency on MCLK frequency with respect to VDD recommended operating range.
(4) Functionality is designed down to $V_{BOR0-(min)}$.

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7.4 Thermal Information

THERMAL METRIC[1]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT)	78.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		35.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		50.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		TBD	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-32 (DGS32)	73.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		40.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		37.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		TBD	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-28 (DGS28)	80.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		42.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-24 (RGE)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		TBD	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-20 (DGS20)	92.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		35.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		49.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		49.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	WQFN-20 (RUK)	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		48.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		21.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		21.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		7.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	3	TBD	3	TBD	3	TBD	3	TBD	3	TBD	mA
IDD_{RUN}, per MHz	MCLK=SYSOSC, While(1), execute from flash	32MHz	53	TBD	53	TBD	53	TBD	53	TBD	53	TBD	uA/Mhz
	MCLK=SYSOSC, CoreMark, execute from flash		92	TBD	92	TBD	92	TBD	92	TBD	92	TBD	
SLEEP Mode													
IDD_{SLEEP}	MCLK=SYSOSC, CPU is halted	32MHz	1348	TBD	1350	TBD	1351	TBD	1354	TBD	1363	TBD	uA
IDD_{SLEEP}	MCLK=LFCLK, CPU is halted	32kHz	536	TBD	536	TBD	538	TBD	542	TBD	552	TBD	uA

7.5.2 STOP/STANDBY Modes

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0	4MHz	416	TBD	419	TBD	421	TBD	423	TBD	428	TBD	uA
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	81	TBD	83	TBD	85	TBD	87	TBD	92	TBD	
STANDBY Mode													
IDD_{STBY0}	LFXT and RTC enabled		2.7	TBD	2.7	TBD	3.9	TBD	5.5	TBD	9.9	TBD	
	LFOSC and IWDT enabled		2.3	TBD	2.3	TBD	3.5	TBD	5.1	TBD	9.6	TBD	
	LFXT and RTC enabled, IWDT enabled		2.7	TBD	2.7	TBD	3.9	TBD	5.5	TBD	9.9	TBD	
	STOPCLKSTBY=0, TIMG0 enabled	32kHz	2.3	TBD	2.3	TBD	3.5	TBD	5.1	TBD	9.6	TBD	uA
IDD_{STBY1}	STOPCLKSTBY=1, TIMG0 enabled		1.9	TBD	2	TBD	3.2	TBD	4.8	TBD	9.3	TBD	
	STOPCLKSTBY=1, GPIOA enabled		1.9	TBD	2	TBD	3.2	TBD	4.8	TBD	9.3	TBD	

7.5.3 SHUTDOWN Mode

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		-40°C		25°C		85°C		105°C		125°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{SHDN}	Supply current in SHUTDOWN mode	50	TBD	63	TBD	235	TBD	485	TBD	1230	TBD	nA

7.6 Power Supply Sequencing

7.6.1 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

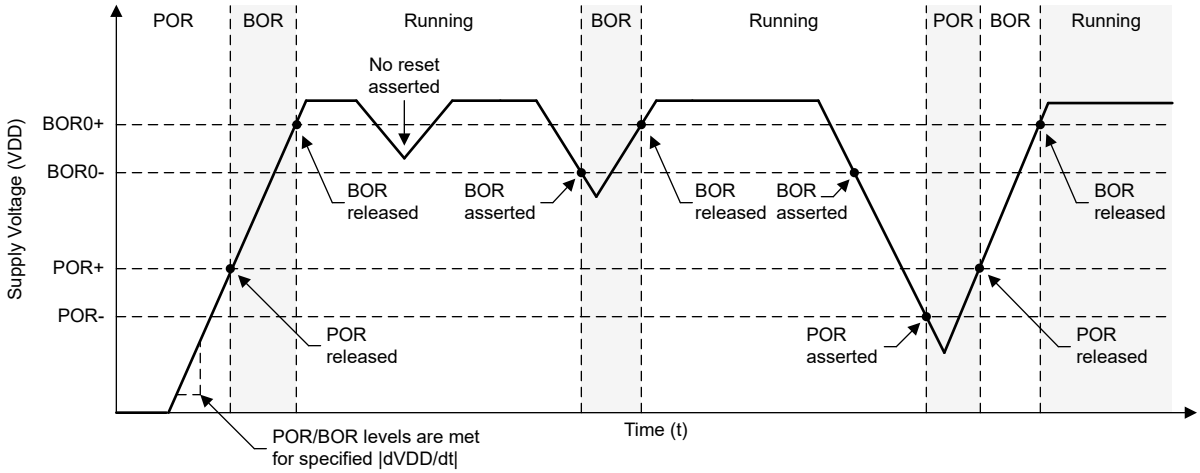

Figure 7-1. Power Cycle POR/BOR Conditions - VDD

7.6.2 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (1)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising(1)	0.95	1.30	1.59	V
V_{POR-}		Falling (1)	0.9	1.25	1.54	V
$V_{HYS, POR}$	POR hysteresis	(1)	30	58	74	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	-40 °C ≤ Ta ≤ 25 °C, Cold start, rising (1)	1.50	1.56	1.63	V
		25 °C ≤ Ta ≤ 125 °C, Cold start, rising (1)	1.51	1.58	1.65	
V_{BOR0+}		Rising (1)	1.56	1.59	1.62	
V_{BOR0-}		Falling (1)	1.55	1.58	1.61	
$V_{BOR0, STBY}$		STANDBY mode (1)	1.51	1.56	1.61	
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1)	2.13	2.17	2.21	V
V_{BOR1-}		Falling (1)	2.10	2.14	2.18	
$V_{BOR1, STBY}$		STANDBY mode (1)	2.06	2.13	2.20	
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1)	2.73	2.77	2.82	V
V_{BOR2-}		Falling (1)	2.7	2.74	2.79	
$V_{BOR2, STBY}$		STANDBY mode (1)	2.62	2.71	2.8	
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1)	2.88	2.96	3.04	V
V_{BOR3-}		Falling (1)	2.85	2.93	3.01	
$V_{BOR3, STBY}$		STANDBY mode (1)	2.82	2.92	3.02	
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (1)		15	21	mV
		Levels 1-3 (1)		34	40	
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			5	us
		STANDBY mode			100	us

(1) Device operating in RUN, SLEEP, or STOP mode.

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7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta		2		mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta		2.5		mA
Endurance						
$NWEC_{(LOWER)}$	Erase/program cycle endurance (lower 32kB flash) (1)		100			k cycles
$NWEC_{(UPPER)}$	Erase/program cycle endurance (remaining flash) (1)		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C ≤T_j ≤ 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C ≤T_j ≤ 105°C	11.4			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 64)}$	Program time for flash word (4) (6)			50	275	µs
$t_{PROG\ (SEC,\ 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤2k erase/program cycles, T_j≥25°C		4	20	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles, T_j≥25°C		20	150	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles		20	200	ms
$t_{ERASE\ (BANK)}$	Bank erase time	≤10k erase/program cycles		22	220	ms

(1) The lower 32kB flash address space supports higher erase/program endurance to enable EEPROM emulation applications. On devices with <=32kB flash memory, the entire flash memory supports $NWEC_{(LOWER)}$ erase/program cycles.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE,\ SLEEP}$	Wakeup time from SLEEP to RUN (1)			2		cycles
$t_{WAKE,\ STOP}$	Wakeup time from STOP1 to RUN (SYSOSC enabled) (1)			14		us
	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)			13		us

VDD=3.3V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE, STBY}$	Wakeup time from STANDBY to RUN (1)			15		us
$t_{WAKE, SHDN}$	Wakeup time from SHUTDOWN to RUN	Fast boot enabled		214		us
$t_{WAKE, SHDN}$	Wakeup time from SHUTDOWN to RUN	Fast boot disabled		230		us
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2		0.9		us
		Mode is STOP1		2.4		us
		Mode is STOP2		0.9		us
		Mode is STANDBY1		3.2		us
Startup Timing						
$t_{START, RESET}$	Device cold start-up time from reset/ power-up (2)	Fast boot enabled		241		us
		Fast boot disabled		284		us
NRST Timing						
$t_{RST, BOOTRST}$	Minimum pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		2		us
		ULPCLK=32kHz		100		us
$t_{RST, POR}$	Minimum pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external signal (GPIO wake-up event) to the time that the first CPU instruction is executed, with the GPIO glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1)
(2) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled	SETUSEFCL=1, T_a = 25 ℃	-1.2		1.2	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-2.1		1.6	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	–2.5		2.5	%
$t_{settle, SYSOSC}$	Settling time to target accuracy (1)	SETUSEFCL=1			30	us

(1) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to $f_{settle,SYSOSC}$ for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 125 ℃	–5		5	%
		-40 ℃ ≤ T_a ≤ 85 ℃	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{start, LFOSC}$	LFOSC start-up time			1		ms

7.9.3 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
		HFXTRSEL=01	8.01		16	
		HFXTRSEL=10	16.01		32	
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
		HFXTRSEL=01	40		60	
		HFXTRSEL=10	40		60	
		HFXTRSEL=11	40		60	
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, HFXT}$	HFXT start-up time (2)			0.5		ms
I_{HFXT}	HFXT current consumption	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		75		µA
		f_{HFXT}=32MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency (3)	USEEXTHFCLK=1	4		32	MHz
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{HFXIN} \times C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT})$, where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual.
(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.9.4 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, LFXT}$	LFXT start-up time			483	640	ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=TBD, LOWCAP=TBD		200		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency (2)	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle (2)	SETUSEEXLF=1	40		60	%
LFCLK Monitor						

ADVANCE INFORMATION

7.9.4 Low Frequency Crystal/Clock (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{FAULTLF}$	LFCLK monitor fault frequency (3)	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(3) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.10 *Digital IO*

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO (1)	VDD≥1.62V	0.7*VDD		5.5	V
			VDD≥2.7V	2		5.5	V
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	V
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
			VDD≥2.7V	-0.3		0.8	V
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			V
I_{lkg}	High-Z leakage current	SDIO(2) (3)				50(4)	nA
R_{PU}	Pull up resistance	All I/O except ODIO			40		kΩ
R_{PD}	Pull down resistance				40		kΩ
C_I	Input capacitance				5		pF
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA			0.4	V
		ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA			0.5	
V_{OH}	High level output voltage	SDIO	VDD ≥ 2.7V, $I_{OH,max}$ = 6mA	VDD-0.5			V
			VDD ≥ 1.71V, $I_{OH,max}$ = 2mA	VDD-0.4			V

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(4) This value is for SDIO not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be as high as 100nA.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO (1)	VDD ≥ 1.71V, C_L= 20pF			16	MHz
			VDD ≥ 2.7V, CL= 20pF			32	
		ODIO	VDD ≥ 1.71V, FM^+, CL= 20pF - 100pF			1	
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 1.71V, C_L= 20pF			3.5	ns

ADVANCE INFORMATION

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 2.7V, C_L= 20pF			6.6	ns
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM^+, CL= 20pF-100pF	20*VDD/5.5		120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA
		MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz		10.6		
$t_{START,VBST}$	VBOOST startup time			12	20	us

7.12 *ADC*

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from external reference pin (VREF+)	1.4		VDD	V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), External Reference			1.6	Msps
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 1.6MSPS, External reference, V_{R+} = VDD		350		µA
		F_S = 500ksps, Internal reference, V_{R+} = VREF = 2.5V		300		
$C_{S/H}$	ADC sample-and-hold capacitance			0.22		pF
Rin	ADC sampling switch resistance			15		kΩ
ENOB	Effective number of bits	Internal reference, V_{R+} = VREF = 2.5V, F_{in} = 10KHz	9.4	10.2		bit
		External reference, F_{in} = 10KHz (2)	10	10.8		
SNR	Signal-to-noise ratio	External reference (2)		68		dB
		Internal reference, V_{R+} = VREF = 2.5V		64		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference (2), VDD = $VDD_{(min)}$ to $VDD_{(max)}$		68		dB
		VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 2.5V		61		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference (2), ΔVDD = 0.1 V at 1 kHz		61		dB
		ΔVDD = 0.1 V at 1 kHz Internal reference, V_{R+} = VREF = 2.5V		49		
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor (3)	-1.5		+1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin
(3) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.

ADVANCE INFORMATION

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency			4		32	MHz
$t_{ADC\ trigger}$	Software trigger minimum width			3			ADCCLK cycles
t_{Sample_step}	Sampling time for step input	12-bit mode, R_S = 50Ω, C_{pext} = 10pF		0.188			µs
t_{Sample_VREF}	Sample time with internal VREF input		ADC CHANNEL=29,12-bit mode, VDD as reference	10			µs
$t_{Sample\_SupplyMon}$	Sample time with Supply Monitor (VDD/3)	12-bit mode		5			µs

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL)	External reference (2)	-2.0		+2.0	LSB
E_D	Differential linearity error (DNL) Designed for no missing codes	External reference, 12-bit (2)	-1.0		+1.0	LSB
E_O	Offset error	External reference (2)	-5		5	mV
		Internal reference, V_{R+} = VREF = 2.5V	-5		5	mV
E_G	Gain error	External reference (2)	-5		5	mV

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(\ E_I{}^2 + |E_O|^2 + E_G{}^2\ )}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate

(2) All external reference specifications are measured with VR+ = VREF+ = VDD = 3.3V and VR- = VREF- = VSS = 0V and external 1uF cap on VREF+ pin

7.12.4 Typical Connection Diagram

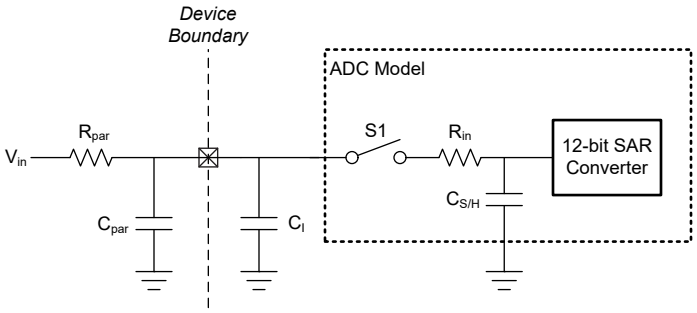

Figure 7-2. ADC Input Network

1. Refer to Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to Electrical Characteristics for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. Tau = $(R_{par} + R_{in})^* C_{S/H} + R_{par}^*(C_{par} + C_I)$
2. K= $\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (Min sampling time) = K*Tau

ADVANCE INFORMATION

7.13 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (internal VREF), BUFCONFIG=1h (1.4V VREF), ADC t_{Sample}=10µs	27	30	33	℃
TS_c	Temperature coefficient		-1.84	-1.75	-1.66	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (2)			2.5	10	us

(1) Higher absolute accuracy may be achieved through user calibration.
(2) This is the maximum time required for the temperature sensor to settle when measured by the ADC. It may be used to specify the minimum ADC sample time when measuring the temperature sensor.

ADVANCE INFORMATION

7.14 VREF

7.14.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		80	100	µA
TC_{VREF}	Temperature coefficient of VREF (1)	BUFCONFIG = {0, 1}			75	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7V to VDDmax, BUFCONFIG = 1	60	70		dB
		VDD = 2.7V to VDDmax, BUFCONFIG = 0	50	60		
V_{noise}	RMS noise at VREF output (0.1 Hz to 100MHz)	BUFFCONFIG = 1		350		µVrms
		BUFFCONFIG = 0		500		
ADC F_S	Max supported ADC sampling frequency	Using VREF as ADC reference			515	ksps
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8V			30	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.14.2 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.379	1.4	1.421	V
		BUFCONFIG = 0	2.462	2.5	2.538	

7.15 *Comparator (COMP)*

7.15.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage		-20		20	mV
V_{hys}	DC input hysteresis	HYST=00h		0.4		mV
		HYST=01h		10		
		HYST=02h		20		
		HYST=03h		30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode			5	µs
		Startup time to reach propagation delay specification, Low Power Mode			10	µs

ADVANCE INFORMATION

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA
8-bit DAC Electrical Characteristics						
V_{dac}	DAC output range		0		VDD	V
$V_{dac-code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
Output Impedance	8-bit DAC output impedance			50		kΩ
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB, DAC output on pin PA11, Cload = 15pF		6		µs
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		µs

7.16 *I2C*

7.16.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0	2	32	8	32	20	32	MHz
f_{SCL}	SCL clock frequency			0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	Low period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us

ADVANCE INFORMATION

7.16.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.16.3 I²C Timing Diagram

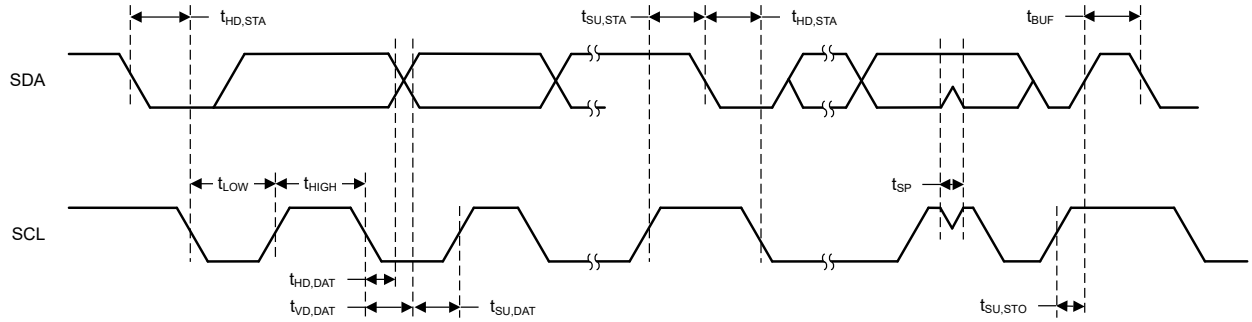

Figure 7-3. I2C Timing Diagram

7.17 SPI

7.17.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.62 < VDD < 3.6V Controller mode			16	MHz
f_{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.62 < VDD < 3.6V Peripheral mode			16	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK\_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1 SPI Clock			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1 SPI Clock			ns
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI Clock	ns
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance				1 SPI Clock	ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
		1.62 < VDD < 2.7V, delayed sampling enabled	8			
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	30			ns
		1.62 < VDD < 2.7V, no delayed sampling	39			

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over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HD.CI}$	POCI input data hold time		0			ns
$t_{VALID.CO}$	PICO output data valid time (2)				16	ns
$t_{HD.CO}$	PICO output data hold time (3)		1			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		13.5			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				40	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance				40	ns
$t_{SU.PI}$	PICO input data setup time		15			ns
$t_{HD.PI}$	PICO input data hold time		31.25			ns
$t_{VALID.PO}$	POCI output data valid time(2)	2.7 < VDD < 3.6V			31	ns
$t_{VALID.PO}$	POCI output data valid time(2)	1.62 < VDD < 2.7V			40	ns
$t_{HD.PO}$	POCI output data hold time(3)		5.5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.17.2 SPI Timing Diagram

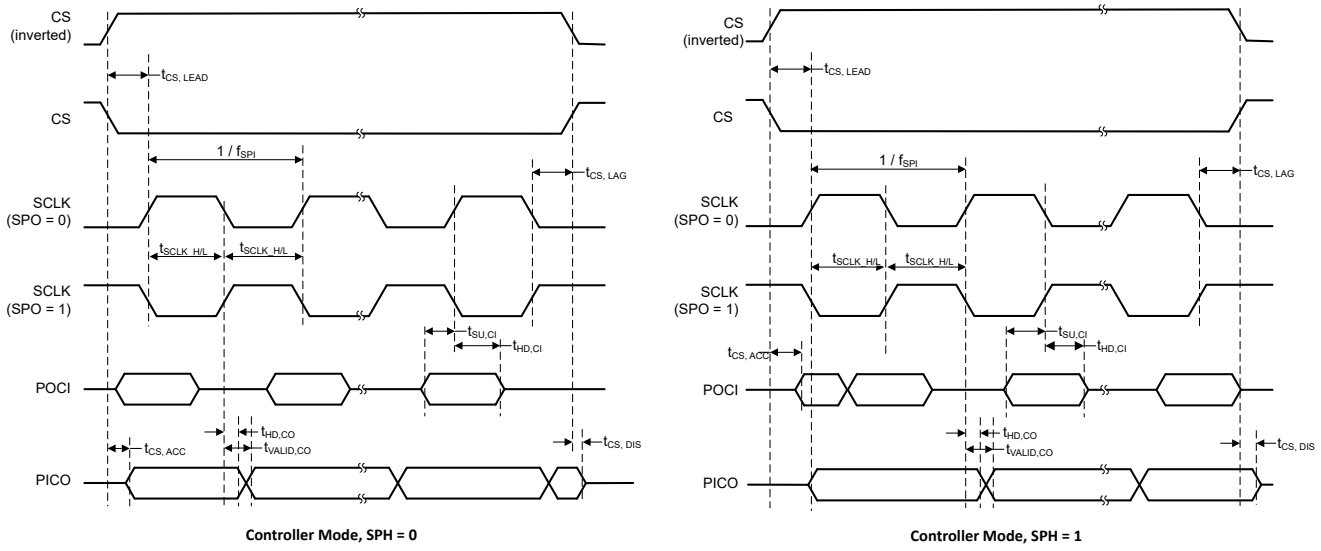

Figure 7-4. SPI Timing Diagram - Controller Mode

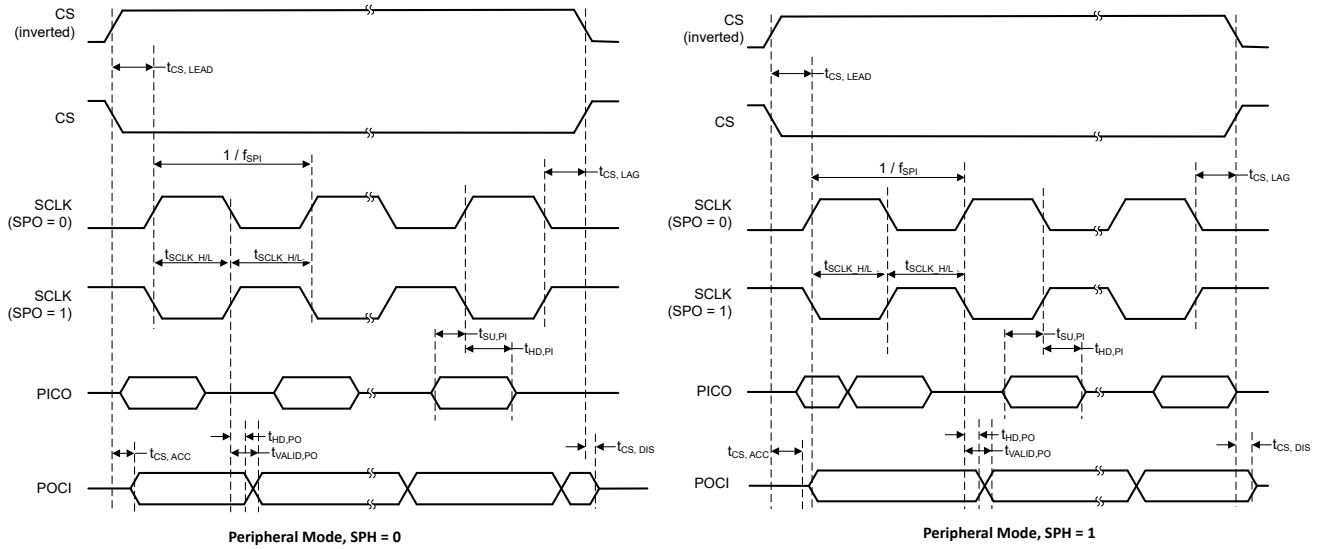

Figure 7-5. SPI Timing Diagram - Peripheral Mode

7.18 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency				32	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				4	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.19 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 64MHz	16.625			ns
		$f_{TIMxCLK}$ = 32MHz	31.25			ns
			1			$t_{TIMxCLK}$
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 64MHz	0.01563		1024	us
		$f_{TIMxCLK}$ = 32MHz	0.03125		2048	us
			1		65536	$t_{TIMxCLK}$

7.20 Emulation and Debug

7.20.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

ADVANCE INFORMATION

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.1 Overview

MSPM0C1105/6 microcontrollers (MCUs) are part of MSP's highly integrated, ultra-low-power 32-bit MSPM0 MCU family based on the Arm® Cortex®-M0+ 32-bit core platform, operating at up to 32MHz frequency. These costoptimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 1.62V to 3.6V.

The MSPM0C1105/6 devices provide up to 64KB embedded flash program memory with 8KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy from -2.1% to +1.6%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.6Msps ADC with VDD as the voltage reference, a comparator with 8-bit reference DAC and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as one 16-bit advanced timer with deadband and timer frequency up to 64MHz, four 16-bit general purpose timer, one windowed watchdog timer, and a variety of communication peripherals including three UART, one SPI, and two I2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

For complete module descriptions, see the MSPM0 C-Series Microcontrollers Technical Reference Manual.

8.2 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction pre-fetch/cache, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized, 32-bit CPU which delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supporting clock frequencies up to 32kHz
  - ARMv6-M Thumb instruction set (little endian) with 32-cycle 32x32 slow multiply instruction
- Pre-fetch logic to improve sequential code execution, and I-cache with two 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining

8.3 Operating Modes

MSPM0 MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0 devices implement two power domains: **PD1** (for the CPU, memories, and high performance peripherals), and **PD0** (for low speed, low power peripherals).

- **PD1** is always powered in RUN and SLEEP modes, but is disabled in all other modes.
- **PD0** is always powered in RUN, SLEEP, STOP, and STANDBY modes.
- **PD1** and **PD0** are both disabled in SHUTDOWN mode.

8.3.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in Supported Functionality by Operating Mode.

Functional key:

- **EN**: The function is enabled in the specified mode.

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- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode but is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Mode

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT(1)	DIS	DIS	DIS	OFF
	LFOSC	EN										OFF
Clocks	CPUCLK	32M	32k	32k	DIS							OFF
	MCLK to PD1	32M	32k	32k	32M	32k	32k	DIS				OFF
	ULPCLK to PD0	32M	32k	32k	32M	32k	32k	4M(1)	32k		DIS	OFF
	ULPCLK to TIMG14/8	32M	32k	32k	32M	32k	32k	4M(1)	32k			OFF
	RTCCLK	32k										OFF
	MFCLK	OPT	DIS		OPT	DIS		OPT	DIS			OFF
	LFCLK	32k									DIS	OFF
	LFCLK to TIMG14/8	32k										OFF
	MCLK Monitor	OPT									DIS	OFF
	LFCLK Monitor	OPT										OFF
PMU	POR Monitor	EN										OFF
	BOR Monitor	EN										OFF
	Core Regulator	FULL DRIVE						REDUCED DRIVE		LOW DRIVE		OFF
Core Functions	CPU	EN			DIS							OFF
	DMA	OPT						NS (triggers supported)				OFF
	Flash	EN						OPT		DIS		OFF
	SRAM	EN						OPT		DIS		OFF
PD1 Peripherals	SPI0	OPT						DIS				OFF
	CRC	OPT						DIS				OFF
PD0 Peripherals	TIMG14/8	OPT										OFF
	TIMG1/2	OPT									DIS	OFF
	TIMA0	OPT									DIS	OFF
	UART0/1/2	OPT									DIS	OFF
	I2C0/1	OPT									DIS	OFF
	GPIOA/B	OPT									OPT2	OFF
	WWDT0	OPT									OPT(2)	OFF
	IWDT	OPT										OFF
	RTC_B	OPT										OFF

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Table 8-1. Supported Functionality by Operating Mode (continued)

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
Analog	ADC0	OPT							NS (triggers supported)			OFF
	COMP	OPT										OFF
	VREF	OPT							NS			OFF
	Temperature Sensor	OPT								OFF		OFF
IOMUX and IO Wakeup		EN										DIS w/ WAKE
Wake Sources		N/A			ANY IRQ			PD0 IRQ				IOMUX, NRST, SWD

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32kHz as it was in RUN2.
(2) When using the STANDBY1 policy for STANDBY, only TIMG14 and TIMG8 is clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

8.4 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY mode to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted
- 4 bytes of shutdown memory

For more details, see the PMU chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.5 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32kHz)
- **SYSOSC**: Internal high-frequency oscillator (32MHz with factory trim)
- **LFXT/LFCKIN** : low-frequency external crystal oscillator or digital clock input (32kHz)
- **HFXT/HFCKIN**: high-frequency external crystal oscillator or digital clock input (4MHz to 32MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes

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- **RTCCLK**: Fixed 32kHz clock direct to RTC
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High speed clock derived from HFCLK, available in RUN and SLEEP mode

For more details, see the CKM chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.6 DMA_B

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA_B in these devices support the following key features:

- 3 DMA transfer channel
  - 2 full-feature channels, supporting repeated transfer modes
  - 1 basic channel, supporting single transfer mode
- Configurable DMA channel priorities
- Direct peripheral to DMA trigger is supported from ADC, UART, SPI or timer triggers.
- Byte (8-bit), short word (16-bit) and word (32-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications
- Gather mode

Table 8-2 shows the DMA features that are supported and the corresponding DMA channel numbers.

Table 8-2. DMA_B Channel Features

DMA Feature	DMA_B	
	Full-Feature Channel	Basic Channel
Channel Number	0, 1	2
Repeated mode	✓	–
Table & fill mode	✓	–
Gather mode	✓	–
Early IRQ notification	✓	–
Auto enable	✓	✓
Long long (128-bit) transfer	✓	✓
Stride mode	✓	✓
Cascading channel support	✓	✓

Table 8-3 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-3. DMA Trigger Mapping

DMACTL.DMATSEL	TRIGGER SOURCE
0	Software
1	Generic Subscriber 0 (FSUB_0)
2	Generic Subscriber 0 (FSUB_1)
9	UART0 PUBLISHER 1
10	UART0 PUBLISHER 2
13	UART2 PUBLISHER 1

Table 8-3. DMA Trigger Mapping (continued)

DMACTL.DMATSEL	TRIGGER SOURCE
14	UART2 PUBLISHER 2
7	SPI0 PUBLISHER 1
8	SPI0 PUBLISHER 2
5	I2C1 PUBLISHER 1
6	I2C1 PUBLISHER 2
3	I2C0 PUBLISHER 1
4	I2C0 PUBLISHER 2
15	ADC0 EVT g
11	UART1 PUBLISHER 1
12	UART1 PUBLISHER 2

8.7 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events which are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the EVENT chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

Table 8-4. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
6	Generic event channel 5 selected	1:1
7	Generic event channel 5 selected	1 : 2 (splitter)
8	Generic event channel 6 selected	1 : 2 (splitter)

8.8 Memory

8.8.1 Memory Organization

Table 8-5 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 C-Series Microcontrollers Technical Reference Manual* .

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Table 8-5. Memory Organization

Memory Region	Subregion	MSPM0C1105	MSPM0C1106
Code (Flash)	Flash	32KB(1) 0x0000.0000 to 0x0000.7FFF	64KB(1) 0x0000.0000 to 0x0000.FFFF
SRAM (SRAM)	SRAM	8KB 0x2000.0000 to 0x2000.1FFF	8KB 0x2000.0000 to 0x2000.1FFF
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	Flash	0x0040.0000 to 0x0040.7FFF	0x0040.0000 to 0x0040.9FFF
	Configuration NVM	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200
	FACTORY	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

(1) First 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program/erase cycles.

8.8.2 Peripheral File Map

Table 8-6 lists the available peripherals and the register base address for each.

Table 8-6. Peripherals Summary

PERIPHERAL NAME	BASE ADDRESS	SIZE
COMP0	0x40008000	0x00001F0
VREF	0x40030000	0x00001F0
WWDT0	0x40080000	0x0000150
TIMG14	0x40084000	0x00001F0
TIMG1	0x40086000	0x00001F0
TIMG2	0x40088000	0x00001F0
TIMG8	0x40090000	0x00001F0
LFSS	0x40094000	0x0000160
RTC_B	0x40094000	0x0000160
IWDT	0x40094000	0x0000160
GPIOA	0x400A0000	0x00001F0
GPIOB	0x400A2000	0x00001F0
SYSCTL	0x400AF000	0x0000310
DEBUGSS	0x400C7000	0x00001F0
EVENTLP	0x400C9000	0x0000300
FLASHCTL	0x4042A000	0x00001F0
I2C0	0x40440000	0x0000200
I2C1	0x400CD000	0x0000200
UART1	0x400F0000	0x00001F0
UART2	0x400F2000	0x00001F0
UART0	0x40100000	0x00001F0
CPUSS	0x40102000	0x00001F0
WUC	0x40108000	0x00001F0
IOMUX	0x40400000	0x00001F0
DMA	0x40424000	0x0000050
CRC	0x40428000	0x0000200
SPI0	0x40468000	0x00001F0
ADC0_SVT	0x4055A000	0x0000100

Table 8-6. Peripherals Summary (continued)

PERIPHERAL NAME	BASE ADDRESS	SIZE
TIMA0	0x40860000	0x00001F0

8.8.3 Peripheral Interrupt Vector

Table 8-7shows the IRQ number and the interrupt group number for each peripheral in this device.

Table 8-7. Interrupt Vector Number

PERIPHERAL NAME	NVIC IRQ
SYSCTL	0
DEBUGSS	1
TIMG8	2
UART1	3
ADC0	4
COMP0	7
UART2	8
SPI0	9
UART0	11
TIMG14	12
TIMG2	15
TIMA0	16
TIMG1	17
GPIOA	18
GPIOB	19
I2C0	22
I2C1	23
FLASHCTL	24
WWDT0	25
LFSS	27
RTC_B	29
IWDT	30
DMA	31

8.9 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 100,000 program/erase cycles on 32 selected sectors of the flash memory, with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32kB support 100,000 cycles on the entire flash memory)

For more details, see the NVM chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.10 SRAM

MSPM0Cxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY operating modes and is lost in SHUTDOWN mode. A write protection mechanism is provided to allow the application to dynamically write protect the SRAM memory with 1KB resolution.
Write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.11 GPIO

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A and Port B GPIO peripheral, these devices support up to 45 GPIO pins.

The key features of the GPIO module include:

- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

For more details, see the GPIO chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.12 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.13 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.6-Msps with 10.2-bit ENOB
- Up to 27 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- Software selectable reference:
  - Configurable internal dedicated ADC reference voltage of 1.4V or 2.5V (VREF)
  - MCU supply voltage (VDD)
  - Support for bringing in an external reference on VREF+/- device pins
  - Requires a decpoupling capacitor placed on VREF+/- pins for proper operation.
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-8. ADC0 Channel Mapping

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME
0	A0	16	A16
1	A1	17	A17
2	A2	18	A18
3	A3	19	A19
4	A4	20	A20
5	A5	21	A21
6	A6	22	A22
7	A7	23	A23
8	A8	24	A24
9	A9	25	A25
10	A10	26	A26

Table 8-8. ADC0 Channel Mapping (continued)

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME
11	A11	27	Reserved
12	A12	28	*Temperature Sensor*
13	A13	29	VREF
14	A14	30	Reserved
15	A15	31	*Supply/Battery Monitor*

Italicized signal names are internal to the SoC. These signals are used for internal peripheral interconnections.

For more details, see the ADC chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual.*

8.14 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4V internal VREF at the factory trim temperature (TS_{TRIM}). This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the *MSPM0 C-Series Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.15 Low-Frequency Sub System (LFSS)

The Low-Frequency Sub-System (LFSS) is a sub-system which combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low freqency clock (LFCLK) or need to be active during low power modes. The LFCLK has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS in this device contains following components:

- *Real Time Clock* with additional prescalar extension and timestamp captures
- An asynchronous IWDT

For more details, see the LFSS chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.16 VREF

The shared voltage reference module (VREF) in these devices contain a configurable voltage reference buffer which allows users to supply a stable reference to on-board analog peripherals. It also supports bringing in an external reference for applications where higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references. Same reference voltage will be selected for ADC and COMP
- Internal reference supports ADC operation up to 515ksps
- Support for bringing in an external reference on VREF+ and VREF- device pins

For more details, see the VREF chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.17 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

- Programmable hysteresis

- Programmable reference voltage:
  - External reference voltage (VREF IO)
  - Integrated 8-bit reference DAC
- Configurable operation modes:
  - High speed mode
  - Lower power mode
- Programmable output glitch filter delay
- Supports 6 blanking sources from TIMx instances (see Table 8-10)
- Support output wake up device from all low power modes
- Output connected to advanced timer fault handling mechanism
- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins
- 8-bit reference DAC can be used to output to device pins

Table 8-9. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x3	COMP0_IN3+	-
0x5	-	Temperature Sensor

Table 8-10. COMP0 Blanking Source Table

CTL2.BLANKSRC	Blanking Source Selected
1	TIMA0.CC2
2	TIMA0.CC3
3	TIMA0.CC1
4	TIMG0.CC1
5	TIMG1.CC1
6	TIMG8.CC1

For more information about device analog connections, refer to Section 8.27.

For more details, see the COMP chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.18 Security

This device offers several security features, including:

- Debug security
- Unique Die ID
- Flexible firewalls for protecting code and data
  - Flash write-erase protection
  - Flash read-execute protection
  - Flash IP protection
  - SRAM write-execute mutual exclusion
- Secure boot
- Secure firmware update
- Customer secure code
- Cyclic redundancy checker (CRC-16) with support for custom polynomial

For more details, see the Security chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*

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8.19 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for bit reversal

For more details, see the CRC chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.20 UART

The UART peripherals (UART0, UART1, UART2) provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See Table 8-11 for detail information on supported protocols.

Table 8-11. UART Features

UART Features	UART0(Extend)	UART1, UART2(Main)
Active in Stop and Standby Mode	Yes	Yes
Separate transmit and receive FIFOs	Yes	Yes
Support hardware flow control	Yes	Yes
Support 9-bit configuration	Yes	Yes
Support LIN mode	Yes	-
Support DALI	Yes	-
Support IrDA	Yes	-
Support ISO7816 Smart Card	Yes	-
Support Manchester coding	Yes	-

For more details, see the UART chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.21 I2C

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100kbps
- Support Fast-mode (Fm), with a bit rate up to 400kbps
- Support Fast-mode Plus (Fm+), with a bit rate up to 1Mbps
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression

For more details, see the I2C chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.22 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 16Mbits/s in both controller and peripheral mode
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode)
- Programmable data frame size from 7 bits to 16 bits (peripheral mode)
- Separated transmit and receive FIFOs support DMA data transfer
- Supports TI mode, Motorola mode, and National Microwire format

For more details, see the SPI chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.23 IWDT

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent power and clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter with closed and open window
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods

For more details, see the IWDT chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.24 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.25 RTC_B

The RTC_B instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. The RTC_B provides common key features in relation to the Low-Frequency Sub System (LFSS).

Common key features of the RTC_B include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128 Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5 Hz
- Calibration for crystal offset error (up to +/- 240ppm)

- Compensation for temperature drift (up to +/- 240ppm)
- RTC clock output to pin for calibration

Table 8-12 shows the RTC features supported in this device.

Table 8-12. RTC_B Key Features

RTC Features	RTC_B
Power enable register	-
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes
Selectable binary or binary-coded decimal (BCD) format	Yes
Leap-year correction (valid for year 1901 through 2099)	Yes
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes
Calibration for crystal offset error and crystal temperature drift (up to ±240 ppm total)	Yes
RTC clock output to pin for calibration (GPIO)	Yes
RTC clock output to pin for calibration (TIO)	-
Three -bit prescaler for heartbeat function with interrupt generation	-
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	-
RTC time stamp capture upon detection of a timer stamp event, including: • TIO event • VDD fail event	-
RTC counter lock function	-

For more details, see the RTC chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.26 Timers (TIMx)

The timer peripherals in these devices support the following key features. For specific configuration, see Table 8-13.

Specific features for the **general-purpose timer (TIMGx)** include:

- 16-bit down, up/down, or up counter with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode

- Support quadrature encoder interface (QEI) for positioning and movement sensing
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Cross-trigger event logic for Hall sensor inputs

Specific features for the **advanced timer (TIMAx)** include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Clock doubler to provide 2x clock source for improved timer resolution
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow register for load and CC register available
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to keep the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-13. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEAD-BAND	FAULT	QEI
TIMG14	PD0	16 bit	8 bit	–	4	–	–	–	–	–	–
TIMG1	PD0	16 bit	8 bit	–	2	–	–	–	–	–	–
TIMG2	PD0	16 bit	8 bit	–	2	–	–	–	–	–	–
TIMG8	PD0	16 bit	8 bit	–	2	–	–	–	–	–	Yes
TIMA0	PD0	16 bit	8 bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	–

For more details, see the TIMx chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

ADVANCE INFORMATION

8.27 Device Analog Connections

Figure 8-1 shows the internal analog connection of the device.

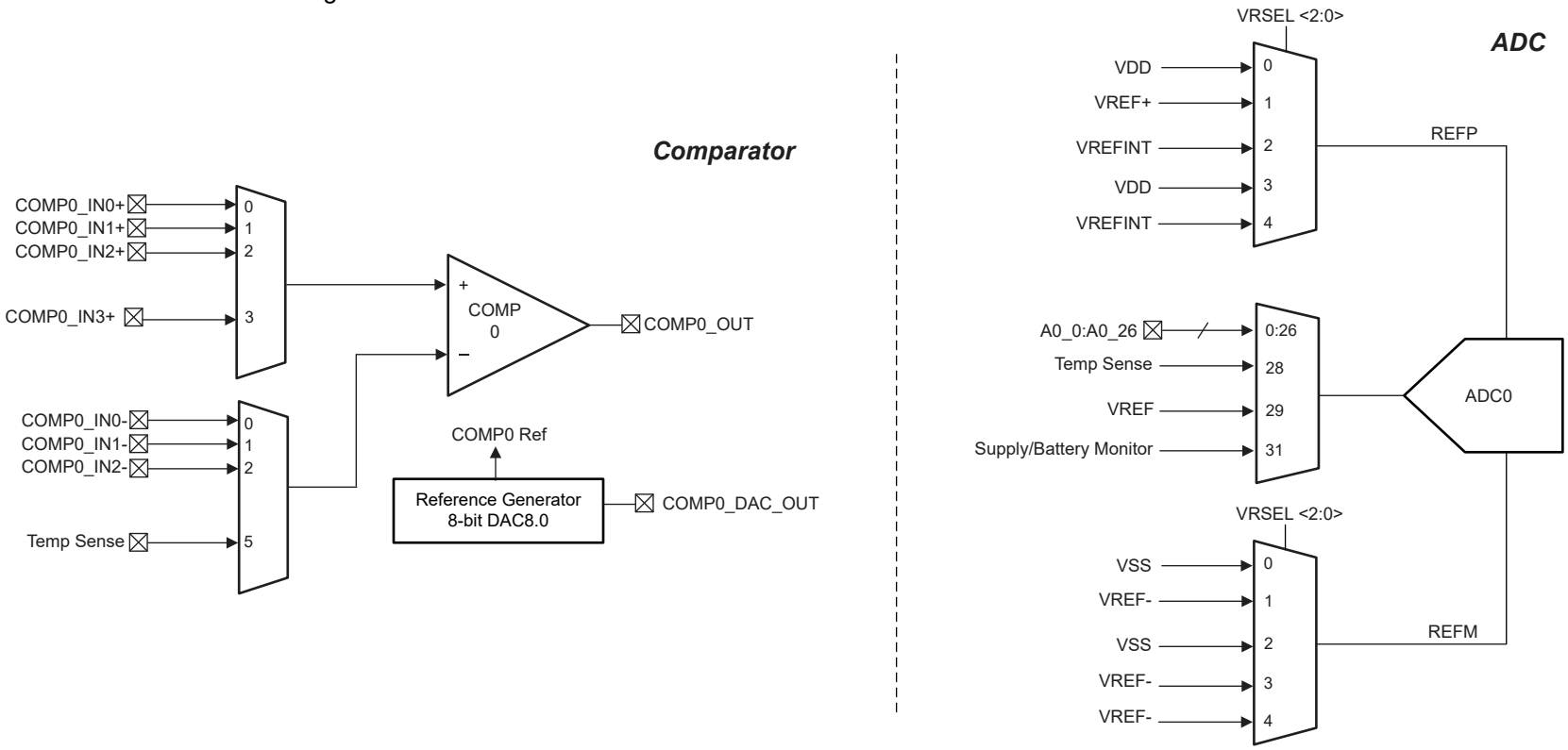


Figure 8-1. Device Analog Connection

ADVANCE INFORMATION

8.28 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-2. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

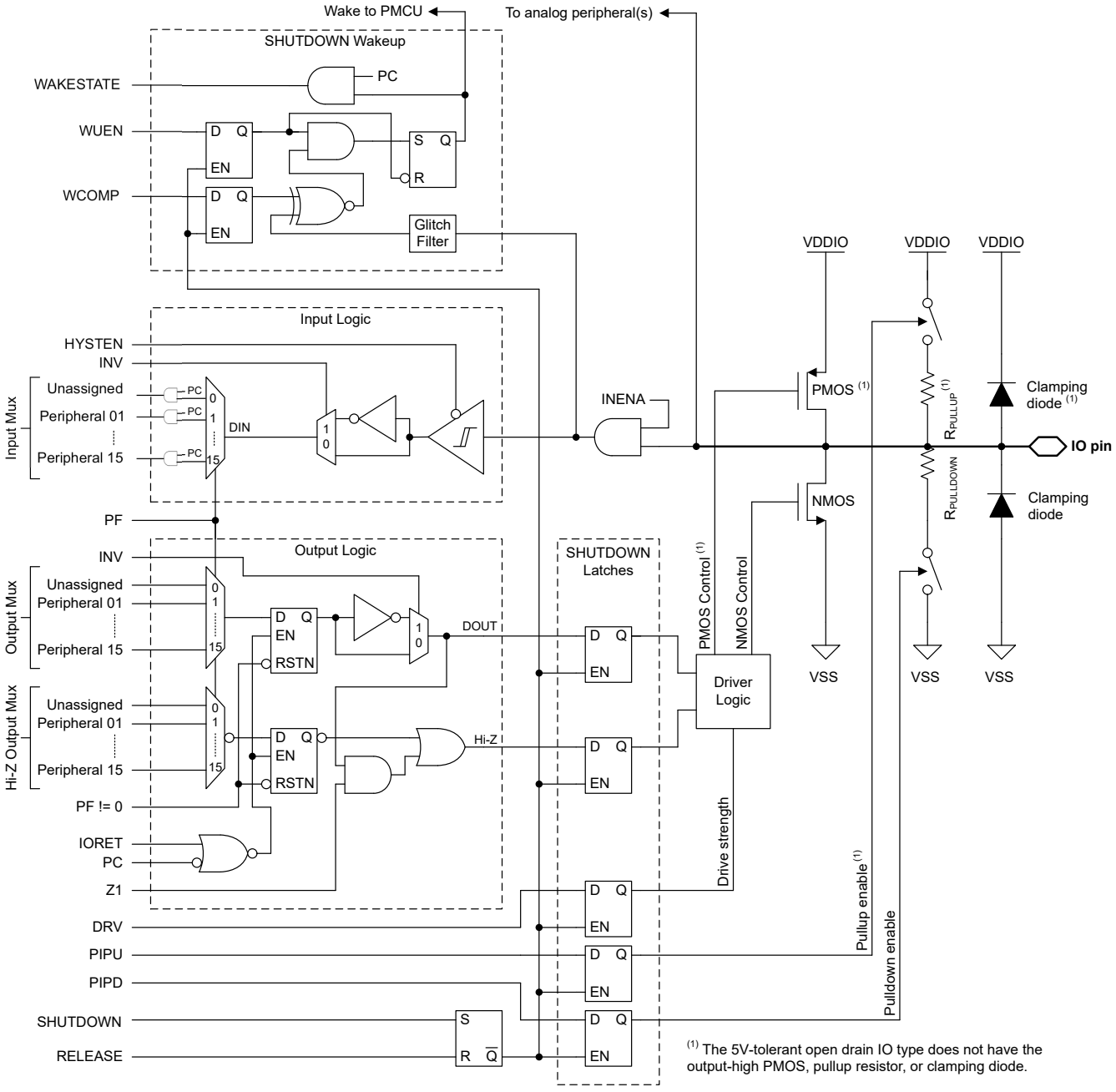


Figure 8-2. Superset Input/Output Diagram

ADVANCE INFORMATION

8.29 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device.

Table 8-14. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

For a complete description of the debug functionality offered on MSPM0 devices, see the Debug chapter of the *MSPM0 C-Series 32MHz Microcontrollers Technical Reference Manual*.

8.30 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please refer to Factory Constants chapter of the*MSPM0 C-Series Microcontrollers Technical Reference Manual* for more information.

Table 8-15. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER
MSPM0C1105	0x0BBB	0x17
MSPM0C1106	0x0BBB	0x17

Table 8-16. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	Part	Variant
M0C1105QPTRQ1	6CEE	43
M0C1105QDGS32RQ1	6CEE	44
M0C1105QDGS28RQ1	6CEE	45
M0C1105QDGS20RQ1	6CEE	46
M0C1105QRGZRQ1	6CEE	47
M0C11105QRHBRQ1	6CEE	48
M0C1105QRGERQ1	6CEE	49
M0C1105QRUKRQ1	6CEE	4A
M0C1106QPTRQ1	FA06	4B
M0C1106QDGS32RQ1	FA06	4C
M0C1106QDGS28RQ1	FA06	4D
M0C1106QDGS20RQ1	FA06	4E
M0C1106QRGZRQ1	FA06	4F
M0C11106QRHBRQ1	FA06	50
M0C1106QRGERQ1	FA06	51
M0C1106QRUKRQ1	FA06	52

8.31 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to the Factory Constants chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual* for more information.

ADVANCE INFORMATION

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4).

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10µF and a 0.1µF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

The NRST reset pin is required to connect an external 47kΩ pullup resistor with a 1000pF pulldown capacitor.

For devices supporting external crystals, external bypass capacitors for the crystal oscillator pins are required. Refer to *MSPM0 C-Series Microcontrollers Technical Reference Manual* which explains how to calculate the capacitor value.

For 5V-tolerant open drain IOs (ODIO), a pullup resistor is required to output a logic high signal. This is required for I^2C and UART functions if the ODIO are used.

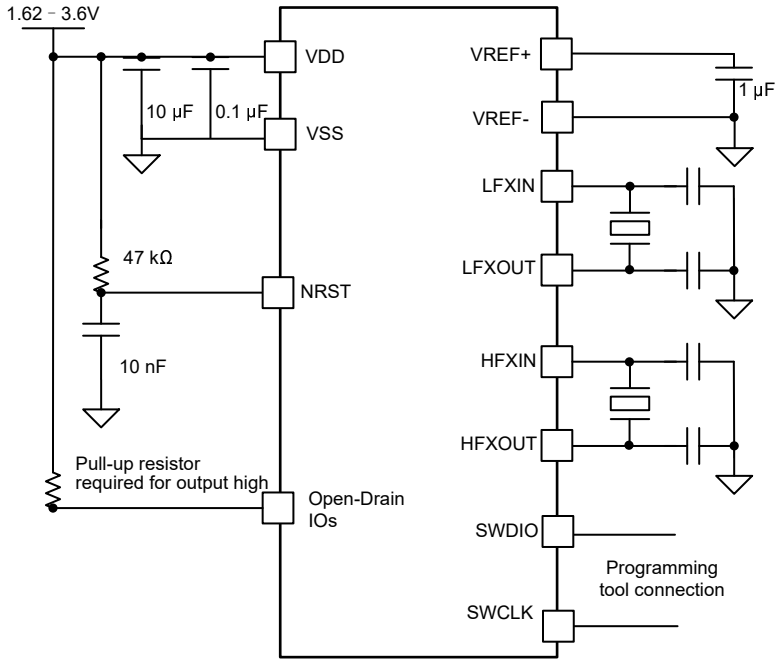


Figure 9-1. Typical Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M0+ MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

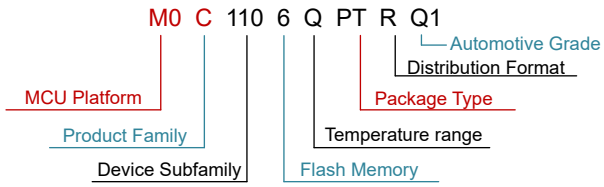


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M0 = Arm based 32-bit M0+
Product Family	L = 32MHz frequency
Device Subfamily	1105/6 = 32MHz frequency, ADC, RTC, CMP
Flash Memory	5 = 32KB 6= 64KB
Temperature Range	Q = –40°C to 125°C, AEC-Q100 qualified
Package Type	See the *Device Comparison* section and https://www.ti.com/packaging
Distribution Format	R = Large reel No marking = Tube or tray

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

ADVANCE INFORMATION

10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0C1106	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/EnergyTrace. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Cloud Tools	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™ (CCS)	Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.
IAR Embedded Workbench® IDE	
Keil® MDK IDE	
GNU Arm Embedded Toolchain	

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 C-Series Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices.

Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

LaunchPad™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2024	1.0	Initial Release

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

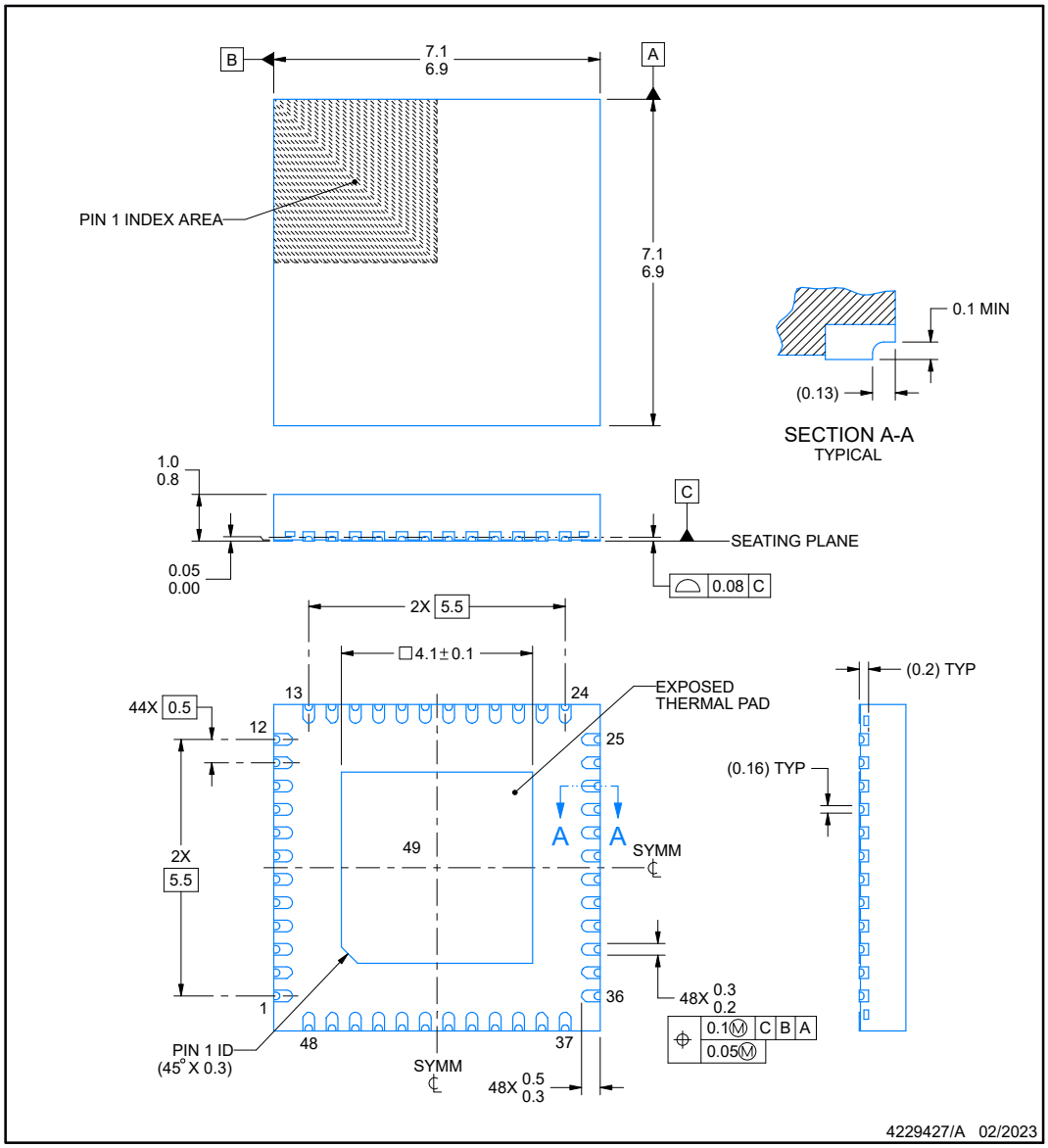
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGE OUTLINE

RGZ0048F — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

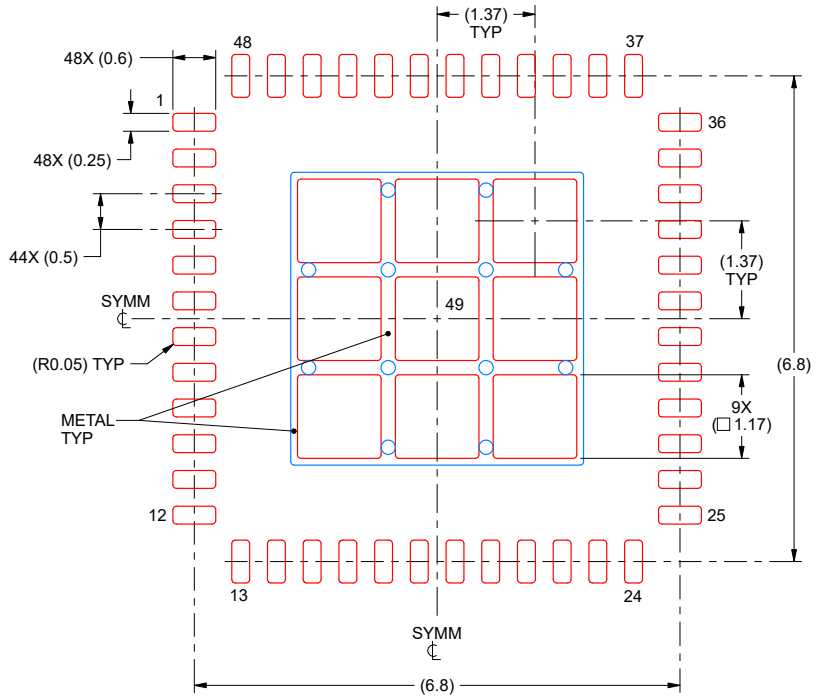
EXAMPLE BOARD LAYOUT

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGZ0048F — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



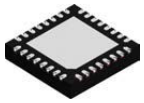
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4229427/A 02/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

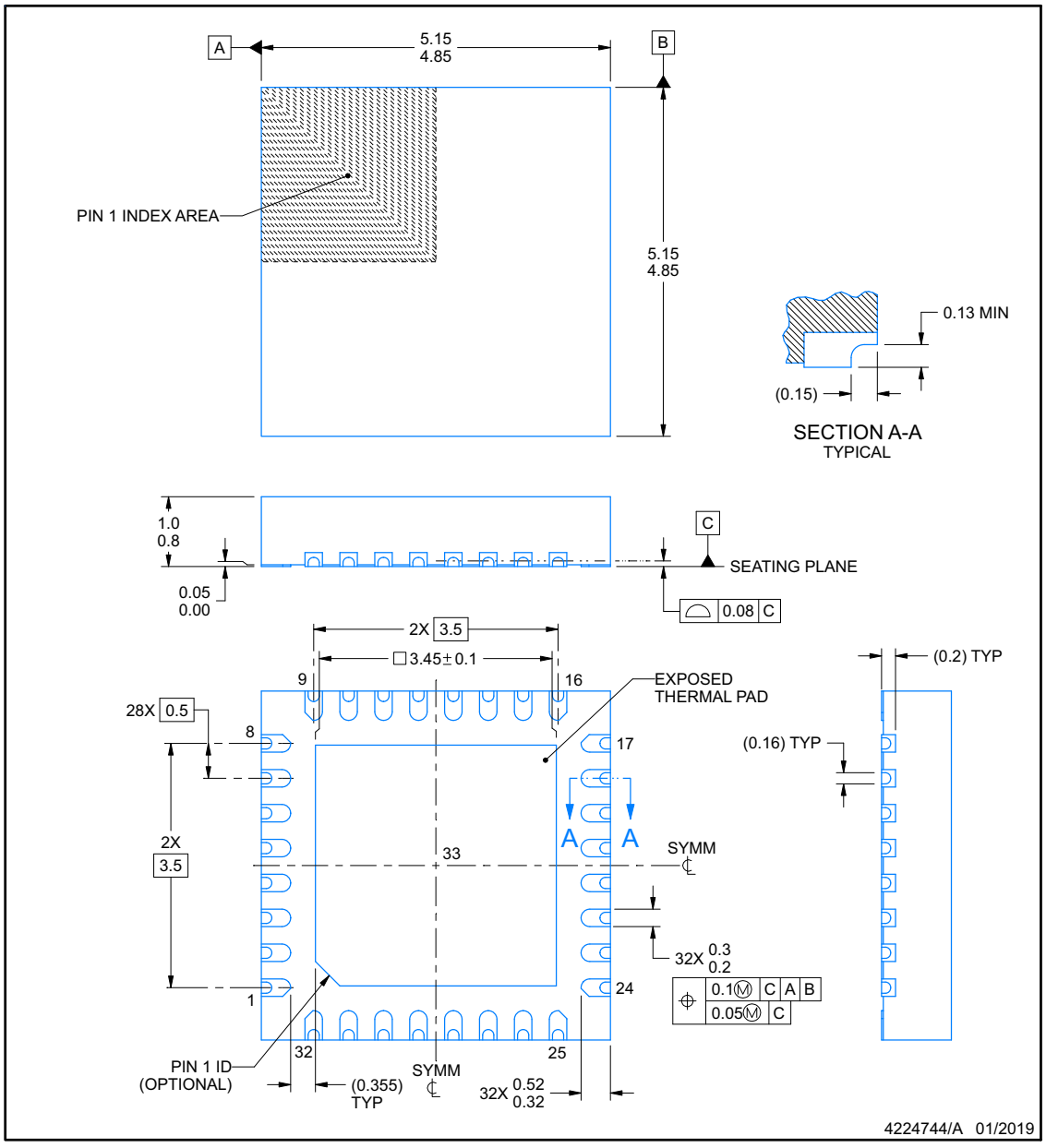


PACKAGE OUTLINE

RHB0032T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

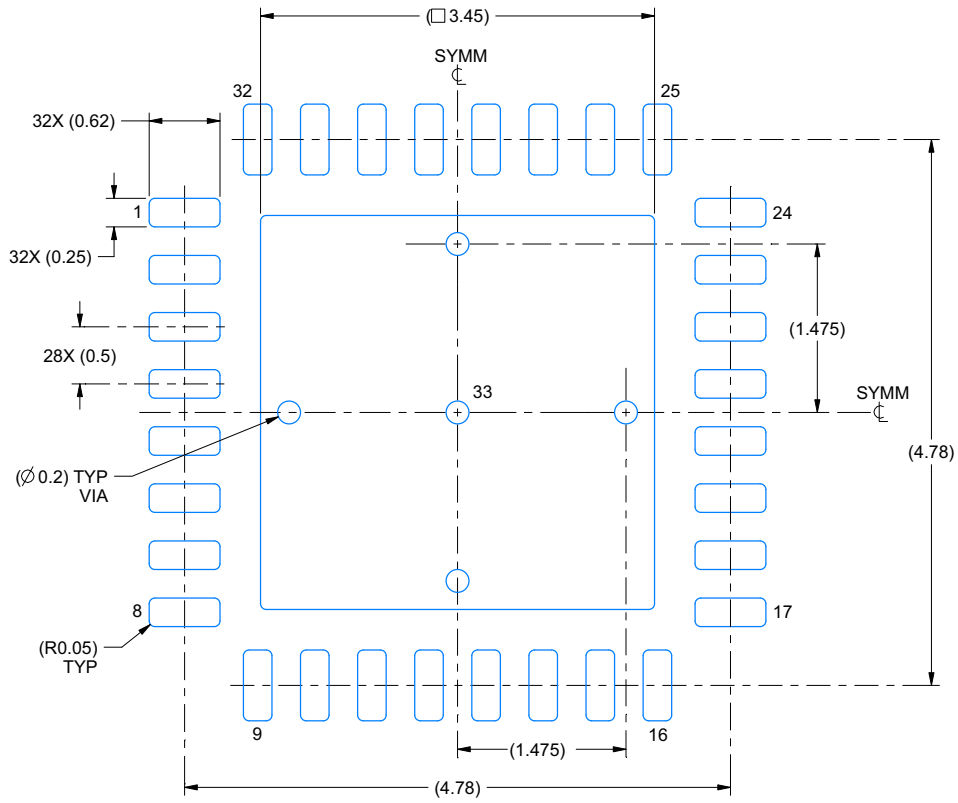
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

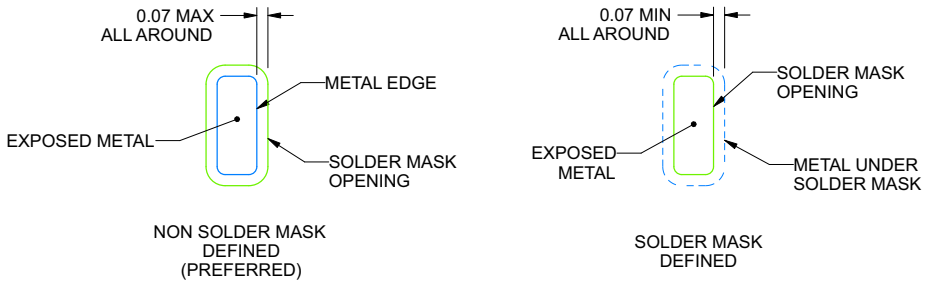
RHB0032T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4224744/A 01/2019

NOTES: (continued)

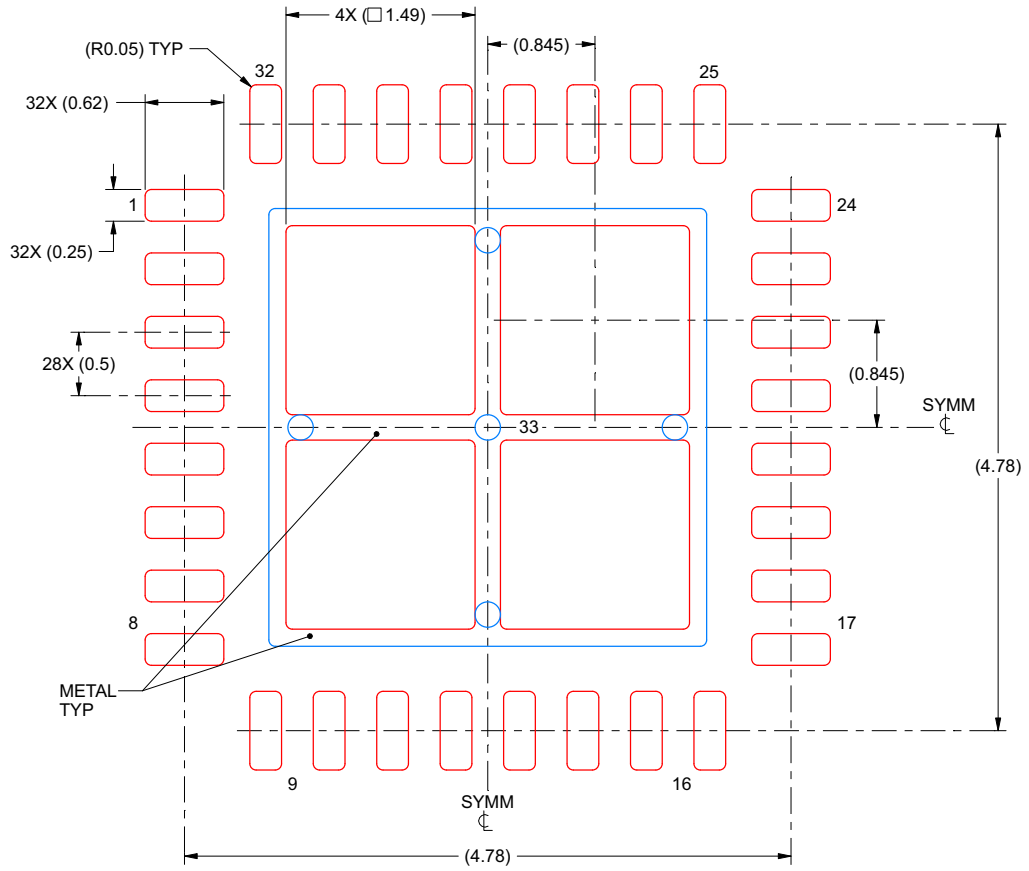
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224744/A 01/2019

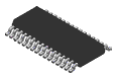
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

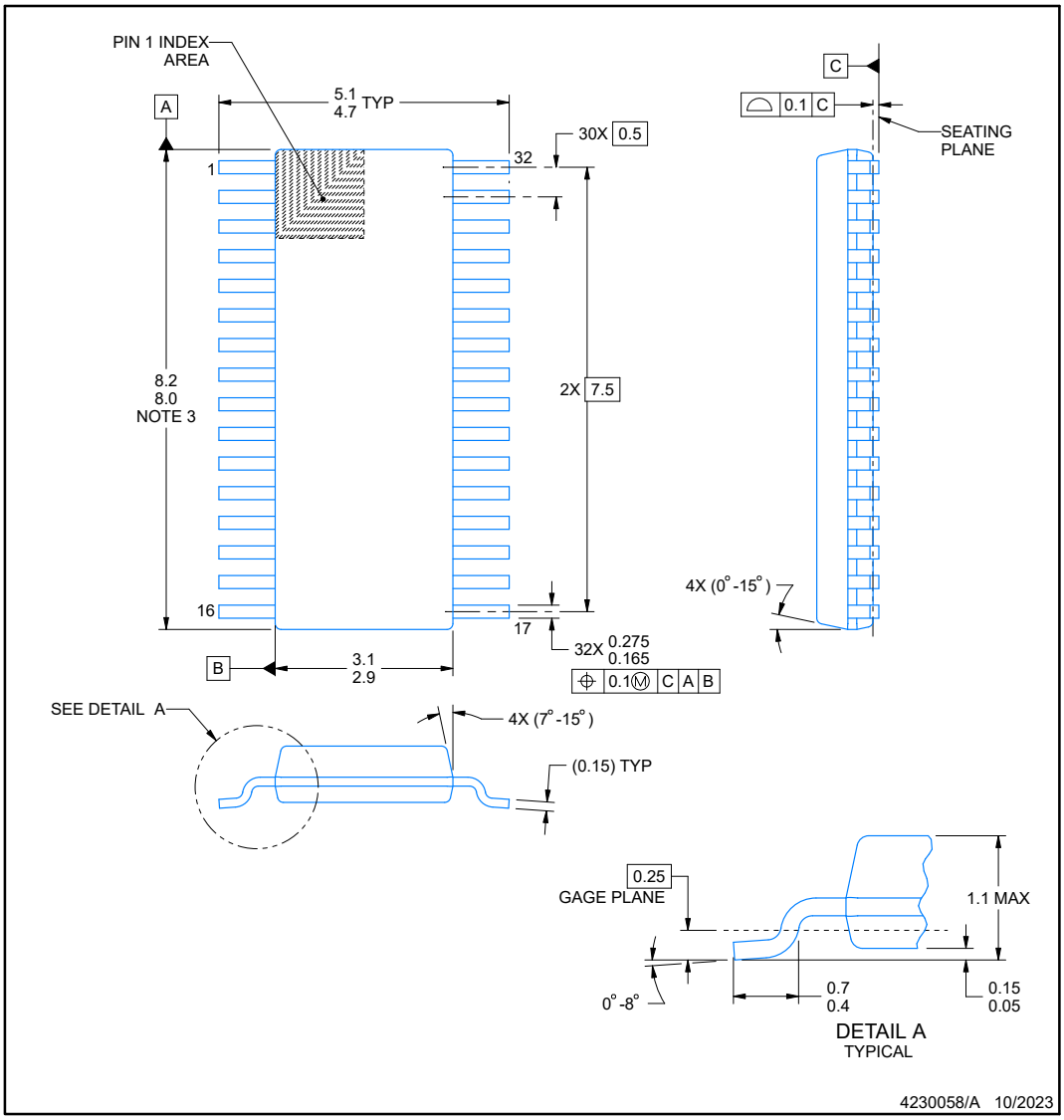
PACKAGE OUTLINE

DGS0032A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

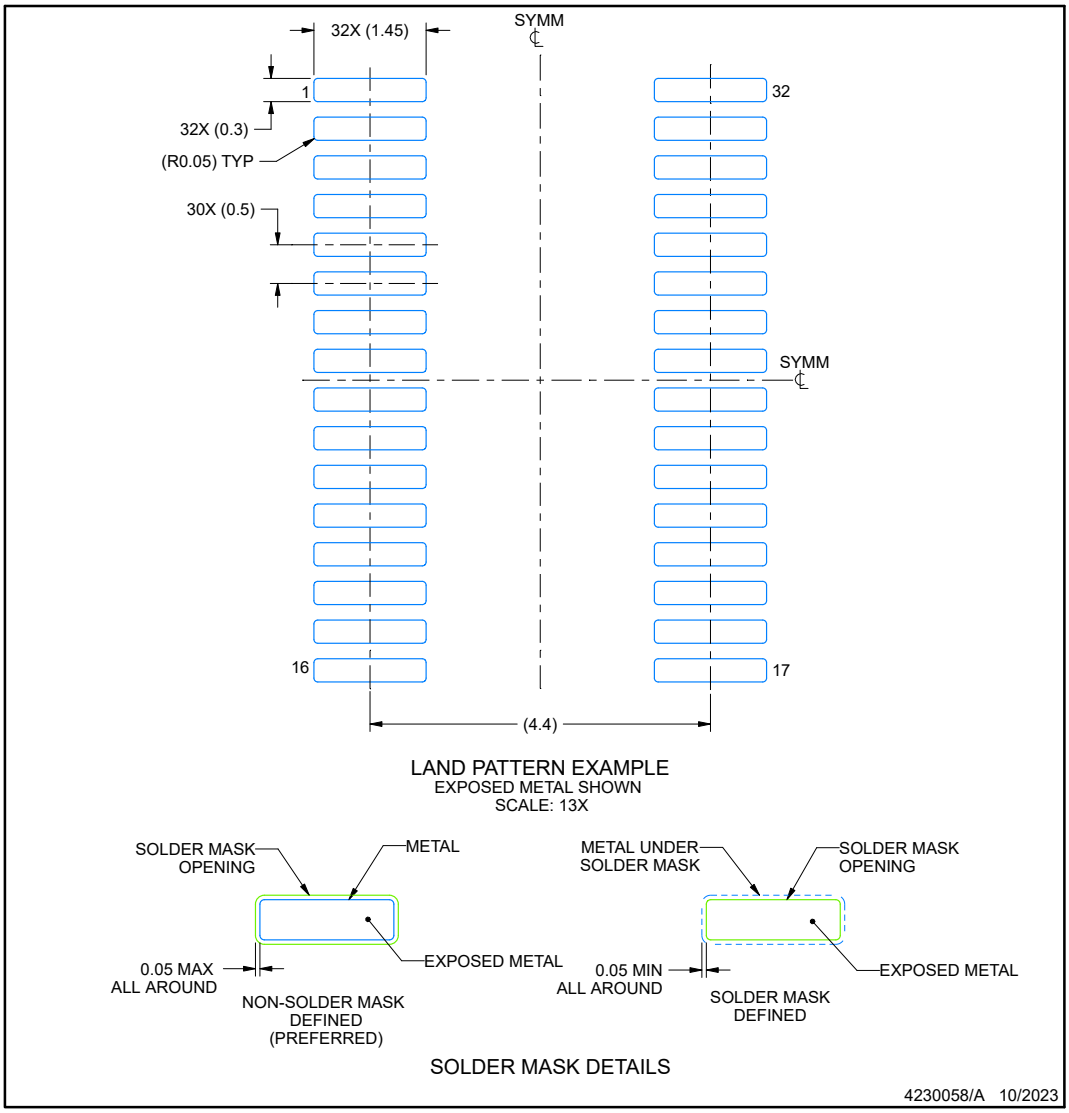
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0032A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

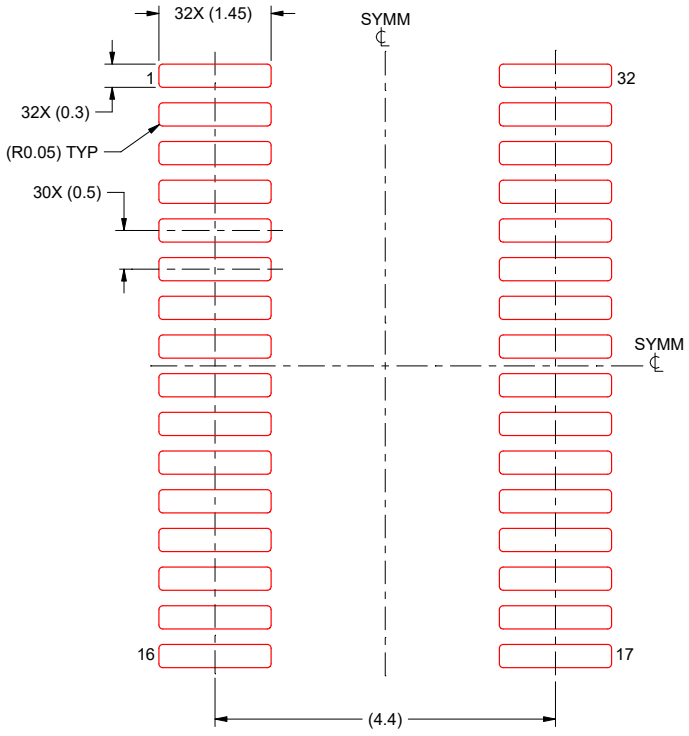
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DGS0032A — **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



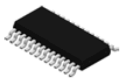
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 13X

4230058/A 10/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

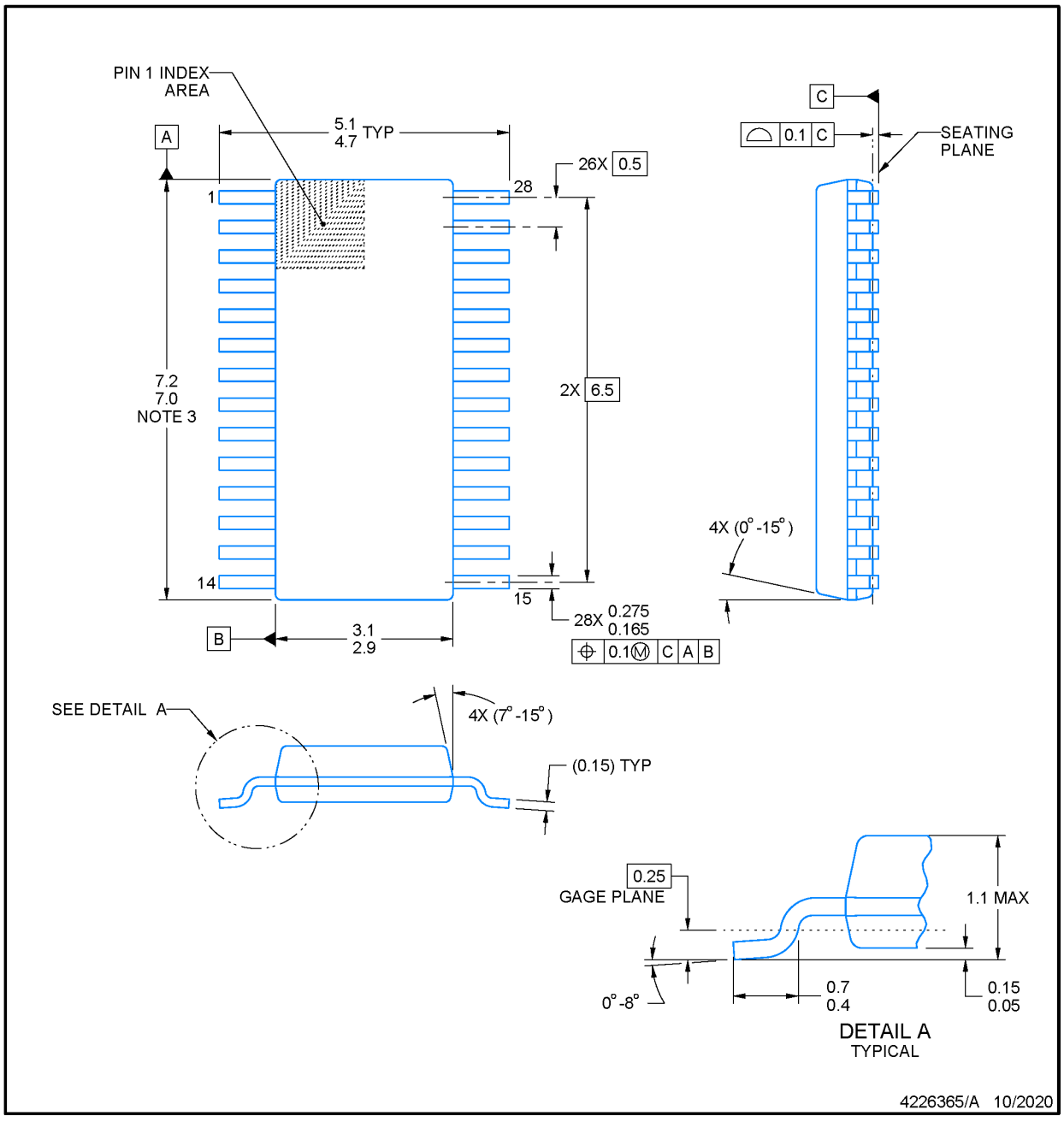
PACKAGE OUTLINE



DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

ADVANCE INFORMATION

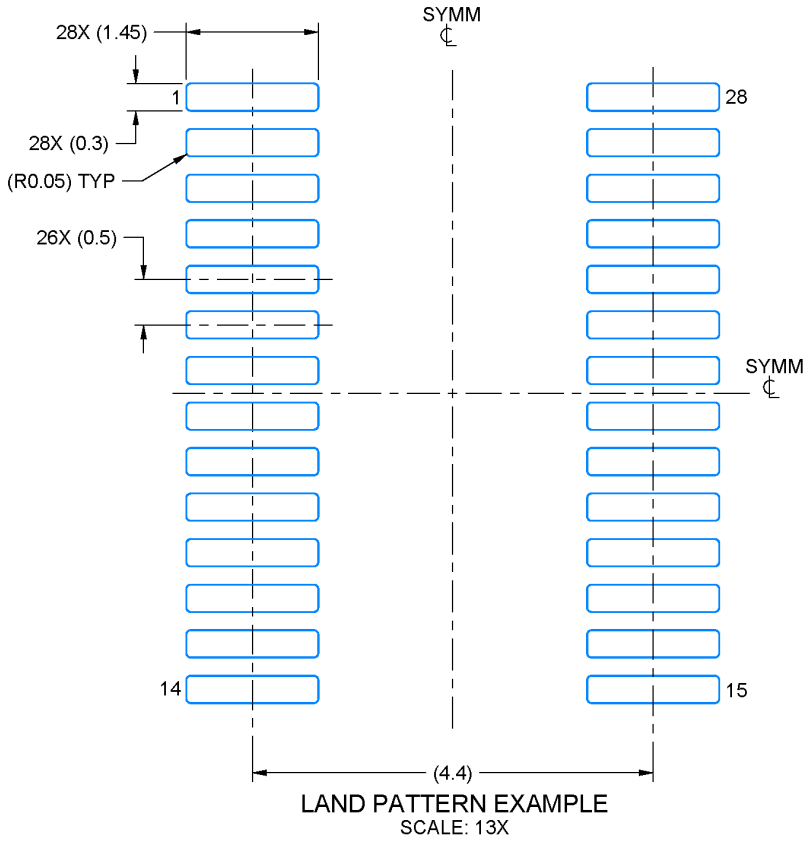
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

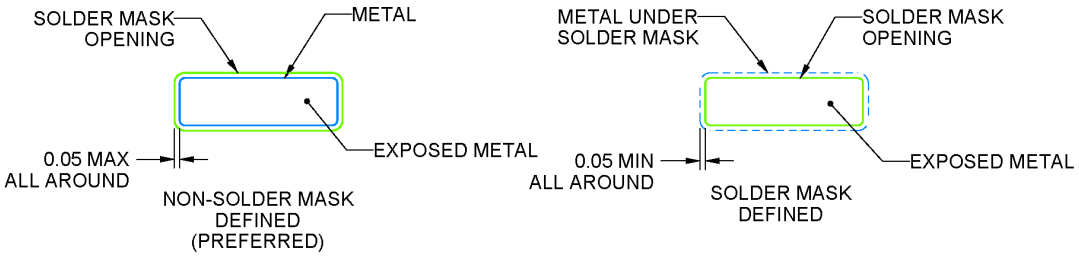
DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE: 13X



SOLDER MASK DETAILS

4226365/A 10/2020

NOTES: (continued)

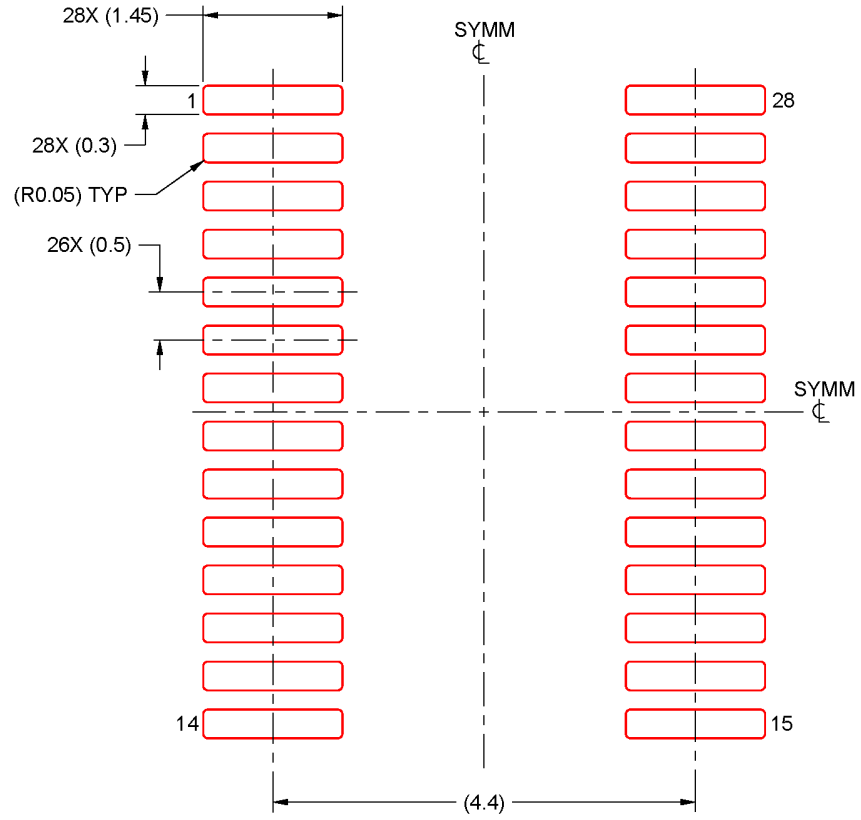
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 13X

4226365/A 10/2020

ADVANCE INFORMATION

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

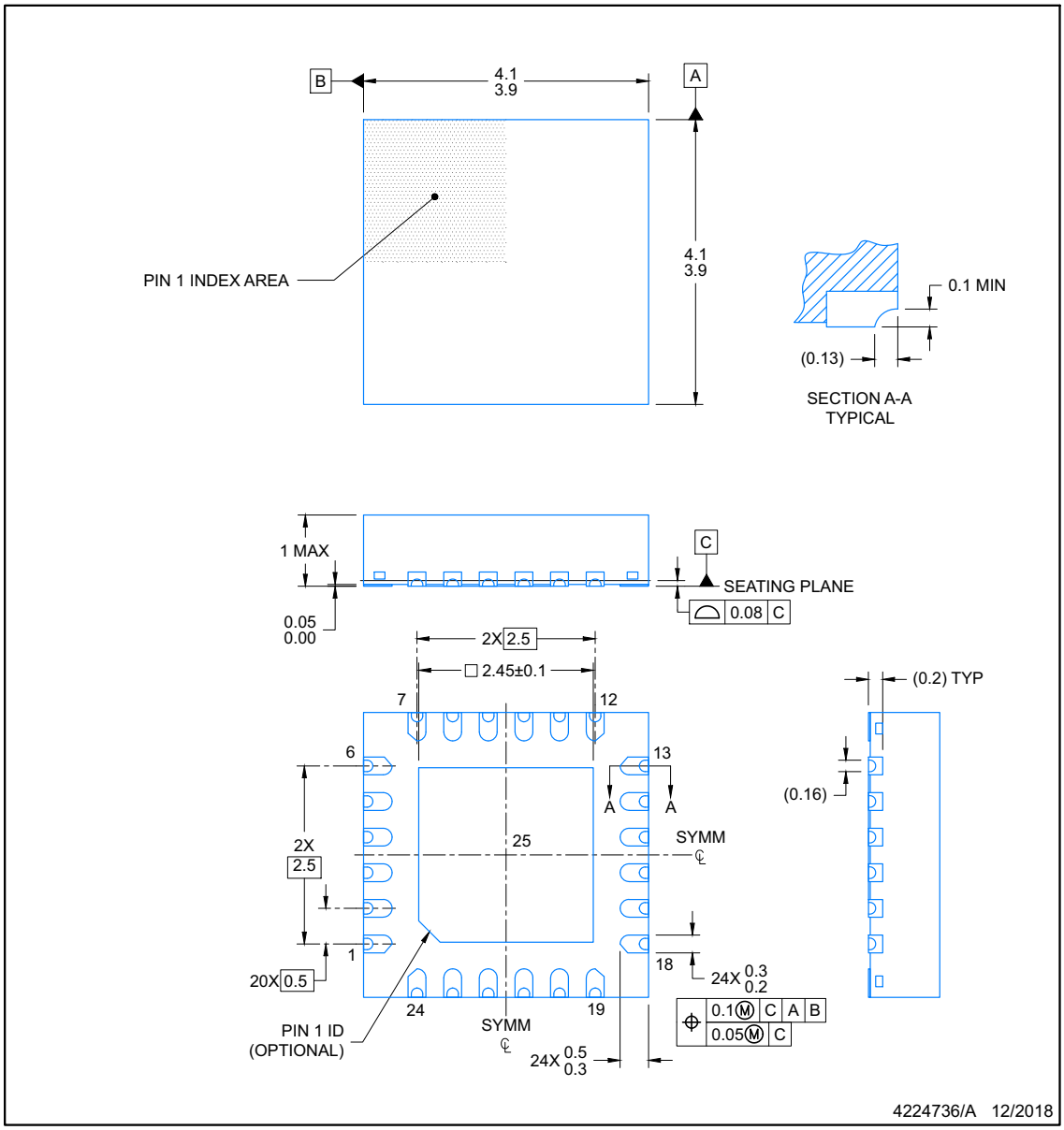
ADVANCE INFORMATION

PACKAGE OUTLINE

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

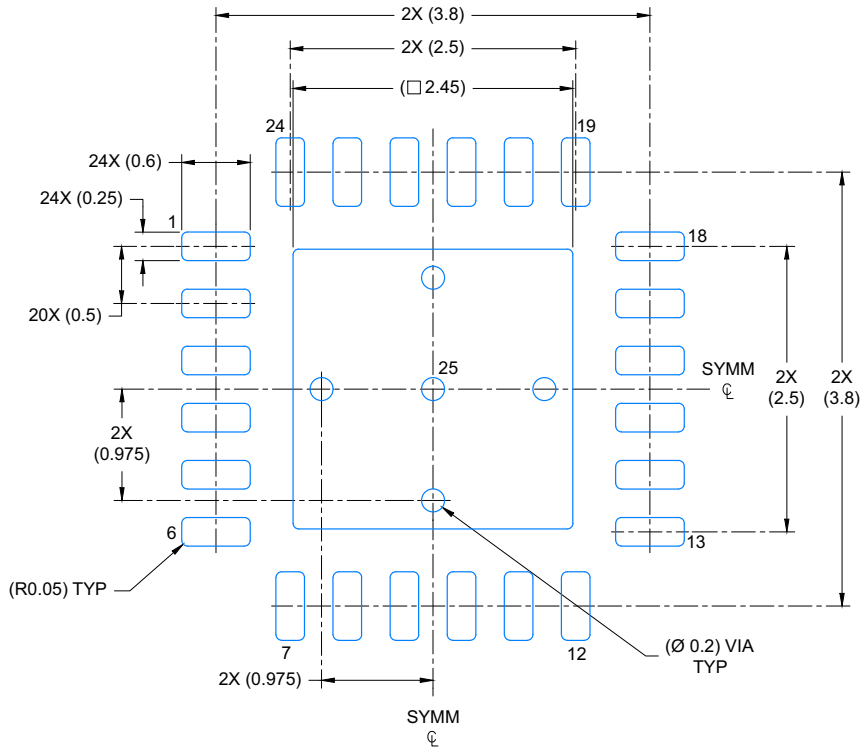
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

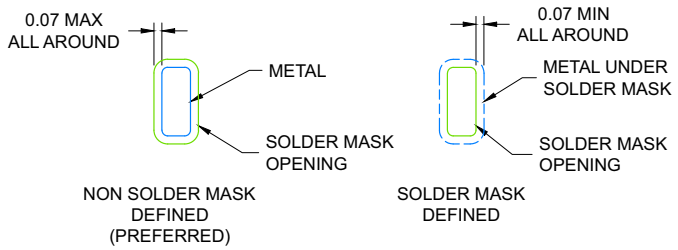
RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

4224736/A 12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

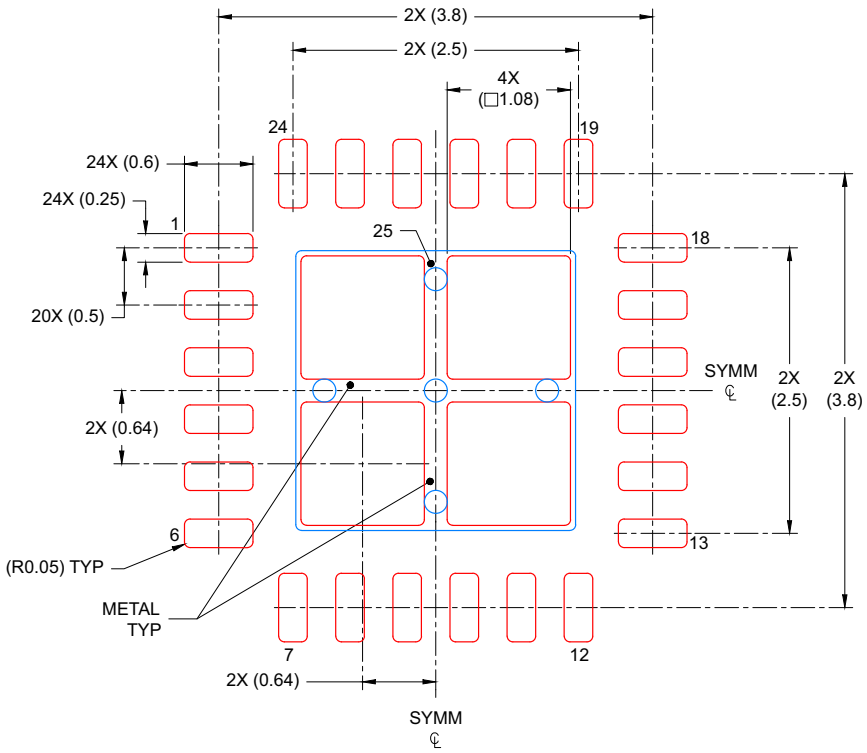
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGE0024N — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

4224736/A 12/2018

NOTES: (continued)

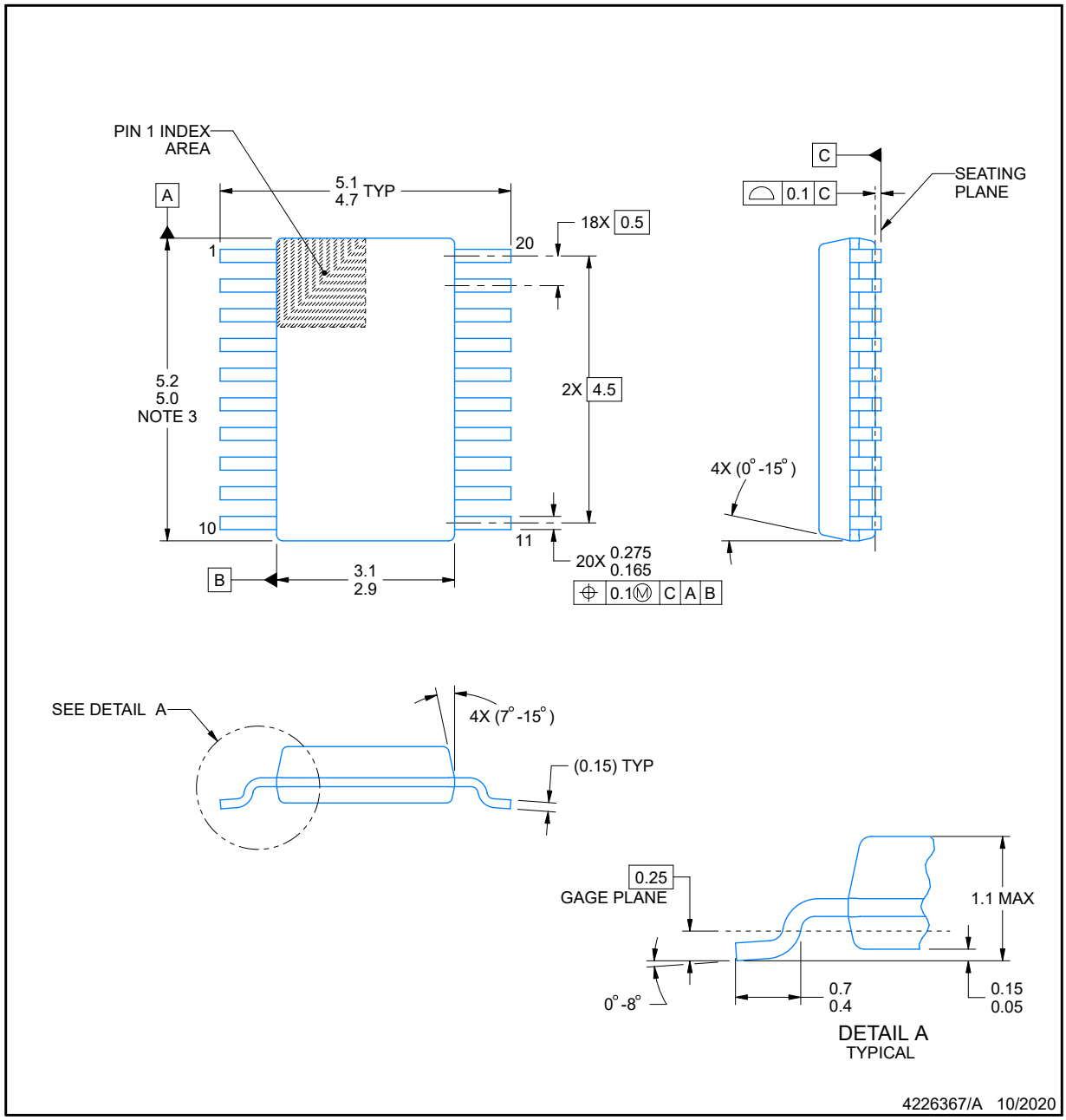
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

ADVANCE INFORMATION

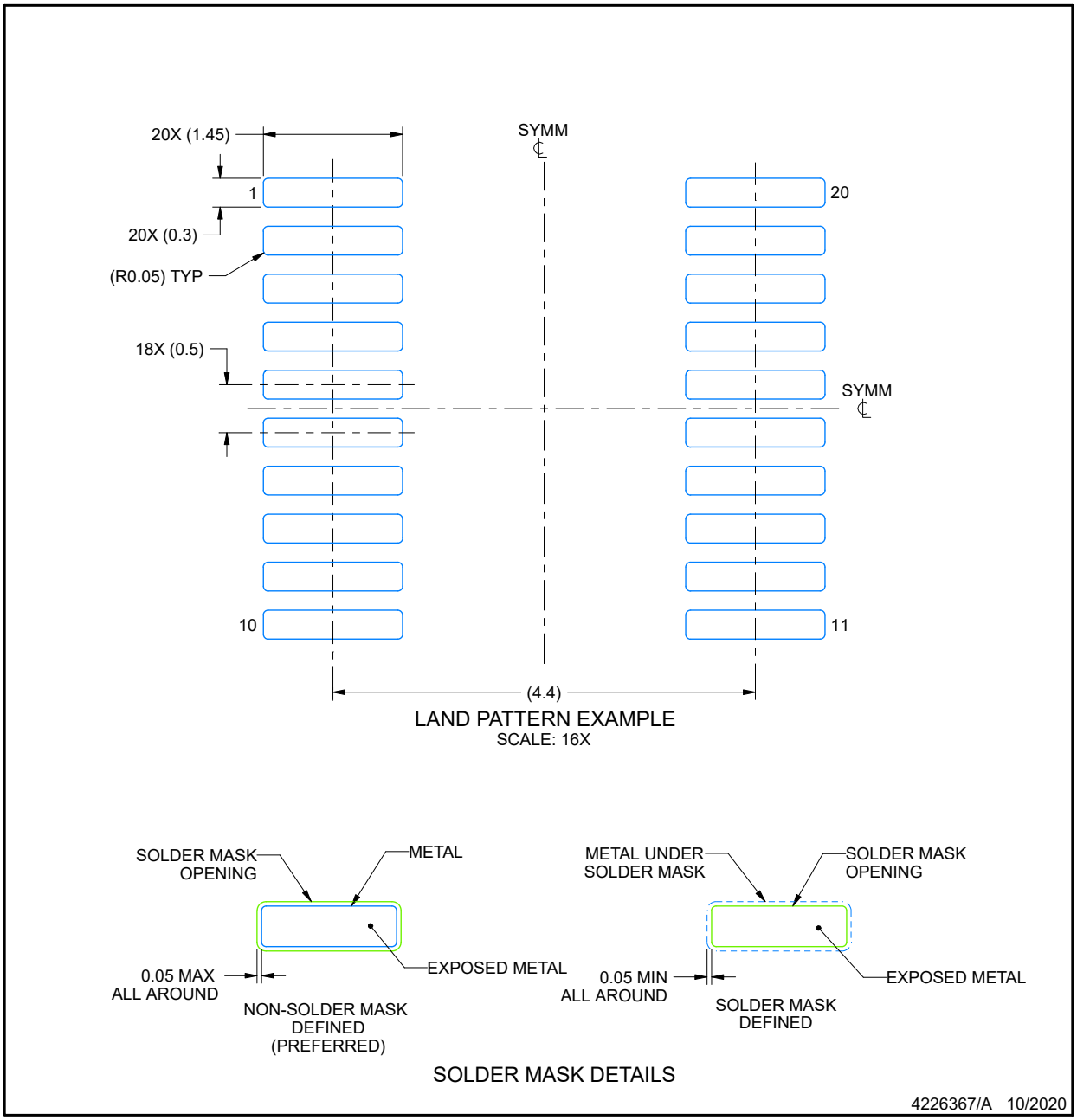
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

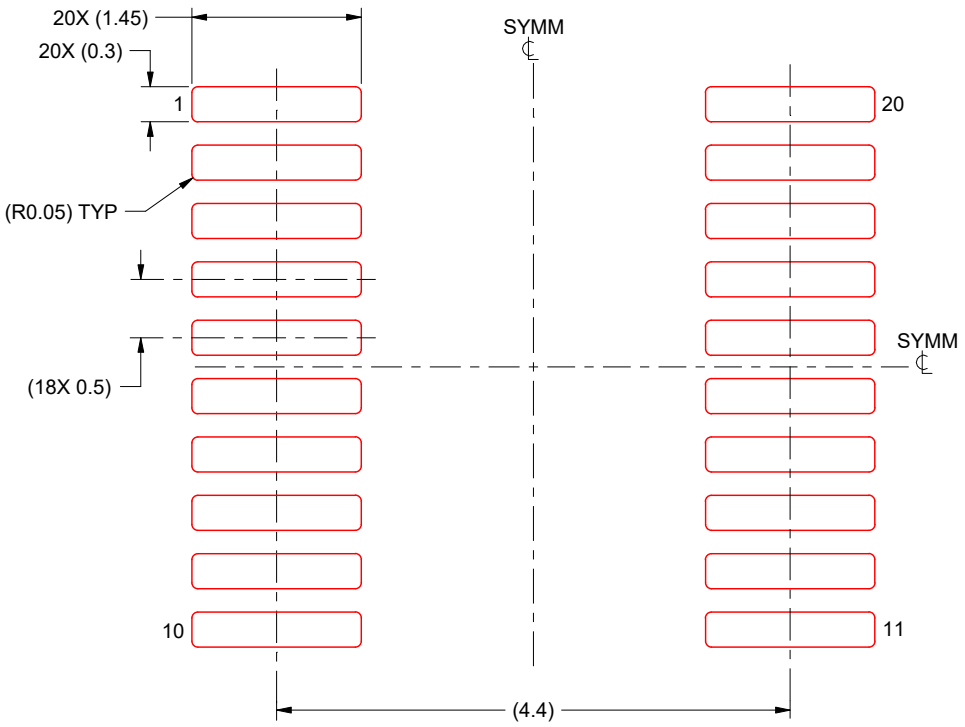
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

ADVANCE INFORMATION

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

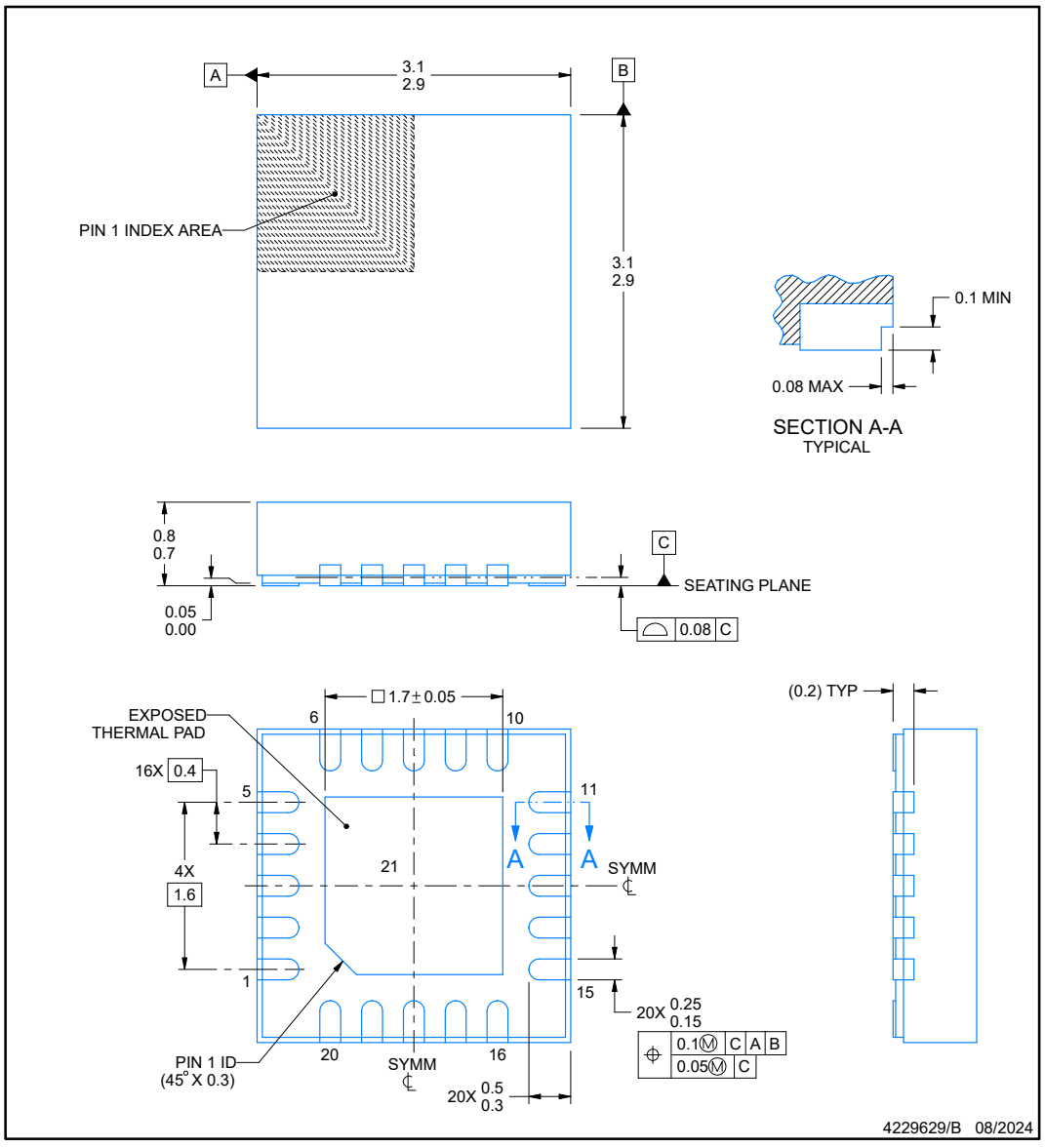
ADVANCE INFORMATION

PACKAGE OUTLINE

RUK0020C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

RUK0020C

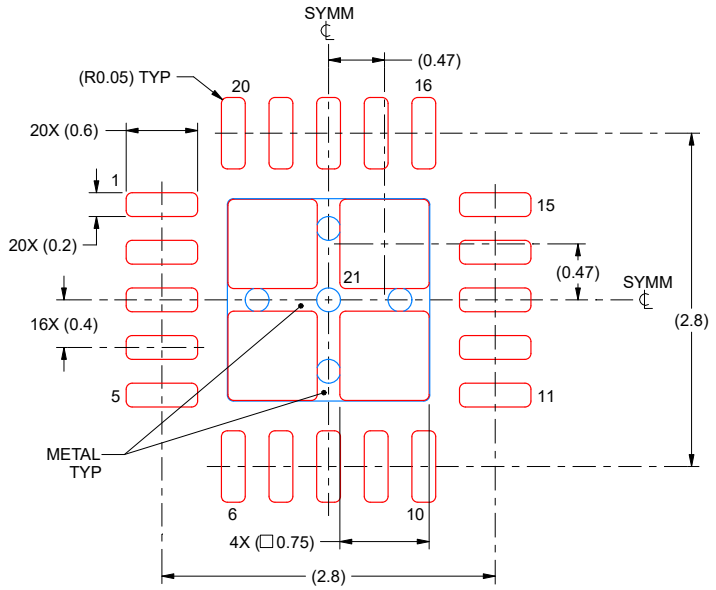
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

EXAMPLE STENCIL DESIGN

RUK0020C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4229629/B 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XM0C1106QDGS32RQ1	Active	Preproduction	VSSOP (DGS) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XM0C1106QPTRQ1	Active	Preproduction	LQFP (PT) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XM0C1106QRGZRQ1	Active	Preproduction	VQFN (RGZ) | 48	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF MSPM0C1106-Q1 :

- Catalog : MSPM0C1106

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

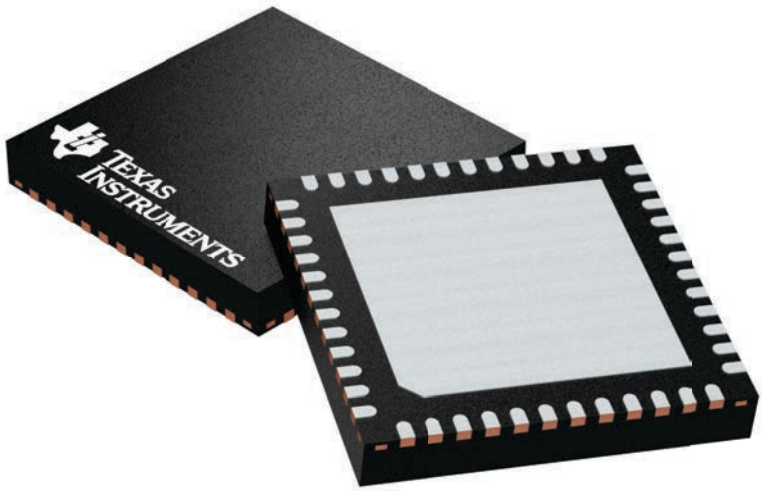
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

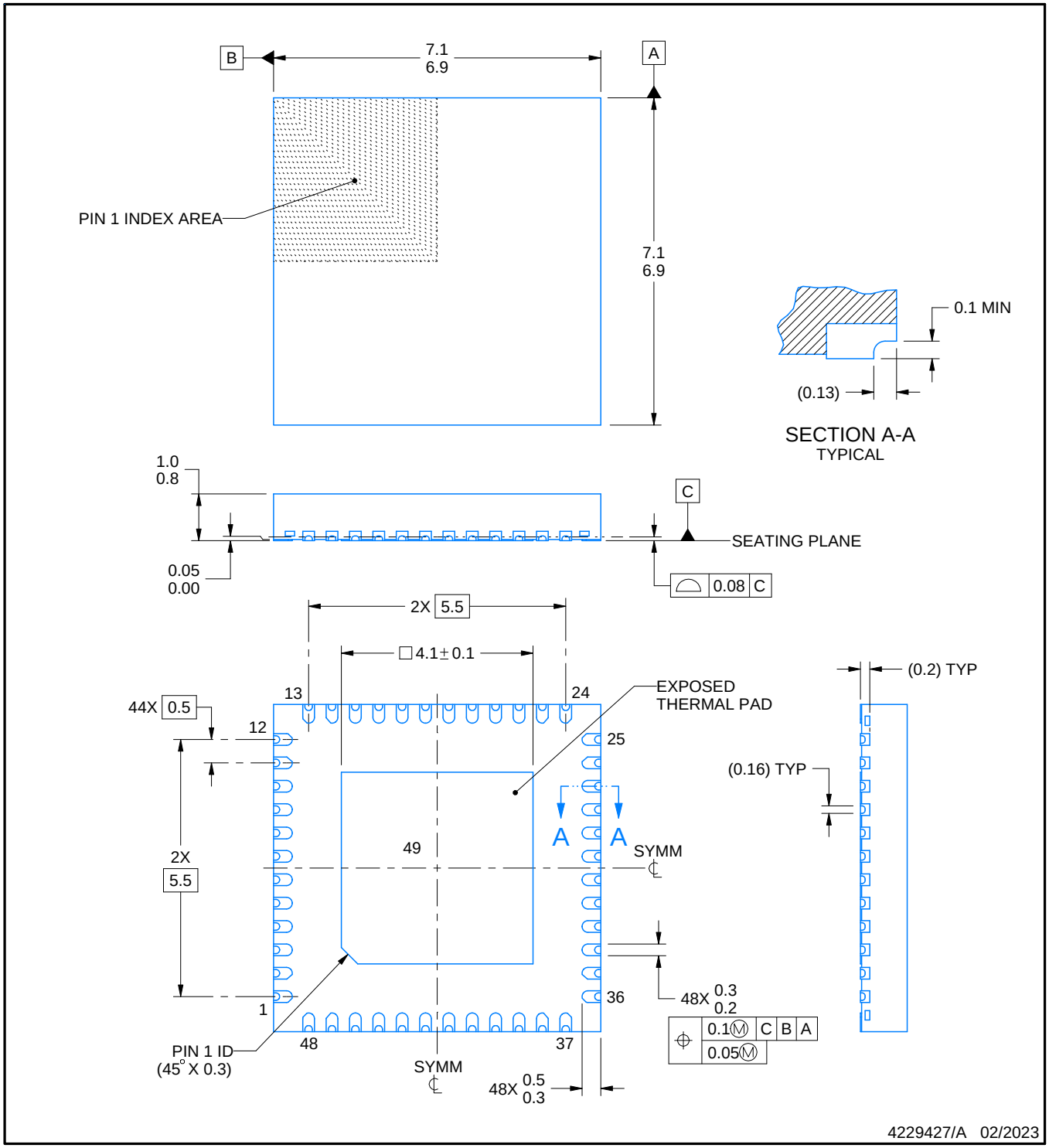
4224671/A

RGZ0048F

PACKAGE OUTLINE

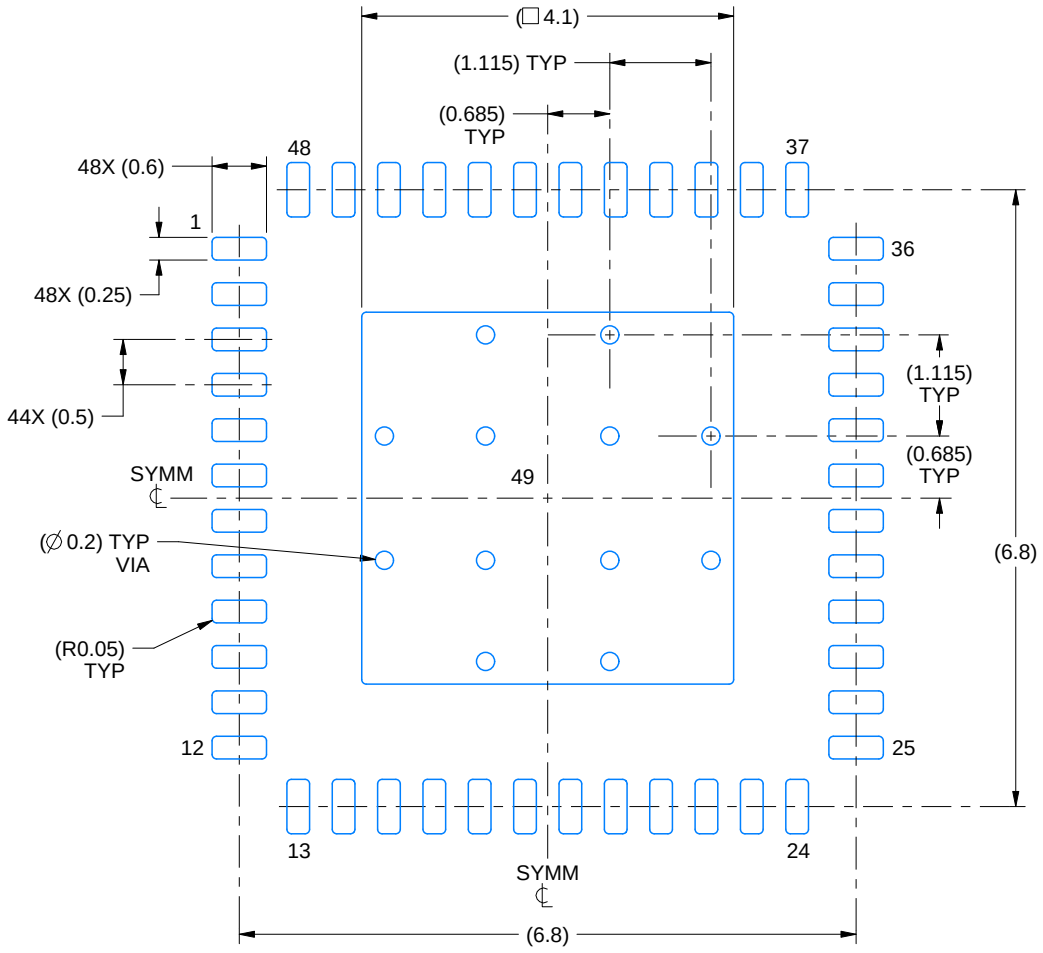
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

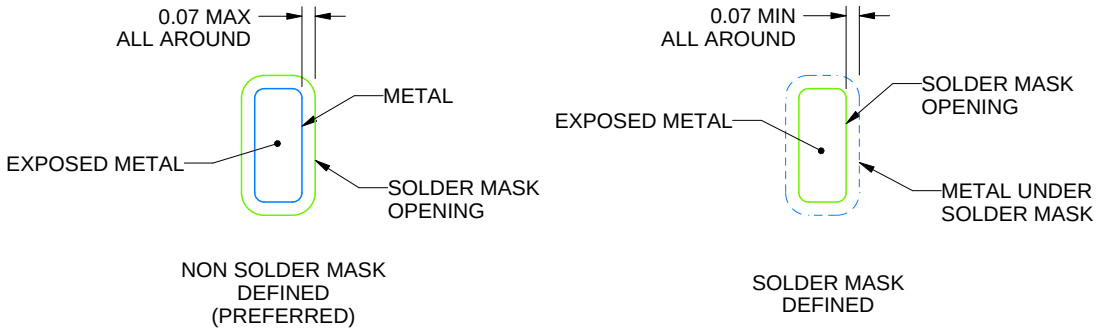


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

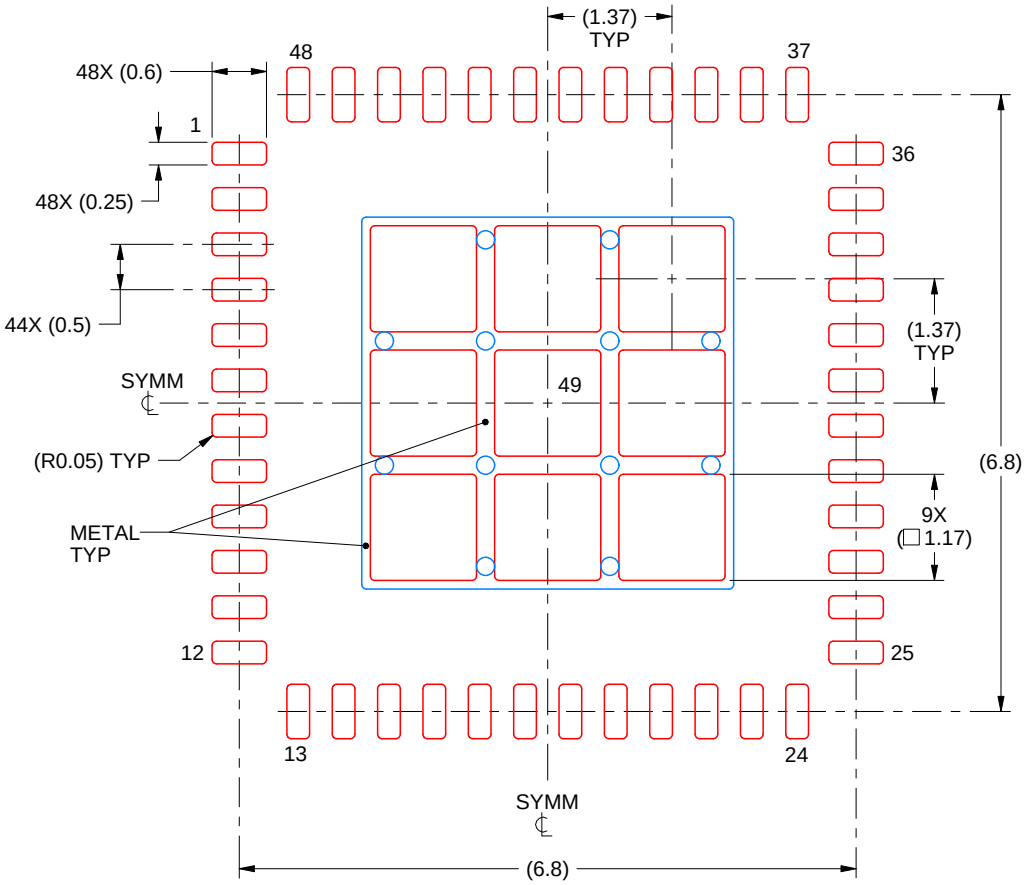


SOLDER MASK DETAILS

4229427/A 02/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4229427/A 02/2023

NOTES: (continued)

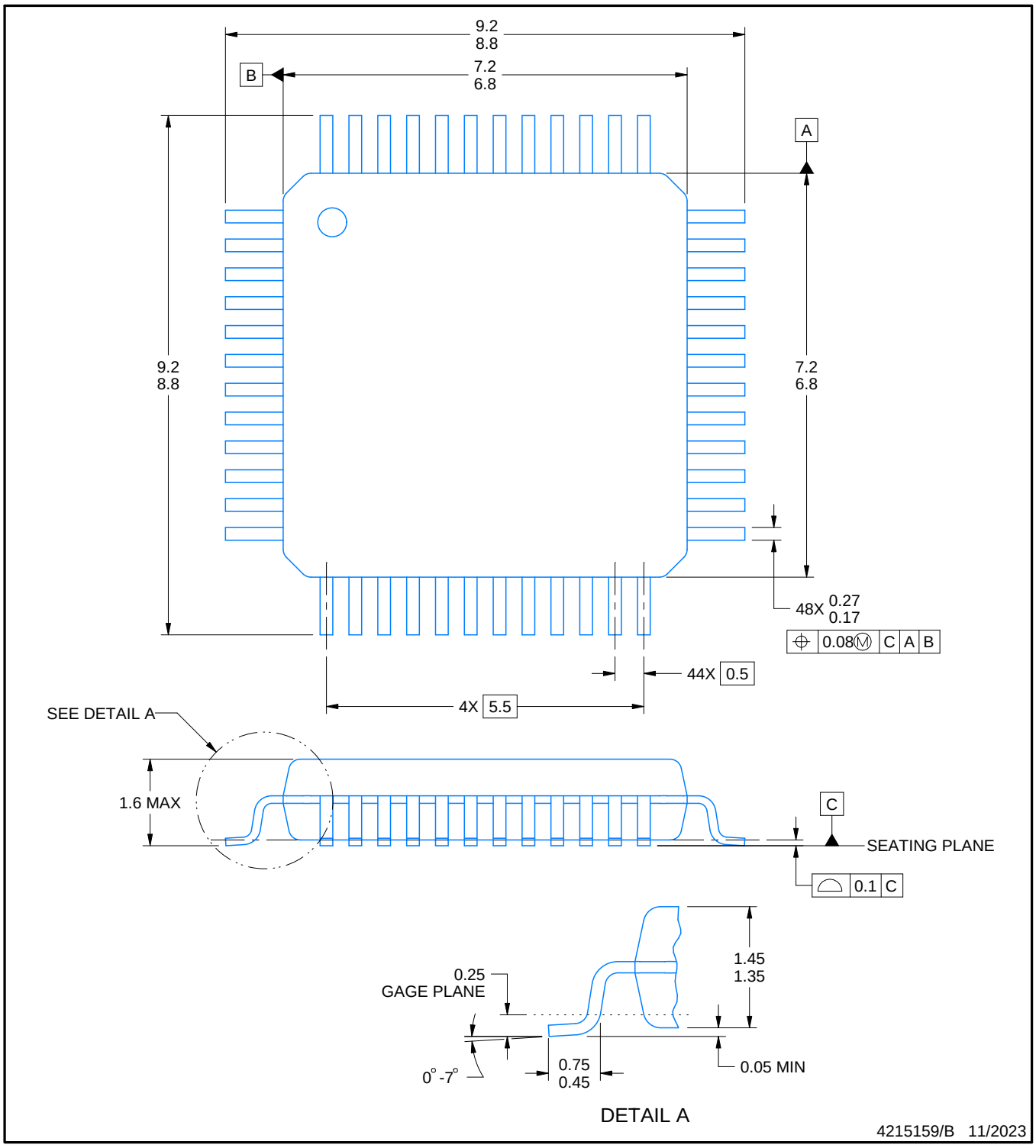
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PT0048A

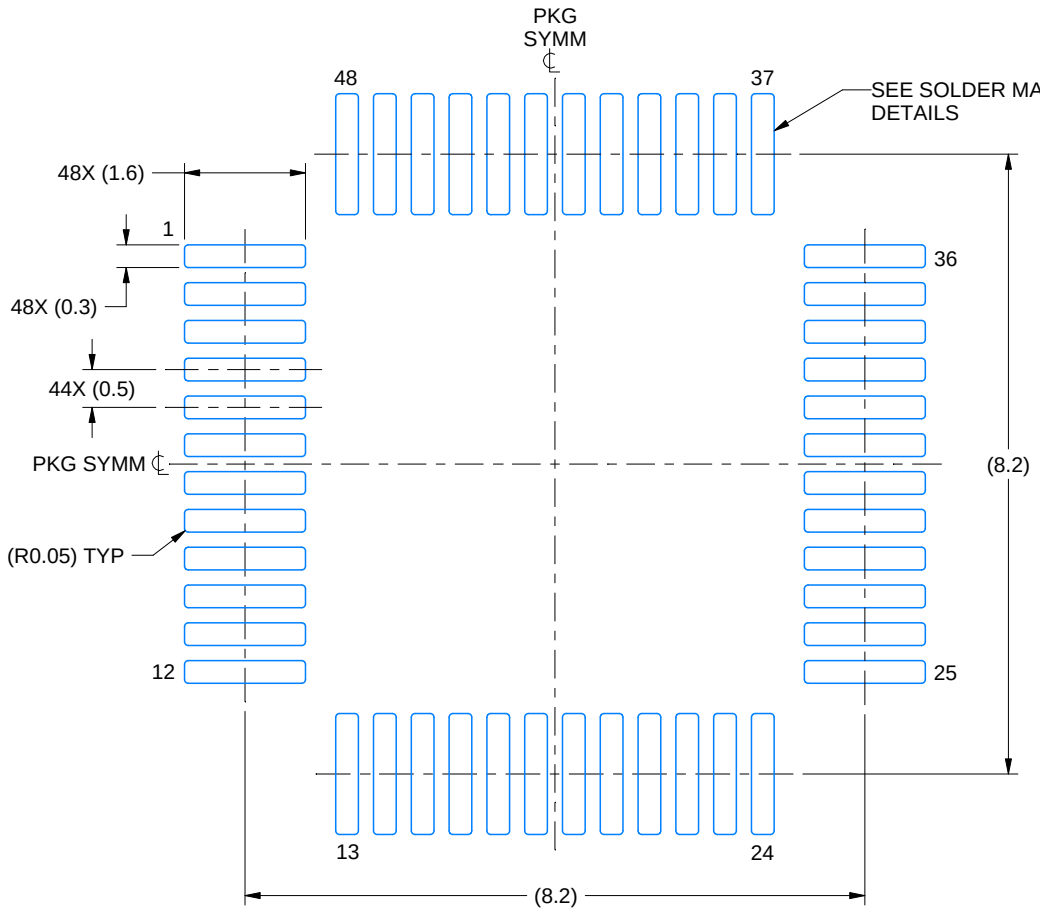
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

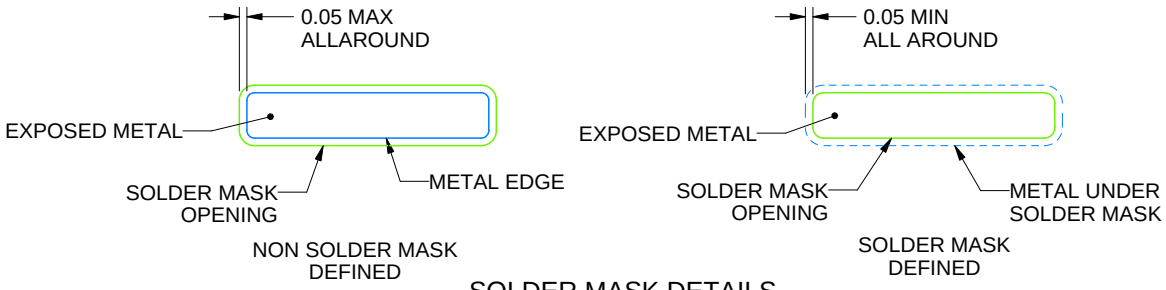


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

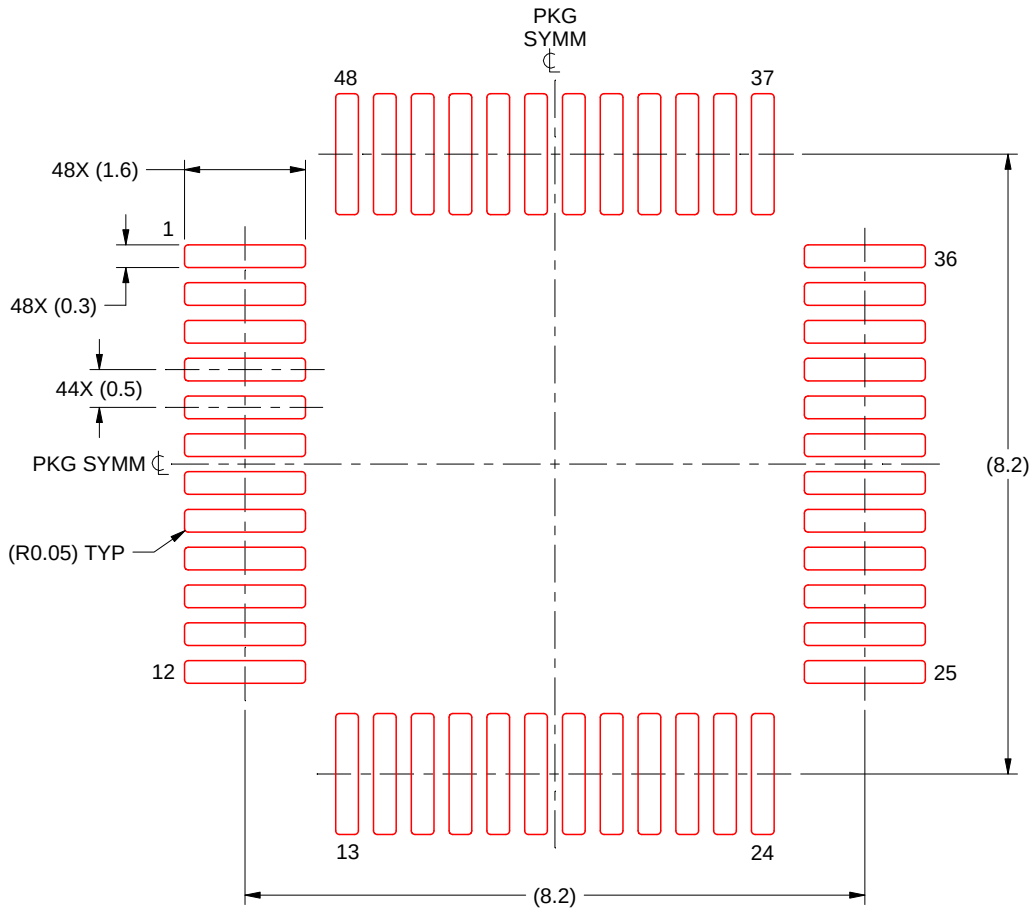


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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