MSPM33C321x Mixed-Signal Microcontrollers

1 Features

- **Core**
  - 160MHz Arm® 32-bit Cortex®-M33 CPU with TrustZone®, FPU, and DSP extensions
  - 4kB instruction cache for 0 wait-state execution
- **Operating characteristics**
  - Extended temperature: –40°C up to 125°C
  - Wide supply voltage range: 1.71 V to 3.6 V
- **Memories**
  - Up to 1MB of flash memory with error correction code (ECC)
    - Dual-bank with address swap
  - 256kB of SRAM with ECC
  - EEPROM operations using 32kB high-endurance data flash
- **Security**
  - Immutable Root of Trust (RoT) in ROM, supports secure firmware installation, boot and key provisioning
  - Global Security Controller with dynamic access controls for flash, SRAM, and peripherals
  - AES256 hardware accelerator with GCM
  - SHA256 hardware accelerator with HMAC
  - Public Key Accelerator (PKA)
  - 32-bit true random number generator (TRNG)
- **High-performance analog peripherals**
  - Two high-speed 9.4-Msps 12bit analog-to-digital converters (ADCs) with up to 36 external channels
  - Two high-speed/low-power comparators (COMP)
  - Two externally available 8-bit DACs
  - Configurable 1.4V or 2.5V internal shared voltage reference (VREF)
  - Integrated temperature & supply monitor
- **Optimized low-power modes**
  - RUN: 207µA/MHz (CoreMark)
  - STANDBY: 16µA with CPU execution resume and 64kB SRAM retention
  - SHUTDOWN: <100nA with IO wake-up capability
- **Optimized digital peripherals**
  - Two DMA controllers with 16 total channels
  - Nine timers support up to 30 PWM channels
    - Two 16-bit advanced timers with deadband, fault handling, and complementary pair
    - Four 16-bit general-purpose timers
    - One 32-bit general-purpose timer
    - Two 16-bit general-purpose timer supporting quadrature encoder interface
  - One window-watchdog timer
  - CRC16/32 module
- **Enhanced communication interfaces**
  - Quad SPI (QSPI) for external memory up to 20Mbytes/s
  - Two Controller Area Network (CAN) interfaces support CAN 2.0A/B and CAN-FD
  - Three configurable serial interfaces supporting UART (LIN) or I^2C (SMBus/PMBus)
  - Four configurable serial interfaces supporting UART, I^2C, or SPI
  - Two dedicated I^2C interfaces support up to FM+ (1Mbit/s), SMBus/PMBus
  - One dedicated SPI interface
  - One dedicated UART interface supporting LIN, IrDA, DALI, Smart Card, Manchester
  - Two digital audio interfaces support full duplex I2S and TDM (16-slots)
- **VBAT island (auxiliary supply)**
  - Independent supply with dedicated VBAT pin
  - Real-time clock (RTC)
  - Three tamper detection IO with timestamp
  - Independent watchdog timer (IWDT)
  - 32B backup memory
- **Clock system**
  - Internal 32MHz oscillator (SYSOSC)
  - Phase-locked loop (PLL)
  - Internal 32kHz oscillator (LFOSC)
  - External 4 to 48MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator (LFXT)
  - External clock input
- **Flexible I/O features**
  - Up to 93 GPIOs
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**
  - 100-pin LQFP (0.4mm & 0.5mm pitch)
  - 80-pin LQFP (0.5mm pitch)
  - 64-pin LQFP (0.5mm pitch)
  - 48-pin VQFN (0.5mm pitch)
  - 100-pin nFBGA (0.8mm pitch)
- **Family members** (also see *Device Comparison*)
  - MSPM33C321A: 1MB flash, 256KB SRAM
  - MSPM33C3219: 512KB flash, 256KB SRAM
- **Development kits and software** (also see *Tools and Software*)
  - LaunchPad EVM LP-MSPM33C321A
  - MSP Software Development Kit (SDK)

ADVANCE INFORMATION

2 Applications

- Grid infrastructure
- Smart metering
- Communication modules
- Medical and healthcare
- Test and measurement
- Factory automation and control
- Motor control
- Home appliances
- Uninterruptible power supplies and inverters
- Electronic point of sale systems
- Industrial transport
- Lighting

3 Description

MSPM33C32xx micontrollers (MCUs) are part of the MSP general purpose 32-bit MCU family operating at up to 160MHz based on the Arm® Cortex®-M33 32-bit core with Arm® TrustZone® technology, DSP, and FPU. This family of MCUs features flexible communication interfaces, high-performance analog, and security accelerators. The extended temperature range and wide supply voltage range make this family of MCUs suitable for a variaety industrial, enterprise and personal electronics applications.

MSPM33C32xx MCUs provide up to 1MB of embbeded flash program memory and 256kB SRAM. An additional high-endurance 32kB flash data bank is provided for application data storage. All memories feature built-in error correction code (ECC) across the entire memory range to ensure robust operation across their entire lifetime.

MSPM33C32xx MCUs offer many different types of digital communication interfaces including CAN, I2S/TDM, Quad SPI (QSPI), UART, I2C, and SPI. Configurable serial interfaces can be dynamically assigned in software as UART, I2C and optionaly SPI. Flexilbity in configuraiton and pinout gives system designers a simple path to support challenging requirments.

MSPM33C32xx MCUs also feature high performance integrated analog peripherals such as two 12bit 9.4 MSPS simultaneous sampling ADC and two high-speed comparators. Comparators can be used internally for fault detection with advanced timers or externally as low-power voltage monitors.

MSPM33C32xx MCUs contain a robust collection of security features. TrustZone technology and the Global Security Controller provide a complete feature set to build secure applications. These devices also feature an immutable root of trust (RoT) which provides secure boot, install and key provisioning out of the box. MSPM33C32xx also includes hardware acceleration for AES, SHA and Public Key algorithms (RSA and ECC).

MSPM33C series of devices is pin-to-pin compatible with other MSPM33C devices in the same package. MSPM33C series is also highly pin-to-pin compatible with MSPM0 devices. In scenerios where there are differences between MSPM33C and MSPM0 devices users can use TI System Configurator or provided documentation to understand how to navigate minor incompatibilities.

MSPM33C family of MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM33C MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM33C MCUs.

ADVANCE INFORMATION

4 Functional Block Diagram

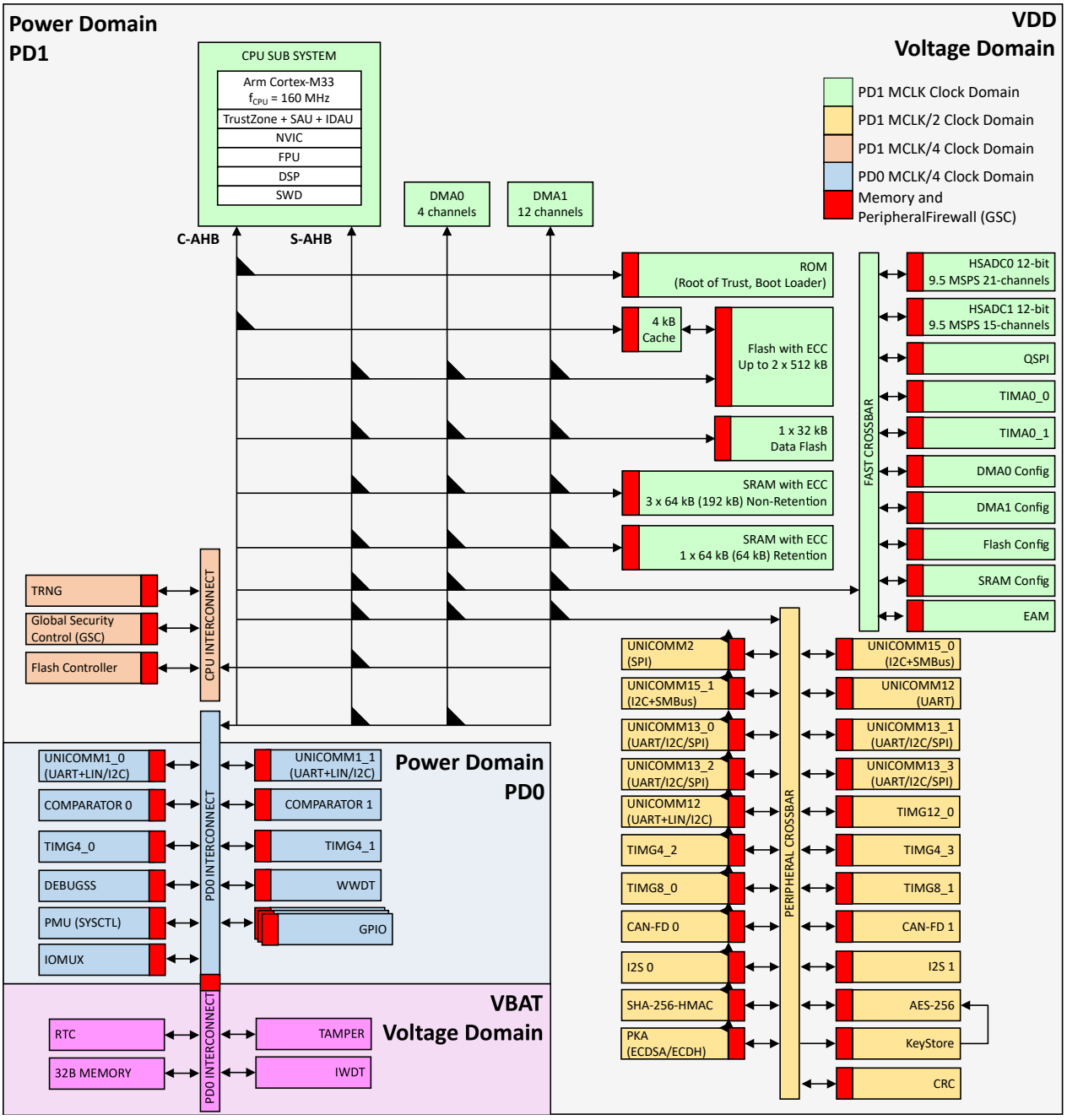

Figure 4-1. MSPM33C321x Functional Block Diagram

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

5 Device Comparison

The following table summarizes the features of each device that is described in this data sheet.

Table 5-1. Device Comparison

PRODUCT PREVIEW only DEVICE NAME(1) (2)	FLASH /SRAM	SECURITY ACCELERATOR	ADC CHANNELS	CAN	GPIO	PACKAGE
MSPM33C321ASPZR	1MB/256kB	AES, SHA, PKA	36	2	93	LQFP100 16mm x 16mm 0.5mm pin pitch
MSPM33C3219SPZR(3)	512kB/256kB	AES, SHA, PKA	36	2	93	
MSPM33C321ASPFAR(3)	1MB/256kB	AES, SHA, PKA	36	2	93	LQFP100 14mm x 14mm 0.4mm pin pitch
MSPM33C3219SPFAR(3)	512kB/256kB	AES, SHA, PKA	36	2	93	
MSPM33C321ASPNR(3)	1MB/256kB	AES, SHA, PKA	35	2	73	LQFP80 14mm x 14mm 0.5mm pin pitch
MSPM33C3219SPNR(3)	512kB/256kB	AES, SHA, PKA	35	2	73	
MSPM33C321ASPMR(3)	1MB/256kB	AES, SHA, PKA	26	2	57	LQFP64 12mm x 12mm 0.5mm pin pitch
MSPM33C3219SPMR(3)	512kB/256kB	AES, SHA, PKA	26	2	57	
MSPM33C321ASRGZR(3)	1MB/256kB	AES, SHA, PKA	21	2	41	VQFN48 7mm x 7mm 0.5mm pin pitch
MSPM33C3219SRGZR(3)	512kB/256kB	AES, SHA, PKA	21	2	41	
MSPM33C321ASZAWR(3)	1MB/256kB	AES, SHA, PKA	36	2	93	NFBGA100 9mm x 9mm 0.8mm ball pitch
MSPM33C3219SZAWR(3)	512kB/256kB	AES, SHA, PKA	36	2	93	

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI website.
(2) For more information about the device name, see Section 10.2.
(3) PRODUCT PREVIEW only

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The following pin diagrams show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout. For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

For full pin configuration and functions for each package option, refer to Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) and Signal Descriptions

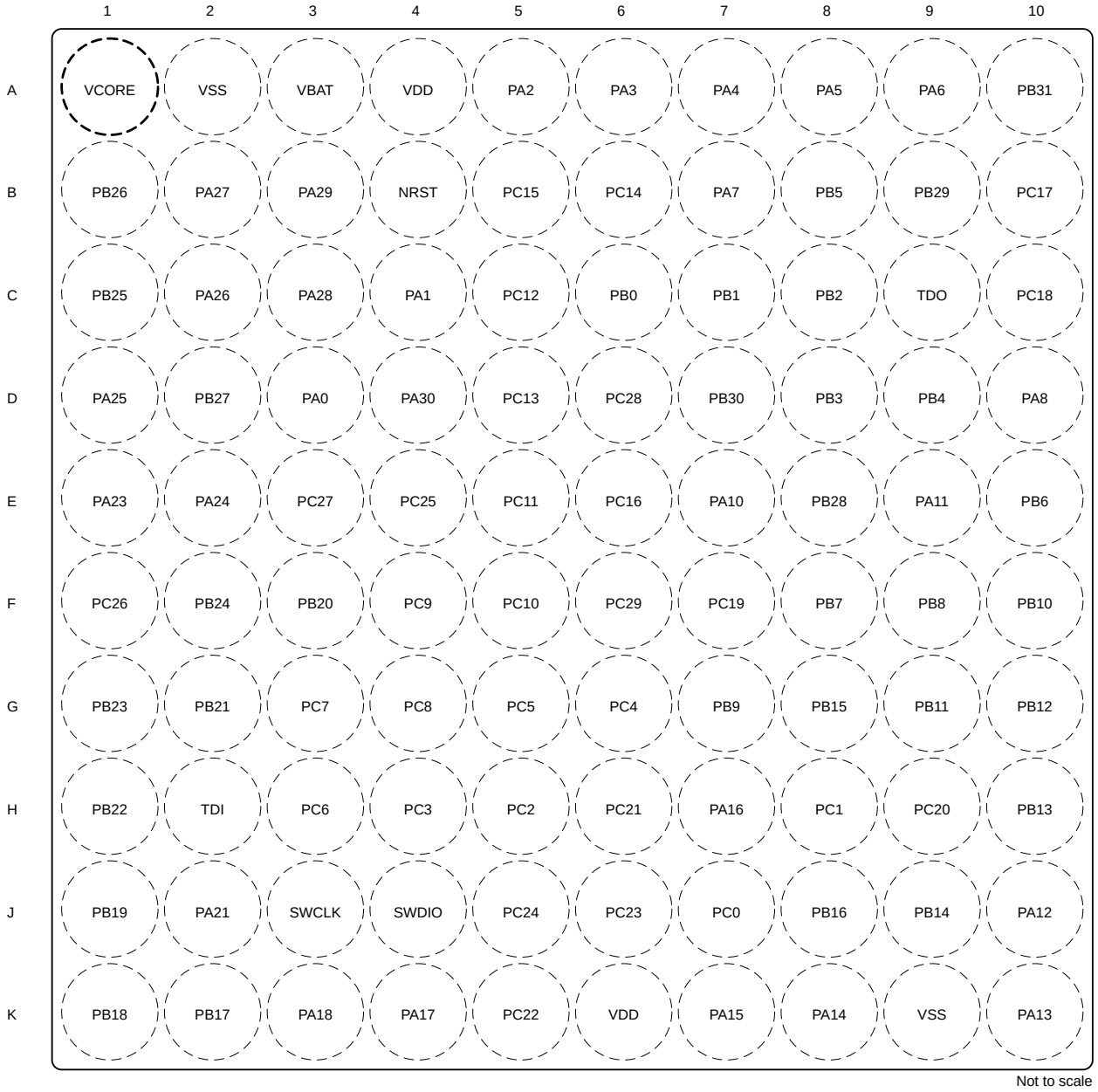

Figure 6-1. 100-pin ZAW (0.8mm) (NFBGA) Package Diagram (Top View)

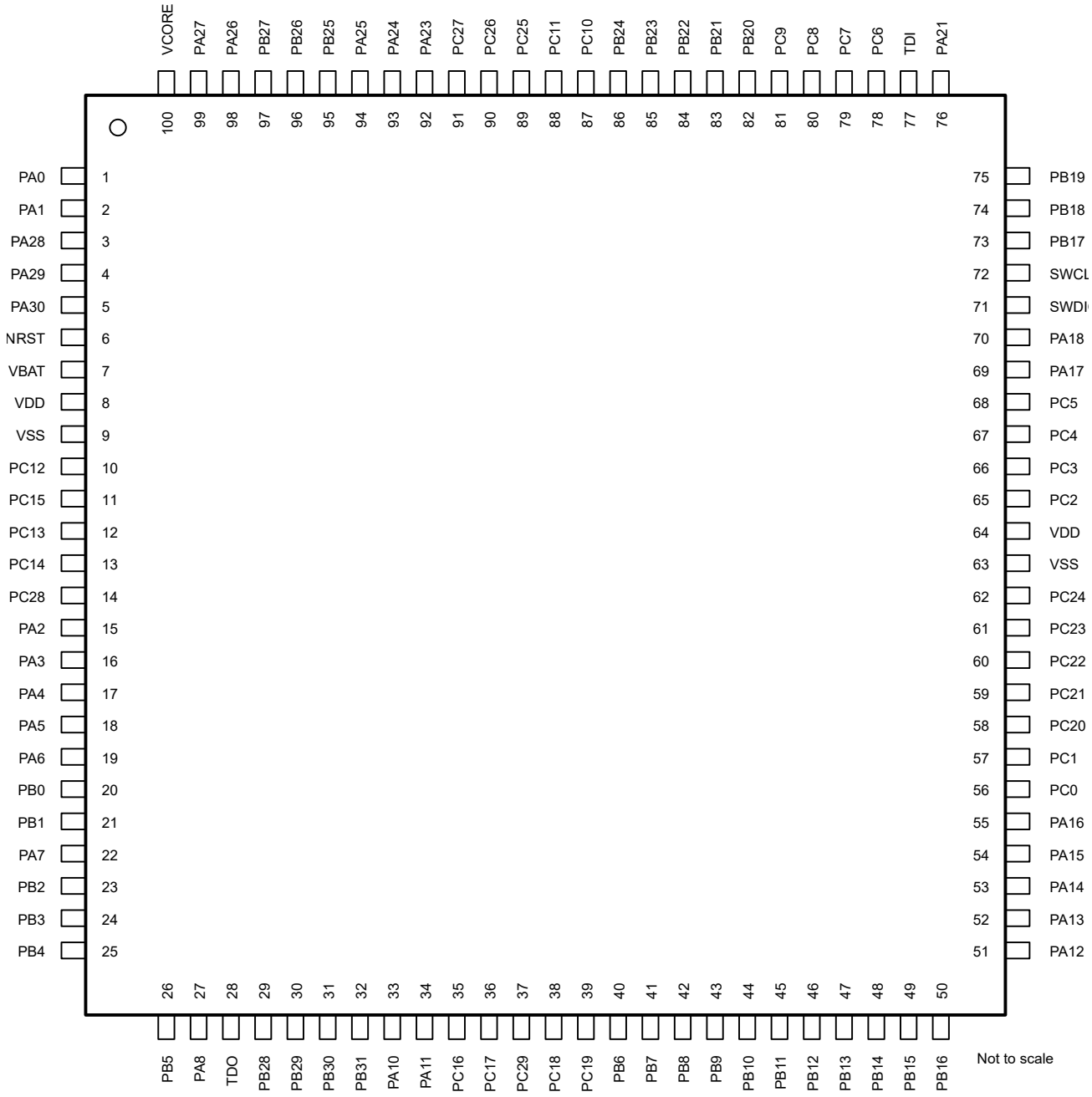

Figure 6-2. 100-pin PFA (0.4mm) and PZ (0.5mm) (LQFP) Package Diagram (Top View)

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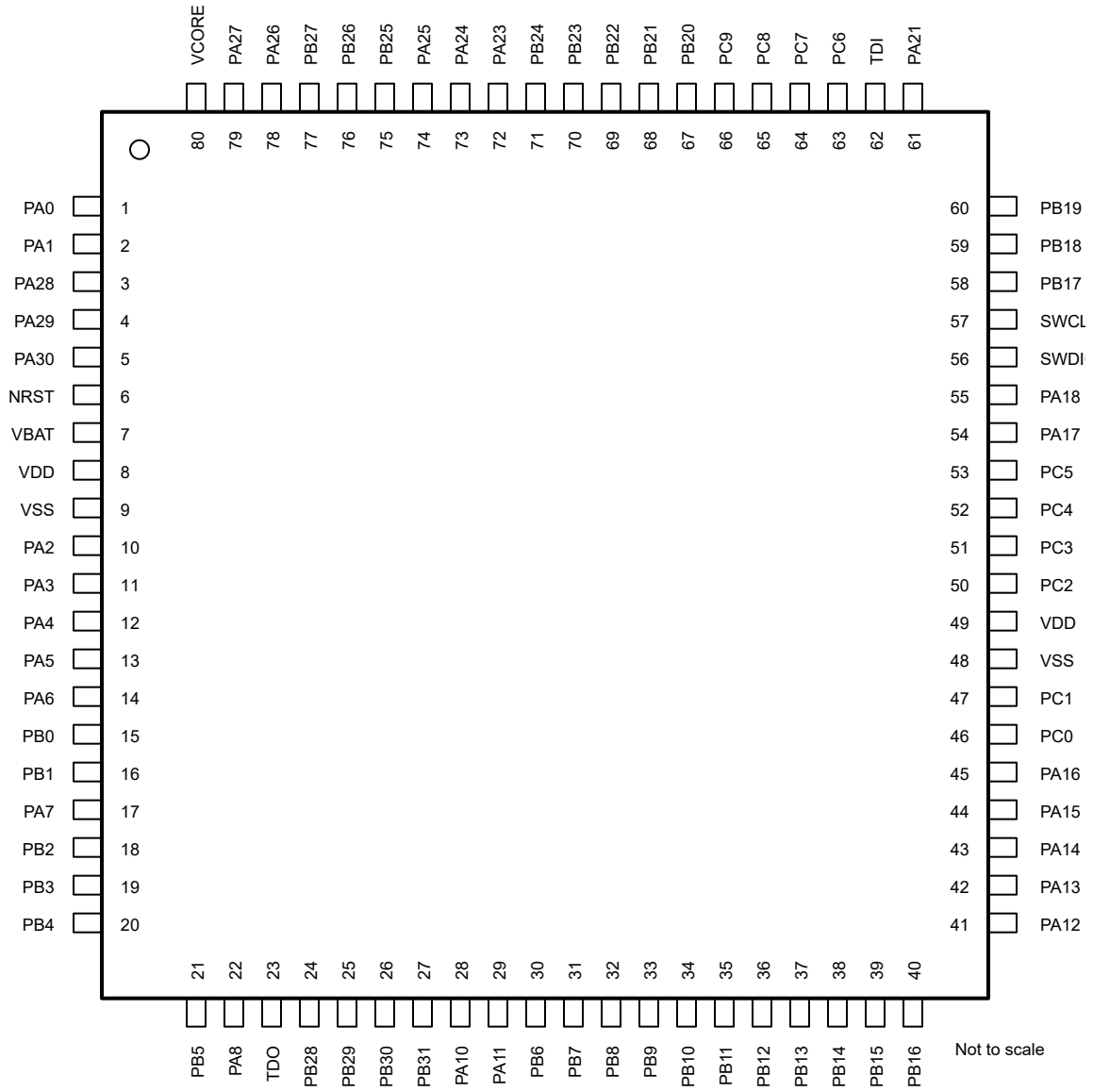

Figure 6-3. 80-pin PN (0.5mm) (LQFP) Package (Top View)

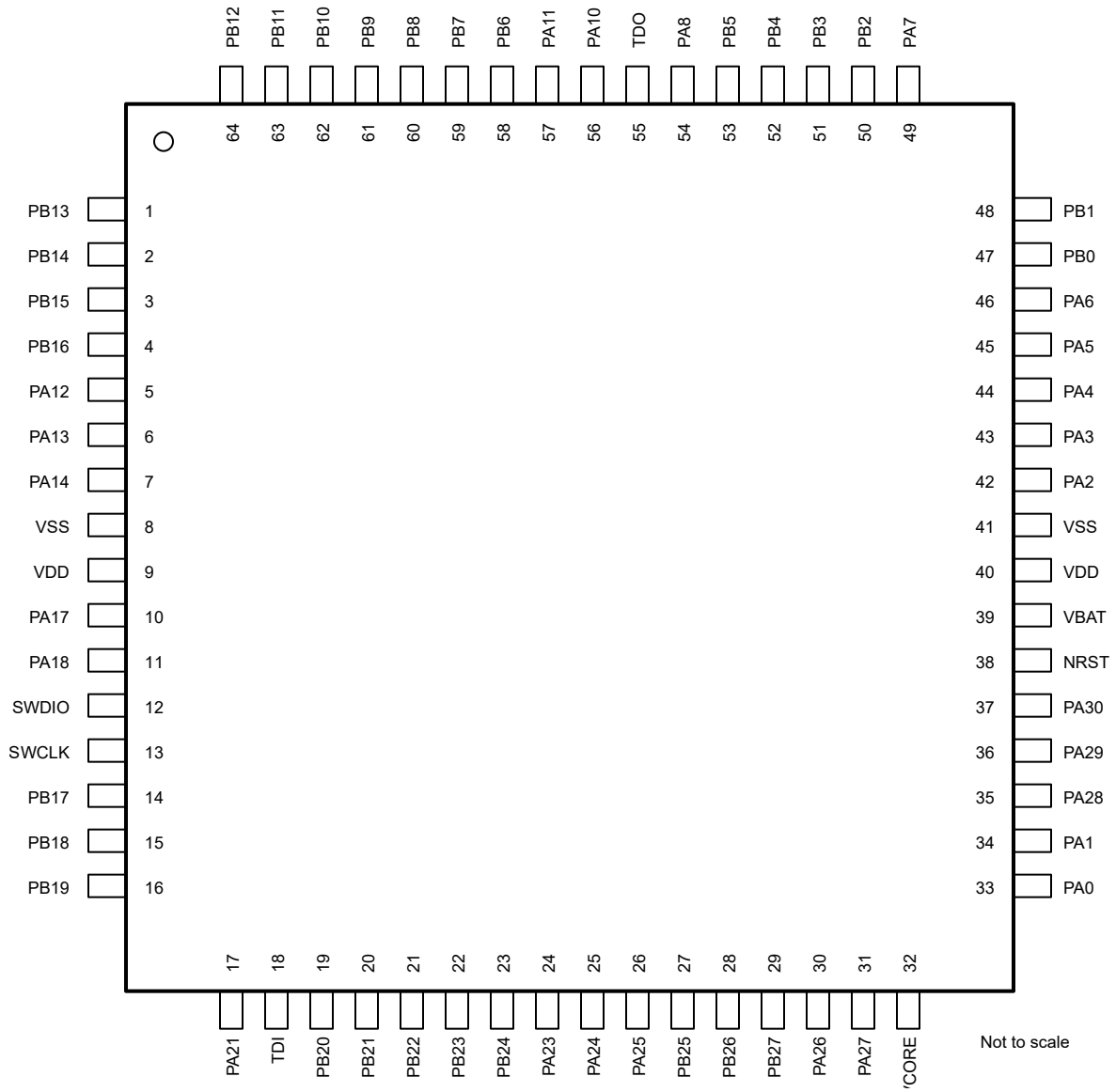

Figure 6-4. 64-pin PM (0.5mm) (LQFP) Package Diagram (Top View)

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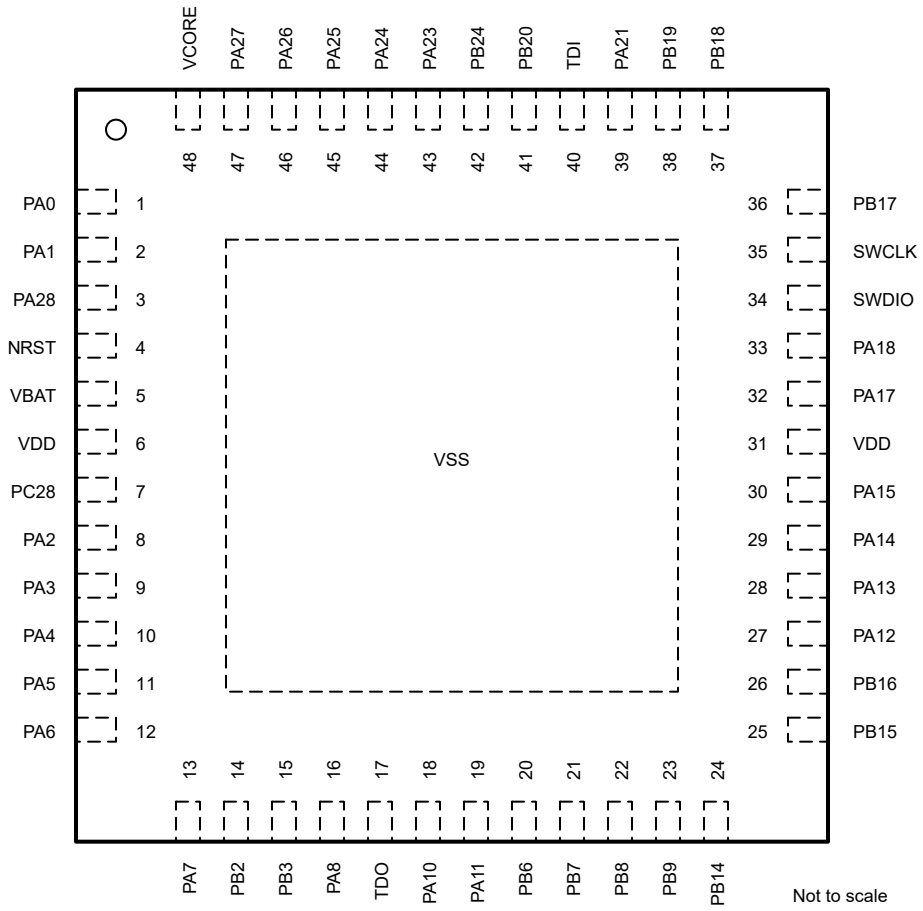


Figure 6-5. 48-pin RGZ (0.5mm) (VQFN) Package Diagram (Top View)

6.2 Pin Attributes

The following table describes the function available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
SDIO (standard drive)	Y		Y	Y	
SDIO (standard drive) with wake	Y		Y	Y	Y
HDIO (High drive)	Y	Y	Y	Y	Y
HSIO (High speed)	Y	Y	Y	Y	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
6	6	6	38	4	B4	NRST	WAKE	(Non-IOMUX 1) 0	I	RESET
							NRST	(Non-IOMUX 2) 0	RESET	
1	1	1	33	1	D3	PA0 PINCM1 0x400cc000	PA0	1	IO	SDIO (standard)with wake
							TIMA0_0_FAL1	2	I	
							UC1_0_SDA_TX	3	IOD	
							UC13_3_SCK_SCL_RX	4	IOD	
							UC12_TX	5	IO	
							UC15_0_SDA	6	IOD	
							BSL_I2C_SDA	(Non-IOMUX 1) 0	IOD	
							WAKE	(Non-IOMUX 2) 0	I	
2	2	2	34	2	C4	PA1 PINCM2 0x400cc004	PA1	1	IO	SDIO (standard)with wake
							TIMA0_1_FAL0	2	I	
							UC1_0_SCL_RX	3	IOD	
							UC13_3_PICO_SDA_TX	4	IOD	
							UC12_RX	5	IO	
							UC15_0_SCL	6	IOD	
							TIMG8_0_IDX	7	I	
							TIMA0_0_C1	8	IO	
							BSL_I2C_SCL	(Non-IOMUX 1) 0	IOD	
							WAKE	(Non-IOMUX 2) 0	I	
15	15	10	42	8	A5	PA2 PINCM7 0x400cc018	PA2	1	IO	SDIO (standard)
							TIMG8_0_C1	2	IO	
							TIMA0_0_C1	3	IO	
							UC12_RX	4	IO	
							UC2_CS0	5	IO	
							UC13_1_POCI_RTS	6	IO	
							UC13_3_POCI_RTS	7	IO	
16	16	11	43	9	A6	PA3 PINCM8 0x400cc01c	PA3	1	IO	SDIO (standard)
							TIMG8_0_C0	2	IO	
							TIMA0_0_C1	3	IO	
							UC1_1_SDA_TX	4	IOD	
							UC2_CS1	5	IO	
							COMP1_OUT	6	O	
							UC15_1_SDA	7	IOD	
							LFXIN	(Non-IOMUX 1) 0	A	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
17	17	12	44	10	A7	PA4 PINCM9 0x400cc020	PA4	1	IO	SDIO (standard)
							LFCLKIN	2	I	
							TIMA0_0_C1N	3	O	
							UC1_1_SCL_RX	4	IOD	
							UC2_POCI	5	IO	
							UC13_1_CS0_CTS	6	IO	
							UC15_1_SCL	7	IOD	
							LFXOUT	(Non-IOMUX 1) 0	A	
18	18	13	45	11	A8	PA5 PINCM10 0x400cc024	PA5	1	IO	SDIO (standard)
							TIMG4_2_C0	2	IO	
							TIMG4_0_C0	3	IO	
							UC2_PICO	5	IO	
							HFXIN	(Non-IOMUX 1) 0	A	
19	19	14	46	12	A9	PA6 PINCM11 0x400cc028	PA6	1	IO	SDIO (standard)
							TIMG4_2_C1	2	IO	
							HFCLKIN	3	I	
							TIMA0_0_C2N	4	O	
							UC2_SCK	5	IOD	
							TIMG4_0_C1	6	IO	
							HFXOUT	(Non-IOMUX 1) 0	A	
22	22	17	49	13	B7	PA7 PINCM14 0x400cc034	PA7	1	IO	SDIO (standard)
							TIMG4_3_C1	2	IO	
							CLK_OUT	3	O	
							COMP0_OUT	4	O	
							TIMA0_0_C2	5	IO	
							I2S0_WCLK	6	IO	
27	27	22	54	16	D10	PA8 PINCM19 0x400cc048	PA8	1	IO	HSIO (high-speed)
							TIMA0_0_C0	2	IO	
							TIMA0_1_C0	3	IO	
							UC1_0_RTS	4	IO	
							UC1_1_SDA_TX	5	IOD	
							UC2_SCK	6	IOD	
							UC12_RTS	7	IO	
							I2S0_WCLK	8	IO	
33	33	28	56	18	E7	PA10 PINCM21 0x400cc050	PA10	1	IO	HDIO (high-drive)with wake
							TIMG12_0_C0	2	IO	
							TIMA0_0_C2	3	IO	
							UC1_0_SDA_TX	4	IOD	
							UC2_POCI	5	IO	
							UC15_0_SDA	6	IOD	
							UC12_TX	7	IO	
							UC13_1_SCK_SCL_RX	8	IOD	
							BSL_UART_TX	(Non-IOMUX 1) 0	O	
							WAKE	(Non-IOMUX 2) 0	I	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
34	34	29	57	19	E9	PA11 PINCM22 0x400cc054	PA11	1	IO	HDIO (high-drive)with wake
							TIMA0_1_C0N	2	O	
							TIMA0_0_C2N	3	O	
							UC1_0_SCL_RX	4	IOD	
							UC2_SCK	5	IOD	
							UC15_0_SCL	6	IOD	
							UC12_RX	7	IO	
							COMP0_OUT	8	O	
							BSL_UART_RX	(Non-IOMUX 1) 0	I	
							WAKE	(Non-IOMUX 2) 0	I	
51	51	41	5	27	J10	PA12 PINCM34 0x400cc084	PA12	1	IO	HSIO (high-speed)
							CAN0_TX	2	O	
							TIMG4_0_C0	3	IO	
							FCC_IN	4	I	
							I2S0_BCLK	5	IO	
							QSPI_IO0	6	IO	
							UC13_0_CS0_CTS	7	IO	
							TIMA0_1_C1	8	IO	
							A0_8	(Non-IOMUX 1) 0	A	
52	52	42	6	28	K10	PA13 PINCM35 0x400cc088	PA13	1	IO	HSIO (high-speed)
							CAN0_RX	2	I	
							TIMG4_0_C1	3	IO	
							TIMA0_1_FAL1	4	I	
							I2S0_AD0	5	IO	
							QSPI_IO2	6	IO	
							UC13_0_SCK_SCL_RX	7	IOD	
							UC13_0_POCI_RTS	8	IO	
							UC12_TX	9	IO	
							A0_9	(Non-IOMUX 1) 0	A	
							COMP0_IN2-	(Non-IOMUX 2) 0	A	
							VMON3	(Non-IOMUX 3) 0	A	
53	53	43	7	29	K8	PA14 PINCM36 0x400cc08c	PA14	1	IO	HSIO (high-speed)
							CLK_OUT	2	O	
							TIMA0_1_C1N	3	O	
							TIMA0_0_C3	4	IO	
							I2S0_AD1	5	IO	
							QSPI_IO1	6	IO	
							UC1_0_CTS	7	IO	
							UC13_0_PICO_SDA_TX	8	IOD	
							UC12_RX	9	IO	
							A0_12	(Non-IOMUX 1) 0	A	
							COMP0_IN2+	(Non-IOMUX 2) 0	A	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
54	54	44		30	K7	PA15 PINCM37 0x400cc090	PA15	1	IO	SDIO (standard)
							TIMG8_0_IDX	2	I	
							TIMA0_0_C2	3	IO	
							UC1_1_SCL_RX	4	IOD	
							UC15_1_SCL	6	IOD	
							UC1_0_RTS	7	IO	
							I2S0_WCLK	8	IO	
							A1_0	(Non-IOMUX 1) 0	A	
							COMP0_IN3+	(Non-IOMUX 2) 0	A	
							COMP1_IN3+	(Non-IOMUX 3) 0	A	
55	55	45			H7	PA16 PINCM38 0x400cc094	PA16	1	IO	SDIO (standard)
							TIMA0_0_C2N	2	O	
							FCC_IN	3	I	
							UC1_1_SDA_TX	4	IOD	
							UC13_0_POCI_RTS	5	IO	
							UC15_1_SDA	6	IOD	
							QSPI_CS3	7	IO	
							A1_1	(Non-IOMUX 1) 0	A	
69	69	54	10	32	K4	PA17 PINCM39 0x400cc098	WAKE	(Non-IOMUX 0) 0	I	SDIO (standard)with wake
							PA17	1	IO	
							TIMG4_3_C0	2	IO	
							TIMA0_0_C3	3	IO	
							UC1_1_SDA_TX	4	IOD	
							UC13_0_SCK_SCL_RX	5	IOD	
							A1_2	(Non-IOMUX 1) 0	A	
							COMP0_IN1-	(Non-IOMUX 2) 0	A	
70	70	55	11	33	K3	PA18 PINCM40 0x400cc09c	PA18	1	IO	SDIO (standard)with wake
							TIMA0_0_C3N	2	O	
							I2S0_WCLK	3	IO	
							UC1_1_SCL_RX	4	IOD	
							UC13_0_PICO_SDA_TX	5	IOD	
							UC13_1_CS0_CTS	6	IO	
							QSPI_CS1	7	IO	
							BSL_INVOKE	(Non-IOMUX 1) 0	I	
							WAKE	(Non-IOMUX 2) 0	I	
							A0_10	(Non-IOMUX 3) 0	A	
							A1_3	(Non-IOMUX 4) 0	A	
							COMP0_IN1+	(Non-IOMUX 5) 0	A	
							VMON0	(Non-IOMUX 6) 0	A	
71	71	56	12	34	J4	PA19 PINCM41 0x400cc0a0	PA19	1	IO	SDIO (standard)
							SWDIO	2	IO	
							UC15_0_SDA	3	IOD	
							UC12_TX	4	IO	
							A0_15	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
72	72	57	13	35	J3	PA20 PINCM42 0x400cc0a4	PA20	1	IO	SDIO (standard)
							SWCLK	2	I	
							UC15_0_SCL	3	IOD	
							UC12_RX	4	IO	
							A0_16	(Non-IOMUX 1) 0	A	
76	76	61	17	39	J2	PA21 PINCM46 0x400cc0b4	PA21	1	IO	SDIO (standard)
							TIMG4_2_C0	2	IO	
							TIMA0_0_C0	3	IO	
							I2S0_AD0	4	IO	
							UC1_1_CTS	5	IO	
							UC13_1_PICO_SDA_TX	6	IOD	
							UC13_2_CS0_CTS	7	IO	
							A1_7	(Non-IOMUX 1) 0	A	
							VREF-	(Non-IOMUX 2) 0	A	
92	92	72	24	43	E1	PA23 PINCM53 0x400cc0d0	PA23	1	IO	SDIO (standard)
							TIMA0_0_C3	2	IO	
							I2S0_WCLK	3	IO	
							UC13_1_PICO_SDA_TX	4	IOD	
							UC13_0_CS0_CTS	5	IO	
							UC2_CS3	6	IO	
							UC13_2_SCK_SCL_RX	7	IOD	
							TIMG4_0_C0	9	IO	
							COMP1_IN1-	(Non-IOMUX 1) 0	A	
							VREF+	(Non-IOMUX 2) 0	A	
93	93	73	25	44	E2	PA24 PINCM54 0x400cc0d4	PA24	1	IO	SDIO (standard)
							TIMA0_0_C3N	2	O	
							I2S0_AD1	3	IO	
							UC13_1_SCK_SCL_RX	4	IOD	
							UC13_0_POCI_RTS	5	IO	
							UC2_CS2	6	IO	
							UC13_2_PICO_SDA_TX	7	IOD	
							TIMG12_0_C1	8	IO	
							TIMG4_0_C1	9	IO	
							A0_3	(Non-IOMUX 1) 0	A	
							COMP0_DAC_OUT	(Non-IOMUX 2) 0	A	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
94	94	74	26	45	D1	PA25 PINCM55 0x400cc0d8	PA25	1	IO	HSIO (high-speed)
							TIMA0_0_C1N	2	O	
							I2S0_AD0	3	IO	
							UC13_0_SCK_SCL_RX	4	IOD	
							UC13_3_SCK_SCL_RX	5	IOD	
							UC13_1_POCI_RTS	6	IO	
							A0_2	(Non-IOMUX 1) 0	A	
							COMP1_DAC_OUT	(Non-IOMUX 2) 0	A	
98	98	78	30	46	C2	PA26 PINCM59 0x400cc0e8	PA26	1	IO	SDIO (standard)
							TIMG4_3_C0	2	IO	
							TIMA0_0_FAL0	3	I	
							CAN0_TX	4	O	
							UC13_0_PICO_SDA_TX	5	IOD	
							UC13_0_CS0_CTS	6	IO	
							UC13_3_PICO_SDA_TX	7	IOD	
							BSL_CAN_TX	(Non-IOMUX 1) 0	O	
							A0_1	(Non-IOMUX 2) 0	A	
							COMP0_IN0+	(Non-IOMUX 3) 0	A	
							VMON1	(Non-IOMUX 4) 0	A	
99	99	79	31	47	B2	PA27 PINCM60 0x400cc0ec	PA27	1	IO	SDIO (standard)
							TIMG4_3_C1	2	IO	
							RTC_OUT	3	O	
							CAN0_RX	4	I	
							TIMG4_1_C0	5	IO	
							TIMA0_0_FAL2	6	I	
							UC13_3_POCI_RTS	7	IO	
							UC2_CS1	8	IO	
							BSL_CAN_RX	(Non-IOMUX 1) 0	I	
							A0_0	(Non-IOMUX 2) 0	A	
							COMP0_IN0-	(Non-IOMUX 3) 0	A	
							VMON2	(Non-IOMUX 4) 0	A	
3	3	3	35	3	C3	PA28 PINCM3 0x400cc008	PA28	1	IO	HDIO (high-drive)with wake
							TIMA0_0_FAL0	2	I	
							UC1_0_SDA_TX	3	IOD	
							UC13_3_CS0_CTS	4	IO	
							UC12_TX	5	IO	
							UC15_0_SDA	6	IOD	
							WAKE	(Non-IOMUX 1) 0	I	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
4	4	4	36		B3	PA29 PINCM4 0x400cc00c	PA29	1	IO	SDIO (standard)
							TIMG4_2_C0	2	IO	
							TIMA0_1_FAL1	3	I	
							UC13_3_POCI_RTS	4	IO	
							UC12_RTS	5	IO	
							UC1_1_SCL_RX	6	IOD	
							UC15_1_SCL	7	IOD	
5	5	5	37		D4	PA30 PINCM5 0x400cc010	PA30	1	IO	SDIO (standard)
							TIMG4_2_C1	2	IO	
							TIMA0_0_FAL2	3	I	
							UC12_CTS	5	IO	
							UC1_1_SDA_TX	6	IOD	
							UC15_1_SDA	7	IOD	
20	20	15	47		C6	PB0 PINCM12 0x400cc02c	PB0	1	IO	SDIO (standard)
							UC1_0_SDA_TX	2	IOD	
							TIMG4_1_C0	3	IO	
							UC12_TX	4	IO	
							TIMA0_1_C2	5	IO	
21	21	16	48		C7	PB1 PINCM13 0x400cc030	PB1	1	IO	SDIO (standard)
							UC1_0_SCL_RX	2	IOD	
							TIMG4_1_C1	3	IO	
							UC12_RX	4	IO	
							TIMA0_1_C2N	5	O	
23	23	18	50	14	C8	PB2 PINCM15 0x400cc038	PB2	1	IO	SDIO (standard)
							TIMG4_2_C0	2	IO	
							TIMA0_0_C3	3	IO	
							UC13_1_CS0_CTS	4	IO	
							UC1_1_SCL_RX	5	IOD	
							UC15_1_SCL	6	IOD	
24	24	19	51	15	D8	PB3 PINCM16 0x400cc03c	PB3	1	IO	SDIO (standard)
							TIMG4_2_C1	2	IO	
							TIMA0_0_C3N	3	O	
							UC13_1_POCI_RTS	4	IO	
							UC1_1_SDA_TX	5	IOD	
							UC15_1_SDA	6	IOD	
25	25	20	52		D9	PB4 PINCM17 0x400cc040	PB4	1	IO	SDIO (standard)
							TIMA0_0_C2	2	IO	
							UC1_1_SDA_TX	3	IOD	
							UC13_0_CS0_CTS	4	IO	
							UC13_1_PICO_SDA_TX	5	IOD	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
26	26	21	53		B8	PB5 PINCM18 0x400cc044	PB5	1	IO	HSIO (high-speed)
							TIMA0_0_C2N	2	O	
							UC1_1_SCL_RX	3	IOD	
							UC13_0_POCI_RTS	4	IO	
							UC13_1_POCI_RTS	5	IO	
							UC2_POCI	6	IO	
40	40	30	58	20	E10	PB6 PINCM23 0x400cc058	PB6	1	IO	HSIO (high-speed)
							TIMG4_2_C0	2	IO	
							TIMA0_1_C0	3	IO	
							I2S1_AD0	4	IO	
							UC1_1_SDA_TX	5	IOD	
							UC12_CTS	6	IO	
							UC2_CS1	7	IO	
							CAN1_RX	9	I	
41	41	31	59	21	F8	PB7 PINCM24 0x400cc05c	PB7	1	IO	HSIO (high-speed)
							TIMG4_2_C1	2	IO	
							TIMG8_1_C0	3	IO	
							TIMA0_1_C0N	4	O	
							I2S1_AD1	5	IO	
							UC1_1_SCL_RX	6	IOD	
							UC12_RTS	7	IO	
							UC13_0_POCI_RTS	8	IO	
							CAN1_TX	9	O	
42	42	32	60	22	F9	PB8 PINCM25 0x400cc060	PB8	1	IO	SDIO (standard)
							TIMG8_1_IDX	2	I	
							COMP1_OUT	3	O	
							TIMA0_1_FAL1	4	I	
							I2S1_WCLK	5	IO	
							UC1_1_CTS	6	IO	
							UC13_0_SCK_SCL_RX	7	IOD	
							UC13_0_PICO_SDA_TX	8	IOD	
43	43	33	61	23	G7	PB9 PINCM26 0x400cc064	PB9	1	IO	HSIO (high-speed)
							TIMG8_1_C1	2	IO	
							TIMA0_0_C0N	3	O	
							I2S1_BCLK	4	IO	
							UC1_1_RTS	5	IO	
							UC13_0_PICO_SDA_TX	6	IOD	
							UC13_0_SCK_SCL_RX	7	IOD	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
44	44	34	62		F10	PB10 PINCM27 0x400cc068	PB10	1	IO	SDIO (standard)
							TIMG4_2_C0	2	IO	
							TIMG4_0_C0	3	IO	
							I2S1_MCLK	4	IO	
							UC13_2_PICO_SDA_TX	5	IOD	
							TIMA0_1_C1	6	IO	
							I2S0_WCLK	8	IO	
45	45	35	63		G9	PB11 PINCM28 0x400cc06c	PB11	1	IO	SDIO (standard)
							TIMG4_2_C1	2	IO	
							CLK_OUT	3	O	
							TIMG4_0_C1	4	IO	
							UC13_2_SCK_SCL_RX	5	IOD	
							TIMA0_1_C1N	6	O	
							I2S0_BCLK	8	IO	
46	46	36	64		G10	PB12 PINCM29 0x400cc070	PB12	1	IO	SDIO (standard)
							TIMA0_0_FAL1	2	I	
							UC13_0_PICO_SDA_TX	3	IOD	
							UC13_2_CS0_CTS	4	IO	
							I2S0_AD0	8	IO	
47	47	37	1		H10	PB13 PINCM30 0x400cc074	PB13	1	IO	SDIO (standard)
							TIMG12_0_C0	2	IO	
							TIMA0_0_C1N	3	O	
							UC13_0_SCK_SCL_RX	4	IOD	
							UC13_2_POCI_RTS	5	IO	
							QSPI_CS2	6	IO	
							I2S0_AD1	8	IO	
48	48	38	2	24	J9	PB14 PINCM31 0x400cc078	PB14	1	IO	SDIO (standard)
							TIMG8_0_IDX	2	I	
							TIMG12_0_C1	3	IO	
							TIMA0_0_C0	4	IO	
							QSPI_CS0	6	IO	
							UC13_0_POCI_RTS	7	IO	
							I2S0_MCLK	8	IO	
49	49	39	3	25	G8	PB15 PINCM32 0x400cc07c	PB15	1	IO	HSIO (high-speed)
							TIMG4_3_C0	2	IO	
							TIMG8_0_C0	3	IO	
							TIMA0_1_C3	4	IO	
							I2S0_MCLK	5	IO	
							QSPI_IO3	6	IO	
							UC13_1_PICO_SDA_TX	7	IOD	
							UC12_TX	8	IO	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
50	50	40	4	26	J8	PB16 PINCM33 0x400cc080	PB16	1	IO	HSIO (high-speed)
							TIMG4_3_C1	2	IO	
							TIMG8_0_C1	3	IO	
							TIMA0_1_C3N	4	O	
							I2S0_WCLK	5	IO	
							QSPI_CLK	6	IOD	
							UC13_1_SCK_SCL_RX	7	IOD	
							UC12_RX	8	IO	
73	73	58	14	36	K2	PB17 PINCM43 0x400cc0a8	PB17	1	IO	SDIO (standard)
							TIMA0_0_C2	2	IO	
							UC13_1_PICO_SDA_TX	3	IOD	
							UC2_PICO	4	IO	
							A1_4	(Non-IOMUX 1) 0	A	
							COMP1_IN2-	(Non-IOMUX 2) 0	A	
74	74	59	15	37	K1	PB18 PINCM44 0x400cc0ac	PB18	1	IO	SDIO (standard)
							TIMA0_0_C2N	2	O	
							UC13_1_SCK_SCL_RX	3	IOD	
							UC2_SCK	4	IOD	
							A1_5	(Non-IOMUX 1) 0	A	
							COMP1_IN2+	(Non-IOMUX 2) 0	A	
75	75	60	16	38	J1	PB19 PINCM45 0x400cc0b0	PB19	1	IO	SDIO (standard)
							TIMG4_3_C1	2	IO	
							TIMA0_1_C2	3	IO	
							UC2_POCI	4	IO	
							UC1_0_CTS	5	IO	
							A1_6	(Non-IOMUX 1) 0	A	
82	82	67	19	41	F3	PB20 PINCM48 0x400cc0bc	PB20	1	IO	SDIO (standard)
							TIMG12_0_C0	2	IO	
							TIMA0_0_C1	3	IO	
							TIMA0_1_C2N	4	O	
							I2S1_AD0	5	IO	
							UC2_CS2	6	IO	
							A0_6	(Non-IOMUX 1) 0	A	
83	83	68	20		G2	PB21 PINCM49 0x400cc0c0	PB21	1	IO	SDIO (standard)
							TIMG8_0_C0	2	IO	
							CAN1_TX	3	O	
							TIMA0_1_C3	4	IO	
							I2S1_AD1	5	IO	
							UC14_SCL_RX	6	IOD	
							A1_8	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
84	84	69	21		H1	PB22 PINCM50 0x400cc0c4	PB22	1	IO	SDIO (standard)
							TIMG8_0_C1	2	IO	
							CAN1_RX	3	I	
							TIMA0_1_C3N	4	O	
							I2S1_WCLK	5	IO	
							UC14_SDA_TX	6	IOD	
							UC13_0_PICO_SDA_TX	7	IOD	
							A1_10	(Non-IOMUX 1) 0	A	
85	85	70	22		G1	PB23 PINCM51 0x400cc0c8	PB23	1	IO	SDIO (standard)
							TIMG4_1_C0	4	IO	
							I2S1_BCLK	5	IO	
							UC14_CTS	6	IO	
							UC13_0_SCK_SCL_RX	7	IOD	
							A1_11	(Non-IOMUX 1) 0	A	
86	86	71	23	42	F2	PB24 PINCM52 0x400cc0cc	PB24	1	IO	SDIO (standard)
							TIMG12_0_C1	2	IO	
							TIMA0_1_FAL2	3	I	
							TIMG4_1_C1	4	IO	
							I2S1_MCLK	5	IO	
							UC14_RTS	6	IO	
							UC2_CS3	7	IO	
							A0_5	(Non-IOMUX 1) 0	A	
							COMP1_IN1+	(Non-IOMUX 2) 0	A	
95	95	75	27		C1	PB25 PINCM56 0x400cc0dc	PB25	1	IO	SDIO (standard)
							TIMA0_0_FAL2	2	I	
							I2S0_BCLK	3	IO	
							UC1_0_CTS	4	IO	
							A0_4	(Non-IOMUX 1) 0	A	
96	96	76	28		B1	PB26 PINCM57 0x400cc0e0	PB26	1	IO	SDIO (standard)
							TIMG4_2_C0	2	IO	
							I2S0_MCLK	3	IO	
							UC1_0_RTS	4	IO	
							A1_13	(Non-IOMUX 1) 0	A	
							COMP1_IN0+	(Non-IOMUX 2) 0	A	
97	97	77	29		D2	PB27 PINCM58 0x400cc0e4	PB27	1	IO	SDIO (standard)
							TIMG4_2_C1	2	IO	
							A1_14	(Non-IOMUX 1) 0	A	
							COMP1_IN0-	(Non-IOMUX 2) 0	A	
29	29	24			E8	PB28 PINCM65 0x400cc100	PB28	1	IO	SDIO (standard)
							TIMA0_0_C0	2	IO	
							UC13_3_SCK_SCL_RX	3	IOD	
							UC13_0_CS0_CTS	4	IO	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
30	30	25			B9	PB29 PINCM66 0x400cc104	PB29	1	IO	SDIO (standard)
							TIMA0_0_C0N	2	O	
							TIMG8_1_C0	3	IO	
							UC13_3_PICO_SDA_TX	4	IOD	
							UC13_0_POCI_RTS	5	IO	
31	31	26			D7	PB30 PINCM67 0x400cc108	PB30	1	IO	SDIO (standard)
							TIMA0_0_C1	2	IO	
							TIMG8_1_C1	3	IO	
							UC13_3_CS0_CTS	4	IO	
							UC13_0_PICO_SDA_TX	5	IOD	
32	32	27			A10	PB31 PINCM68 0x400cc10c	PB31	1	IO	SDIO (standard)
							TIMG8_0_IDX	2	I	
							TIMA0_0_C1N	3	O	
							UC13_3_POCI_RTS	4	IO	
							UC13_0_SCK_SCL_RX	5	IOD	
							TIMG8_1_IDX	6	I	
56	56	46			J7	PC0 PINCM74 0x400cc124	PC0	1	IO	SDIO (standard)
							TIMG8_0_C0	2	IO	
							TIMA0_0_C2	3	IO	
							QSPI_CS0	7	IO	
57	57	47			H8	PC1 PINCM75 0x400cc128	PC1	1	IO	SDIO (standard)
							TIMG8_0_C1	2	IO	
							TIMA0_0_C2N	3	O	
65	65	50			H5	PC2 PINCM76 0x400cc12c	PC2	1	IO	SDIO (standard)
							TIMA0_0_C0	2	IO	
							TIMA0_1_FAL0	3	I	
							UC13_0_SCK_SCL_RX	4	IOD	
							TIMG4_1_C1	5	IO	
							UC13_0_CS0_CTS	6	IO	
							UC13_3_CS0_CTS	7	IO	
							UC2_CS0	8	IO	
66	66	51			H4	PC3 PINCM77 0x400cc130	PC3	1	IO	SDIO (standard)
							TIMG4_3_C1	2	IO	
							TIMA0_0_C0N	3	O	
							UC13_0_PICO_SDA_TX	4	IOD	
							A0_21	(Non-IOMUX 1) 0	A	
67	67	52			G6	PC4 PINCM78 0x400cc134	PC4	1	IO	SDIO (standard)
							TIMA0_0_C1	2	IO	
							A0_13	(Non-IOMUX 1) 0	A	
68	68	53			G5	PC5 PINCM79 0x400cc138	PC5	1	IO	SDIO (standard)
							TIMA0_0_C1N	2	O	
							A0_14	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
78	78	63			H3	PC6 PINCM84 0x400cc14c	PC6	1	IO	SDIO (standard)
							TIMG4_2_C0	2	IO	
							TIMA0_0_C0	3	IO	
							UC13_0_PICO_SDA_TX	4	IOD	
							UC2_CS1	5	IO	
							A0_17	(Non-IOMUX 1) 0	A	
79	79	64			G3	PC7 PINCM85 0x400cc150	PC7	1	IO	SDIO (standard)
							TIMG4_2_C1	2	IO	
							TIMA0_0_C0N	3	O	
							UC13_0_SCK_SCL_RX	4	IOD	
							UC2_CS0	5	IO	
							A0_18	(Non-IOMUX 1) 0	A	
80	80	65			G4	PC8 PINCM86 0x400cc154	PC8	1	IO	SDIO (standard)
							TIMA0_0_C1	2	IO	
							UC13_0_CS0_CTS	3	IO	
							A0_19	(Non-IOMUX 1) 0	A	
81	81	66			F4	PC9 PINCM87 0x400cc158	PC9	1	IO	SDIO (standard)
							TIMA0_0_C1N	2	O	
							UC13_0_POCI_RTS	3	IO	
							A0_20	(Non-IOMUX 1) 0	A	
87	87				F5	PC10 PINCM88 0x400cc15c	PC10	1	IO	SDIO (standard)
							TIMG8_1_C0	2	IO	
							UC14_SCL_RX	3	IOD	
							A1_12	(Non-IOMUX 1) 0	A	
88	88				E5	PC11 PINCM89 0x400cc160	PC11	1	IO	SDIO (standard)
							TIMG8_1_C1	2	IO	
							UC14_SDA_TX	3	IOD	
10	10				C5	PC12 PINCM61 0x400cc0f0	PC12	1	IO	SDIO (standard)
							TIMA0_1_C0	2	IO	
12	12				D5	PC13 PINCM62 0x400cc0f4	PC13	1	IO	SDIO (standard)
							TIMG4_1_C0	2	IO	
							UC13_1_PICO_SDA_TX	3	IOD	
							UC12_RTS	4	IO	
13	13				B6	PC14 PINCM63 0x400cc0f8	PC14	1	IO	SDIO (standard)
							TIMG4_1_C1	2	IO	
							UC13_1_SCK_SCL_RX	3	IOD	
							UC12_CTS	4	IO	
11	11				B5	PC15 PINCM64 0x400cc0fc	PC15	1	IO	SDIO (standard)
							TIMA0_1_C0N	2	O	
35	35				E6	PC16 PINCM69 0x400cc110	PC16	1	IO	SDIO (standard)

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
36	36				B10	PC17 PINCM70 0x400cc114	PC17	1	IO	SDIO (standard)
							TIMA0_1_C1	2	IO	
38	38				C10	PC18 PINCM71 0x400cc118	PC18	1	IO	SDIO (standard)
							TIMA0_1_C3	2	IO	
39	39				F7	PC19 PINCM72 0x400cc11c	PC19	1	IO	SDIO (standard)
							TIMA0_1_C3N	2	O	
58	58				H9	PC20 PINCM73 0x400cc120	PC20	1	IO	SDIO (standard)
							TIMA0_1_FAL2	2	I	
59	59				H6	PC21 PINCM80 0x400cc13c	PC21	1	IO	SDIO (standard)
							CAN1_TX	2	O	
60	60				K5	PC22 PINCM81 0x400cc140	PC22	1	IO	SDIO (standard)
							CAN1_RX	2	I	
61	61				J6	PC23 PINCM82 0x400cc144	PC23	1	IO	SDIO (standard)
							TIMA0_1_C2	2	IO	
62	62				J5	PC24 PINCM83 0x400cc148	PC24	1	IO	SDIO (standard)
							TIMA0_1_C2N	2	O	
89	89				E4	PC25 PINCM90 0x400cc164	PC25	1	IO	SDIO (standard)
							TIMG8_1_IDX	2	I	
							UC14_CTS	3	IO	
90	90				F1	PC26 PINCM91 0x400cc168	PC26	1	IO	SDIO (standard)
							CAN1_TX	2	O	
							UC14_RTS	3	IO	
91	91				E3	PC27 PINCM92 0x400cc16c	PC27	1	IO	SDIO (standard)
							CAN1_RX	2	I	
14	14			7	D6	PC28 PINCM93 0x400cc170	PC28	1	IO	SDIO (standard)
							UC13_3_SCK_SCL_RX	2	IOD	
							UC12_TX	4	IO	
37	37				F6	PC29 PINCM94 0x400cc174	PC29	1	IO	SDIO (standard)
							TIMA0_1_C1N	2	O	
							UC13_3_PICO_SDA_TX	3	IOD	

Table 6-2. Pin Attributes (PFA, PZ, PN, PM, RGZ, ZAW Packages) (continued)

PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX NAME	SIGNAL TYPE	BUFFER TYPE
77	77	62	18	40	H2	TDI PINCM47 0x400cc0b8	PA22	1	IO	SDIO (standard)
							TIMG4_2_C1	2	IO	
							TIMA0_0_C0N	3	O	
							I2S0_BCLK	4	IO	
							CLK_OUT	5	O	
							UC13_1_SCK_SCL_RX	6	IOD	
							UC13_2_POCI_RTS	7	IO	
							UC1_1_RTS	8	IO	
							TDI	9	I	
							A0_7	(Non-IOMUX 1) 0	A	
							A1_9	(Non-IOMUX 2) 0	A	
28	28	23	55	17	C9	TDO PINCM20 0x400cc04c	PA9	1	IO	HSIO (high-speed)
							TIMA0_0_C0N	2	O	
							RTC_OUT	3	O	
							UC1_0_CTS	4	IO	
							UC1_1_SCL_RX	5	IOD	
							UC2_PICO	6	IO	
							UC12_CTS	7	IO	
							CLK_OUT	8	O	
							I2S0_MCLK	9	IO	
							TDO	10	IO	
7	7	7	39	5	A3	VBAT	VBAT	(Non-IOMUX 1) 0	PWR	PWR
100	100	80	32	48	A1	VCORE	VCORE	(Non-IOMUX 1) 0	PWR	PWR
64, 8	64, 8	49, 8	40, 9	31, 6	A4, K6	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
63, 9	63, 9	48, 9	41, 8	MP	A2, K9	VSS	VSS	(Non-IOMUX 1) 0	PWR	PWR

ADVANCE INFORMATION

6.3 Signal Descriptions

Many MSPM33 signals are made available on multiple device pins. The following list describes the column headers:

1. **SIGNAL NAME**: The name of the signal which can be connected to one of the specified pins.
2. **PIN TYPE**: The signal direction and signal type:
   - I = Input
   - O = Output
   - IO = Input, output, or simultaneous input and output
   - ID = Input with open-drain behavior
   - OD = Output with open-drain behavior
   - IOD = Input, output, or simultaneous input and output with open-drain behavior
   - A = Analog
   - PWR = Power function
3. **DESCRIPTION**: A description of the signal.
4. PIN: Associated pin number.

Note

The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Note

The MP pin referes to the thermal disapation pad at the center of the package.

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
A0_0	A	ADC0 analog input channel 0	99	99	79	31	47	B2
A0_1	A	ADC0 analog input channel 1	98	98	78	30	46	C2
A0_2	A	ADC0 analog input channel 2	94	94	74	26	45	D1
A0_3	A	ADC0 analog input channel 3	93	93	73	25	44	E2
A0_4	A	ADC0 analog input channel 4	95	95	75	27		C1
A0_5	A	ADC0 analog input channel 5	86	86	71	23	42	F2
A0_6	A	ADC0 analog input channel 6	82	82	67	19	41	F3
A0_7	A	ADC0 analog input channel 7	77	77	62	18	40	H2
A0_8	A	ADC0 analog input channel 8	51	51	41	5	27	J10
A0_9	A	ADC0 analog input channel 9	52	52	42	6	28	K10
A0_10	A	ADC0 analog input channel 10	70	70	55	11	33	K3
A0_12	A	ADC0 analog input channel 12	53	53	43	7	29	K8
A0_13	A	ADC0 analog input channel 13	67	67	52			G6
A0_14	A	ADC0 analog input channel 14	68	68	53			G5
A0_15	A	ADC0 analog input channel 15	71	71	56	12	34	J4
A0_16	A	ADC0 analog input channel 16	72	72	57	13	35	J3
A0_17	A	ADC0 analog input channel 17	78	78	63			H3
A0_18	A	ADC0 analog input channel 18	79	79	64			G3
A0_19	A	ADC0 analog input channel 19	80	80	65			G4
A0_20	A	ADC0 analog input channel 20	81	81	66			F4
A0_21	A	ADC0 analog input channel 21	66	66	51			H4
A1_0	A	ADC1 analog input channel 0	54	54	44		30	K7
A1_1	A	ADC1 analog input channel 1	55	55	45			H7
A1_2	A	ADC1 analog input channel 2	69	69	54	10	32	K4
A1_3	A	ADC1 analog input channel 3	70	70	55	11	33	K3
A1_4	A	ADC1 analog input channel 4	73	73	58	14	36	K2
A1_5	A	ADC1 analog input channel 5	74	74	59	15	37	K1
A1_6	A	ADC1 analog input channel 6	75	75	60	16	38	J1
A1_7	A	ADC1 analog input channel 7	76	76	61	17	39	J2
A1_8	A	ADC1 analog input channel 8	83	83	68	20		G2
A1_9	A	ADC1 analog input channel 9	77	77	62	18	40	H2
A1_10	A	ADC1 analog input channel 10	84	84	69	21		H1
A1_11	A	ADC1 analog input channel 11	85	85	70	22		G1
A1_12	A	ADC1 analog input channel 12	87	87				F5

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
A1_13	A	ADC1 analog input channel 13	96	96	76	28		B1
A1_14	A	ADC1 analog input channel 14	97	97	77	29		D2

Table 6-4. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
CLK_OUT	O	CLK_OUT digital clock output from the PMCU	22, 28, 45, 53, 77	22, 28, 45, 53, 77	17, 23, 35, 43, 62	18, 49, 55, 63, 7	13, 17, 29, 40	B7, C9, G9, H2, K8
FCC_IN	I	Frequency clock counter (FCC) input signal	51, 55	51, 55	41, 45	5	27	H7, J10
HFCLKIN	I	High frequency clock digital clock input signal	19	19	14	46	12	A9
HFXIN	A	High frequency crystal oscillator (HFXT) signal	18	18	13	45	11	A8
HFXOUT	A	High frequency crystal oscillator (HFXT) signal	19	19	14	46	12	A9
LFCLKIN	I	Low frequency clock digital clock input signal	17	17	12	44	10	A7
LFXIN	A	Low frequency crystal oscillator (LFXT) signal	16	16	11	43	9	A6
LFXOUT	A	Low frequency crystal oscillator (LFXT) signal	17	17	12	44	10	A7

Table 6-5. Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
BSL_CAN_RX	I	BSL CAN receive signal (RX)	99	99	79	31	47	B2
BSL_CAN_TX	O	BSL CAN transmit signal (TX)	98	98	78	30	46	C2
BSL_I2C_SCL	IOD	BSL I2C clock signal (SCL)	2	2	2	34	2	C4
BSL_I2C_SDA	IOD	BSL I2C data signal (SDA)	1	1	1	33	1	D3
BSL_INVOKE	I	BSL invoke signal (if BSL is enabled, must be HIGH during BOOTRST for a BSL entry, and LOW during BOOTRST to prevent BSL entry)	70	70	55	11	33	K3
BSL_UART_RX	I	BSL UART receive signal (RXD)	34	34	29	57	19	E9
BSL_UART_TX	O	BSL UART transmit signal (TXD)	33	33	28	56	18	E7

Table 6-6. Comparator (COMP) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
COMP0_DAC_OUT	A	COMP0 DAC output	93	93	73	25	44	E2
COMP0_OUT	O	COMP0 output	22, 34	22, 34	17, 29	49, 57	13, 19	B7, E9
COMP1_DAC_OUT	A	COMP1 DAC output	94	94	74	26	45	D1
COMP1_OUT	O	COMP1 output	16, 42	16, 42	11, 32	43, 60	22, 9	A6, F9

ADVANCE INFORMATION

Table 6-6. Comparator (COMP) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
COMP0_IN0+	A	COMP0 non-inverting input 0	98	98	78	30	46	C2
COMP0_IN0-	A	COMP0 inversting input 0	99	99	79	31	47	B2
COMP0_IN1+	A	COMP0 non-inverting input 1	70	70	55	11	33	K3
COMP0_IN1-	A	COMP0 inversting input 1	69	69	54	10	32	K4
COMP0_IN2+	A	COMP0 non-inverting input 2	53	53	43	7	29	K8
COMP0_IN2-	A	COMP0 inversting input 2	52	52	42	6	28	K10
COMP0_IN3+	A	COMP0 non-inverting input 3	54	54	44		30	K7
COMP1_IN0+	A	COMP1 non-inverting input 0	96	96	76	28		B1
COMP1_IN0-	A	COMP1 inversting input 0	97	97	77	29		D2
COMP1_IN1+	A	COMP1 non-inverting input 1	86	86	71	23	42	F2
COMP1_IN1-	A	COMP1 inversting input 1	92	92	72	24	43	E1
COMP1_IN2+	A	COMP1 non-inverting input 2	74	74	59	15	37	K1
COMP1_IN2-	A	COMP1 inversting input 2	73	73	58	14	36	K2
COMP1_IN3+	A	COMP1 non-inverting input 3	54	54	44		30	K7
VMON0	A	Low power voltage monitor input 0 signal	70	70	55	11	33	K3
VMON1	A	Low power voltage monitor input 1 signal	98	98	78	30	46	C2
VMON2	A	Low power voltage monitor input 2 signal	99	99	79	31	47	B2
VMON3	A	Low power voltage monitor input 3 signal	52	52	42	6	28	K10

Table 6-7. Controller Area Network (CAN) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
CAN0_RX	I	CANFD0 receive signal	52, 99	52, 99	42, 79	31, 6	28, 47	B2, K10
CAN0_TX	O	CANFD0 transmit signal	51, 98	51, 98	41, 78	30, 5	27, 46	C2, J10
CAN1_RX	I	CANFD1 receive signal	40, 60, 84, 91	40, 60, 84, 91	30, 69	21, 58	20	E10, E3, H1, K5
CAN1_TX	O	CANFD1 transmit signal	41, 59, 83, 90	41, 59, 83, 90	31, 68	20, 59	21	F1, F8, G2, H6

Table 6-8. Digital Audio Interface (I2S) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
I2S0_BCLK	IO	Digital audio interface (I2S0) bit clock signal	45, 51, 77, 95	45, 51, 77, 95	35, 41, 62, 75	18, 27, 5, 63	27, 40	C1, G9, H2, J10
I2S0_MCLK	IO	Digital audio interface (I2S0) auxiliary output signal	28, 48, 49, 96	28, 48, 49, 96	23, 38, 39, 76	2, 28, 3, 55	17, 24, 25	B1, C9, G8, J9
I2S0_WCLK	IO	Digital audio interface (I2S0) word clock signal	22, 27, 44, 50, 54, 70, 92	22, 27, 44, 50, 54, 70, 92	17, 22, 34, 40, 44, 55, 72	11, 24, 4, 49, 54, 62	13, 16, 26, 30, 33, 43	B7, D10, E1, F10, J8, K3, K7
I2S1_BCLK	IO	Digital audio interface (I2S1) bit clock signal	43, 85	43, 85	33, 70	22, 61	23	G1, G7
I2S1_MCLK	IO	Digital audio interface (I2S1) auxiliary output signal	44, 86	44, 86	34, 71	23, 62	42	F10, F2

Table 6-8. Digital Audio Interface (I2S) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
I2S1_WCLK	IO	Digital audio interface (I2S1) word clock signal	42, 84	42, 84	32, 69	21, 60	22	F9, H1
I2S0_AD0	IO	Digital audio interface (I2S0) audio data 0 signal	46, 52, 76, 94	46, 52, 76, 94	36, 42, 61, 74	17, 26, 6, 64	28, 39, 45	D1, G10, J2, K10
I2S0_AD1	IO	Digital audio interface (I2S0) audio data 0 signal	47, 53, 93	47, 53, 93	37, 43, 73	1, 25, 7	29, 44	E2, H10, K8
I2S1_AD0	IO	Digital audio interface (I2S1) audio data 0 signal	40, 82	40, 82	30, 67	19, 58	20, 41	E10, F3
I2S1_AD1	IO	Digital audio interface (I2S1) audio data 0 signal	41, 83	41, 83	31, 68	20, 59	21	F8, G2

Table 6-9. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
PA0	IO	GPIO port A input/output 0	1	1	1	33	1	D3
PA1	IO	GPIO port A input/output 1	2	2	2	34	2	C4
PA2	IO	GPIO port A input/output 2	15	15	10	42	8	A5
PA3	IO	GPIO port A input/output 3	16	16	11	43	9	A6
PA4	IO	GPIO port A input/output 4	17	17	12	44	10	A7
PA5	IO	GPIO port A input/output 5	18	18	13	45	11	A8
PA6	IO	GPIO port A input/output 6	19	19	14	46	12	A9
PA7	IO	GPIO port A input/output 7	22	22	17	49	13	B7
PA8	IO	GPIO port A input/output 8	27	27	22	54	16	D10
PA9	IO	GPIO port A input/output 9	28	28	23	55	17	C9
PA10	IO	GPIO port A input/output 10	33	33	28	56	18	E7
PA11	IO	GPIO port A input/output 11	34	34	29	57	19	E9
PA12	IO	GPIO port A input/output 12	51	51	41	5	27	J10
PA13	IO	GPIO port A input/output 13	52	52	42	6	28	K10
PA14	IO	GPIO port A input/output 14	53	53	43	7	29	K8
PA15	IO	GPIO port A input/output 15	54	54	44		30	K7
PA16	IO	GPIO port A input/output 16	55	55	45			H7
PA17	IO	GPIO port A input/output 17	69	69	54	10	32	K4
PA18	IO	GPIO port A input/output 18	70	70	55	11	33	K3
PA19	IO	GPIO port A input/output 19	71	71	56	12	34	J4
PA20	IO	GPIO port A input/output 20	72	72	57	13	35	J3
PA21	IO	GPIO port A input/output 21	76	76	61	17	39	J2
PA22	IO	GPIO port A input/output 22	77	77	62	18	40	H2
PA23	IO	GPIO port A input/output 23	92	92	72	24	43	E1
PA24	IO	GPIO port A input/output 24	93	93	73	25	44	E2
PA25	IO	GPIO port A input/output 25	94	94	74	26	45	D1
PA26	IO	GPIO port A input/output 26	98	98	78	30	46	C2
PA27	IO	GPIO port A input/output 27	99	99	79	31	47	B2
PA28	IO	GPIO port A input/output 28	3	3	3	35	3	C3
PA29	IO	GPIO port A input/output 29	4	4	4	36		B3
PA30	IO	GPIO port A input/output 30	5	5	5	37		D4

ADVANCE INFORMATION

Table 6-9. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
PB0	IO	GPIO port B input/output 0	20	20	15	47		C6
PB1	IO	GPIO port B input/output 1	21	21	16	48		C7
PB2	IO	GPIO port B input/output 2	23	23	18	50	14	C8
PB3	IO	GPIO port B input/output 3	24	24	19	51	15	D8
PB4	IO	GPIO port B input/output 4	25	25	20	52		D9
PB5	IO	GPIO port B input/output 5	26	26	21	53		B8
PB6	IO	GPIO port B input/output 6	40	40	30	58	20	E10
PB7	IO	GPIO port B input/output 7	41	41	31	59	21	F8
PB8	IO	GPIO port B input/output 8	42	42	32	60	22	F9
PB9	IO	GPIO port B input/output 9	43	43	33	61	23	G7
PB10	IO	GPIO port B input/output 10	44	44	34	62		F10
PB11	IO	GPIO port B input/output 11	45	45	35	63		G9
PB12	IO	GPIO port B input/output 12	46	46	36	64		G10
PB13	IO	GPIO port B input/output 13	47	47	37	1		H10
PB14	IO	GPIO port B input/output 14	48	48	38	2	24	J9
PB15	IO	GPIO port B input/output 15	49	49	39	3	25	G8
PB16	IO	GPIO port B input/output 16	50	50	40	4	26	J8
PB17	IO	GPIO port B input/output 17	73	73	58	14	36	K2
PB18	IO	GPIO port B input/output 18	74	74	59	15	37	K1
PB19	IO	GPIO port B input/output 19	75	75	60	16	38	J1
PB20	IO	GPIO port B input/output 20	82	82	67	19	41	F3
PB21	IO	GPIO port B input/output 21	83	83	68	20		G2
PB22	IO	GPIO port B input/output 22	84	84	69	21		H1
PB23	IO	GPIO port B input/output 23	85	85	70	22		G1
PB24	IO	GPIO port B input/output 24	86	86	71	23	42	F2
PB25	IO	GPIO port B input/output 25	95	95	75	27		C1
PB26	IO	GPIO port B input/output 26	96	96	76	28		B1
PB27	IO	GPIO port B input/output 27	97	97	77	29		D2
PB28	IO	GPIO port B input/output 28	29	29	24			E8
PB29	IO	GPIO port B input/output 29	30	30	25			B9
PB30	IO	GPIO port B input/output 30	31	31	26			D7
PB31	IO	GPIO port B input/output 31	32	32	27			A10
PC0	IO	GPIO port C input/output 0	56	56	46			J7
PC1	IO	GPIO port C input/output 1	57	57	47			H8
PC2	IO	GPIO port C input/output 2	65	65	50			H5
PC3	IO	GPIO port C input/output 3	66	66	51			H4
PC4	IO	GPIO port C input/output 4	67	67	52			G6
PC5	IO	GPIO port C input/output 5	68	68	53			G5
PC6	IO	GPIO port C input/output 6	78	78	63			H3
PC7	IO	GPIO port C input/output 7	79	79	64			G3
PC8	IO	GPIO port C input/output 8	80	80	65			G4
PC9	IO	GPIO port C input/output 9	81	81	66			F4
PC10	IO	GPIO port C input/output 10	87	87				F5
PC11	IO	GPIO port C input/output 11	88	88				E5

Table 6-9. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
PC12	IO	GPIO port C input/output 12	10	10				C5
PC13	IO	GPIO port C input/output 13	12	12				D5
PC14	IO	GPIO port C input/output 14	13	13				B6
PC15	IO	GPIO port C input/output 15	11	11				B5
PC16	IO	GPIO port C input/output 16	35	35				E6
PC17	IO	GPIO port C input/output 17	36	36				B10
PC18	IO	GPIO port C input/output 18	38	38				C10
PC19	IO	GPIO port C input/output 19	39	39				F7
PC20	IO	GPIO port C input/output 20	58	58				H9
PC21	IO	GPIO port C input/output 21	59	59				H6
PC22	IO	GPIO port C input/output 22	60	60				K5
PC23	IO	GPIO port C input/output 23	61	61				J6
PC24	IO	GPIO port C input/output 24	62	62				J5
PC25	IO	GPIO port C input/output 25	89	89				E4
PC26	IO	GPIO port C input/output 26	90	90				F1
PC27	IO	GPIO port C input/output 27	91	91				E3
PC28	IO	GPIO port C input/output 28	14	14			7	D6
PC29	IO	GPIO port C input/output 29	37	37				F6

Table 6-10. IOMUX Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
WAKE	I	Input signal to wake the device from SHUTDOWN mode	1, 2, 3, 33, 34, 6, 69, 70	1, 2, 3, 33, 34, 6, 69, 70	1, 2, 28, 29, 3, 54, 55, 6	10, 11, 33, 34, 35, 38, 56, 57	1, 18, 19, 2, 3, 32, 33, 4	B4, C3, C4, D3, E7, E9, K3, K4

Table 6-11. Power Management Unit (PMU) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
VBAT	PWR	VBAT (backup island) supply	7	7	7	39	5	A3
VCORE	PWR	VCORE capacitor connection	100	100	80	32	48	A1
VDD	PWR	VDD supply	64, 8	64, 8	49, 8	40, 9	31, 6	A4, K6
VSS	PWR	VSS (ground)	63, 9	63, 9	48, 9	41, 8	MP	A2, K9

Table 6-12. Programming and Debug Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
SWCLK	I	Serial wire debug interface clock input signal	72	72	57	13	35	J3
SWDIO	IO	Serial wire debug interface data input/output signal	71	71	56	12	34	J4

ADVANCE INFORMATION

Table 6-12. Programming and Debug Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
TDI	I	TDI for boundary scan only	77	77	62	18	40	H2
TDO	IO	TDO for boundary scan only	28	28	23	55	17	C9

Table 6-13. Quad Serial Peripherial Interface (QSPI)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
QSPI_CLK	IOD	Quad SPI CLK signal	50	50	40	4	26	J8
QSPI_CS0	IO	Quad SPI chip select 0	48, 56	48, 56	38, 46	2	24	J7, J9
QSPI_CS1	IO	Quad SPI chip select 1	70	70	55	11	33	K3
QSPI_CS2	IO	Quad SPI chip select 2	47	47	37	1		H10
QSPI_CS3	IO	Quad SPI chip select 3	55	55	45			H7
QSPI_IO0	IO	Quad SPI IO0	51	51	41	5	27	J10
QSPI_IO1	IO	Quad SPI IO1	53	53	43	7	29	K8
QSPI_IO2	IO	Quad SPI IO2	52	52	42	6	28	K10
QSPI_IO3	IO	Quad SPI IO3	49	49	39	3	25	G8

Table 6-14. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
RTC_OUT	O	Real-time clock output signal	28, 99	28, 99	23, 79	31, 55	17, 47	B2, C9

Table 6-15. System Controller (SYSCTL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
NRST	RESET	Active-low reset signal (must be logic high for the device to start)	6	6	6	38	4	B4

Table 6-16. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
TIMA0_0_C0	IO	TIMA0_0 capture/compare 0 signal	27, 29, 48, 65, 76, 78	27, 29, 48, 65, 76, 78	22, 24, 38, 50, 61, 63	17, 2, 54	16, 24, 39	D10, E8, H3, H5, J2, J9
TIMA0_0_C1	IO	TIMA0_0 capture/compare 1 signal	15, 16, 2, 31, 67, 80, 82	15, 16, 2, 31, 67, 80, 82	10, 11, 2, 26, 52, 65, 67	19, 34, 42, 43	2, 41, 8, 9	A5, A6, C4, D7, F3, G4, G6
TIMA0_0_C2	IO	TIMA0_0 capture/compare 2 signal	22, 25, 33, 54, 56, 73	22, 25, 33, 54, 56, 73	17, 20, 28, 44, 46, 58	14, 49, 52, 56	13, 18, 30, 36	B7, D9, E7, J7, K2, K7
TIMA0_0_C3	IO	TIMA0_0 capture/compare 3 signal	23, 53, 69, 92	23, 53, 69, 92	18, 43, 54, 72	10, 24, 50, 7	14, 29, 32, 43	C8, E1, K4, K8
TIMA0_0_C0N	O	TIMA0_0 capture/compare 0 complementary output	28, 30, 43, 66, 77, 79	28, 30, 43, 66, 77, 79	23, 25, 33, 51, 62, 64	18, 55, 61	17, 23, 40	B9, C9, G3, G7, H2, H4

Table 6-16. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
TIMA0_0_C1N	O	TIMA0_0 capture/compare 1 complementary output	17, 32, 47, 68, 81, 94	17, 32, 47, 68, 81, 94	12, 27, 37, 53, 66, 74	1, 26, 44	10, 45	A10, A7, D1, F4, G5, H10
TIMA0_0_C2N	O	TIMA0_0 capture/compare 2 complementary output	19, 26, 34, 55, 57, 74	19, 26, 34, 55, 57, 74	14, 21, 29, 45, 47, 59	15, 46, 53, 57	12, 19, 37	A9, B8, E9, H7, H8, K1
TIMA0_0_C3N	O	TIMA0_0 capture/compare 3 complementary output	24, 70, 93	24, 70, 93	19, 55, 73	11, 25, 51	15, 33, 44	D8, E2, K3
TIMA0_0_FAL0	I	TIMA fault input 0	3, 98	3, 98	3, 78	30, 35	3, 46	C2, C3
TIMA0_0_FAL1	I	TIMA fault input 1	1, 46	1, 46	1, 36	33, 64	1	D3, G10
TIMA0_0_FAL2	I	TIMA fault input 2	5, 95, 99	5, 95, 99	5, 75, 79	27, 31, 37	47	B2, C1, D4
TIMA0_1_C0	IO	TIMA0_1 capture/compare 0 signal	10, 27, 40	10, 27, 40	22, 30	54, 58	16, 20	C5, D10, E10
TIMA0_1_C1	IO	TIMA0_1 capture/compare 1 signal	36, 44, 51	36, 44, 51	34, 41	5, 62	27	B10, F10, J10
TIMA0_1_C2	IO	TIMA0_1 capture/compare 2 signal	20, 61, 75	20, 61, 75	15, 60	16, 47	38	C6, J1, J6
TIMA0_1_C3	IO	TIMA0_1 capture/compare 3 signal	38, 49, 83	38, 49, 83	39, 68	20, 3	25	C10, G2, G8
TIMA0_1_C0N	O	TIMA0_1 capture/compare 0 complementary output	11, 34, 41	11, 34, 41	29, 31	57, 59	19, 21	B5, E9, F8
TIMA0_1_C1N	O	TIMA0_1 capture/compare 1 complementary output	37, 45, 53	37, 45, 53	35, 43	63, 7	29	F6, G9, K8
TIMA0_1_C2N	O	TIMA0_1 capture/compare 2 complementary output	21, 62, 82	21, 62, 82	16, 67	19, 48	41	C7, F3, J5
TIMA0_1_C3N	O	TIMA0_1 capture/compare 3 complementary output	39, 50, 84	39, 50, 84	40, 69	21, 4	26	F7, H1, J8
TIMA0_1_FAL0	I	TIMA fault input 0	2, 65	2, 65	2, 50	34	2	C4, H5
TIMA0_1_FAL1	I	TIMA fault input 1	4, 42, 52	4, 42, 52	32, 4, 42	36, 6, 60	22, 28	B3, F9, K10
TIMA0_1_FAL2	I	TIMA fault input 2	58, 86	58, 86	71	23	42	F2, H9
TIMG12_0_C0	IO	TIMG12_0 capture/compare 0 signal	33, 47, 82	33, 47, 82	28, 37, 67	1, 19, 56	18, 41	E7, F3, H10
TIMG12_0_C1	IO	TIMG12_0 capture/compare 1 signal	48, 86, 93	48, 86, 93	38, 71, 73	2, 23, 25	24, 42, 44	E2, F2, J9
TIMG4_0_C0	IO	TIMG4_0 capture/compare 0 signal	18, 44, 51, 92	18, 44, 51, 92	13, 34, 41, 72	24, 45, 5, 62	11, 27, 43	A8, E1, F10, J10
TIMG4_0_C1	IO	TIMG4_0 capture/compare 1 signal	19, 45, 52, 93	19, 45, 52, 93	14, 35, 42, 73	25, 46, 6, 63	12, 28, 44	A9, E2, G9, K10
TIMG4_1_C0	IO	TIMG4_1 capture/compare 0 signal	12, 20, 85, 99	12, 20, 85, 99	15, 70, 79	22, 31, 47	47	B2, C6, D5, G1
TIMG4_1_C1	IO	TIMG4_1 capture/compare 1 signal	13, 21, 65, 86	13, 21, 65, 86	16, 50, 71	23, 48	42	B6, C7, F2, H5
TIMG4_2_C0	IO	TIMG4_2 capture/compare 0 signal	18, 23, 4, 40, 44, 76, 78, 96	18, 23, 4, 40, 44, 76, 78, 96	13, 18, 30, 34, 4, 61, 63, 76	17, 28, 36, 45, 50, 58, 62	11, 14, 20, 39	A8, B1, B3, C8, E10, F10, H3, J2
TIMG4_2_C1	IO	TIMG4_2 capture/compare 1 signal	19, 24, 41, 45, 5, 77, 79, 97	19, 24, 41, 45, 5, 77, 79, 97	14, 19, 31, 35, 5, 62, 64, 77	18, 29, 37, 46, 51, 59, 63	12, 15, 21, 40	A9, D2, D4, D8, F8, G3, G9, H2
TIMG4_3_C0	IO	TIMG4_3 capture/compare 0 signal	49, 69, 98	49, 69, 98	39, 54, 78	10, 3, 30	25, 32, 46	C2, G8, K4

ADVANCE INFORMATION

Table 6-16. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
TIMG4_3_C1	IO	TIMG4_3 capture/compare 1 signal	22, 50, 66, 75, 99	22, 50, 66, 75, 99	17, 40, 51, 60, 79	16, 31, 4, 49	13, 26, 38, 47	B2, B7, H4, J1, J8
TIMG8_0_IDX	I	TIMG8_0 quadrature encoder index pulse signal	2, 32, 48, 54	2, 32, 48, 54	2, 27, 38, 44	2, 34	2, 24, 30	A10, C4, J9, K7
TIMG8_1_IDX	I	TIMG8_1 quadrature encoder index pulse signal	32, 42, 89	32, 42, 89	27, 32	60	22	A10, E4, F9
TIMG8_0_C0	IO	TIMG8_0 capture/compare 0 signal	16, 49, 56, 83	16, 49, 56, 83	11, 39, 46, 68	20, 3, 43	25, 9	A6, G2, G8, J7
TIMG8_0_C1	IO	TIMG8_0 capture/compare 1 signal	15, 50, 57, 84	15, 50, 57, 84	10, 40, 47, 69	21, 4, 42	26, 8	A5, H1, H8, J8
TIMG8_1_C0	IO	TIMG8_1 capture/compare 0 signal	30, 41, 87	30, 41, 87	25, 31	59	21	B9, F5, F8
TIMG8_1_C1	IO	TIMG8_1 capture/compare 1 signal	31, 43, 88	31, 43, 88	26, 33	61	23	D7, E5, G7

Table 6-17. Unified Communication Module (UniComm) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
UC2_PICO	IO	Unified Communication Module UC2: SPI PICO signal	18, 28, 73	18, 28, 73	13, 23, 58	14, 45, 55	11, 17, 36	A8, C9, K2
UC2_POCI	IO	Unified Communication Module UC2: SPI POCI signal	17, 26, 33, 75	17, 26, 33, 75	12, 21, 28, 60	16, 44, 53, 56	10, 18, 38	A7, B8, E7, J1
UC2_SCK	IOD	Unified Communication Module UC2: SPI SCLK signal	19, 27, 34, 74	19, 27, 34, 74	14, 22, 29, 59	15, 46, 54, 57	12, 16, 19, 37	A9, D10, E9, K1
UC12_CTS	IO	Unified Communication Module UC12: UART CTS signal	13, 28, 40, 5	13, 28, 40, 5	23, 30, 5	37, 55, 58	17, 20	B6, C9, D4, E10
UC12_RTS	IO	Unified Communication Module UC12: UART RTS signal	12, 27, 4, 41	12, 27, 4, 41	22, 31, 4	36, 54, 59	16, 21	B3, D10, D5, F8
UC12_RX	IO	Unified Communication Module UC12: UART RX signal	15, 2, 21, 34, 50, 53, 72	15, 2, 21, 34, 50, 53, 72	10, 16, 2, 29, 40, 43, 57	13, 34, 4, 42, 48, 57, 7	19, 2, 26, 29, 35, 8	A5, C4, C7, E9, J3, J8, K8
UC12_TX	IO	Unified Communication Module UC12: UART TX signal	1, 14, 20, 3, 33, 49, 52, 71	1, 14, 20, 3, 33, 49, 52, 71	1, 15, 28, 3, 39, 42, 56	12, 3, 33, 35, 47, 56, 6	1, 18, 25, 28, 3, 34, 7	C3, C6, D3, D6, E7, G8, J4, K10
UC14_CTS	IO	Unified Communication Module UC14: UART CTS signal	85, 89	85, 89	70	22		E4, G1
UC14_RTS	IO	Unified Communication Module UC14: UART RTS signal	86, 90	86, 90	71	23	42	F1, F2
UC14_SCL_RX	IOD	Unified Communication Module UC14: I2C SCL or UART RX signal	83, 87	83, 87	68	20		F5, G2
UC14_SDA_TX	IOD	Unified Communication Module UC14: I2C SDA or UART TX signal	84, 88	84, 88	69	21		E5, H1
UC13_0_PICO_SDA_TX	IOD	Unified Communication Module UC13: 0 or SPI PICO or I2C SDA or UART TX signal	31, 42, 43, 46, 53, 66, 70, 78, 84, 98	31, 42, 43, 46, 53, 66, 70, 78, 84, 98	26, 32, 33, 36, 43, 51, 55, 63, 69, 78	11, 21, 30, 60, 61, 64, 7	22, 23, 29, 33, 46	C2, D7, F9, G10, G7, H1, H3, H4, K3, K8

ADVANCE INFORMATION

Table 6-17. Unified Communication Module (UniComm) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
UC13_0_POCI_RTS	IO	Unified Communication Module UC13: 0 or SPI POCI or UART RTS signal	26, 30, 41, 48, 52, 55, 81, 93	26, 30, 41, 48, 52, 55, 81, 93	21, 25, 31, 38, 42, 45, 66, 73	2, 25, 53, 59, 6	21, 24, 28, 44	B8, B9, E2, F4, F8, H7, J9, K10
UC13_0_SCK_SCL_RX	IOD	Unified Communication Module UC13: 0 or SPI SCLK or I2C SCL or UART RX signal	32, 42, 43, 47, 52, 65, 69, 79, 85, 94	32, 42, 43, 47, 52, 65, 69, 79, 85, 94	27, 32, 33, 37, 42, 50, 54, 64, 70, 74	1, 10, 22, 26, 6, 60, 61	22, 23, 28, 32, 45	A10, D1, F9, G1, G3, G7, H10, H5, K10, K4
UC13_1_PICO_SDA_TX	IOD	Unified Communication Module UC13: 1 or SPI PICO or I2C SDA or UART TX signal	12, 25, 49, 73, 76, 92	12, 25, 49, 73, 76, 92	20, 39, 58, 61, 72	14, 17, 24, 3, 52	25, 36, 39, 43	D5, D9, E1, G8, J2, K2
UC13_1_POCI_RTS	IO	Unified Communication Module UC13: 1 or SPI POCI or UART RTS signal	15, 24, 26, 94	15, 24, 26, 94	10, 19, 21, 74	26, 42, 51, 53	15, 45, 8	A5, B8, D1, D8
UC13_1_SCK_SCL_RX	IOD	Unified Communication Module UC13: 1 or SPI SCLK or I2C SCL or UART RX signal	13, 33, 50, 74, 77, 93	13, 33, 50, 74, 77, 93	28, 40, 59, 62, 73	15, 18, 25, 4, 56	18, 26, 37, 40, 44	B6, E2, E7, H2, J8, K1
UC13_2_PICO_SDA_TX	IOD	Unified Communication Module UC13: 2 or SPI PICO or I2C SDA or UART TX signal	44, 93	44, 93	34, 73	25, 62	44	E2, F10
UC13_2_POCI_RTS	IO	Unified Communication Module UC13: 2 or SPI POCI or UART RTS signal	47, 77	47, 77	37, 62	1, 18	40	H10, H2
UC13_2_SCK_SCL_RX	IOD	Unified Communication Module UC13: 2 or SPI SCLK or I2C SCL or UART RX signal	45, 92	45, 92	35, 72	24, 63	43	E1, G9
UC13_3_PICO_SDA_TX	IOD	Unified Communication Module UC13: 3 or SPI PICO or I2C SDA or UART TX signal	2, 30, 37, 98	2, 30, 37, 98	2, 25, 78	30, 34	2, 46	B9, C2, C4, F6
UC13_3_POCI_RTS	IO	Unified Communication Module UC13: 3 or SPI POCI or UART RTS signal	15, 32, 4, 99	15, 32, 4, 99	10, 27, 4, 79	31, 36, 42	47, 8	A10, A5, B2, B3
UC13_3_SCK_SCL_RX	IOD	Unified Communication Module UC13: 3 or SPI SCLK or I2C SCL or UART RX signal	1, 14, 29, 94	1, 14, 29, 94	1, 24, 74	26, 33	1, 45, 7	D1, D3, D6, E8
UC13_0_CS0_CTS	IO	Unified Communication Module UC13: 0 or SPI CS0 or UART CTS signal	25, 29, 51, 65, 80, 92, 98	25, 29, 51, 65, 80, 92, 98	20, 24, 41, 50, 65, 72, 78	24, 30, 5, 52	27, 43, 46	C2, D9, E1, E8, G4, H5, J10
UC13_1_CS0_CTS	IO	Unified Communication Module UC13: 1 or SPI CS0 or UART CTS signal	17, 23, 70	17, 23, 70	12, 18, 55	11, 44, 50	10, 14, 33	A7, C8, K3
UC13_2_CS0_CTS	IO	Unified Communication Module UC13: 2 or SPI CS0 or UART CTS signal	46, 76	46, 76	36, 61	17, 64	39	G10, J2
UC13_3_CS0_CTS	IO	Unified Communication Module UC13: 3 or SPI CS0 or UART CTS signal	3, 31, 65	3, 31, 65	26, 3, 50	35	3	C3, D7, H5
UC15_0_SCL	IOD	Unified Communication Module UC15: 0 or I2C SCL signal	2, 34, 72	2, 34, 72	2, 29, 57	13, 34, 57	19, 2, 35	C4, E9, J3

ADVANCE INFORMATION

Table 6-17. Unified Communication Module (UniComm) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
UC15_0_SDA	IOD	Unified Communication Module UC15: 0 or I2C SDA signal	1, 3, 33, 71	1, 3, 33, 71	1, 28, 3, 56	12, 33, 35, 56	1, 18, 3, 34	C3, D3, E7, J4
UC15_1_SCL	IOD	Unified Communication Module UC15: 1 or I2C SCL signal	17, 23, 4, 54	17, 23, 4, 54	12, 18, 4, 44	36, 44, 50	10, 14, 30	A7, B3, C8, K7
UC15_1_SDA	IOD	Unified Communication Module UC15: 1 or I2C SDA signal	16, 24, 5, 55	16, 24, 5, 55	11, 19, 45, 5	37, 43, 51	15, 9	A6, D4, D8, H7
UC1_0_CTS	IO	Unified Communication Module UC1: 0 or UART CTS signal	28, 53, 75, 95	28, 53, 75, 95	23, 43, 60, 75	16, 27, 55, 7	17, 29, 38	C1, C9, J1, K8
UC1_0_RTS	IO	Unified Communication Module UC1: 0 or UART RTS signal	27, 54, 96	27, 54, 96	22, 44, 76	28, 54	16, 30	B1, D10, K7
UC1_0_SCL_RX	IOD	Unified Communication Module UC1: 0 or I2C SCL or UART RX signal	2, 21, 34	2, 21, 34	16, 2, 29	34, 48, 57	19, 2	C4, C7, E9
UC1_0_SDA_TX	IOD	Unified Communication Module UC1: 0 or I2C SDA or UART TX signal	1, 20, 3, 33	1, 20, 3, 33	1, 15, 28, 3	33, 35, 47, 56	1, 18, 3	C3, C6, D3, E7
UC1_1_CTS	IO	Unified Communication Module UC1: 1 or UART CTS signal	42, 76	42, 76	32, 61	17, 60	22, 39	F9, J2
UC1_1_RTS	IO	Unified Communication Module UC1: 1 or UART RTS signal	43, 77	43, 77	33, 62	18, 61	23, 40	G7, H2
UC1_1_SCL_RX	IOD	Unified Communication Module UC1: 1 or I2C SCL or UART RX signal	17, 23, 26, 28, 4, 41, 54, 70	17, 23, 26, 28, 4, 41, 54, 70	12, 18, 21, 23, 31, 4, 44, 55	11, 36, 44, 50, 53, 55, 59	10, 14, 17, 21, 30, 33	A7, B3, B8, C8, C9, F8, K3, K7
UC1_1_SDA_TX	IOD	Unified Communication Module UC1: 1 or I2C SDA or UART TX signal	16, 24, 25, 27, 40, 5, 55, 69	16, 24, 25, 27, 40, 5, 55, 69	11, 19, 20, 22, 30, 45, 5, 54	10, 37, 43, 51, 52, 54, 58	15, 16, 20, 32, 9	A6, D10, D4, D8, D9, E10, H7, K4
UC2_CS0	IO	Unified Communication Module UC2: SPI CS0 signal	15, 65, 79	15, 65, 79	10, 50, 64	42	8	A5, G3, H5
UC2_CS1	IO	Unified Communication Module UC2: SPI CS1 signal	16, 40, 78, 99	16, 40, 78, 99	11, 30, 63, 79	31, 43, 58	20, 47, 9	A6, B2, E10, H3
UC2_CS2	IO	Unified Communication Module UC2: SPI CS2 signal	82, 93	82, 93	67, 73	19, 25	41, 44	E2, F3
UC2_CS3	IO	Unified Communication Module UC2: SPI CS3 signal	86, 92	86, 92	71, 72	23, 24	42, 43	E1, F2

Table 6-18. Voltage Reference Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PFA PIN	PZ PIN	PN PIN	PM PIN	RGZ PIN	ZAW PIN
VREF+	A	Voltage reference positive input	92	92	72	24	43	E1
VREF-	A	Voltage reference negative input	76	76	61	17	39	J2

6.4 Connections for Unused Pins

Table 6-19 lists the correct termination of unused pins.

Table 6-19. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx and PBx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with the internal pullup or pulldown resistor enabled.
NRST	VCC	NRST is an active-low reset signal. Pull the pin high to VCC, or the device cannot start. For more information, see Section 9.1.

(1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAx and PBx" unused pin connection guidelines.

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
VBAT	Battery Backup Supply	At VBAT pin, with respect to VSS	–0.3	4.1	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Maximum current into each VDD pin			160	mA
I_{VSS}	Maximum current out of each VSS pin			160	mA
I_{IO}	Current of SD IO pin	Current sunk or sourced by SD IO pin		6	mA
	Current of HS IO pin	Current sunk or sourced by HS IO pin		6	mA
	Current of HD IO pin	Current sunk or sourced by HD IO pin		20	mA
T_J		Junction temperature	-40	140	°C
T_{stg}		Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.71		3.6	V
VBAT	At VBAT pin, with respect to VSS	1.62		3.6	V
VCORE	Voltage on VCORE pin in Run/Sleep mode (2)		1.35		V
	Voltage on VCORE pin in Stop/Standby mode (2)		1.1		V
C_{VDD}	Capacitor connected betwen VDD and VSS (1)		10		uF
C_{VBAT}	Capacitor connected between VBAT and VSS		1		µF
C_{VCORE}	Capacitor connected between VCORE and VSS (1) (2)		2.2		µF
T_A	Ambient temperature	–40		125	°C
f_{MCLK}	CPUCLK, MCLK frequency with 2 flash wait state (3)			160	MHz
	CPUCLK, MCLK frequency with 1 flash wait state (3)			110	
	CPUCLK, MCLK frequency with 0 flash wait state (3)			40	

(1) Connect C_{VDD} ,C_{VBAT} and C_{VCORE} between VDD/VSS , VBAT/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} ,C_{VBAT} and C_{VCORE}.
(2) The VCORE pin must only be connected to C_{VCORE}. Do not supply any voltage or apply any external load to the VCORE pin.

(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software unless

7.4 Thermal Information

THERMAL METRIC[1]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-100 (PZ)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-80 (PN)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-64 (PM)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		TBD	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Supply Current Characteristics

ADVANCE INFORMATION

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		VDD	MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode														
I_{DD} (Run)	MCLK=SYSPLL, SYSPLLREF=SYSOSC CoreMark, execute from flash	3.3V	160MHz	33.6		33.7		34.8		35.8		37.9		mA
		3.3V	80MHz	17.8		17.9		18.9		19.8		21.8		
	MCLK=SYSOSC, CoreMark, execute from flash	3.3V	32MHz	12.6		12.8		14.1		15.4		18.3		
I_{DD} (Run) per MHz	MCLK=SYSPLL, SYSPLLREF=SYSOSC CoreMark, execute from flash	3.3V	160MHz	210		211		217		224		237		µA/Mhz
	MCLK=SYSPLL, SYSPLLREF=SYSOSC While(1), execute from flash	3.3V	160MHz	206		207		213		220		232		
SLEEP Mode														
I_{DD} (Sleep)	MCLK=SYSPLL, SYSPLLREF=SYSOSC CPU is halted		160MHz	9.5		9.7		10.7		11.6		13.6		mA
	MCLK=SYSOSC, CPU is halted		32MHz	3.2		3.3		4.2		5.2		7.2		

7.5.2 STOP/STANDBY Modes

VDD=3.3V, VBAT=3.3V. All inputs in VDD domain tied to 0V or VDD, All inputs in VBAT Island tied to 0V or VBAT. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
I_{DD} (Stop)	SYSOSC=32MHz, USE4MHZSTOP=1, DISABLESTOP=0	4MHz	129		143		257		380		609		uA
STANDBY Mode													
I_{DD} (Standby)	TIMG4_0 enabled	32kHz	3.8		16		128		251		482		uA
	GPIOA enabled		3.8		16		128		251		486		

7.5.3 SHUTDOWN Mode

All inputs in VDD domain tied to 0V or VDD. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{DD} (Shutdown)	Supply current in SHUTDOWN mode	3.3V	46		72		452		1065		2932		nA

7.5.4 VBAT current consumption

VBAT=3.3V. All inputs in VBAT Island tied to 0V or VBAT. Outputs do not source or sink any current.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{DD} (VBAT)	LF-XT and RTC is running	32kHz	2.1		2.2		2.8		3.6		5.1		uA
	LFOSC and IWDG is running	32kHz	2.5		2.5		3.2		3.9		5.5		uA

7.6 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.71		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
$NWEC_{(CODEFLASH)}$	Erase/program cycle endurance (code flash)		20			k cycles
$NWEC_{(DATAFLASH)}$	Erase/program cycle endurance (data flash)		100			k cycles
$NE_{(MAX)}$	Total erase operations before failure (1)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (2)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C <= Tj <= 105°C	11.4			years
t_{RET_130}	Flash memory data retention	-40°C <= Tj <= 130°C	2.4			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 128)}$	Program time for flash word (3) (5)			75		µs
$t_{PROG\ (SEC,\ 128)}$	Program time for 2kB sector (4) (5)			5.1		ms
$t_{ERASE\ (SEC)}$	Sector erase time	<10k erase/program cycles		20		ms
$t_{ERASE\ (BANK)}$	Bank erase time	<10k erase/program cycles		22		ms

(1) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(2) Maximum number of write operations allowed per word line (256 bytes) before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
(3) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(4) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(5) Flash word size is 128 data bits (16 bytes). On devices with ECC, the total flash word size is 144 bits (128 data bits plus 16 ECC bits).

7.7 Power Supply Sequencing

7.7.1 Power Supply Ramp

Figure 7-1 shows the relationships of POR-, POR+, BOR0-, and BOR0+ during powerup and powerdown.

ADVANCE INFORMATION

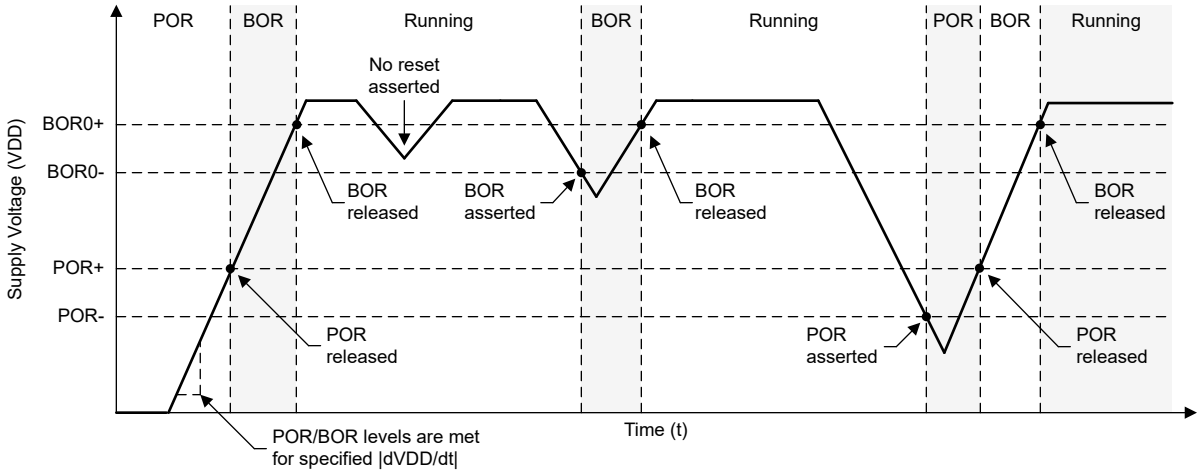


Figure 7-1. Power Cycle POR and BOR Conditions

7.7.2 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Power supply range		1.71		3.6	V
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling (1)			0.01	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level (2)	Rising	0.95	1.30	1.56	V
V_{POR-}	Power-on reset voltage level (2)	Falling	0.9	1.25	1.53	V
$V_{HYS, POR}$	POR hysteresis (2)			45		mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	Cold start, rising (2)	1.5	1.6	1.7	V
V_{BOR0+}	Brown-out reset voltage level 0 (default level)	Rising (2) (1)	1.625	1.66	1.695	V
V_{BOR0-}	Brown-out reset voltage level 0 (default level)	Falling (2) (1)	1.61	1.645	1.68	V
$V_{BOR0, STBY}$	Brown-out reset voltage level 0 (default level)	STANDBY mode (2)	1.54	1.625	1.69	V
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (2) (1)	2.13	2.17	2.21	V
V_{BOR1-}	Brown-out-reset voltage level 1	Falling (2) (1)	2.10	2.14	2.18	V
$V_{BOR1, STBY}$	Brown-out-reset voltage level 1	STANDBY mode (2)	2.06	2.13	2.215	V
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (2) (1)	2.73	2.77	2.82	V
V_{BOR2-}	Brown-out-reset voltage level 2	Falling (2) (1)	2.7	2.74	2.79	V
$V_{BOR2, STBY}$	Brown-out-reset voltage level 2	STANDBY mode (2)	2.62	2.71	2.8	V
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (2) (1)	2.88	2.96	3.04	V
V_{BOR3-}	Brown-out-reset voltage level 3	Falling (2) (1)	2.85	2.93	3.01	V
$V_{BOR3, STBY}$	Brown-out-reset voltage level 3	STANDBY mode (2)	2.82	2.92	3.02	V
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (2)		15		mV
$V_{HYS,BOR}$	Brown-out reset hysteresis	Levels 1-3 (2)		34		mV
$t_{PD:BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
$t_{PD:BOR}$	BOR propagation delay	STANDBY mode			100	us

(1) Device operating in RUN, SLEEP, or STOP mode.
(2) |dVDD/dt| ≤ 3V/s

ADVANCE INFORMATION

7.7.3 VBat Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBAT	Power supply range		1.62		3.6	V
dVBAT/dt	VBAT (supply voltage) slew rate	Rising			0.1	V/us
dVBAT/dt	VBAT (supply voltage) slew rate	Falling,standby (2)			0.1	V/ms
$V_{POR+(VBAT)}$	Power-on reset voltage level	Rising (1)	0.95	1.3	1.59	V
$V_{POR-(VBAT)}$	Power-on reset voltage level	Falling (1)	0.9	1.25	1.54	V
$V_{HYS,POR(VBAT)}$	POR hysteresis			45		mV
$V_{BOR0+,COLD(VBAT)}$	Brown-out reset voltage level	Cold start, rising (1)	1.4	1.48	1.59	V
$V_{BOR0+(VBAT)}$	Brown-out reset voltage level	Rising (1) (2)	1.56	1.58	1.62	V
$V_{BOR0-(VBAT)}$	Brown-out reset voltage level	Falling (1) (2)	1.51	1.56	1.61	V
$V_{HYS,BOR(VBAT)}$	BOR hysteresis			15	21	mV
$t_{PU(VBAT)}$	Cold power up time			1.2		ms
I_{CHARGE}	Charging peak current	VDD=3.3, VBAT=0V		1.7		mA
R_{SWITCH}	Internal switch resistance between VBAT and VDD		0.9	1.4	2.7	kΩ
I_{TRIP}	Min current for internal comparator to detect reverse current from VBAT to VDD	VDD sinking , 1.6<VBAT<3.3	100			µA

(1) |dVDD/dt| ≤ 3V/s
(2) Device operating in Standby Mode

7.7.4 Timing Characteristics

VDD=3.3V, T_a=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE:SLEEP}$	Wakeup time from SLEEP to RUN (1)			1.6		µs
$t_{WAKE:STOP}$	Wakeup time from STOP to RUN (SYSOSC enabled) (1)			25.3		µs
$t_{WAKE:STBY}$	Wakeup time from STANDBY0 to RUN (1)			26.6		µs
	Wakeup time from STANDBY1 to RUN (1)			26.8		µs
$t_{WAKEUP:SHDN}$	Wakeup time from SHUTDOWN to RUN (2)	Fast boot enabled		TBD		µs
		Fast boot disabled		702		
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP		6.3		µs
	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY0		7.6		
	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1		7.9		
Startup Timing						

ADVANCE INFORMATION

VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{START:RESET}$	Device cold startup time from reset/ power-up (3)	Fast boot enabled		TBD		µs
		Fast boot disabled		746		
NRST Timing						
$t_{RST:BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		1.5		µs
		ULPCLK=32kHz		80		
$t_{RST:POR}$	Pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external wake-up signal (GPIO wake-up event) to the time that the first instruction of the user program is executed, with glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1) .
(2) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.
(3) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

7.8 Clock Specifications

7.8.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=0 (BASE)		32		MHz
		SYSOSCCFG.FREQ=1		4		
SYSOSC ACC	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled(1)	SETUSEFCL=1 -40 ℃ ≤ Ta ≤ 125 ℃	-1.4		1.8	%
	SYSOSC raw accuracy with FCL disabled, 32MHz	SETUSEFCL=0,SYSOSCCFG.FREQ=0 -40 ℃ ≤ T_a ≤ 125 ℃	-2.6		1.8	%
	SYSOSC raw accuracy with FCL disabled, 4MHz	SETUSEFCL=0,SYSOSCCFG.FREQ=1 -40 ℃ ≤ T_a ≤ 125 ℃	-2.7		2.3	%

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.

7.8.2 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
		HFXTRSEL=01	8.01		16	
		HFXTRSEL=10	16.01		32	
		HFXTRSEL=11	32.01		48	MHz
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
		HFXTRSEL=01	40		60	
		HFXTRSEL=10	40		60	
		HFXTRSEL=11	40		60	
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, HFXT}$	HFXT start-up time (2)	HFXTRSEL=11, 32MHz crystal		0.5		ms

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HFXT}	HFXT current consumption	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		75		uA
		f_{HFXT}=32MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency (3)	USEEXTHFCLK=1	4		48	MHz
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as C_{HFXIN}×C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT}), where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual
(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.8.3 System Phase Lock Loop (SYSPLL)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SYSPLLREF}$	SYSPLL reference frequency range		4		48	MHz
f_{VCO}	VCO output frequency		160		400	MHz
f_{SYSPLL}	SYSPLL output frequency range (1)	SYSPLLCLK0, SYSPLLCLK1	5		160	MHz
DC_{PLL}	SYSPLL output duty cycle	$f_{SYSPLLREF}$=32MHz, f_{VCO}=320MHz, SYSPLLCLK0/1	45		55	%
$Jitter_{SYSPLL}$	SYSPLL RMS cycle-to-cycle jitter	PDIV=2, Loop clock=8MHz,$f_{SYSPLLREF}$=32MHz, f_{VCO}=320MHz		43		ps
	SYSPLL RMS period jitter			32		
I_{SYSPLL}	SYSPLL current consumption	$f_{SYSPLLREF}$=32MHz, f_{VCO}=320MHz, PDIV=2; SYSPLL =160 MHz		1.3		uA
$t_{start, SYSPLL}$	SYSPLL start-up time	$f_{SYSPLLREF}$=32MHz, f_{VCO}=320MHz, PDIV=2; SYSPLL =160 MHz, ±0.5% accuracy			25	us

(1) The SYSPLL may support higher output frequencies than the device clock system supports. Ensure that the device maximum frequency specifications are not violated when configuring the SYSPLL output frequencies.

7.8.4 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 °C ≤ T_a ≤ 125 °C	–5		5	%
		-40 °C ≤ T_a ≤ 85 °C	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1.7		ms

7.8.5 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, LFXT}$	LFXT start-up time			483	640	ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=TBD, LOWCAP=TBD		200		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency (2)	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle (2)	SETUSEEXLF=1	40		60	%
LFCLK Monitor						
$f_{FAULTLF}$	LFCLK monitor fault frequency (3)	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(3) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.9 Analog Specifications

7.9.1 ADC Specifications

7.9.1.1 ADC Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from external reference pin (VREF+)	1.4		VDD	V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
F_S	ADC sampling frequency	12-bit mode, External Reference, $V_{DD} \geq 2.7V$ and $V_{R+} \geq 2.5V$			9.4	Msps
		12-bit mode, External Reference			7.25	Msps
$I_{(ADC)}$ (2)	Operating supply current into VDD terminal	F_S = 9.4 MSPS, Internal reference OFF, V_{R+} = VDD		2.8		mA
		F_S = 4 MSPS, Internal reference OFF, V_{R+} = VDD		1.9		mA
$C_{S/H}$	ADC sample-and-hold capacitance			3.3		pF
Rin	ADC input resistance			0.2		kΩ
ENOB	Effective number of bits	External reference, f_{IN} = 100kHz, HW averaging 8x		12.3		bit
		External reference, f_{IN} = 100kHz		10.8		
		Internal reference, f_{IN} = 100kHz, V_{R+} = VREF = 2.5V (3)		10.5		
SNR	Signal-to-noise ratio	External reference, f_{IN} = 100kHz		66.7		dB
		Internal reference, f_{IN} = 100kHz, V_{R+} = VREF = 2.5V (3)		65.5		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference, VDD = $VDD_{(MIN)}$ to $VDD_{(MAX)}$		60		dB
		VDD = $VDD_{(MIN)}$ to $VDD_{(MAX)}$ Internal reference, V_{R+} = VREF = 2.5V (3)		50		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference, ΔVDD = 0.1 V at 1 kHz		57		dB
		ΔVDD = 0.1 V at 1 kHz Internal reference, V_{R+} = VREF = 2.5V (3)		47		
t_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			10	us
$V_{SupplyMon}$	Supply Monitor voltage divider accuracy	ADC input channel: Supply Monitor (VDD/3), (VBAT/3) (4)	–1.5		1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference (VREF) supply current is not included in current consumption parameter $I_{(ADC)}$.
(3) Minimum values based on characterization data

ADVANCE INFORMATION

(4) Analog power supply monitor. Analog input on channel 15 of ADC0 VDD monitor and ADC1 for VBAT monitor is internally connected to the voltage divider. Both the supply monitors are measured with external reference

7.9.1.2 ADC Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency	VDD ≥ 2.7V and VREF ≥ 2.5V	4		160	MHz
		VDD < 2.7V or VREF < 2.5V	4		107	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample}	Sampling time	12-bit mode, R_S = 50Ω, C_{pext} = 10pF	37.5			ns
$t_{Sample\_SupplyMon}$	Sample time with Supply Monitor (VDD/3), (VBAT/3)		5			µs

7.9.1.3 ADC Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ej	Integral linearity error (INL)	External reference	-2.0		+2.0	LSB
Ek	Differential linearity error (DNL) Guaranteed no missing codes	External reference	-1.0		+1.0	LSB
E_O	Offset error	External reference	-3		3	mV
		Internal reference, V_{R+} = VREF = 2.5V				
E_G	Gain error	External reference	-5		5	LSB
		Internal reference, V_{R+} = VREF = 2.5V	-45		45	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$. All of the errors must be converted in the same unit, usually LSB, for the above equation to be accurate.
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD and V_{R-} = VSS = 0V, external 1uF cap on VREF+ Pin, HW Averaging feature.

7.9.1.4 Typical Connection Diagram

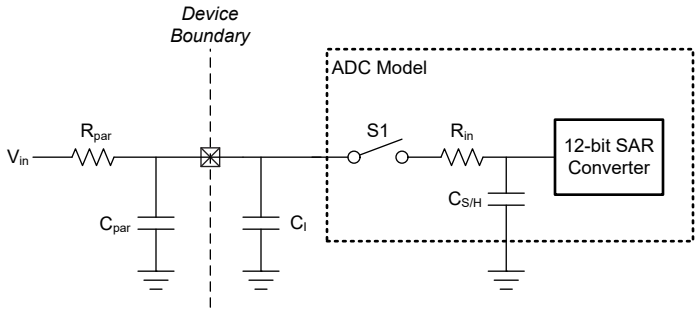


Figure 7-2. ADC Input Network

1. Refer to ADC Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to Digital IO Electrical Characteristics for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. Tau = $(R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_I)$
2. K= $\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (Min sampling time) = K × Tau

7.9.2 COMP Specifications

ADVANCE INFORMATION

ADVANCE INFORMATION

7.9.2.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage				±20	mV
V_{hys}	DC input hysteresis	HYST = 00h		0.4		mV
		HYST = 01h		10		
		HYST = 02h		20		
		HYST = 03h		30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode			5	µs
		Startup time to reach propagation delay specification, Low Power Mode			10	µs
I_{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA
I_{comp}	Comparator +VREF current consumption in low power	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, Internal VREF is reference for DAC, Low Power Mode		2.5		uA
8-bit DAC Electrical Characteristics						
V_{DAC}	DAC output range		0		VDD	V
$V_{DAC-CODE}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
R_{OUT}	Output resistance	V_{DAC} = 0.3V to (V_{DD} - 0.3V)		56		Ω
t_{dac_enable}	Turn on time from off state	DACCODE = 255		0.8		µs
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		µs

7.9.2.2 COMP DAC Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{dac}	DAC output range			0		VDD	V
$V_{dac-code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, n = 0 to 255			VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC			-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC			-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD		-2		2	% of FSR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Offset error	Offset error of 8-bit DAC			-5		5	mV
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB			1		µs
t_{dac_settle}	8-bit DAC settling time in sample mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB			40		µs

7.9.3 VREF Specifications

7.9.3.1 VREF Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 0	2.7			V
		BUFCONFIG = 1	1.71			
VREF	Voltage reference output voltage	BUFCONFIG = 0	2.46	2.5	2.54	V
		BUFCONFIG = 1	1.38	1.4	1.42	

7.9.3.2 VREF Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		200	370	µA
I_{Drive}	VREF output drive strength (1)	Drive strength supported on VREF+ device pin			50	µA
I_{SC}	VREF short circuit current			68	TBD	mA
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (2)				75	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.71 V to VDDmax, BUFCONFIG = 1	57	63		dB
		VDD = 2.7 V to VDDmax, BUFCONFIG = 0	49	53		
C_{VREF}	Recommended ±20% tolerance decoupling capacitor on VREF+ pin (3) (4)			1		µF
$t_{startup}$	VREF startup time	C_{VREF} = 1µF			350	µS
$t_{refresh}$	VREF External capacitor refresh time		31.25			

(1) The specified MAX output drive strength is supported regardless of which peripherals are being used in the device.
(2) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.
(3) Decoupling capacitor (C_{VREF}) is required when using the internal voltage reference VREF and should be connected from the VREF+ pin to VREF-/GND. When using the VREF+/- pins to supply an external reference, a decoupling capacitor value should be selected based on the external reference source.
(4) The VREF module should only be enabled when C_{VREF} is connected and should not be enabled otherwise.

7.9.4 Analog VBOOST Specification

7.9.4.1 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz		10.6		uA
$t_{START,VBST}$	VBOOST startup time			12	20	us

7.9.5 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL= 2h (VREF = 1.4V), ADC t_{sample} = 12.5uS	27	30	33	℃
TS_c	Temperature coefficient	-40℃ ≤ T_j ≤ 130℃	-2.1	-2	-1.9	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (VREF=1.4V), ADC CHANNEL=29			10	us

(1) Higher absolute accuracy may be achieved through user calibration. Please refer to temperature sensor chapter in detailed description section.
(2) This is the minimum required ADC sampling time when measuring the temperature sensor.

7.10 Serial Interface Specifications

7.10.1 UART

7.10.1.1 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	UART in Power Domain1			80	MHz
		UART in Power Domain0			40	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain1			10	Mbps
		UART in Power Domain0			4	Mbps
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.10.2 I2C

7.10.2.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain1		80		80		80	MHz
		I2C in Power Domain0		40		40		40	MHz
f_{SCL}	SCL clock frequency			0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

7.10.2.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.10.2.3 I²C Timing Diagram

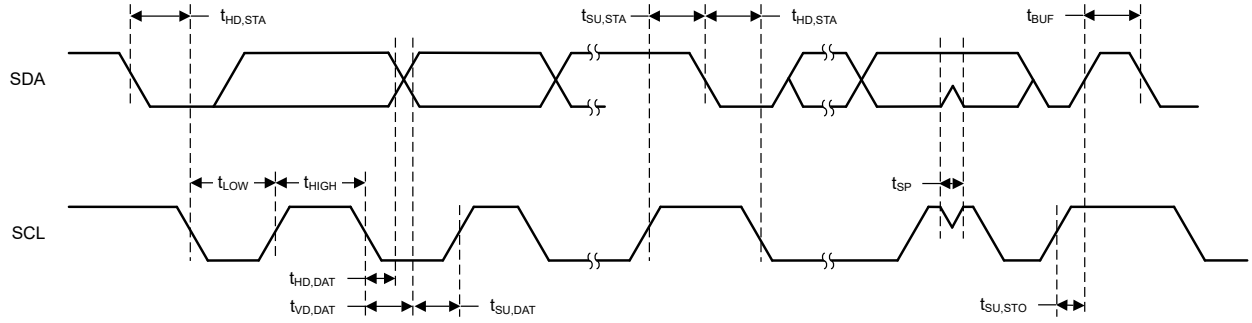


Figure 7-3. I2C Timing Diagram

7.10.3 SPI

7.10.3.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	VDD ≥ 2.7V, HSIO			30	MHz
		VDD ≥ 1.71V, HSIO			23	MHz
		VDD ≥ 2.7V, SDIO			25	MHz
		VDD ≥ 1.71V, SDIO			20	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK\_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=0	1 SPI Clock			ns
		SPH=1	1/2 SPI Clock			ns

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1 SPI Clock			ns
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI Clock	ns
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance				1 SPI Clock	ns
$t_{SU.CI}$	POCI input data setup time (1)	Delayed sampling enabled	1			ns
$t_{HD.CI}$	POCI input data hold time	VDD ≥ 2.7V, delayed sampling enabled	20			ns
		VDD ≥ 1.71V, delayed sampling enabled	25			ns
$t_{SU.CI}$	POCI input data setup time (1)	VDD ≥ 2.7V, no delayed sampling	18			ns
		VDD ≥ 1.71V, no delayed sampling	24			ns
$t_{HD.CI}$	POCI input data hold time	no delayed sampling enabled	0			ns
$t_{VALID.CO}$	PICO output data valid time (2)				10	ns
$t_{HD.CO}$	PICO output data hold time (3)		6			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock	VDD ≥ 2.7V	19			ns
		VDD ≥ 1.71V	22			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDD ≥ 2.7V			25	ns
		VDD ≥ 1.71V			31	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance	VDD ≥ 2.7V			39	ns
		VDD ≥ 1.71V			41.5	ns
$t_{SU.PI}$	PICO input data setup time		7			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(2)	VDD ≥ 2.7V			19	ns
		VDD ≥ 1.71V			24	ns
$t_{HD.PO}$	POCI output data hold time(3)		5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

ADVANCE INFORMATION

7.10.3.2 SPI Timing Diagram

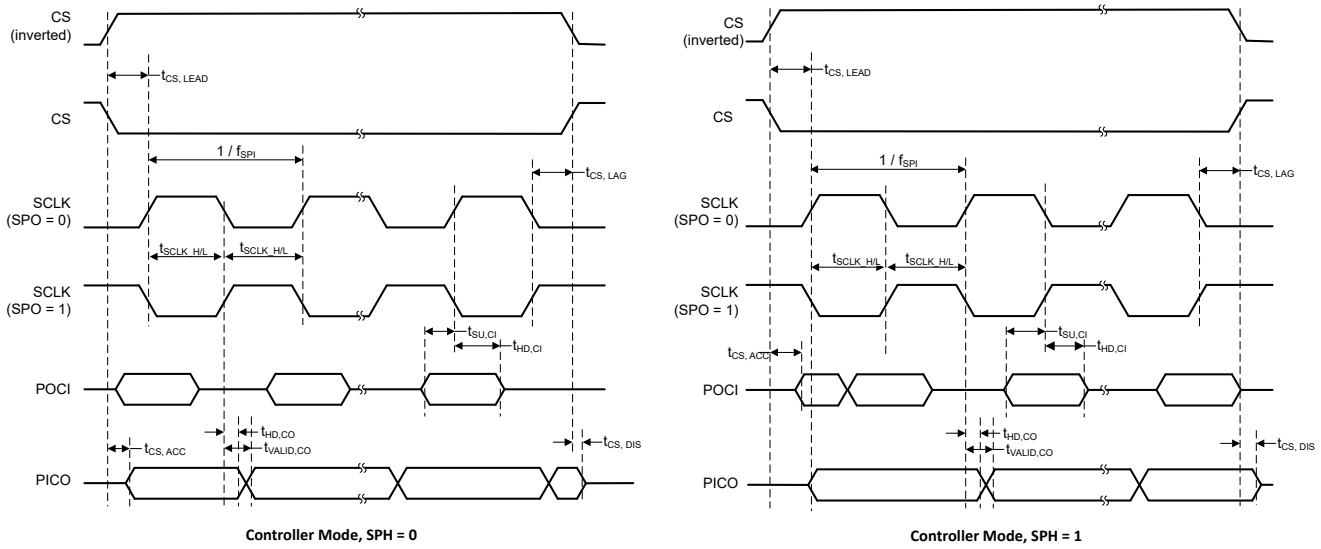


Figure 7-4. SPI Timing Diagram - Controller Mode

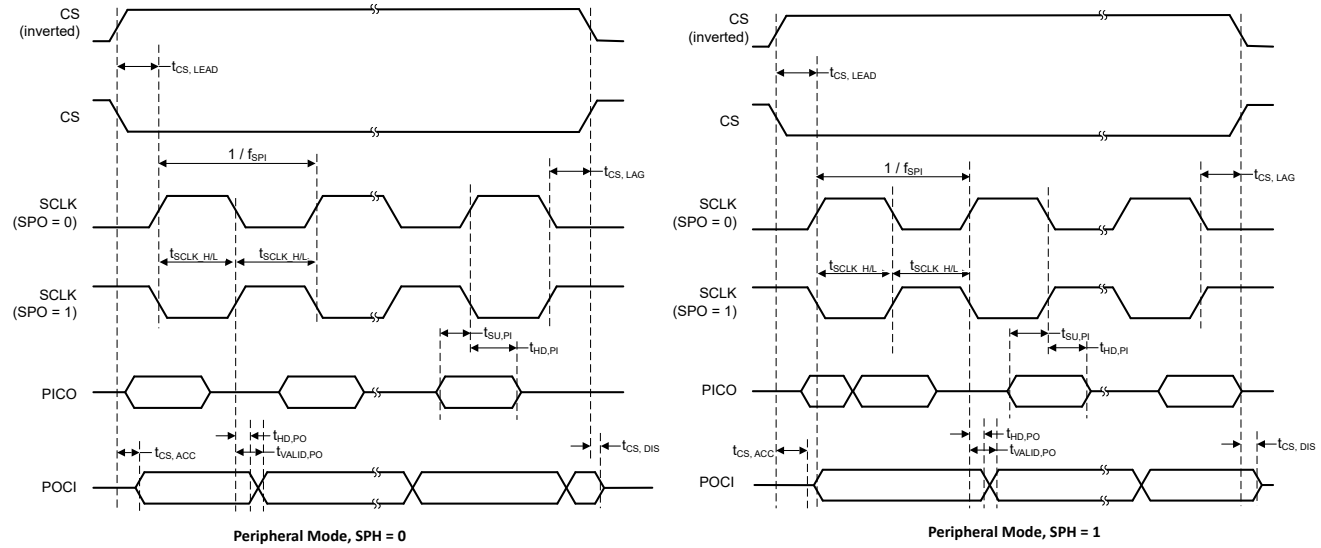


Figure 7-5. SPI Timing Diagram - Peripheral Mode

7.10.4 CAN

7.10.4.1 CAN

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CANCLK}	CAN input clock frequency				80	MHz
f_{BAUD}	CAN Baud rate				5	Mbps

7.10.5 QSPI

ADVANCE INFORMATION

7.10.5.1 QSPI

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{QSPI_CLK}	QSPI clock frequency	VDD ≥ 2.7V			40	MHz
		VDD ≥ 1.71V			20	MHz
DC_{QSPI_CLK}	Duty cycle QSPI clock		40	50	60	%
$t_{QSPI\_CLKH/L}$	QSPI clock high or low time			$1/(2\times f_{QSPI\_CLK})$		ns
$t_{CS:LEAD}$	CS lead-time, CS active to first clock edge	SPH = 0	1 QSPI clock			ns
$t_{CS:LEAD}$	CS lead-time, CS active to first clock edge	SPH = 1	1/2 QSPI clock			ns
$t_{CS:LAG}$	CS lag-time, last clock edge to CS inactive				1/2 QSPI clock	ns
$t_{CS:ACC}$	CS access time, CS active to IOx data out				1/2 QSPI clock	ns
$t_{SU:QSPI\_IOx}$	QSPI_IOx input setup time	VDD ≥ 2.7V	2.5			ns
		VDD ≥ 1.71V	9			ns
$t_{HDI:QSPI\_IOx}$	QSPI_IOx input hold time		5			ns
$t_{VALID:QSPI\_IOx}$	QSPI_IOx output valid time	VDD ≥ 2.7V			6	ns
		VDD ≥ 1.71V			6.5	ns
$t_{HDO:QSPI\_IOx}$	QSPI_IOx output hold time		3			ns

7.10.5.2 QSPI Timing Diagram

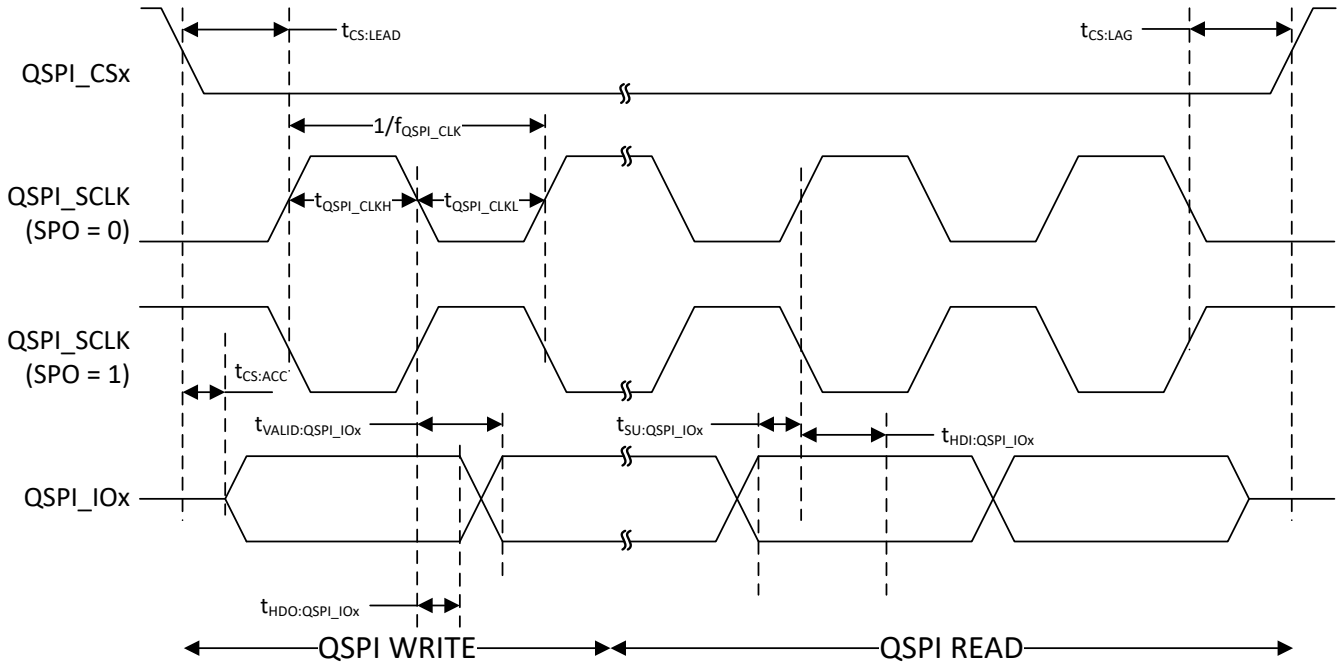


Figure 7-6. QSPI Timing Diagram - Controller Mode

7.10.6 I2S/TDM

7.10.6.1 Serial Audio

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Controller Mode						
f_{BCLK}	Serial Audio bit clock frequency	Transmitter mode			12.5	MHz
		Receiver mode			12.5	MHz
$t_{VALID.WCLK}$	Word Clock output valid time	VDD ≥ 2.7V			18	ns
		VDD ≥ 1.71V			21	ns
$t_{HOLD:WCLK}$	Word Clock output hold time		1			ns
$t_{VALID:ADx}$	Data output valid time	VDD ≥ 2.7V, Transmitter mode			20.5	ns
		VDD ≥ 1.71V, Transmitter mode			28.5	ns
$t_{HOLD:ADx}$	Data output hold time	Transmitter mode	3			ns
$t_{SU.ADx}$	Data input setup time	VDD ≥ 2.7V, Receiver mode	8.5			ns
		VDD ≥ 1.71V, Receiver mode	10			ns
$t_{HOLD.ADx}$	Data input hold time	VDD ≥ 2.7V, Receiver mode	2			ns
		VDD ≥ 1.71V, Receiver mode	3.1			ns
Target Mode						
f_{BCLK}	Serial Audio bit clock frequency	Transmitter mode			25	MHz
		Receiver mode			25	MHz
$t_{SU.WCLK}$	Word Clock input setup time		10			ns
$t_{HOLD:WCLK}$	Word Clock input hold time		1			ns
$t_{VALID:ADx}$	Data output valid time	VDD ≥ 2.7V, Transmitter mode			18	ns
		VDD ≥ 1.71V, Transmitter mode			24.5	ns
$t_{HOLD:ADx}$	Data output hold time	Transmitter mode	3			ns
$t_{SU.ADx}$	Data input setup time	Receiver mode	6.5			ns
$t_{HOLD.ADx}$	Data input hold time	Receiver mode	1.5			ns

7.10.6.2 I2S/TDM Timing Diagram

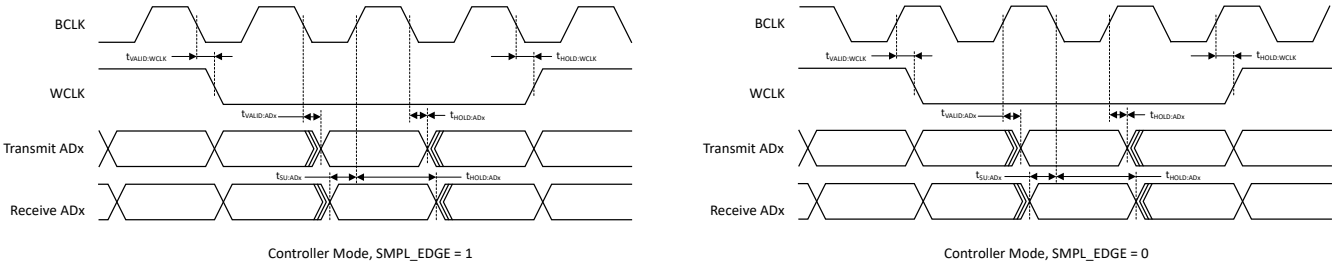


Figure 7-7. I2S/TDM Timing Diagram - Controller Mode

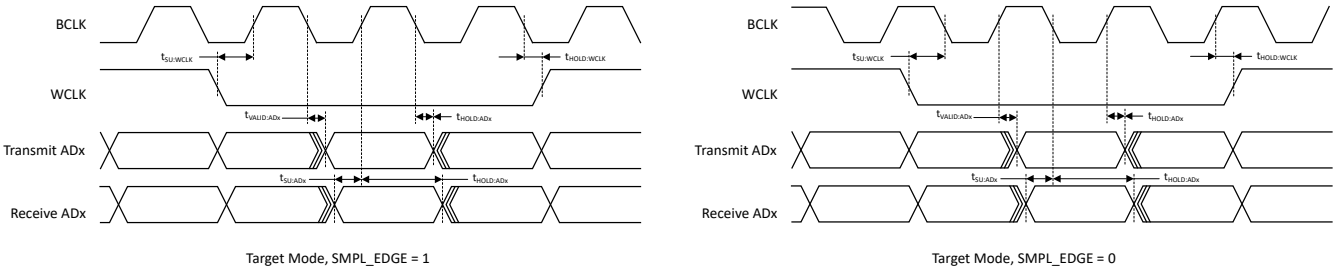


Figure 7-8. I2S/TDM Timing Diagram - Target Mode

ADVANCE INFORMATION

7.11 Digital IO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Electrical Characteristics							
V_{IH}	High level input voltage	All I/O except Reset		0.7*VDD		VDD+0.3	V
		Reset pin		0.85*VDD		VDD+0.3	
V_{IL}	Low level input voltage	All I/O except Reset		-0.3		0.3*VDD	
		Reset pin		-0.3		0.15*VDD	V
V_{HYS}	Hysteresis	All I/O except Reset		0.1*VDD			
		Reset pin		0.3*VDD			
I_{lkg}	High-Z leakage current[2] [3]	SDIO				50	nA
		HSIO				200	nA
		HDIO				280	nA
R_{PU}	Pull up resistance				40		kΩ
R_{PD}	Pull down resistance				40		kΩ
C_I	Input capacitance				5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, I_{IO}=–6mA VDD≥1.71V, I_{IO}=–2mA	VDD-0.4			V
		HSIO	VDD≥2.7V, DRV=1, I_{IO}=–6mA VDD≥1.71V, DRV=1, I_{IO}=–3mA	VDD-0.4			
			VDD≥2.7V, DRV=0, I_{IO}=–4mA VDD≥1.71V, DRV=0, I_{IO}=–2mA	VDD-0.4			
		HDIO	VDD≥2.7V, DRV=1, I_{IO}=–20mA VDD≥1.71V, DRV=1, I_{IO}=–10mA	VDD-0.4			
			VDD≥2.7V, DRV=0, I_{IO}=–6mA VDD≥1.71V, DRV=0, I_{IO}=–2mA	VDD-0.4			
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, I_{IO}=6mA VDD≥1.71V, I_{IO}=2mA			0.4	V
		HSIO	VDD≥2.7V, DRV=1, I_{IO}=6mA VDD≥1.71V, DRV=1, I_{IO}=3mA			0.4	
			VDD≥2.7V, DRV=0, I_{IO}=4mA VDD≥1.71V, DRV=0, I_{IO}=2mA			0.4	
		HDIO	VDD≥2.7V, DRV=1, I_{IO}=20mA VDD≥1.71V, DRV=1, I_{IO}=10mA			0.4	
			VDD≥2.7V, DRV=0, I_{IO}=6mA VDD≥1.71V, DRV=0, I_{IO}=2mA			0.4	
Switching Characteristics							
f_{max}	Port output frequency	SDIO [1]	VDD ≥ 2.7V, C_L= 20pF			32	MHz
			VDD ≥ 1.71V, C_L= 20pF			16	
		HSIO	VDD ≥ 2.7V, DRV = 1, C_L= 20pF			40	
			VDD ≥ 2.7V, DRV = 0, C_L= 20pF			32	
			VDD ≥ 1.71V, DRV = 1, C_L= 20pF			24	
			VDD ≥ 1.71V, DRV = 0, C_L= 20pF			16	
		HDIO	VDD ≥ 2.7V, DRV = 1[4], C_L= 20pF			20	
			VDD ≥ 2.7V, DRV = 0, C_L= 20pF			20	
			VDD ≥ 1.71V, DRV = 1[4], C_L= 20pF			16	
			VDD ≥ 1.71V, DRV = 0, C_L= 20pF			16	

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 2.7V, C_L = 20pF			3.5	ns
			VDD ≥ 1.71V, C_L = 20pF			6.6	
		HSIO	VDD ≥ 2.7V, DRV = 1, C_L = 20pF			1.8	
			VDD ≥ 2.7V, DRV = 0, C_L = 20pF			5.9	
			VDD ≥ 1.71V, DRV = 1, C_L = 20pF			3.7	
			VDD ≥ 1.71V, DRV = 0, C_L = 20pF			12.6	
		HDIO	VDD ≥ 2.7V, DRV = 1, C_L = 20pF			1.7	
			VDD ≥ 2.7V, DRV = 0, C_L = 20pF			3.8	
			VDD ≥ 1.71V, DRV = 1, C_L = 20pF			3.1	
			VDD ≥ 1.71V, DRV = 0, C_L = 20pF			8.2	

(1) The sum of the $|I_{IO}|$ current sourced or sunk by the device must always respect the absolute maximum rating
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(4) When operating a HDIO in DRV=1 high drive strength configuration, a series resistor is ncessary to limit the signal slew rate

7.12 TRNG

7.12.1 TRNG Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNG_{IACT}$	TRNG active current	TRNG clock = 20MHz		115		µA

7.12.2 TRNG Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNGCLK_F$	TRNG input clock frequency		9.5	10	25	MHz
$TRNG_{STARTUP}$	TRNG startup time			520		µs
$TRNG_{LAT32}$	Latency to generate 32 random bits	Decimation ratio = 4, TRNG clock = 20MHz		6.4		µs
$TRNG_{LAT256}$	Latency to generate 256 random bits	Decimation ratio = 4, TRNG clock = 20MHz		51.2		µs

7.13 Emulation and Debug

7.13.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz
t_{setup}	SWDIO setup time		4			ns
t_{hold}	SWDIO hold time		1			ns
t_{ovalid}	SWDIO output valid time				10	ns
t_{ohold}	SWDIO output hold time		5			ns

ADVANCE INFORMATION

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM33C3 Series 160-MHz Microcontrollers Technical Reference Manual*.

8.1 Arm Cortex-M33 core with TrustZone and FPU

The Arm Cortex-M33 is a high performance low-power 32-bit CPU, delivering efficient security to embedded applications. The 160 MHz CPU sub system (MCPUSS) implements an Arm Cortex-M33 CPU with TrustZone technology, FPU, DSP extentions and includes a 4kB instruction cache, a system timer (SYSTICK), a memory protection unit, and interrupt management features. Key features of the MCPUSS:

- Arm TrusztZone technology, using Armv8-M extension supporting secure and non-secure states
- Floating point unit (FPU) with support for IEEE 754 single precision floating point operations
- Digital signal processing (DSP) extension
- 4kB instruction cache with 0-wait state exectution at 160 MHz

  Configurable memory protection unit (MPU), supporting up to 16 regions for secure and non-secure applications
- Configurable secure attribution unit (SAU) with up to 8 regions as secure or non secure
- System timer (SysTick) with 24-bit down counter and automatic reload
- Nested vectored interrupt controller (NVIC) with 64 programmable priority levels
- Micro-trace buffer (MTB) capable of storing 4 of the previous CPU branch addresses
- Full debug capabilities with support 4 data watchpoints and 8 breakpoint comparators

8.2 Power Management and Clock Unit (PMCU)

8.2.1 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brownout reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.2.2 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim)
- **LFXT/LFCKIN** : Low-frequency external crystal oscillator or digital clock input (32 kHz)
- **HFXT/HFCKIN**: High-frequency external crystal oscillator or digital clock input (4 to 48 MHz)
- **SYSPLL**: System phase locked loop with 1 output (32 to 160 MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals in MCLK domain, derived from SYSOSC, or HSCLK, active in RUN and SLEEP modes
- **MCLK/2**: Main system clock for PD1 peripherals in MCLK/2 domain, derived MCLK and divided by 2

- **MCLK/4**: Main system clock for PD1 peripherals in MCLK/4 domain, derived MCLK and divided by 4
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4-MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32-kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High-frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High-speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode
- **CANCLK**: CAN functional clock, derived from HFCLK or SYSPLL
- **I2SCLK**: I2SCLK functional clock, derived from HFCLK or SYSPLL
- **LFOSCCLK**: Used for IWDT & WWDT, derived from LFOSC

For more details, see the CKM chapter of the *MSPM33 C3-Series 160-MHz Microcontrollers Technical Reference Manual* .

8.2.3 Operating Modes

MSPM33C3x MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code when in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD interface, a logic level match on certain IOs, or an interrupt from the low freqnecy sub system (LFSS).

To further balance performance and power consumption, MSPM33C3x devices implement three power domains: PD1, PD0, VBAT. PD1 contains the CPU, memories, and high performance peripherals. PD1 contains is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 contains low speed, low power peripherals which are always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode. VBAT can be powered[1] by a seperate power source other than V_{dd} or can be externally connected to V_{dd}. VBAT power domain contains the low frequency sub system and is always active when power is applied.

8.2.3.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in Table 8-1.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but it is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Modes

OPERATING MODE		RUN	SLEEP	STOP	STANDBY	SHUTDOWN
Oscillators	SYSOSC	EN		OPT	DIS	OFF
	LFOSC or LFXT	EN (LFOSC or LFXT)				
	HFXT	OPT		DIS		OFF
	SYSPLL	OPT		DIS		OFF

[1] VQFN32 package internally connects VBAT and VDD. VBAT pin is not accessible by the user

ADVANCE INFORMATION

Table 8-1. Supported Functionality by Operating Modes (continued)

OPERATING MODE		RUN	SLEEP	STOP	STANDBY	SHUTDOWN
Clocks	CPUCLK	160MHz	DIS			OFF
	MCLK	160MHz		DIS		OFF
	MCLK/2	80MHz		DIS		OFF
	MCLK/4 (PD1)	40MHz		DIS		OFF
	ULPCLK	40MHz		4MHz	32kHz	OFF
	MFCLK	4MHz				
	LFCLK	32 kHz				OFF
	HFCLK	OPT		DIS		OFF
	CANCLK	OPT		DIS		OFF
	I2SCLK	OPT		DIS		OFF
	RTCCLK	OPT				OPT
	LFCLK Monitor	OPT				OPT
	MCLK Monitor	OPT			DIS	OFF
PMU	POR monitor	EN				OFF
	BOR monitor	EN				OFF
	Core regulator	FULL DRIVE	FULL DRIVE	REDUCED DRIVE	LOW DRIVE	OFF
Core Functions	CPU	EN	DIS			OFF
	Flash	EN		DIS		OFF
	SRAM0	EN		DIS		OFF
	SRAM1/2/3	EN		OFF		OFF

ADVANCE INFORMATION

Table 8-1. Supported Functionality by Operating Modes (continued)

OPERATING MODE		RUN	SLEEP	STOP	STANDBY	SHUTDOWN
PD1 Peripherals	ADC0	OPT		DIS		OFF
	ADC1	OPT		DIS		OFF
	AES	OPT		DIS		OFF
	CAN-FD0	OPT		DIS		OFF
	CAN-FD1	OPT		DIS		OFF
	CRC	OPT		DIS		OFF
	DMA0	OPT		DIS		OFF
	DMA1	OPT		DIS		OFF
	EVENTLP	OPT		DIS		OFF
	GSC	OPT		DIS		OFF
	I2S0	OPT		DIS		OFF
	I2S1	OPT		DIS		OFF
	KEYSTORE	OPT		DIS		OFF
	PKA	OPT		DIS		OFF
	QSPI	OPT		DIS		OFF
	UC2 (SPI)	OPT		DIS		OFF
	UC15_0 (I2C)	OPT		DIS		OFF
	UC15_1 (I2C)	OPT		DIS		OFF
	UC12 (UART)	OPT		DIS		OFF
	UC13_0 (UART/SPI/I2C)	OPT		DIS		OFF
	UC13_1 (UART/SPI/I2C)	OPT		DIS		OFF
	UC13_2 (UART/SPI/I2C)	OPT		DIS		OFF
	UC13_3 (UART/SPI/I2C)	OPT		DIS		OFF
	UC14 (UART/I2C)	OPT		DIS		OFF
	SHA256	OPT		DIS		OFF
	TIMA0_0	OPT		DIS		OFF
	TIMA0_1	OPT		DIS		OFF
	TIMG12_0	OPT		DIS		OFF
	TIMG4_2	OPT		DIS		OFF
	TIMG4_3	OPT		DIS		OFF
	TIMG8_0	OPT		DIS		OFF
	TIMG8_1	OPT		DIS		OFF
	TRNG	OPT		DIS		OFF
	VREF	OPT		DIS		OFF
PD0 Peripherals	COMP0	OPT				OFF
	COMP1	OPT				OFF
	UC1_0 (UART/ I2C)	OPT				OFF
	UC1_1 (UART/ I2C)	OPT				OFF
	TIMG4_0	OPT				OFF
	TIMG4_1	OPT				OFF
	WWDT	OPT				OFF

ADVANCE INFORMATION

Table 8-1. Supported Functionality by Operating Modes (continued)

OPERATING MODE		RUN	SLEEP	STOP	STANDBY	SHUTDOWN
VBAT	RTC	OPT				
	IWDT	OPT				
	LFXT	OPT				
	BACKUP_REG	OPT				
	TAMPER	OPT				
IOMUX and IO Wakeup		EN				DIS w/ WAKE
Wake Sources		N/A	ANY IRQ	PD0 IRQ, LFSS IRQ	PD0 IRQ, LFSS IRQ	IOMUX, NRST, SWD

8.3 Device Memory Map

8.3.1 Memory Organization

Table 8-2 summarizes the platform memory map of the device.

Table 8-2. Platform Memory Map

MEMORY REGION	SUBREGION	MSPM33C32xA	MSPM33C32x9
Flash	Non-Secure	0x0000.0000 to 0x00FF.FFFF	0x0000.0000 to 0x007F.FFFF
	Secure	0x1000.0000 to 0x10FF.FFFF	0x1000.0000 to 0x107F.FFFF
SRAM	Non-Secure	0x2000.0000 to 0x203F.FFFF	0x2000.0000 to 0x203F.FFFF
	Secure	0x3000.0000 to 0x303F.FFFF	0x3000.0000 to 0x303F.FFFF
Peripheral	Non-Secure	0x4000.0000 to 0x4FFF.FFFF	0x4000.0000 to 0x4FFF.FFFF
	Secure	0x5000.0000 to 0x5FFF.FFFF	0x5000.0000 to 0x5FFF.FFFF
Subsystem	Non-Secure Region 0	0x6000.0000 to 0x6FFF.FFFF	0x6000.0000 to 0x6FFF.FFFF
	Secure Region 0	0x7000.0000 to 0x7FFF.FFFF	0x7000.0000 to 0x7FFF.FFFF
	Data Flash Non Secure	0x8000.0000 to 0x8000.7FFF	0x8000.0000 to 0x8000.7FFF
	Non-Secure Region 1	0x8008.0000 to 0x8FFF.FFFF	0x8000.8000 to 0x8FFF.FFFF
	Data Flash Secure	0x9000.0000 to 0x9000.7FFF	0x9000.0000 to 0x9000.7FFF
	Secure Region 1	0x9000.8000 to 0x9FFF.FFFF	0x9000.8000 to 0x9FFF.FFFF
	Non-Secure Region 2	0xA000.0000 to 0xAFFF.FFFF	0xA000.0000 to 0xAFFF.FFFF
	Secure Region 2	0xB000.0000 to 0xBFFF.FFFF	0xB000.0000 to 0xBFFF.FFFF
	Non-Secure Region 3	0xC000.0000 to 0xCFFF.FFFF	0xC000.0000 to 0xCFFF.FFFF
	Secure Region 3	0xD000.0000 to 0xDFFF.FFFF	0xD000.0000 to 0xDFFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

8.3.2 Peripheral Memory Map

Table 8-3 lists the available peripherals and the register base address for each in the secure and non-secure regions.

Table 8-3. Peripherals Memory Map

Peripheral Name	Non-Secure Base Address	Secure Base Address	Size
HSADC0.CONFIG	0x4000.0000	0x5000.0000	0x2000
HSADC1.CONFIG	0x4000.2000	0x5000.2000	0x2000
HSADC0.FIFO	0x4000.5000	0x5000.5000	0x1000
HSADC1.FIFO	0x4000.7000	0x5000.7000	0x1000
TIMA0_0	0x4001.0000	0x5001.0000	0x2000
TIMA0_1	0x4001.2000	0x5001.2000	0x2000
DMA0	0x4002.0000	0x5002.0000	0x2000
DMA1	0x4002.2000	0x5002.2000	0x2000

ADVANCE INFORMATION

Table 8-3. Peripherals Memory Map (continued)

Peripheral Name	Non-Secure Base Address	Secure Base Address	Size
FRI	0x4002.8000	0x5002.8000	0x2000
SYSMEM.CONFIG	0x4002.B000	0x5002.B000	0x2000
EAM	0x4002.D000	0x5002.D000	0x2000
QSPI	0x4003.2000	0x5003.2000	0x2000
NVMNW	0x4004.2000	0x5004.2000	0x2000
TRNG	0x4004.4000	0x5004.4000	0x2000
GSC	0x4004.7000	0x5004.7000	0x1000
UNICOMM1_0 (UC1_0)	0x4058.2000	0x5058.2000	0x2000
UC1_0.UART	0x4050.3000	0x5050.3000	0x1000
UC1_0.I2CC	0x4052.3000	0x5052.3000	0x1000
UC1_0.I2CT	0x4054.3000	0x5054.3000	0x1000
UNICOMM1_1 (UC1_1)	0x4058.4000	0x5058.4000	0x2000
UC1_1.UART	0x4050.5000	0x5050.5000	0x1000
UC1_1.I2CC	0x4052.5000	0x5052.5000	0x1000
UC1_1.I2CT	0x4054.5000	0x5054.5000	0x1000
SPG0	0x405A.1000	0x505A.1000	0x1000
UNICOMM2 (UC2)	0x4068.A000	0x5068.A000	0x2000
UC2.SPI	0x4066.1000	0x5066.1000	0x1000
UNICOMM15_0 (UC15_0)	0x4068.4000	0x5068.4000	0x2000
UC15_0.I2CC	0x4062.5000	0x5062.5000	0x1000
UC15_0.I2CT	0x4064.5000	0x5064.5000	0x1000
UNICOMM15_1 (UC15_1)	0x4068.6000	0x5068.6000	0x2000
UC15_1.I2CC	0x4062.7000	0x5062.7000	0x1000
UC15_1.I2CT	0x4064.7000	0x5064.7000	0x1000
UNICOMM12 (UC12)	0x4068.8000	0x5068.8000	0x2000
UC12.UART	0x4060.9000	0x5060.9000	0x1000
UNICOMM13_0 (UC13_0)	0x4068.0000	0x5068.0000	0x2000
UC13_0.UART	0x4060.B000	0x5060.B000	0x1000
UC13_0.I2CC	0x4062.B000	0x5062.B000	0x1000
UC13_0.I2CT	0x4064.B000	0x5064.B000	0x1000
UC13_0.SPI	0x4066.B000	0x5066.B000	0x1000
SPG1	0x406A.1000	0x506A.1000	0x1000
UNICOMM13_1 (UC13_1)	0x4076.1000	0x5076.1000	0x1000
UC13_1.UART	0x4070.1000	0x5070.1000	0x1000
UC13_1.I2CC	0x4072.1000	0x5072.1000	0x1000
UC13_1.I2CT	0x4074.1000	0x5074.1000	0x1000
UC13_1.SPI	0x4076.1000	0x5076.1000	0x1000
UNICOMM13_2 (UC13_2)	0x4078.2000	0x5078.2000	0x2000
UC13_2.UART	0x4070.3000	0x5070.3000	0x1000
UC13_2.I2CC	0x4072.3000	0x5072.3000	0x1000
UC13_2.I2CT	0x4074.3000	0x5074.3000	0x1000
UC13_2.SPI	0x4076.3000	0x5076.3000	0x1000
UNICOMM13_3 (UC13_3)	0x4078.4000	0x5078.4000	0x2000
UC13_3.UART	0x4070.5000	0x5070.5000	0x1000
UC13_3.I2CC	0x4072.5000	0x5072.5000	0x1000

ADVANCE INFORMATION

Table 8-3. Peripherals Memory Map (continued)

Peripheral Name	Non-Secure Base Address	Secure Base Address	Size
UC13_3.I2CT	0x4074.5000	0x5074.5000	0x1000
U13_3.SPI	0x4076.5000	0x5076.5000	0x1000
UNICOMM14 (UC14)	0x4078.6000	0x5078.6000	0x2000
UC14.UART	0x4070.7000	0x5070.7000	0x1000
UC14.I2CC	0x4072.7000	0x5072.7000	0x1000
UC14.I2CT	0x4074.7000	0x5074.7000	0x1000
SPG2	0x407A.1000	0x507A.1000	0x1000
SYSCTL	0x400A.F000	0x500A.F000	0x4000
TIMG4_0	0x400C.0000	0x500C.0000	0x2000
TIMG4_1	0x400C.2000	0x500C.2000	0x2000
DEBUGSS	0x400C.7000	0x500C.7000	0x2000
EVENT	0x400C.9000	0x500C.9000	0x3000
IOMUX	0x400C.C000	0x500C.C000	0x2000
LFSS	0x400D.8000	0x500D.8000	0x2000
COMP0	0x400E.0000	0x500E.0000	0x2000
COMP1	0x400E.2000	0x500E.2000	0x2000
VREF	0x400E.8000	0x500E.8000	0x2000
GPIO0	0x400F.0000	0x500F.0000	0x2000
GPIO1	0x400F.2000	0x500F.2000	0x2000
GPIO2	0x400F.4000	0x500F.4000	0x2000
CAN-FD0	0x4011.0000	0x5011.0000	0x8000
CAN-FD1	0x4011.8000	0x5011.8000	0x8000
TIMG4_2	0x4018.0000	0x5018.0000	0x2000
TIMG4_3	0x4018.2000	0x5018.2000	0x2000
TIMG8_0	0x4018.4000	0x5018.4000	0x2000
TIMG8_1	0x4018.6000	0x5018.6000	0x2000
TIMG12_0	0x4018.8000	0x5018.8000	0x2000
I2S0	0x401A.0000	0x501A.0000	0x2000
I2S1	0x401A.2000	0x501A.2000	0x2000
AES	0x401B.0000	0x501B.0000	0x2000
CRC	0x401B.2000	0x501B.2000	0x2000
SHA256	0x401B.4000	0x501B.4000	0x2000
KEYSTORE.CONTROL	0x401B.7000	0x501B.7000	0x1000
PKA	0x401C.0000	0x501C.0000	0x20000
MTB	0x4040.2000	0x5040.2000	0x1000
MTBRAM	0x4040.3000	0x5040.3000	0x0020

8.4 NVIC Interrupt Map

Table 8-4 shows the IRQ mapping for each peripherals in this device.

Table 8-4. Interrupt Vector Number

PERIPHERAL NAME	NVIC IRQ
SYSCTL	0
DEBUGSS	1
Flash Controller	2
WWDT	3
EVENT SUB PORT0	4
EVENT SUB PORT1	5
GPIO0	6
GPIO1	7
GPIO2	8
HSADC0 SEQ0	9
HSADC0 SEQ1	10
HSADC0 SEQ2	11
HSADC0 SEQ3	12
HSADC0 DCOMP	13
HSADC1 SEQ0	14
HSADC1 SEQ1	15
HSADC1 SEQ2	16
HSADC1 SEQ3	17
HSADC1 DCOMP	18
CAN-FD0	19
TIMA0_0	20
TIMG4_0	21
TIMG4_1	22
TIMG8_0	23
TIMG12_0	24
UNICOMM1_0	25
UNICOMM1_1	26
UNICOMM2	27
UNICOMM15_0	28
UNICOMM15_1	29
UNICOMM12	30
UNICOMM13_0	31
UNICOMM13_1	32
CAN-FD1	33
TIMA0_1	34
TIMG4_2	35
TIMG4_3	36
TIMG8_1	37
COMP0	38
COMP1	39
TRNG	40
AES	41

Table 8-4. Interrupt Vector Number (continued)

PERIPHERAL NAME	NVIC IRQ
LFSS	42
DMA0	43
DMA1	44
I2S0	45
I2S1	46
QSPI0	47
SHA256	48
PKA	49
UNICOMM13_2	50
UNICOMM13_3	51
UNICOMM14	52

8.5 Embedded Flash Memory

A dual bank of non-volatile flash memory (up to 1MB/512kB total) and a separate data flash bank (32kB) is provided for storing executable program code and application data.

Key features of the flash include:

- Hardware ECC protection (encode and decode) with single bit error correction and double-bit error detection.
- In-circuit program and erase operations supported across the entire recommended supply range.
- Read while write operation supported in dual bank mode.
- Small 2kB sector sizes (minimum erase resolution of 2kB)
- Flash write/erase protection
  - First 32 sectors of each flash bank has write/erase protection with a granularity of 2kB.
  - Remaining sectors of each flash bank write/erase protection with a granularity of 16kB.
- Trustzone security and MPU protections extended for all initiators using Global Security Controller (GSC)

Refer to the NVM chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.6 Embedded SRAM

The device includes a 256kB of SRAM across four banks fully protected by error correction code (ECC). SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code.

- Hardware ECC protection (encode and decode) with single bit error correction and double-bit error detection.
- SRAM0 (64kB) memory fully retained in low power modes of STOP and STANDBY operating mode.
- Trustzone security and MPU protections extended for all initiators using Global Security Controller (GSC).
  - 16-kB SRAM chunk size with variable size for ease of memory allocation for secure/non-secure and privilege/user mode threads.
- Automatic zeroisation of memory contents at power up.
- No arbitrated access to intiiators accessing different memory bank simultaneously.
- Interleaved access between SRAM banks 2 and 3.
- 4-deep SRAM cache buffer for read and write operations for improved access time for same bank access

The Table 8-5 describes the operational conditions for the multiple SRAM banks on the device.

Table 8-5. SRAM Bank Property

	SRAM0	SRAM1/2/3
0-Wait State Frequency	90 MHz	120 MHz
RUN Mode State	ACTIVE	ACTIVE
SLEEP Mode State	ACTIVE	ACTIVE
STOP Mode State	RETAINED	OFF

Table 8-5. SRAM Bank Property (continued)

	SRAM0	SRAM1/2/3
STANDBY Mode State	RETAINED	OFF
SHUTDOWN Mode State	OFF	OFF

For more details, see the SRAM chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual* .

8.7 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

- DMA0: 4 independent DMA transfer channels
  - Secure resource on reset
  - 2 full-feature channel (DMA0-DMA1) supporting repeated transfer modes
  - 2 basic channels (DMA2-DMA3) supporting single transfer modes and scatter mode
- DMA1: 12 indpendent DMA transfer channels
  - Non-Secure resource on reset
  - 6 full-feature channel (DMA0-DMA5) supporting repeated transfer modes
  - 6 basic channels (DMA6-DMA11) supporting single transfer modes and scatter mode
- Configurable DMA channel priorities
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications

Table 8-6 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Note

DMA0 has limited access to peripherals in PD0 and can only access PMU (SYSCTL) & UC1 in PD0.

Table 8-6. DMA Trigger Mapping

Trigger 0:41	DMA0	DMA1
0	Software	Software
1	Generic Subscriber 0 (FSUB_0)	Generic Subscriber 0 (FSUB_0)
2	Generic Subscriber 1 (FSUB_1)	Generic Subscriber 1 (FSUB_1)
3	AES Publisher 1	AES Publisher 1
4	AES Publisher 2	AES Publisher 2
5	ADC0 SEQ0	ADC0 SEQ0
6	ADC0 SEQ1	ADC0 SEQ1
7	ADC0 SEQ2	ADC0 SEQ2
8	ADC0 SEQ3	ADC0 SEQ3
9	ADC1 SEQ0	ADC1 SEQ0
10	ADC1 SEQ1	ADC1 SEQ1

ADVANCE INFORMATION

Table 8-6. DMA Trigger Mapping (continued)

Trigger 0:41	DMA0	DMA1
11	ADC1 SEQ2	ADC1 SEQ2
12	ADC1 SEQ3	ADC1 SEQ3
13	SHA Publisher 1	SHA Publisher 1
14	I2S0 Publisher 1	I2S0 Publisher 1
15	I2S0 Publisher 2	I2S0 Publisher 2
16	I2S1 Publisher 1	I2S1 Publisher 1
17	I2S1 Publisher 2	I2S1 Publisher 2
18	QSPI RX	QSPI RX
19	QSPI TX	QSPI TX
20	UNICOMM1_0.TX	Reserved
21	UNICOMM1_0.RX	Reserved
22	UNICOMM1_1.TX	Reserved
23	UNICOMM1_1.RX	Reserved
24	UNICOMM2.TX	UNICOMM2.TX
25	UNICOMM2.RX	UNICOMM2.RX
26	UNICOMM15_0.TX	UNICOMM15_0.TX
27	UNICOMM15_0.RX	UNICOMM15_0.RX
28	UNICOMM15_1.TX	UNICOMM15_1.TX
29	UNICOMM15_1.RX	UNICOMM15_1.RX
30	UNICOMM12.TX	UNICOMM12.TX
31	UNICOMM12.RX	UNICOMM12.RX
32	UNICOMM13_0.TX	UNICOMM13_0.TX
33	UNICOMM13_0.RX	UNICOMM13_0.RX
34	UNICOMM13_1.TX	UNICOMM13_1.TX
35	UNICOMM13_1.RX	UNICOMM13_1.RX
36	UNICOMM13_2.TX	UNICOMM13_2.TX
37	UNICOMM13_2.RX	UNICOMM13_2.RX
38	UNICOMM13_3.TX	UNICOMM13_3.TX
39	UNICOMM13_3.RX	UNICOMM13_3.RX
40	UNICOMM14.TX	UNICOMM14.TX
41	UNICOMM14.RX	UNICOMM14.RX

For more details, see the DMA chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.8 Event Manager

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)

– Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

Refer to the Event chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

Table 8-7. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
5	Generic event channel 5 selected	1 : 1
6	Generic event channel 6 selected	1 : 1
7	Generic event channel 7 selected	1 : 1
8	Generic event channel 8 selected	1 : 1
9	Generic event channel 9 selected	1 : 1
10	Generic event channel 10 selected	1 : 1
11	Generic event channel 11 selected	1 : 1
12	Generic event channel 12 selected	1 : 2 (splitter)
13	Generic event channel 13 selected	1 : 2 (splitter)
14	Generic event channel 14 selected	1 : 2 (splitter)
15	Generic event channel 15 selected	1 : 2 (splitter)

8.9 Error Aggregator Module (EAM)

The Error Aggregator Module (EAM) aggregates single error correction (SEC) and double error detection (DED) for the system memory and security errors. EAM generates interrupt or NMI to the CPU based on the priority of the error. The EAM module is protected by a security firewall to allow customer critical code in secure mode of the application to handle the error in a context safe method.

The EAM supports the following features:

- ECC error logging for SEC and DED from flash and SRAM
- Security error logging for non-secure access to a firewall region for memory and peripherals
- Security error logging for hide protected region in the flash
- First error logged with initiator and type of access error logged

8.10 GPIO

The general purpose input/output (GPIO) peripheral provides the user with a means to write data out and read data in to and from the device pins. Through the use of the Port A, Port B and Port C GPIO peripherals, these devices support up to 93 GPIO pins.

The key features of the GPIO module include:

- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

For more details, see the GPIO chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.11.1 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-1. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

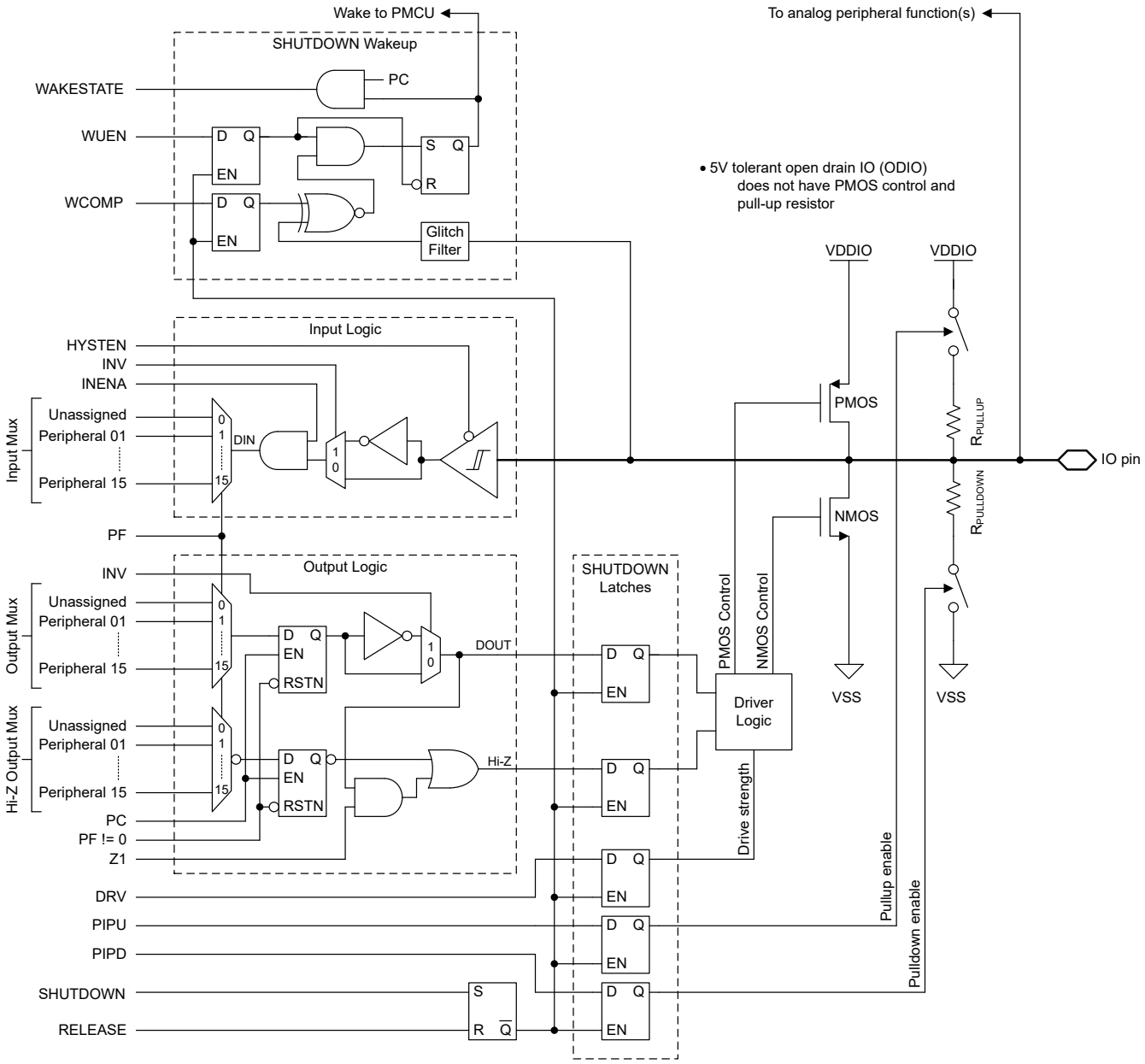


Figure 8-1. Superset Input/Output Diagram

8.12 Analog Modules

8.12.1 HSADC

The device has two analog-to-digital converter (ADC) modules, HSADC0 and HSADC1, support fast 12-bit conversions with single-ended inputs and simultaneous sampling operation.

HSADC features include:

- 12-bit output resolution at 9.4Msps with greater than 11.2 ENOB
- HW averaging enables 14-bit effective resolution at 587ksps
- Up to 36 total external input channels
- Up to 4 independent and variable length sequencers with FIFO result read out
  - Maps up to 4 analog channel sequences for conversion

ADVANCE INFORMATION

  - Independent Sample and Hold Window up to 1472 sample clocks for high impedance analog signals
  - User configurable automatic abort to pre-empt high priority sequencer during active conversion
- Sample cap reset option with preset to VREF- or (VREF+ - VREF-)/2
- Up to 4 post processing blocks (PPB) with offset correction, zero-crossing detection and compare high/low function
- Internal channels for temperature sensing and supply monitoring
- Software selectable reference:
  - Configurable internal reference voltage of 1.4V and 2.5V (requires decoupling capacitor on VREF+/- pins)
  - External reference supplied to the ADC through the VREF+/- pins

Table 8-8. ADC Channel Mapping

CHANNEL[0:31]	SIGNAL NAME(1)	
	HSADC0	HSADC1
0	A0_0	A1_0
1	A0_1	A1_1
2	A0_2	A1_2
3	A0_3	A1_3
4	A0_4	A1_4
5	A0_5	A1_5
6	A0_6	A1_6
7	A0_7	A1_7
8	A0_8	A1_8
9	A0_9	A1_9
10	A0_10	A1_10
11	*Temperature Sensor*	A1_11
12	A0_12	A1_12
13	A0_13	A1_13
14	A0_14	A1_14
15	A0_15	-
16	A0_16	-
17	A0_17	-
18	A0_18	-
19	A0_19	-
20	A0_20	-
21	A0_21	-
22 - 29	-	-
30	*VBAT Monitor*	*VBAT Monitor*
31	*Supply Monitor*	*Supply Monitor*

(1) For more information about device analog connections please refer to Section 8.12.5

For more details, see the ADC chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.12.2 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
  - External reference voltage (VREF IO)

  - Internal reference voltage (1.4V, 2.5V)
  - Integrated 8-bit reference DAC, the output of which is also available to connect to an external op-amp.
- Configurable operation modes:
  - High speed mode
  - Lower power mode
- Programmable output glitch filter delay
- Supports 6 blanking sources (refer to the CTL2 register of the COMP chapter)
- Supports device wake up from up to 4 ADC channels in most low-power modes
- Output connected to advanced timer fault handling mechanism
- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins or from internal analog modules.

Table 8-9. COMP Blanking Source Table

CTL2.BLANKSRC VALUE	BLANKING SOURCE
1	TIMA0_0.CC2
2	TIMA0_0.CC3
3	TIMA0_1.CC2
4	TIMA0_1.CC3
5	TIMG4_0.CC1
6	TIMG4_1.CC1

Table 8-10. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x3	COMP0_IN3+	COMP0_IN3-

Table 8-11. COMP1 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP1_IN0+	COMP1_IN0-
0x1	COMP1_IN1+	COMP1_IN1-
0x2	COMP1_IN2+	COMP1_IN2-
0x3	COMP1_IN3+	COMP1_IN3-

For more information about device analog connections, see *Device Analog Connections*.

For more details, see the COMP chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.12.3 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly (-2 mV/°C) with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

See the temperature sensor section of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual* for guidance on calculating the device temperature with the factory trim value.

8.12.4 VREF

The shared voltage reference module (VREF) in these devices contain a configurable voltage reference buffer which allows users to supply a stable reference to on-board analog peripherals. It also supports bringing in an external reference for applications where higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports full speed ADC operation
- Support for bringing in an external reference on VREF+/- device pins
- Requires a decoupling capacitor placed on VREF+/- pins for proper operation. See VREF specification section for more details

For more details, see the VREF chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.12.5 Device Analog Connections

Figure 8-2 shows the internal analog connection of the device.

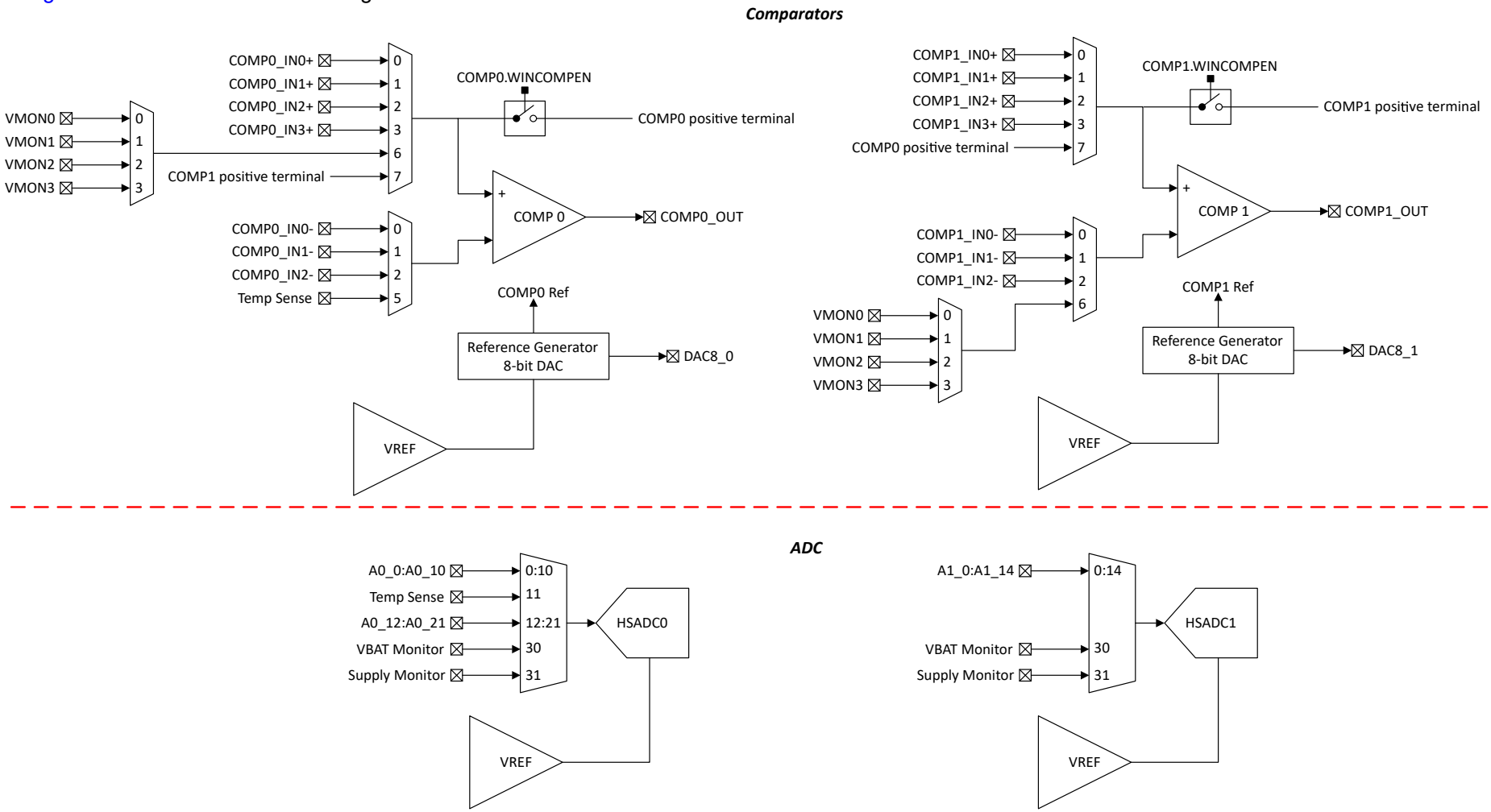


Figure 8-2. Device Analog Connection

ADVANCE INFORMATION

8.13 Security and Cryptography

The device security comprises of the following peripherals

- Global Security Controller (GSC) for device security
- Advanced Encryption Standard (AES) accelerator
- Secure Hash Algorith (SHA256) accelerator with Hashed Message Authentication Control (HMAC) capability
- Public Key Accelerator (PKA) for assymetric cryptographic operations
- True Random Number Generator (TRNG)
- Keystore controller
- Cyclic Redundancy Check (CRC)

8.13.1 Global Security Controller (GSC)

The Global Security Controller (GSC) configures the secure and privilege attributes for the full device. The GSC consists of multiple blocks that ensure the device's security and peripheral properties are seen same by all bus initiators.

- Configures the secure and privilege attribute for the flash, SRAM and peripherals
- Configures the level of security and privilege state violation as NMI or bus-fault
- Configures the hide protection of flash sectors using watermark for start and end sector
- Logs security violation in the error aggregator module (EAM) for CPU to identify the initiator and destination address
- Provides the result of DICE checksum for application to read

For more details, see the GSC chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.13.2 AESADV

The AES advanced (AESADV) accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware according to the advanced encryption standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AESADV accelerator features include:

- AES operation with 128-bit and 256-bit keys
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- Support for AES-CCM and AES-GCM modes
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AESADV ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the *Operating Modes* section of the device technical reference manual)

For more details, see the AESADV chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.13.3 SHA256

The SHA256 provides hardware-acclerated hash functions. These has functions can generate a condensed representation of a message or a data file call digest which can then be used to verify the message integrity.

- SHA-2 (SHA-224 and SHA-256) algorithm compliant with the FIPS 180-3 standard
- Hash message authentication code (HMAC) operation
- Hashing of 0 to 2^{33} bytes of data SHA-224, or SHA-256 hash algorithm at byte granularity
- Host-assisted HMAC key preprocessing for HMAC keys larger than 64 bytes
- HMAC from precomputes (inner/outer digest) for improved performance on small blocks
- Supports DMA for efficient data transfer

- Auto-count and compute function up to size of data transfer to generate digest (signature) without host-assistance.
- Interrupt generation to read digest (signature)

For more details, see the SHA256 chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.13.4 Public Key Algorithm (PKA)

The PKA accelerator supports mathematical operations needed for elliptic curves up to 521 bits and RSA key pair geenration up to 1024 bits. The module enables the following capabilities for user application.

- Key Agreement Schemes
  - Elliptic curve Diffie–Hellman (ECDH)
  - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- Signature Generation and Verification
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- Curve Support
  - Short Weierstrass form: NIST-P224, NIST-P256, NIST-P384, NIST-P521, Brainpool-256R1, Brainpool-384R1, Brainpool-512R1, secp256r1
  - Montgomery form: Curve25519

For more details, see the PKA chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.13.5 TRNG

The true random number generator (TRNG) utilizes an internal circuit to generate 32-bit random numbers. The TRNG is intended to be used as a source to a deterministic random number generator (DRNG) to build a FIPS-140-2 compliant system. Key features of the TRNG include:

- Generation of 32-bit random numbers
- A new 32-bit number may be generated every 32 × 4 = 128 TRNG clock cycles
- Built-in health tests
- Available in RUN and SLEEP modes

For more details, see the TRNG chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.13.6 Keystore

The Keystore controller provides secure management of the Advanced Encryption Engine (AES) keys. The use-model of the keystore controller is to securely deposit keys into it during the execution of customer secure code, and have the AES engine access them subsequently in a secure manner without leaking any key data to observers. Both 128 and 256-bit keys can be stored in the keystore's key slots. The keystore and its interaction with the AES engine are designed for secure operation including thwarting partial key modification attacks.

- Support for storage of up to 4 keys

For more details, see the KEYSTORE chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.13.7 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal
- Support for custom polynomials

For more details, see the CRC chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.14 Serial Communication Interfaces

8.14.1 UNICOMM (UART/I²C/SPI)

UNICOMM is a highly flexible peripheral which can be configured as a UART, SPI, I²C-Controller or I²C-Target function. The user can select one of the serial interfaces before configuration and data transfer. The peripheral uses a common FIFO per instance to maximize the device capability based on the operating state. A serial peripheral group combines one or more UNICOMM for special functions like I²C loopback and is an optional configuration. Table 8-12 describes the grouping of UNICOMM, peripheral serial interfaces available and FIFO depth.

Table 8-12. UNICOMM (UCx) Serial Peripheral

UNICOMM INSTANCE	SERIAL PERIPHERAL GROUP	UART	I²C Controller	I²C Target	SPI	FIFO depth
UC1	SPG0 (PD0)	Yes	Yes	Yes	-	16
UC2	SPG1 (PD1)	-	-	-	Yes	4
UC15		-	Yes	Yes	-	4
UC12		Yes	-	-	-	4
UC13_0		Yes	Yes	Yes	Yes	4
UC13_1	SPG2 (PD1)	Yes	Yes	Yes	Yes	4
UC13_2		Yes	Yes	Yes	Yes	4
UC13_3		Yes	Yes	Yes	Yes	4
UC14		Yes	Yes	Yes	-	4

8.14.1.1 UART (UNICOMM)

The UART peripheral function provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Support transmit and receive loopback mode operation
- See Table 8-13 for detail information on supported protocols

Table 8-13. UART (UNICOMM) Features

Supported Features	UC1.UART	UC12.UART	UC13.UART	UC14.UART
Active in Stop and Standby Mode	Yes	-	-	-
Support hardware flow control	Yes	Yes	Yes	Yes
Support 9-bit configuration	Yes	Yes	Yes	Yes
Support LIN mode	Yes	Yes	-	Yes
Support DALI	-	Yes	-	-
Support IrDA	-	Yes	-	-

Table 8-13. UART (UNICOMM) Features (continued)

Supported Features	UC1.UART	UC12.UART	UC13.UART	UC14.UART
Support ISO7816 Smart Card	-	Yes	Yes	-
Support Manchester coding	-	Yes	-	-

For more details, see the UART (UNICOMM) chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.14.1.2 I2C (UNICOMM)

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
  - Supported on high-drive (HDIO) IOs only
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression
- See Table 8-14 and Table 8-15 for detailed information on supported features for controller and target functions

Table 8-14. I2C Controller (UNICOMM) Features

Supported Features	UC1.I2C, UC14.I2C, UC15.I2C	UC13
Supports standard-mode (Sm)	Yes	Yes
Supports Fast-mode (Fm)	Yes	Yes
Supports Fast-mode Plus (Fm+)	Yes	Yes
Supports analog glitch filter	Yes	-
Supports digital glitch filter	-	Yes
Supports burst mode	Yes	-
Supports SMBus mode	Yes	-

Table 8-15. I2C Target (UNICOMM) Features

Supported Features	UC1.I2C	UC14.I2C, UC15.I2C	UC13
Supports standard-mode (Sm)	Yes	Yes	Yes
Supports Fast-mode (Fm)	Yes	Yes	Yes
Supports Fast-mode Plus (Fm+)	Yes	Yes	Yes
Supports analog glitch filter	Yes	Yes	-
Supports digital glitch filter	-	-	Yes
Supports second target address & mask	Yes	Yes	-
Supports SMBus mode	Yes	Yes	-
Supports low power wakeup	Yes	-	Yes

ADVANCE INFORMATION

For more details, see the I2C (UNICOMM) chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.14.1.3 SPI (UNICOMM)

The serial peripheral interface (SPI) peripherals function support the following key features:

- Supports up to 40 Mbits/s in both controller and peripheral mode [2]
- Configurable as a controller or a peripheral
- Support for up to 4 chip select for both controller and peripheral
- Supports single parity for transmit and receive
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit (peripheral mode)
- Supports TI mode, Motorola mode and National Microwire format
- See Table 8-16 for detailed information on supported features

Table 8-16. SPI (UNICOMM) Features

Supported Features	UC2.SPI	UC13.SPI
Controller and Peripheral mode	Yes	Yes
Supports Parity function	Yes	Yes
Supports Repeat mode transfer	Yes	-
Supports Receive timeout	Yes	-
Supports Command/Data control	Yes	-
Supports 4 chip selects	Yes	-

For more details, see the SPI (UNICOMM) chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.14.2 CAN-FD

The controller area network (CAN) controller enables communication with a CAN2.0A, CAN2.0B, or CAN-FD bus and is compliant to ISO 11898-1:2015 standard supporting up to 5Mbit/s bit rate. Key features of the CAN-FD peripheral include:

- Full support for 64-byte CAN-FD frames
- Dedicated 1KB message SRAM with ECC
- Configurable transmit FIFO, transmit queue and event FIFO (up to 32 elements)
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs (up to 64 elements each)
- Up to 128 filter elements
- Two interrupt lines
- Power-down and wake-up support
- Timestamp counter

For more details, see the CAN-FD chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.14.3 Quad SPI (QSPI)

The Quad SPI (QSPI) controller interfaces to an external serial flash memory over 4 data lines to provide fast data transfer up to 20Mbytes/s.

- Supports single, bi (dual) and quad data operations for data communication upto 40MHz serial clock
- Programmable interface supports QSPI operation in both Mode-0 and Mode-3
- Supports both 3-byte and 4-byte address external QSPI flash memory
- Preconfigured read frame formats and dummy clock insertion for optimized read operations

[2] Only SPI signals on HSIO pins support data rates up to 40 Mbits/s; see the *Pin Diagrams* section for HSIO pins.

- Configurable automatic prefetch function for continous data read without CPU intervention
- Separate transmit and receive FIFOs, upto 4 locations deep, support DMA data transfer

For more details, see the QSPI chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.14.4 Digital Audio Interface - I2S/TDM

The I2S/TDM module provides a standardized serial interface to transfer audio data. The module can be configured in different modes including I2S standards, LSB or MSB-justified, PCM/DSP and TDM for example. It can be used in conjunction with the DMA controller.

- Configurable and independent transmitter and receiver functions on data lines
- Configurable controller or target function
- Integrated transmitted and receiver 4-location deep FIFO with packing feature
- Clock generator to target specific audio frequency generation
- Data size configuration from 8 to 32-but audio word size
- Audio protocol: I2S, LSB or MSB-justied, PCM/DSP, TDM
- Up to 16 slots available in TDM format
- Empty slot configuration for sendinds 0's, 1's or Hi-Z
- Configurable bit clock sampling edge
- Frame synchronization configurable for offset and bit length
- Independent DMA request for transmitter and receiver functions

Table 8-17. Digital Audio Interface Parameters

I2S/TDM parameters	I2S0	I2S1
TxFIFO depth	4	4
RxFIFO depth	4	4
Maximum TDM slots	16	16

For more details, see the I2S/TDM chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.15 LFSS

The Low-Frequency Subsystem (LFSS) combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low-frequency clock (LFCLK) or need to be active during low-power modes. In this device, LFSS is powered by a separate battery backup domain called VBAT. The low-frequency clock has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS in this device contains following components:

- A dedicated battery backup domain supply and dedicated pin (VBAT)
- Real-time clock (RTC_A) with additional prescalar extension and timestamp captures
- An asynchronous Independent Watchdog Timer (IWDT)
- Tamper detection input / output (TIO) module
- Tamper detection with timestamp
- A small scratchpad memory storage (SPM)
- Heartbeat generator

For more details, see the LFSS chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.16 Timers, RTC and Watchdogs

ADVANCE INFORMATION

8.16.1 Timers (TIMx)

The timer peripherals in these devices support the following key features, for specific configuration see Table 8-18:

Specific features for the general-purpose timer (TIMGx) include:

- 16-bit and 32-bit timers with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow CC register available in TIMG4_n (n = 0, 1, 2, 3) and TIMG12_0
- Shadow load register available in TIMG4_n (n = 0, 1, 2, 3) and TIMG12_0
- Support quadrature encoder interface (QEI) for positioning and movement sensing available in TIMG8_n (n = 0, 1)
- Support synchronization and cross trigger among different timer instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals trigger capability
- Cross trigger event logic for Hall sensor inputs TIMG8_n (n = 0, 1)

Specific features for the advanced timer (TIMA0_x) include:

- 16-bit timer with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Internal 5th and 6th internal CC channel for capture/compare events
- Shadow register for load and CC register available in both TIMA0_0 and TIMA0_1
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to ensure the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt and DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-18. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEADBAND	FAULT	QEI
TIMA0_0	PD1	16-bit	8-bit	8-bit	4 + 2	Yes	Yes	Yes	Yes	Yes	–
TIMA0_1	PD1	16-bit	8-bit	8-bit	4 + 2	Yes	Yes	Yes	Yes	Yes	–
TIMG4_0	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG4_1	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG4_2	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG4_3	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG8_0	PD0	16-bit	8-bit	–	2	–	–	–	–	–	Yes
TIMG8_1	PD0	16-bit	8-bit	–	2	–	–	–	–	–	Yes

Table 8-18. TIMx Configurations (continued)

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEADBAND	FAULT	QEI
TIMG12_0	PD1	32-bit	–	–	2	–	–	Yes	–	–	–

Table 8-19. TIMx Cross Trigger Map (PD1)

TSEL.ETSEL Selection	TIMA0_0, TIMA0_1	TIMG8_0, TIMG8_1	TIMG4_2, TIMG4_3	TIMG12_0
0	TIMA0_0.TRIGO	Reserved	Reserved	Reserved
1	TIMA0_1.TRIGO	Reserved	Reserved	Reserved
2	TIMG4_2.TRIGO	TIMG4_2.TRIGO	TIMG4_2.TRIGO	TIMG4_2.TRIGO
3	TIMG4_3.TRIGO	TIMG4_3.TRIGO	TIMG4_3.TRIGO	TIMG4_3.TRIGO
4	TIMG12_0.TRIGO	TIMG12_0.TRIGO	TIMG12_0.TRIGO	TIMG12_0.TRIGO
5	TIMG8_0.TRIGO	TIMG8_0.TRIGO	TIMG8_0.TRIGO	TIMG8_0.TRIGO
6	TIMG8_1.TRIGO	TIMG8_1.TRIGO	TIMG8_1.TRIGO	TIMG8_1.TRIGO
7 to 31	Reserved			
18-31	Reserved			

Table 8-20. TIMx Cross Trigger Map (PD0)

TSEL.ETSEL Selection	TIMG4_0	TIMG4_1
0	TIMG4_0.TRIG0	TIMG4_0.TRIG0
1	TIMG4_1.TRIG0	TIMG4_1.TRIG0
2 to 31	Reserved	

For more details, see the TIMx chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.16.2 RTC_A

The RTC_A instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. RTC_A provides common key features in relation to the Low-Frequency Subsystem (LFSS).

Common key features of RTC_A include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz
- Calibration for crystal offset error (up to ±240ppm)
- Compensation for temperature drift (up to ±240ppm)
- RTC clock output to pin for calibration
- Three bit prescaler for heartbeat function with interrupt generation
- RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz, or 1Hz
- RTC time stamp capture upon detection of a timer stamp event, including tamper (TIO) event and VDD fail event
- RTC counter lock function

Table 8-21 shows the RTC features supported in this device.

Table 8-21. RTC Instances and Key Features

RTC Features	RTC_A
Power enable register	-
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes

ADVANCE INFORMATION

Table 8-21. RTC Instances and Key Features (continued)

RTC Features	RTC_A
Selectable binary or binary-coded decimal (BCD) format	Yes
Leap-year correction (valid for year 1901 through 2099)	Yes
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes
Calibration for crystal offset error and crystal temperature drift (up to ±240ppm total)	Yes
RTC clock output to pin for calibration (GPIO)	Yes
RTC clock output to pin for calibration (TIO)	Yes
Three bit prescaler for heartbeat function with interrupt generation	Yes
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	Yes
RTC time stamp capture upon detection of a timer stamp event, including: • TIO event • VDD fail event	Yes
RTC counter lock function	Yes

For more details, see the RTC chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.16.3 IWDT

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent power and clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter with closed and open window
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods

For more details, see the IWDT chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.16.4 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

8.17 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality, see the debug chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual.*

Table 8-22. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

8.18 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined HASH password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSL_UART_RX and BSL_UART_TX signals (for UART), or the BSL_I^{2}C_SCL and BSL_I^{2}C_SDA signals (for I^{2}C) or the BSL_CAN_RX and BSL_CAN_TX signals (for CAN). Additionally, one or two additional pins (BSL_INVOKE and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-23. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSL_UART_RX	Required for UART	UART receive signal (RX), an input
BSL_UART_TX	Required for UART	UART transmit signal (TX) an output
BSL_I2C_SCL	Required for I2C	I^{2}C BSL clock signal (SCL)
BSL_I2C_SDA	Required for I2C	I^{2}C BSL data signal (SDA)
BSL_CAN_RX	Required for CAN	CAN receive signal (RX), an input
BSL_CAN_TX	Required for CAN	CAN receive signal (TX), an output
BSL_INVOKE	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the *MSPM33C3x Bootloader User's Guide.*

8.19 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please refer to Factory Constants chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual* for more information.

ADVANCE INFORMATION

Table 8-24. DEVICEID

DEVICEID address is 0x8011.1004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER
MSPM33C321A, MSPM33C3219, MSPM33C322A, MSPM33C3229	0xBBBC	0x17

Table 8-25. USERID

USERID address is 0x8011.1008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	PART	VARIANT
MSPM33C321ASPZR	0x43B6	0x10
MSPM33C321ASPFAR	0x43B6	0x11
MSPM33C321ASPNR	0x43B6	0x12
MSPM33C321ASPMR	0x43B6	0x13
MSPM33C321ASRGZR	0x43B6	0x14
MSPM33C322ASPZR	0x3869	0x15
MSPM33C322ASPFAR	0x3869	0x16
MSPM33C322ASPNR	0x3869	0x17
MSPM33C322ASPMR	0x3869	0x18
MSPM33C322ASRGZR	0x3869	0x19
MSPM33C322ASZAW	0x3869	0x20
MSPM33C3219SPZR	0xC637	0x27
MSPM33C3219SPFAR	0xC637	0x28
MSPM33C3219SPNR	0xC637	0x29
MSPM33C3219SPMR	0xC637	0x30
MSPM33C3219SRGZR	0xC637	0x31
MSPM33C3229SPZR	0xEF32	0x32
MSPM33C3229SPFAR	0xEF32	0x33
MSPM33C3229SPNR	0xEF32	0x34
MSPM33C3229SPMR	0xEF32	0x35
MSPM33C3229SRGZR	0xEF32	0x36
MSPM33C3229SZAW	0xEF32	0x37

ADVANCE INFORMATION

8.20 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to Factory Constants chapter of the *MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual* for more information.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4)

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10-µF and a 0.1-µF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10-µF bulk decoupling capacitor is a recommended value for most applications, but this capacitance can be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The $\overline{\text{NRST}}$ reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor for most applications, enabling the $\overline{\text{NRST}}$ pin to be controlled by another device or a debug probe.

A 2.2-µF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

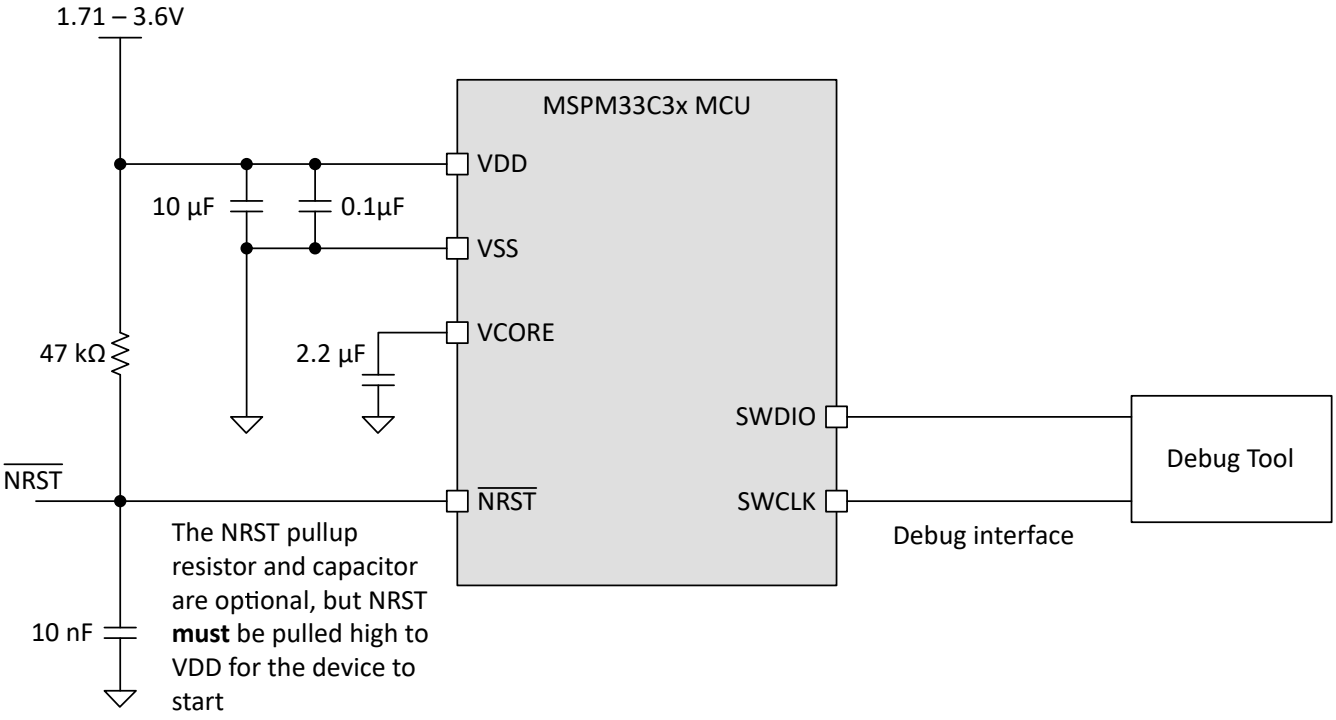


Figure 9-1. Basic Application Schematic

ADVANCE INFORMATION

ADVANCE INFORMATION

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M33 MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

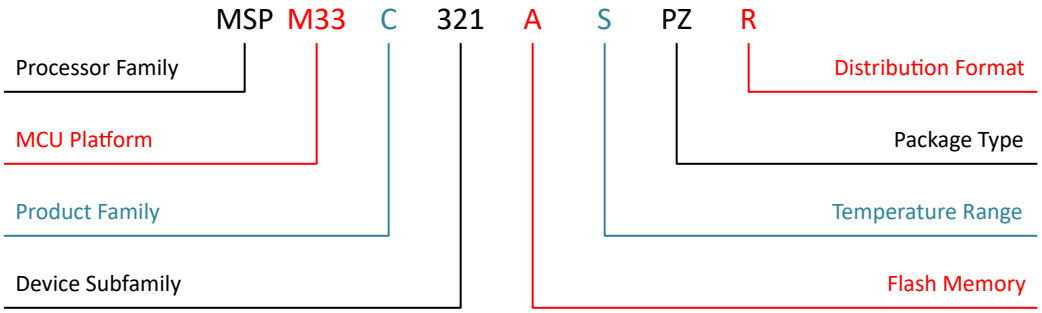


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M33 = Arm based 32-bit M33
Product Family	C = Up to 160-MHz frequency
Device Subfamily	321 = 2x CAN-FD, AES, SHA, PKA
Flash Memory	9 = 512KB A = 1024KB
Temperature Range	S = –40°C to 125°C
Package Type	See the Device Comparison section and https://www.ti.com/packaging
Distribution Format	R = Large reel

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM33 LaunchPad (LP) Boards: LP-MSPM33C321A	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM33 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/ EnergyTrace. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM33 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Developer Zone	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE ,in TI Cloud Tools or a standalone version. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™ (CCS)	Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. CCS is completely free to use and is available on Eclipse and Theia frameworks.
IAR Embedded Workbench® IDE	IAR Embedded Workbench for Arm delivers a complete development toolchain for building and debugging embedded applications for MSPM0.The included IAR C/C++ Compiler generates highly optimized code for your application, and the C-SPY Debugger is a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint.
Keil® MDK IDE	Arm Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications for MSPM0.Keil MDK includes a fully integrated debugger for source and disassembly level debugging. MDK provides full CMSIS compliance.
TI Arm-Clang	TI Arm Clang is included in the Code Composer Studio IDE.
GNU Arm Embedded Toolchain	The MSPM0 SDK supports development using the open-source Arm GNU Toolchain. Arm GCC is supported by Code Composer Studio IDE (CCS).

ADVANCE INFORMATION

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM33 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM33C3x 160-MHz Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the MSPM33C family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

Code Composer Studio™ and TI E2E™ are trademarks of Texas Instruments.
Arm®, Cortex®, and TrustZone® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

11 Revision History

DATE	REVISION	NOTES
December 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

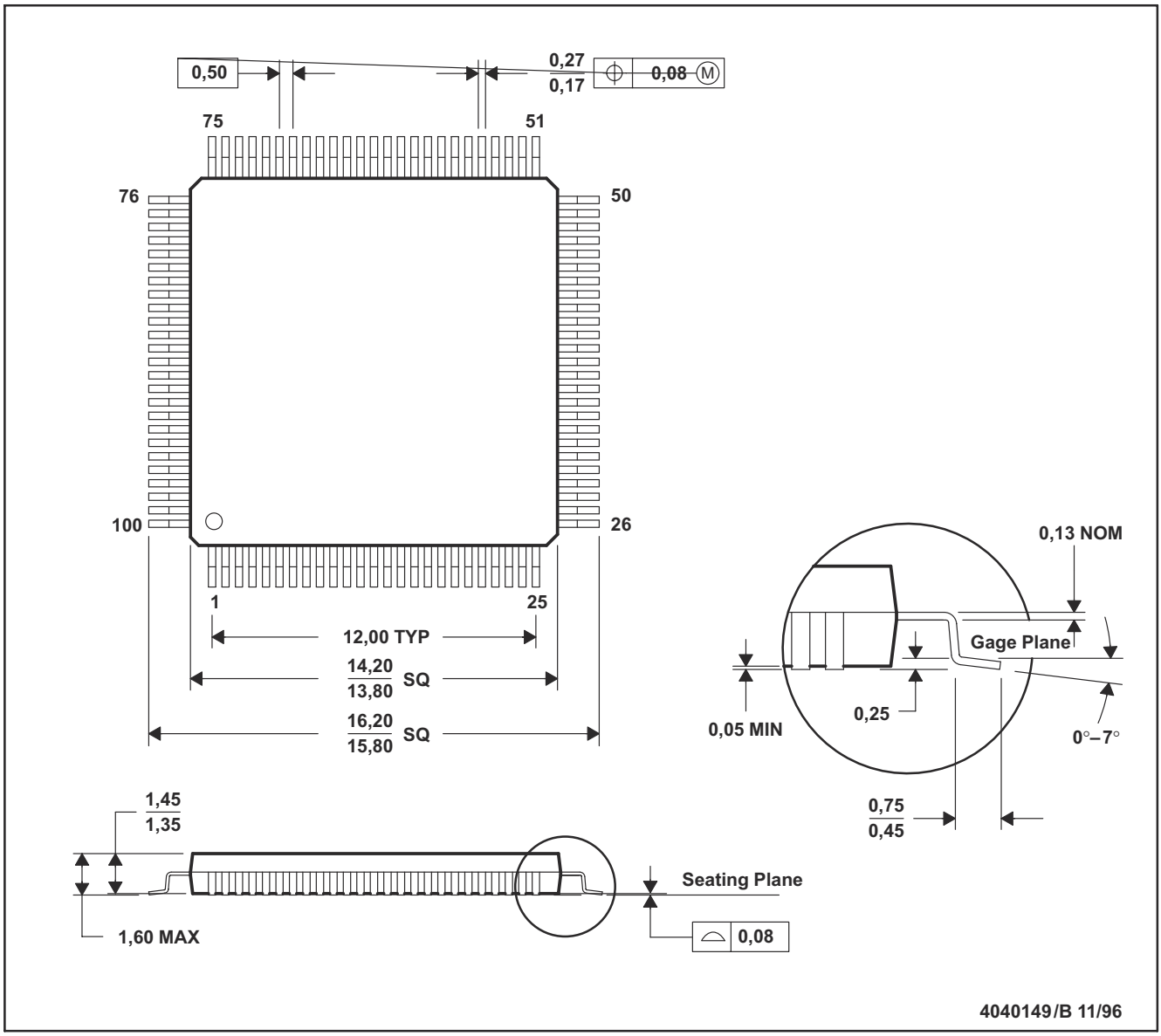
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

MECHANICAL DATA

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

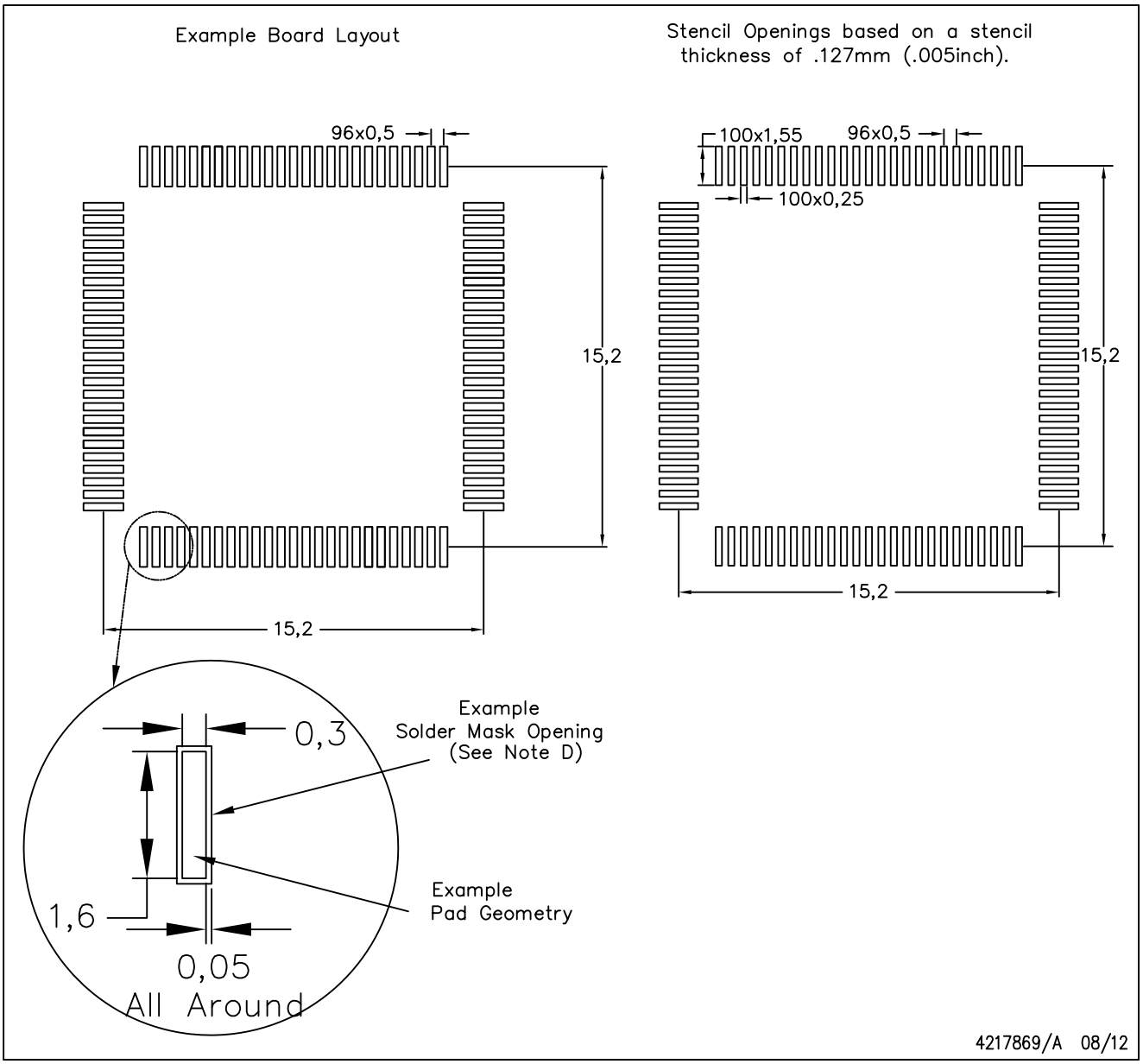
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

LAND PATTERN DATA

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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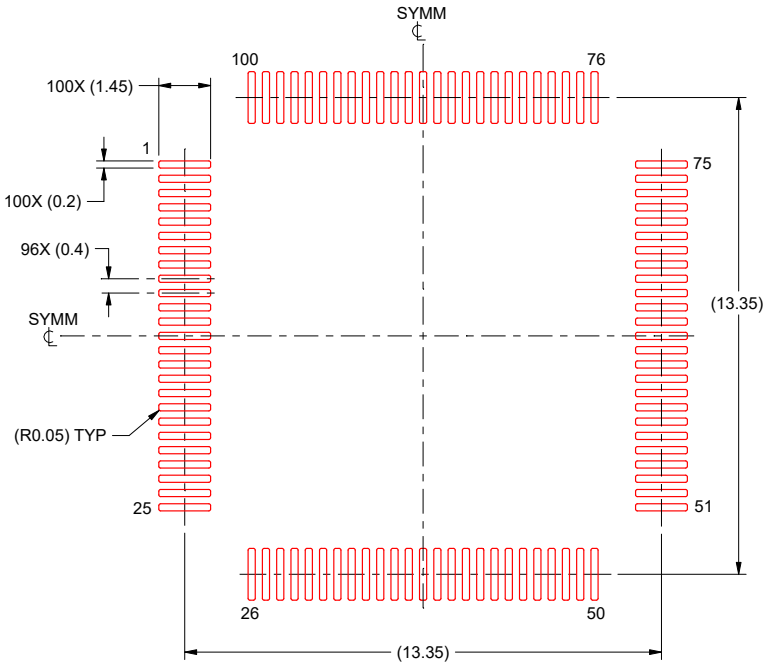
EXAMPLE STENCIL DESIGN

PFA0100A — **TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4229797/A 07/2023

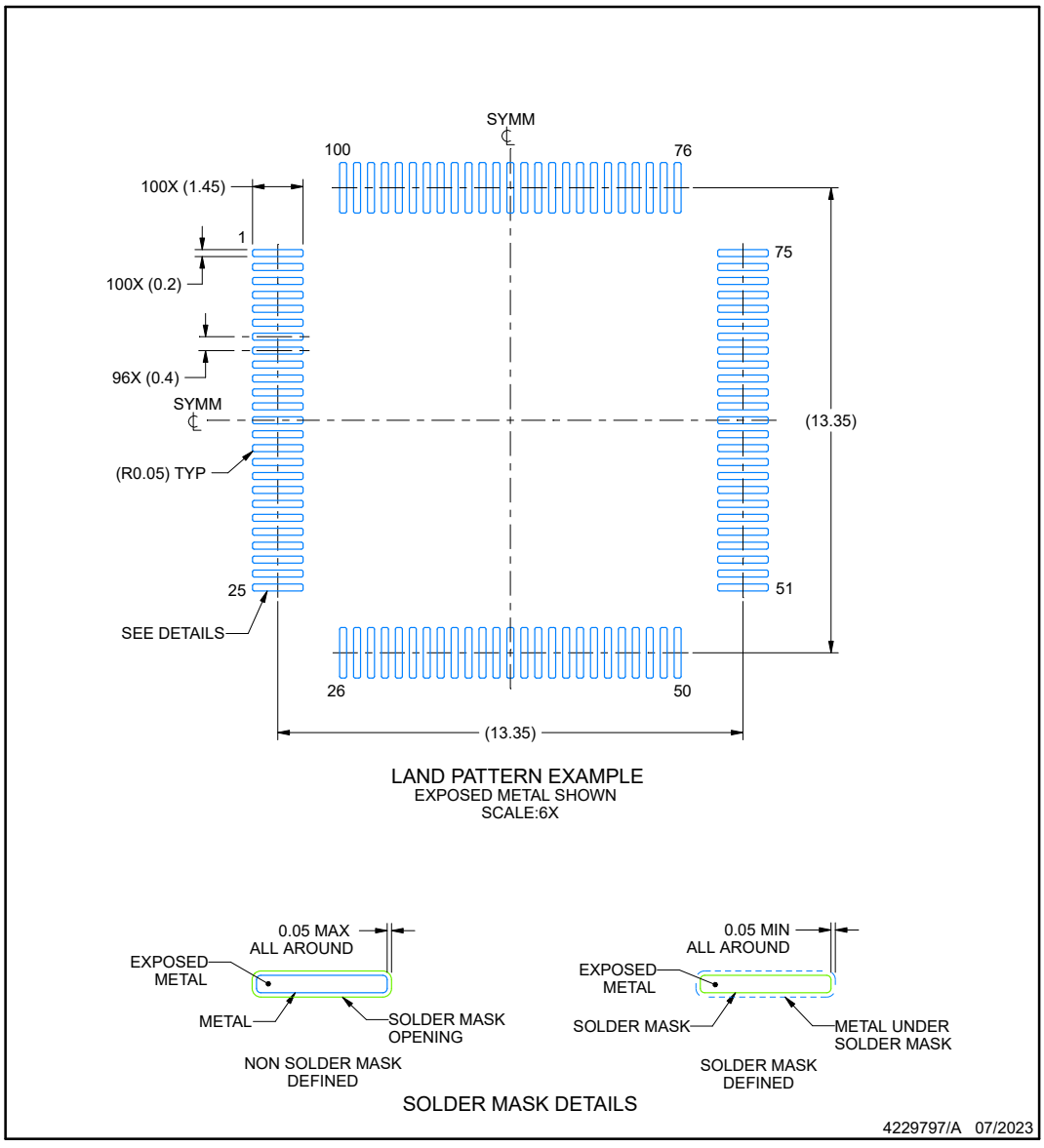
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

PFA0100A — **TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

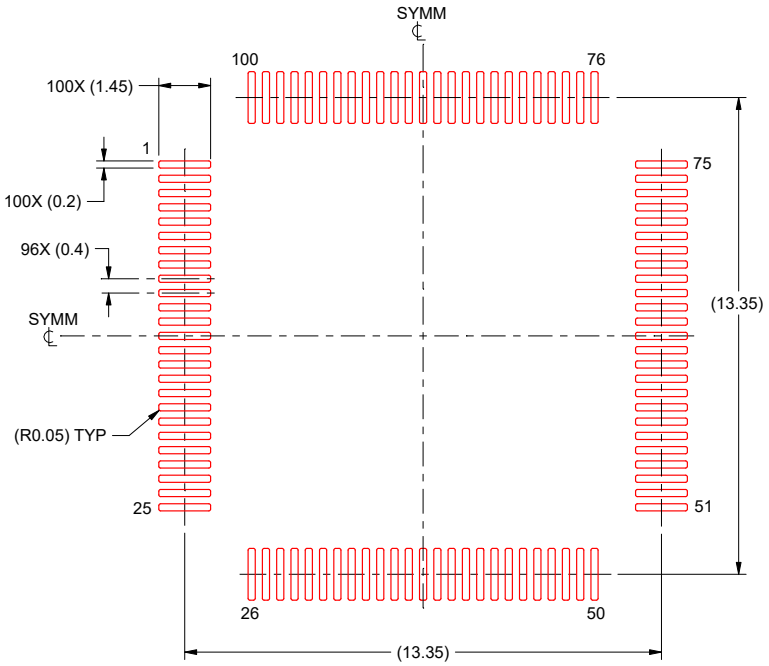
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PFA0100A — **TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK

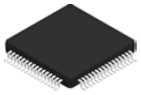


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4229797/A 07/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

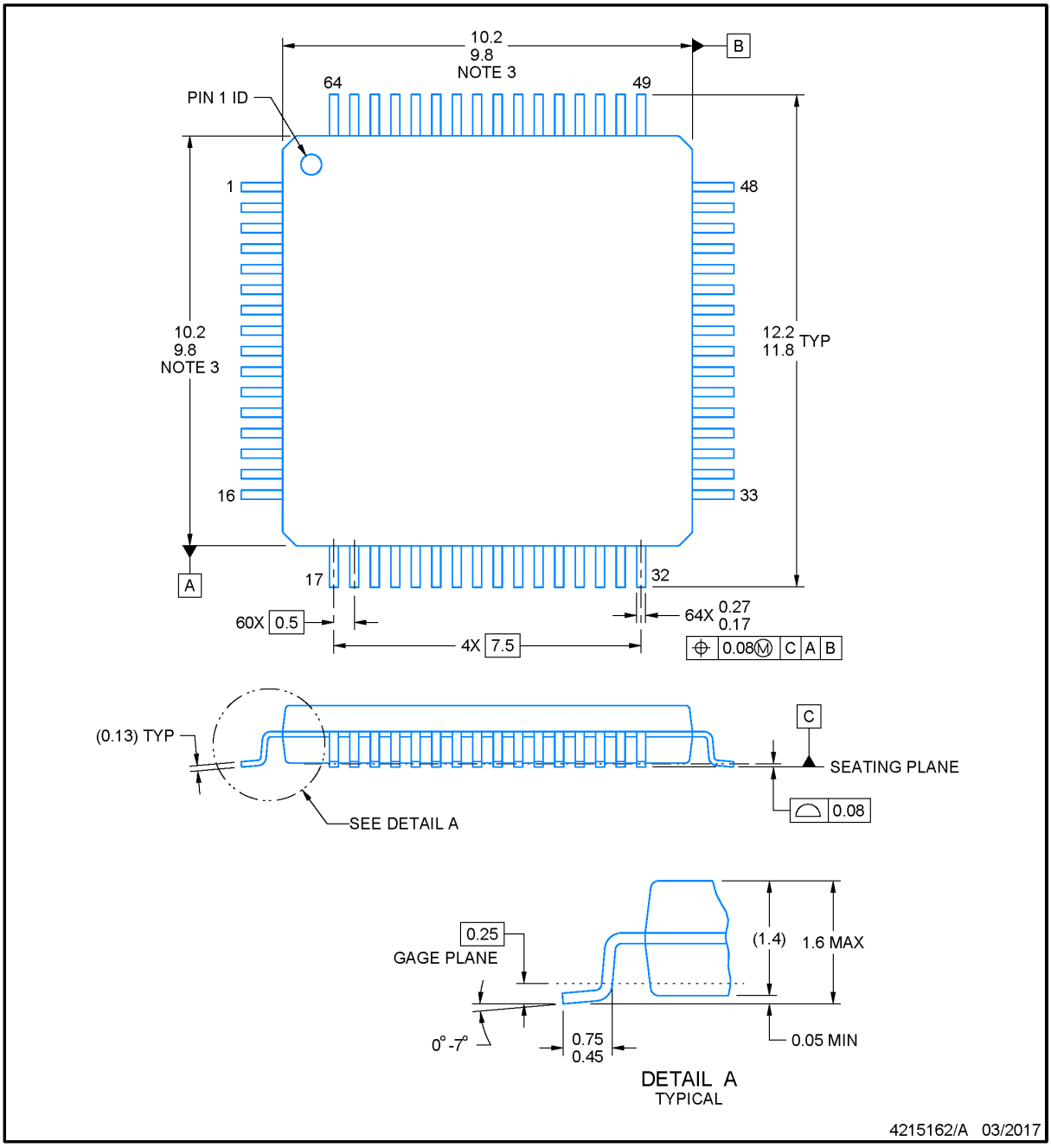


PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

ADVANCE INFORMATION

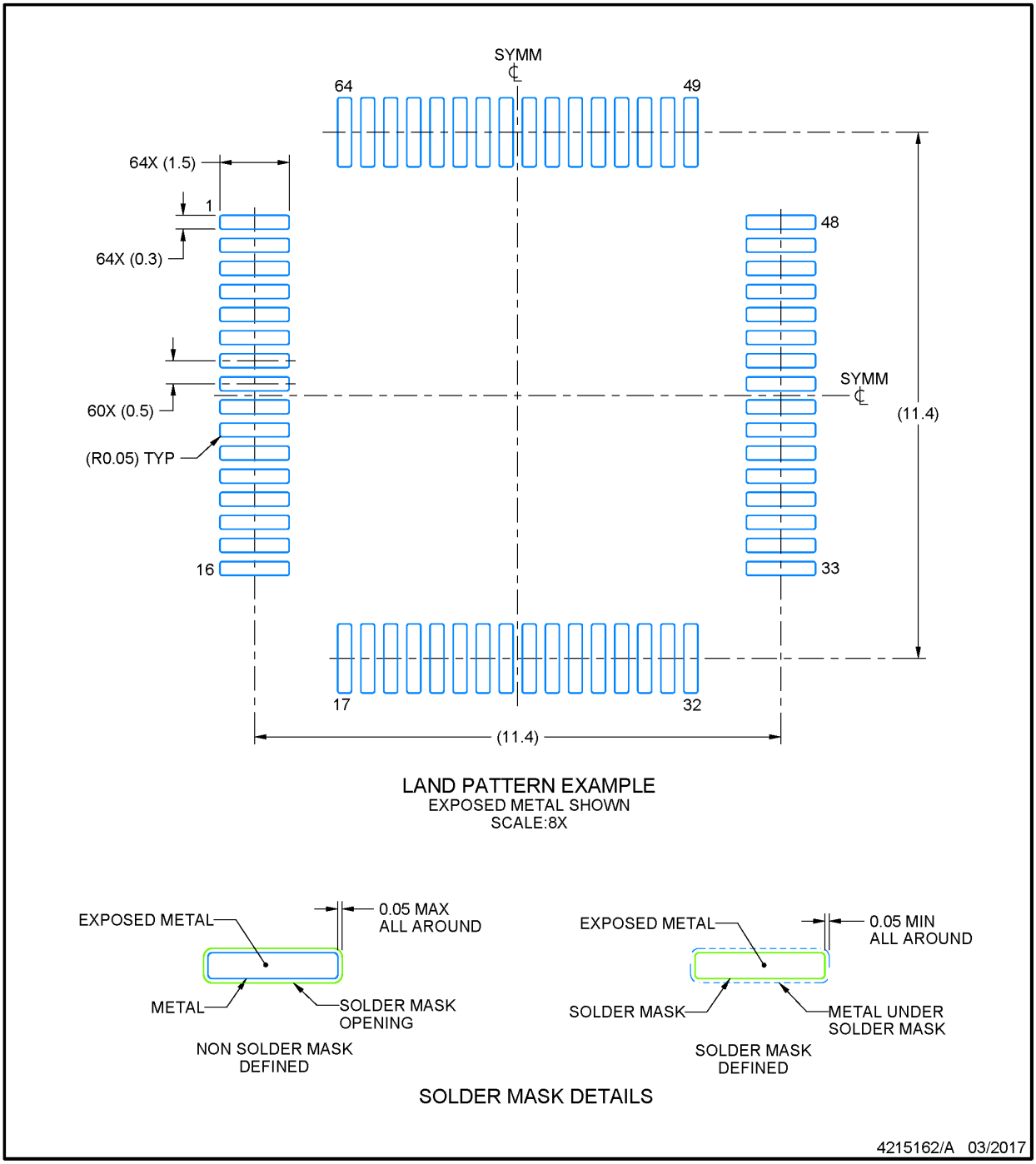
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

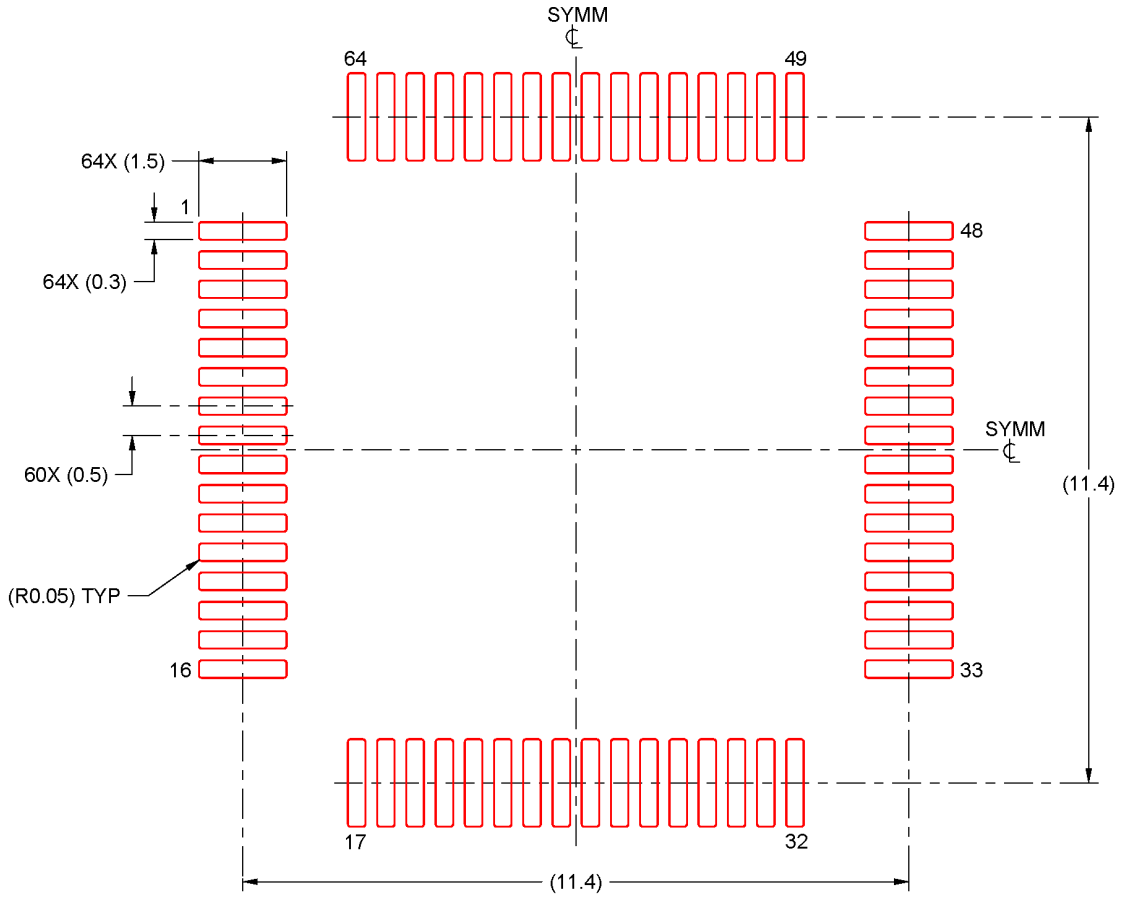
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



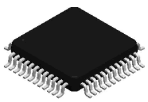
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

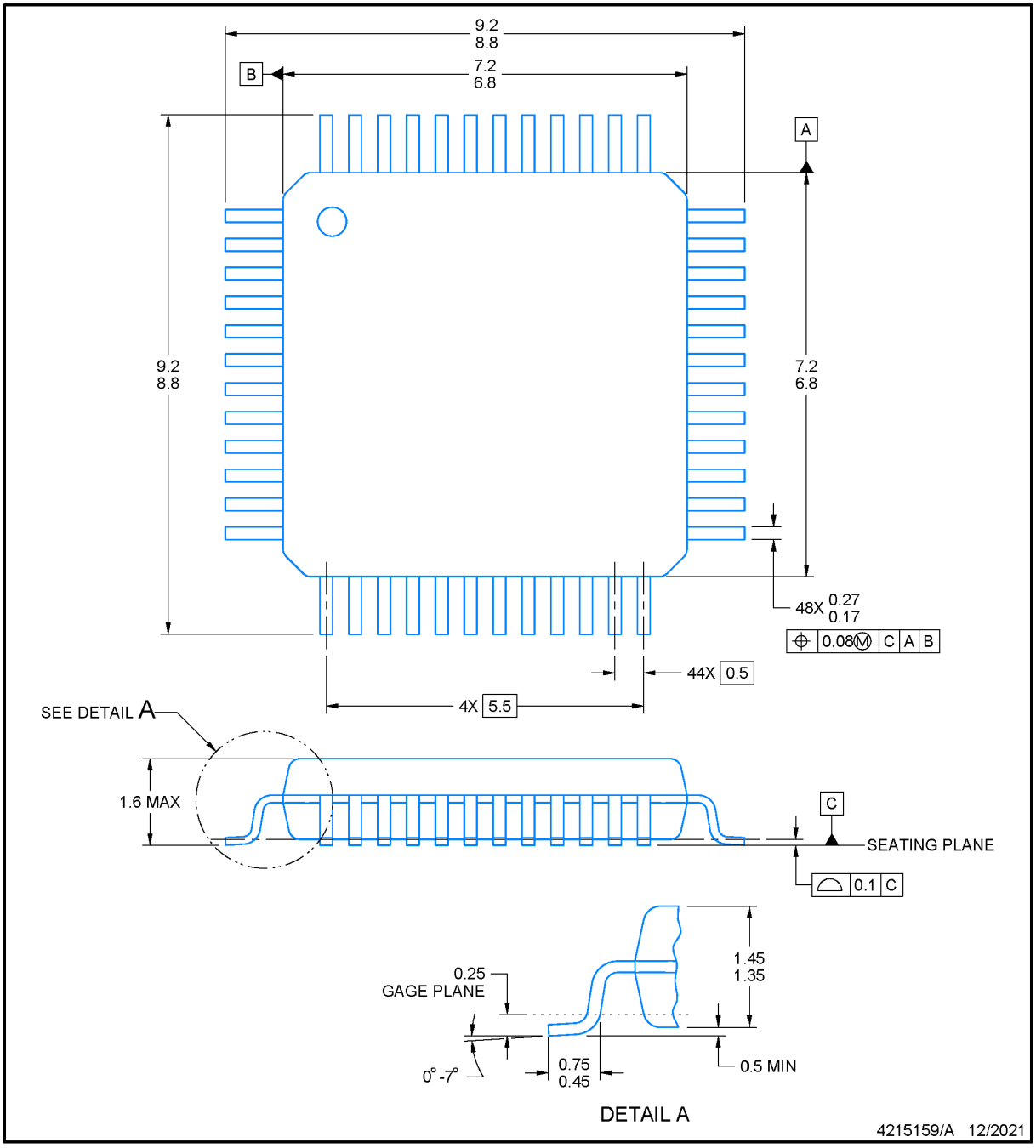


PACKAGE OUTLINE

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES:

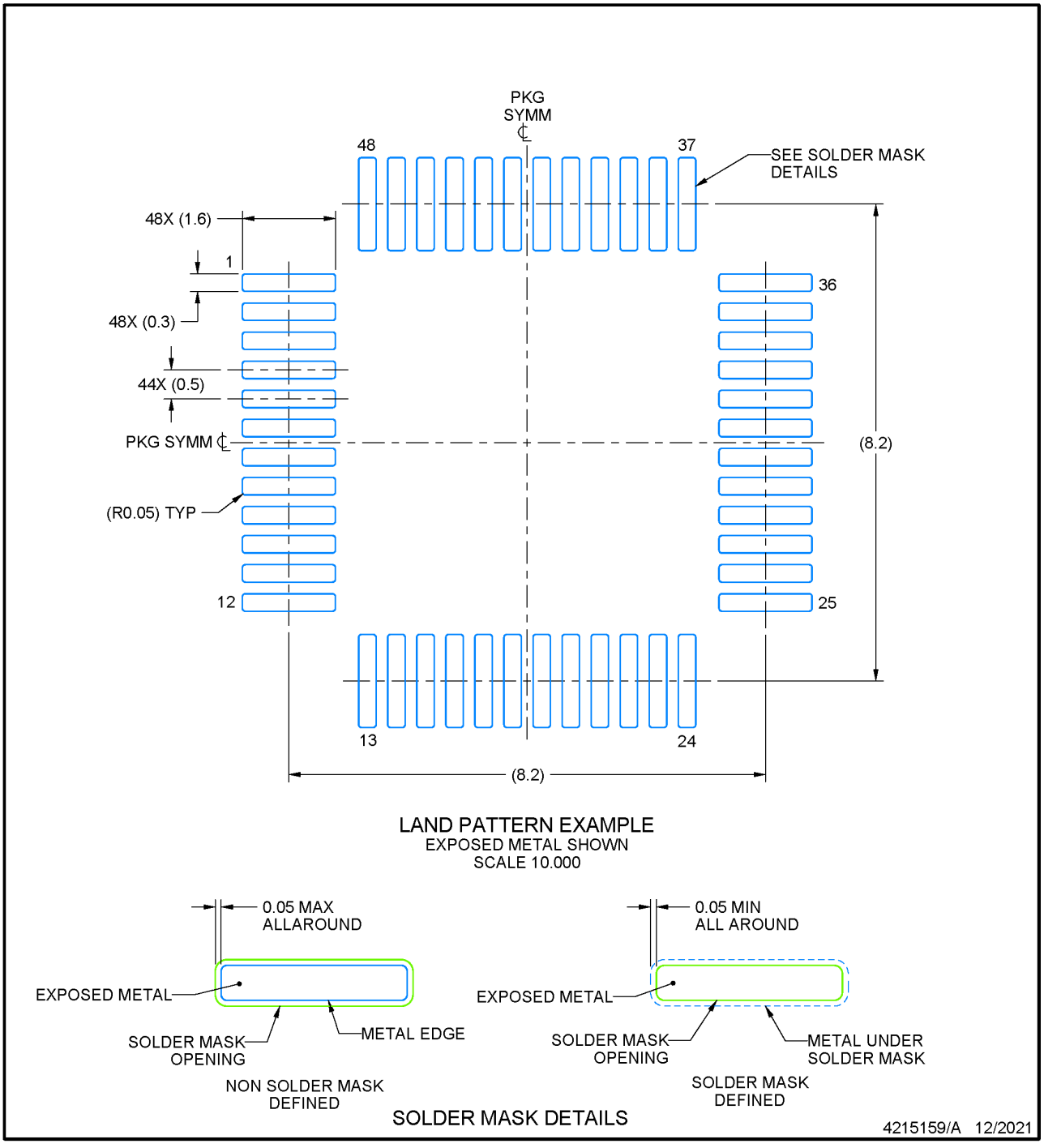
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.

EXAMPLE BOARD LAYOUT

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

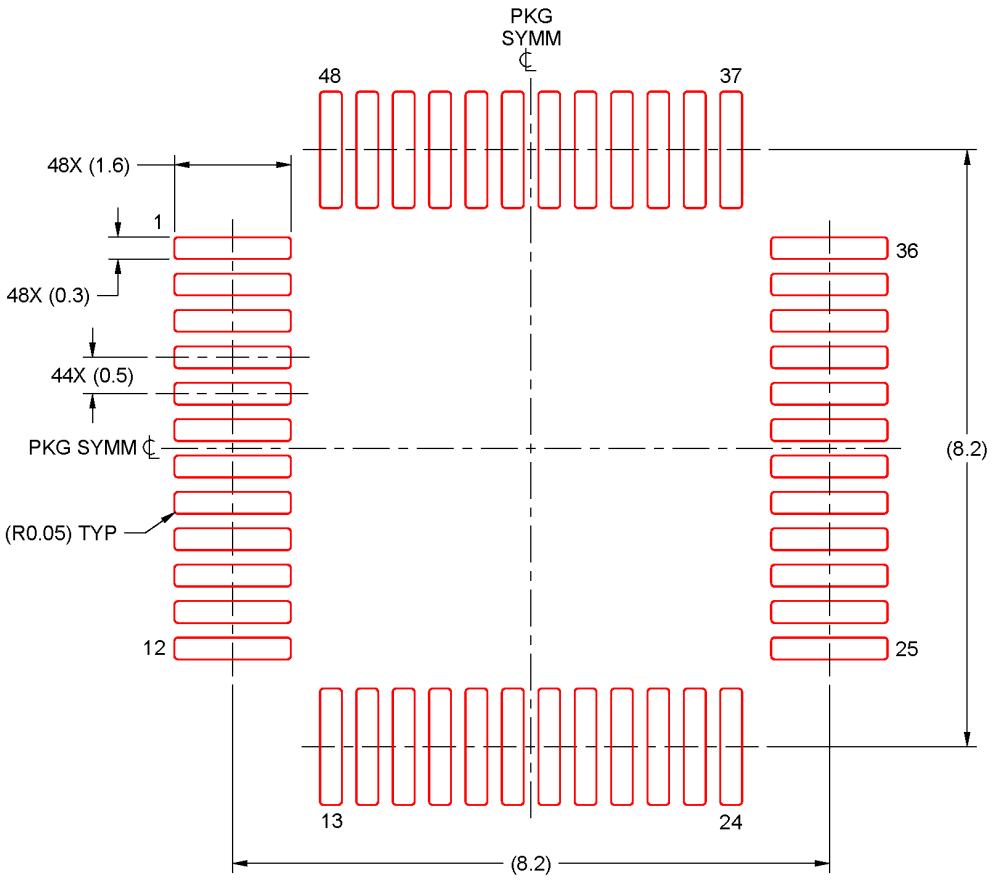
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/A 12/2021

NOTES: (continued)

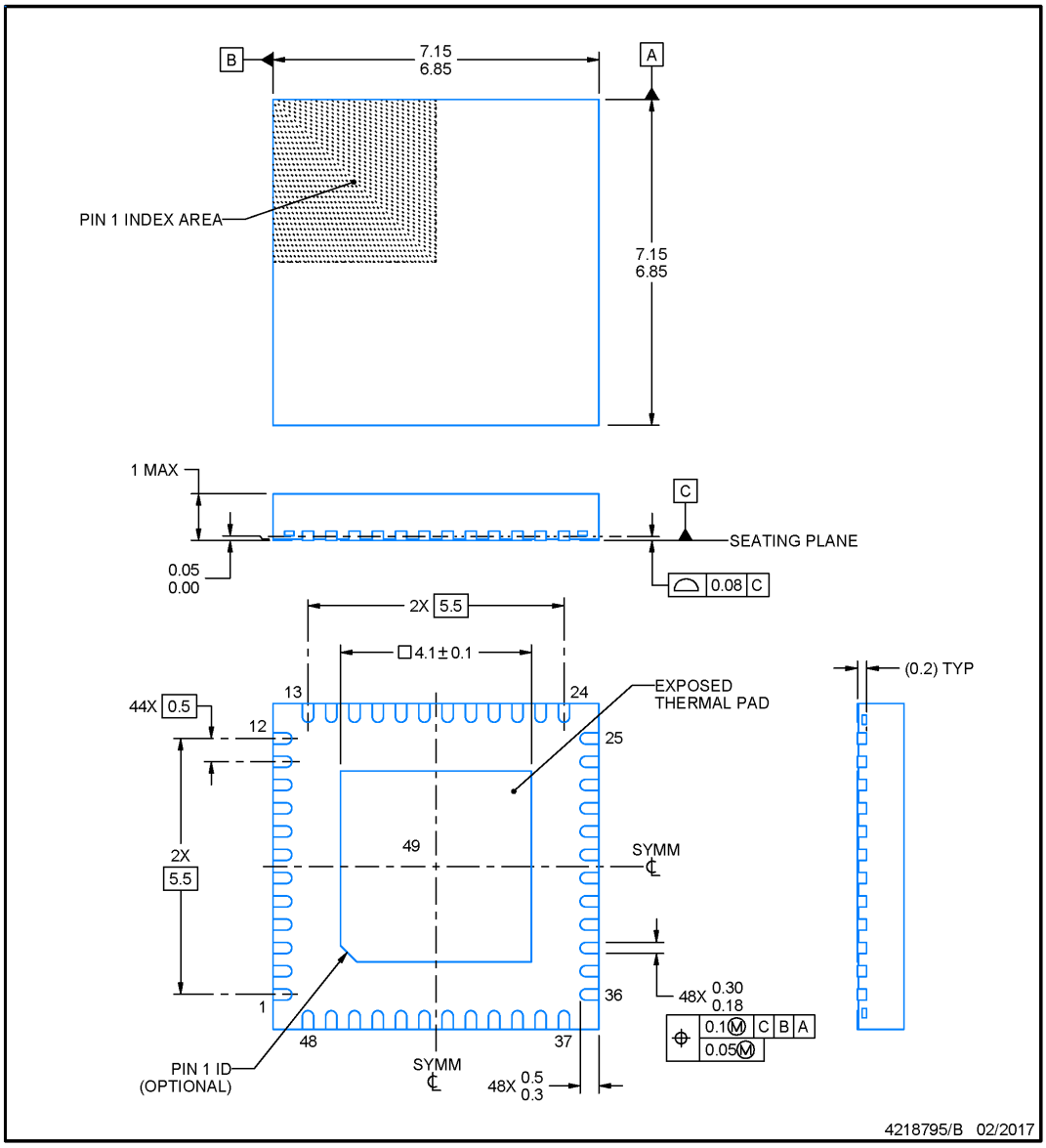
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

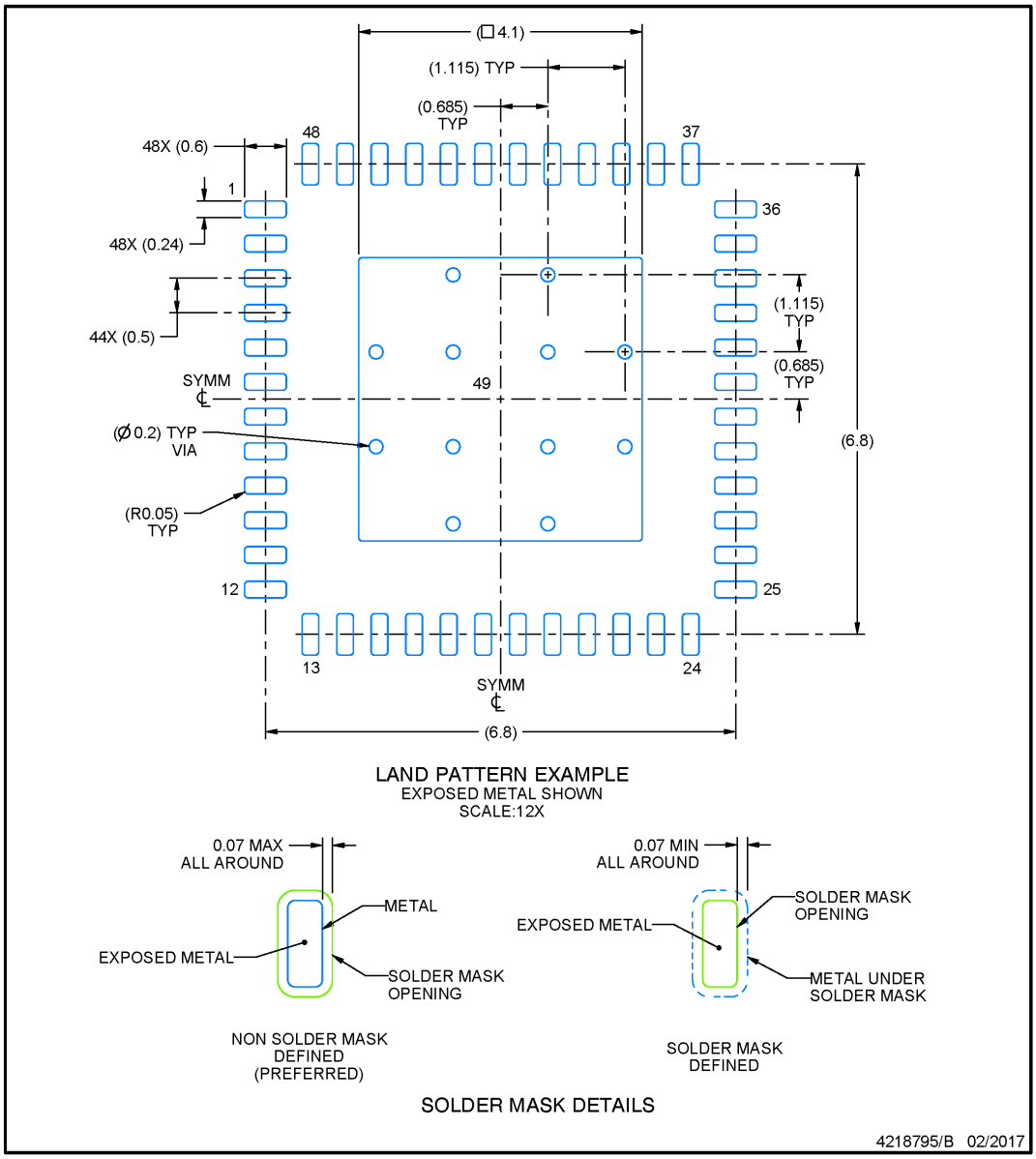
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



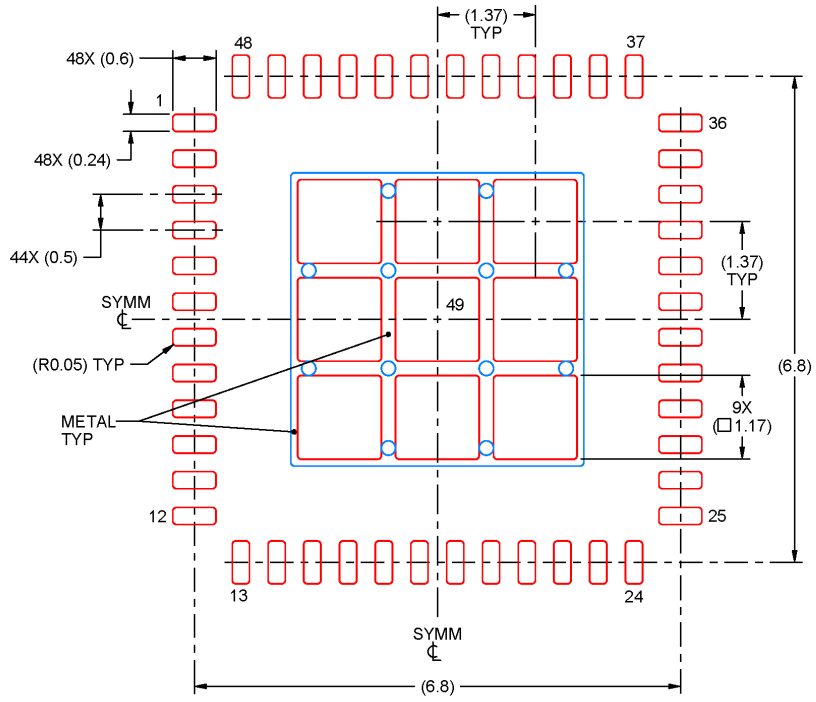
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

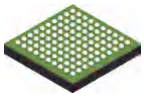
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

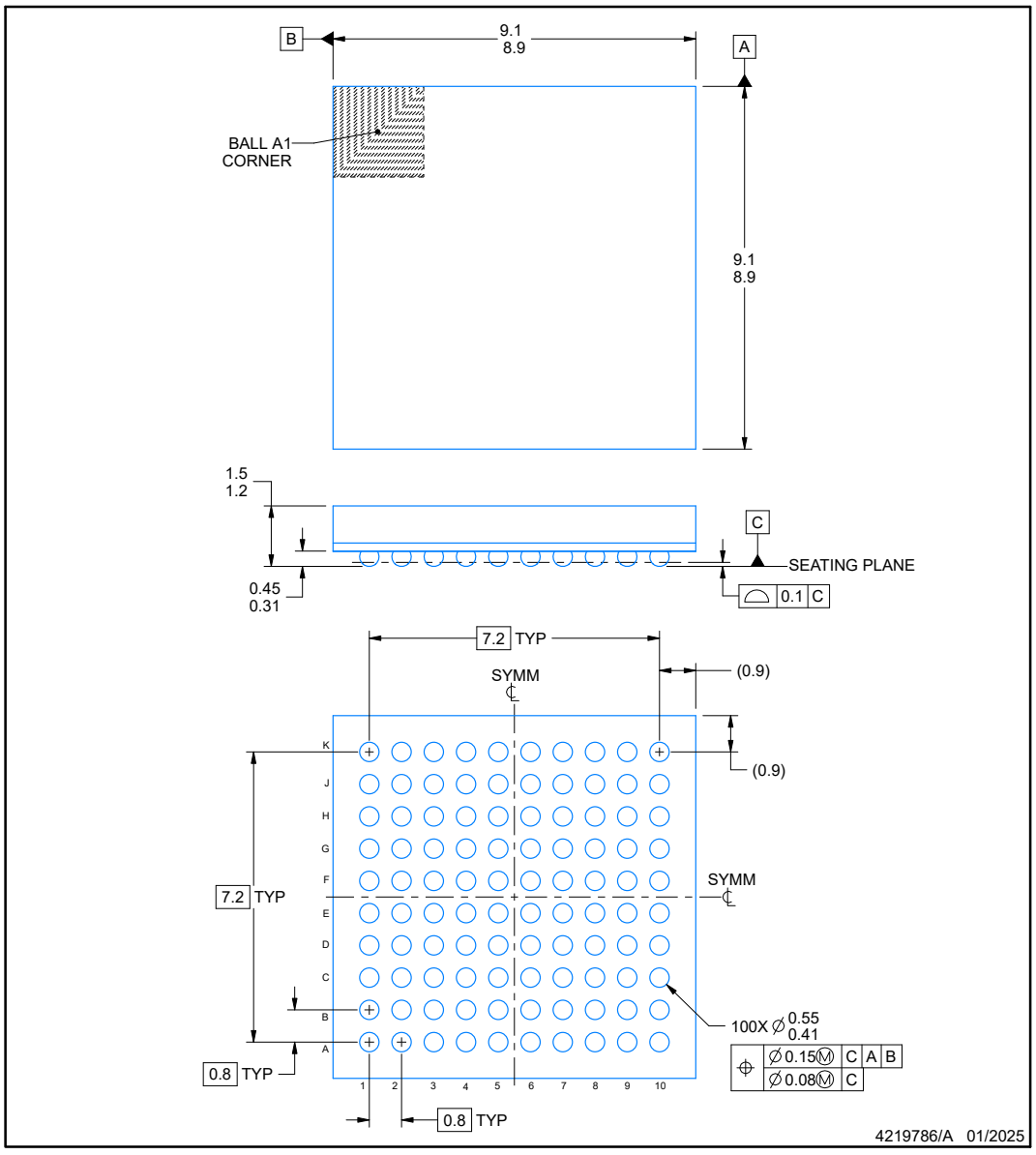
PACKAGE OUTLINE

ZAW0100A



NFBGA - 1.5 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

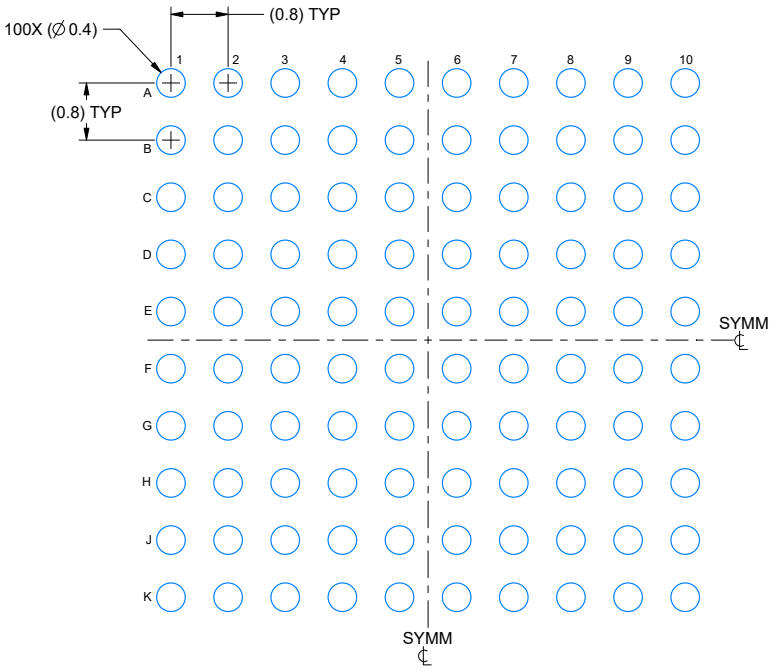
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Texas Instruments
www.ti.com

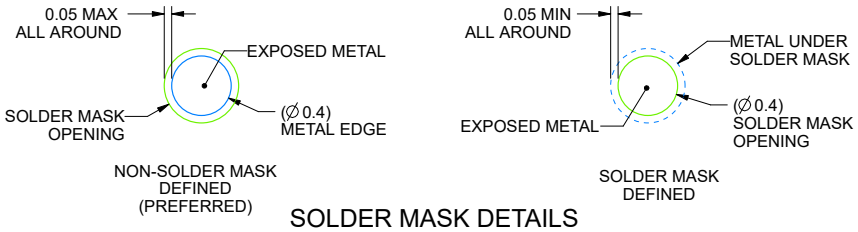
EXAMPLE BOARD LAYOUT

ZAW0100A — **NFBGA - 1.5 mm max height**

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS
NOT TO SCALE

4219786/A 01/2025

NOTES: (continued)

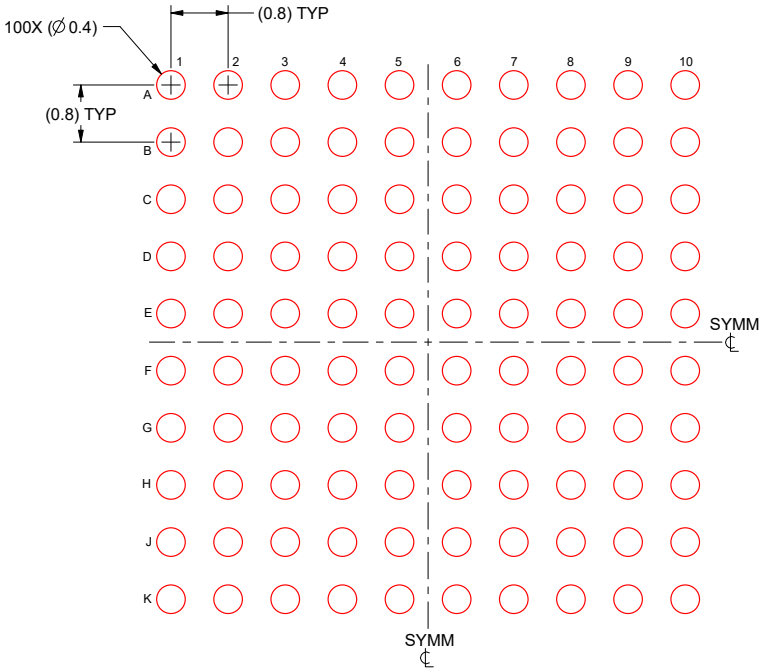
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

ZAW0100A — **NFBGA - 1.5 mm max height**

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4219786/A 01/2025

NOTES: (continued)

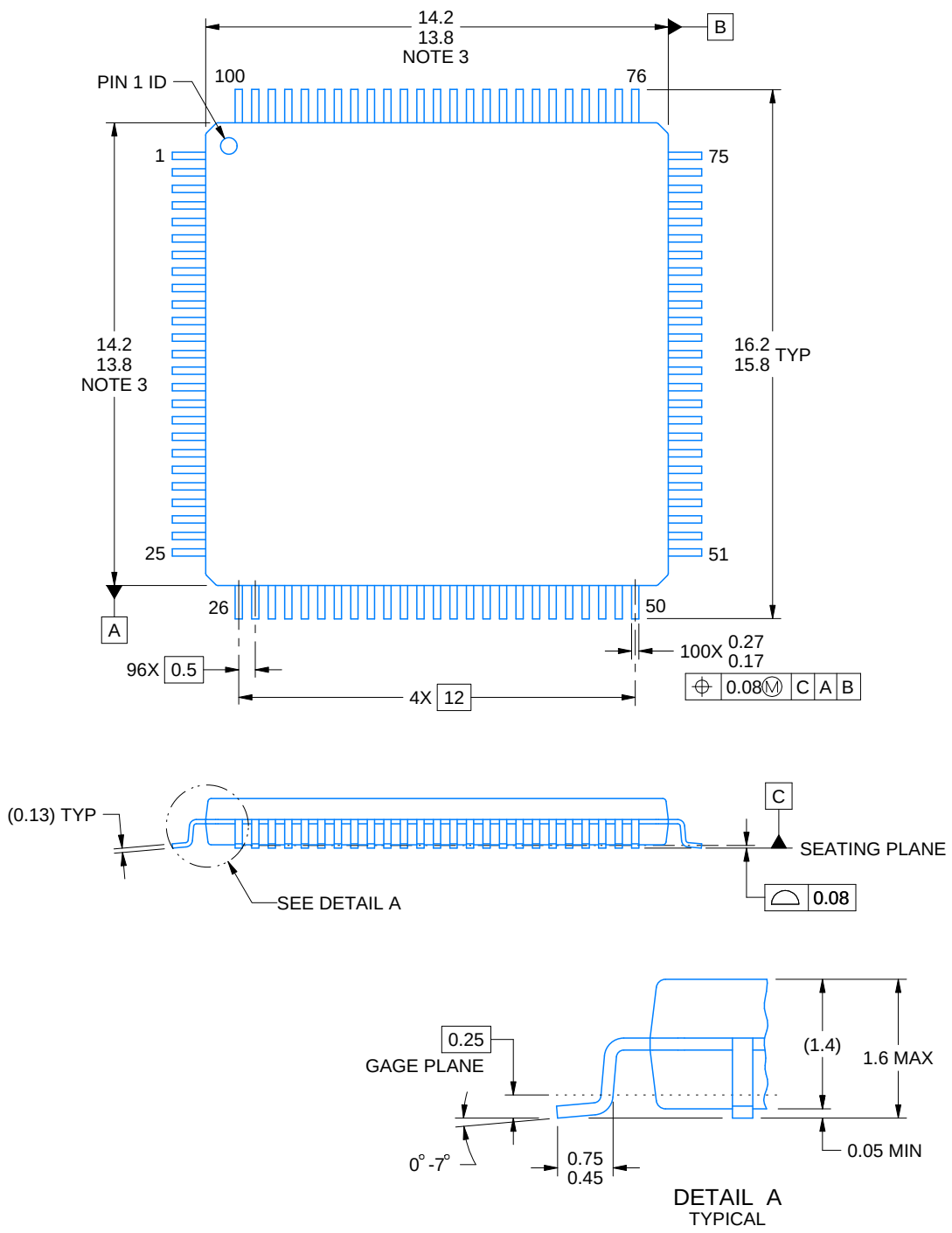
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

PZ0100A

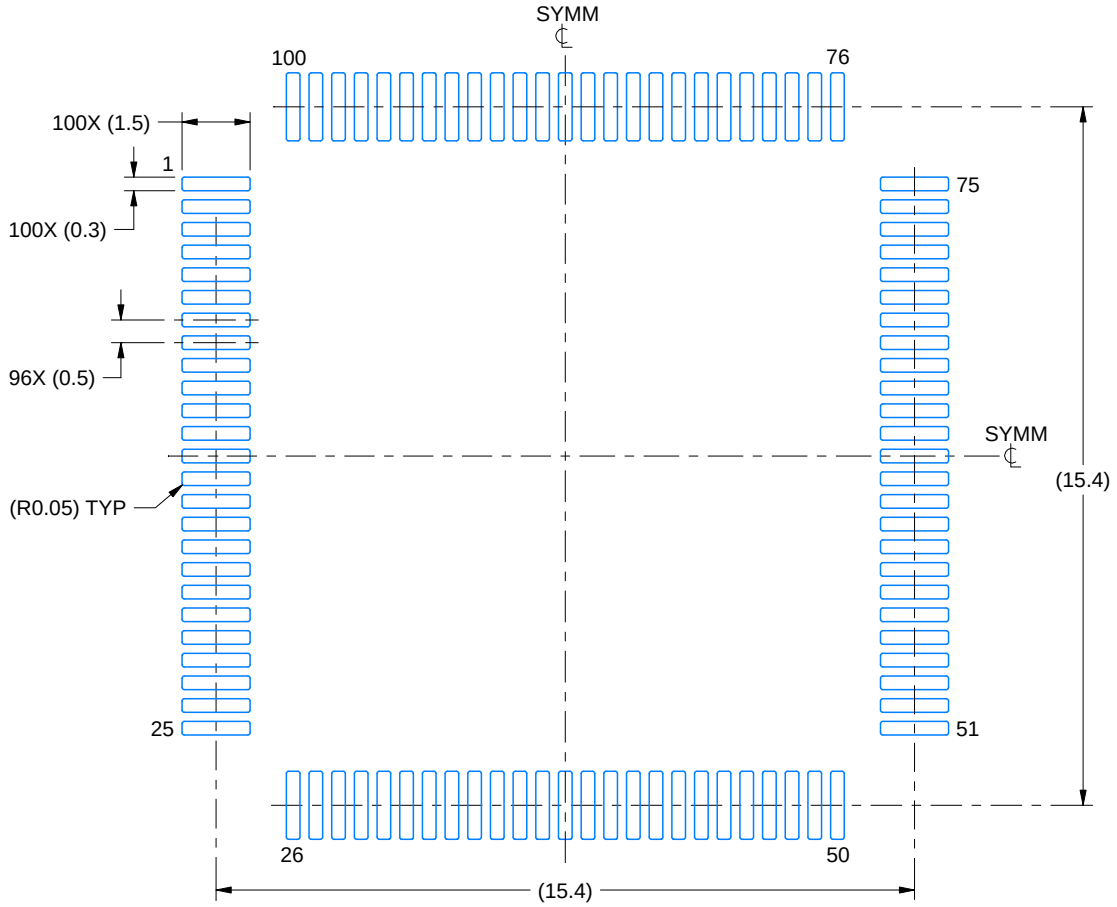
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

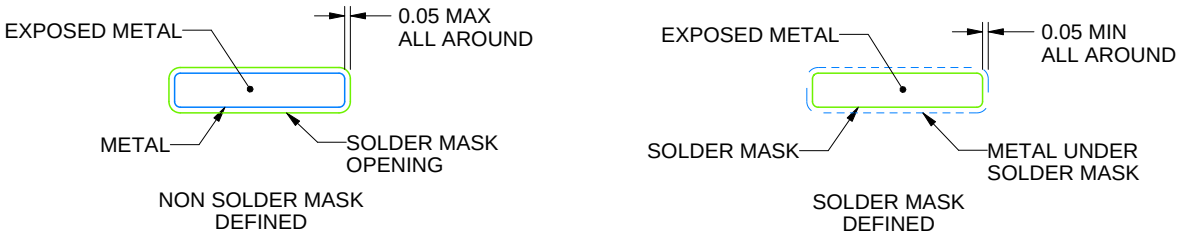


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

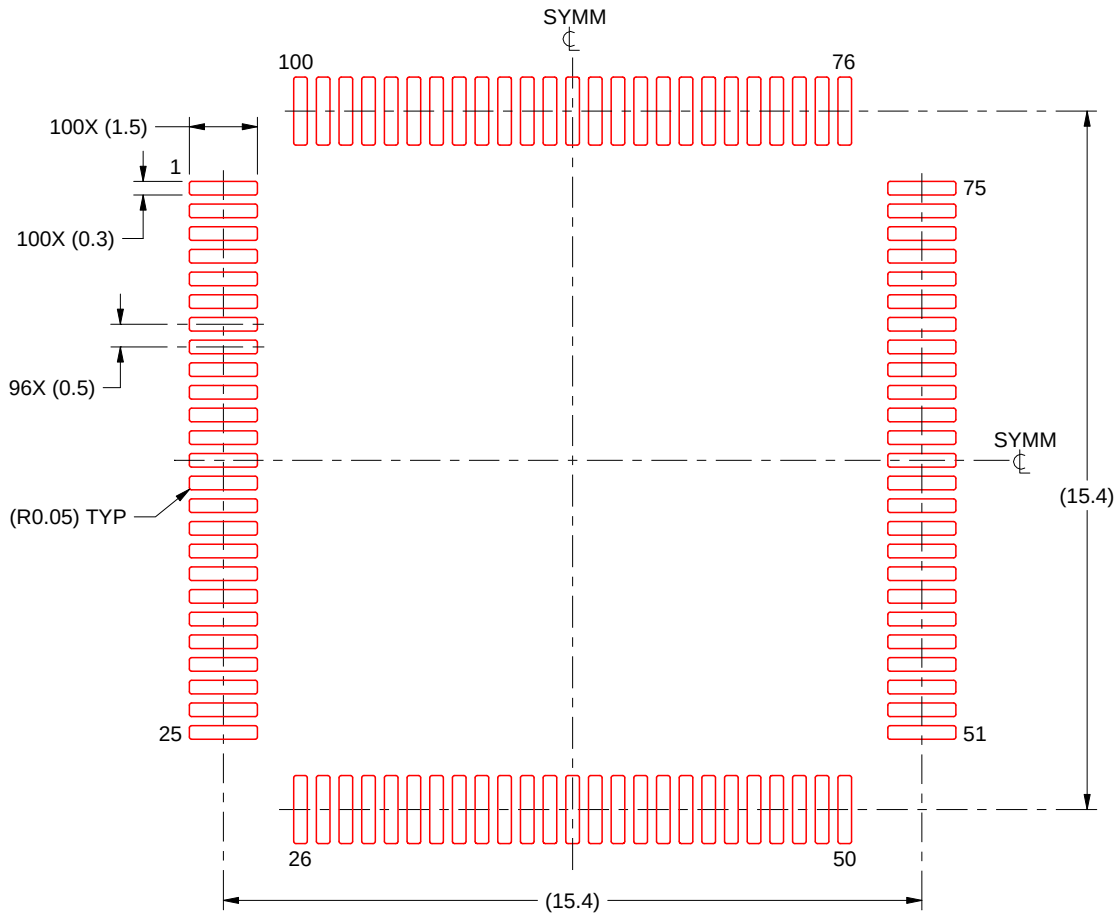


SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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