TEXAS INSTRUMENTS

OPA1641-Q1, OPA1642-Q1

SBOS791A – JUNE 2017 – REVISED NOVEMBER 2017

OPA164x-Q1 SoundPlus™ JFET-Input, Automotive-Grade, Audio Operational Amplifiers

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Low Noise: 5.1 nV/√Hz at 1 kHz
- Ultra-low Distortion: 0.00005% at 1 kHz
- High Slew Rate: 20 V/µs
- Unity Gain Stable
- No Phase Reversal
- Low Quiescent Current: 1.8 mA per Channel
- Rail-to-Rail Output
- Wide Supply Range: ±2.25 V to ±18 V
- Single, Dual, and Quad Versions Available

2 Applications

- Automotive
- HEV and EV Power Train
- Advanced Driver Assist (ADAS)
- Infotainment Systems
- In-Cabin Microphones

3 Description

The OPA1641-Q1 (single) and OPA1642-Q1 (dual) series are JFET-input, ultra-low distortion, low-noise operational amplifiers (op amps) fully specified for audio applications.

The rail-to-rail output swing allows increased headroom, making these devices ideal for use in any audio circuit. Features include 5.1-nV/√Hz noise, low total harmonic distortion + noise (THD+N) (0.00005%), a low input bias current of 2 pA, and low quiescent current of 1.8 mA per channel.

These devices operate over a very wide supply voltage range of ±2.25 V to ±18 V. The OPA164x-Q1 series of operational amplifiers are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

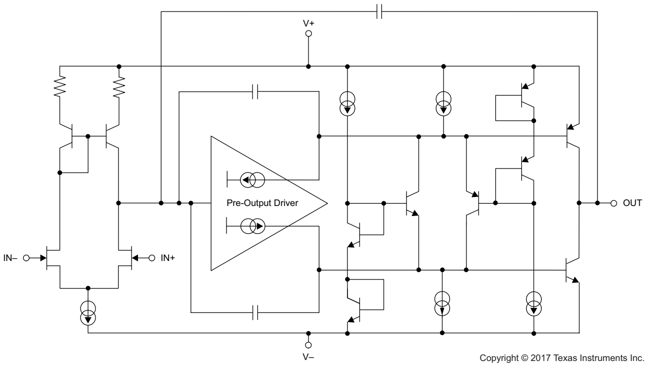
The dual version features completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1641-Q1	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA1642-Q1	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Internal Schematic



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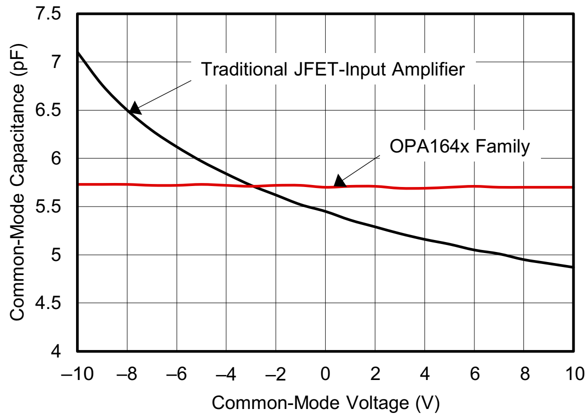
Extremely Stable Input Capacitance



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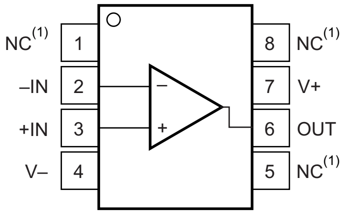
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2017) to Revision A	Page
• Added separate A_{OL} values for OPA1642-Q1	6

5 Pin Configuration and Functions

OPA1641-Q1: D and DGK Packages
8-Pin SOIC and VSSOP
Top View

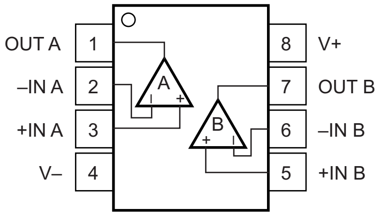


(1) NC - no internal connection

Pin Functions: OPA1641-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	2	I	Inverting input
+IN	3	I	Noninverting input
NC	1, 5, 8	—	No connection
OUT	6	O	Output
V–	4	—	Negative (lowest) power supply
V+	7	—	Positive (highest) power supply

OPA1642-Q1: D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Pin Functions: OPA1642-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		40	V
V_{IN}	Input voltage(2)	(V–) – 0.5	(V+) + 0.5	V
I_{IN}	Input current(2)		±10	mA
$V_{IN(DIFF)}$	Differential input voltage		±VS	V
I_O	Output short-circuit(3)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature	–65	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less. The input voltage and output negative-voltage ratings can be exceeded if the input and output current ratings are followed.

(3) Short-circuit to V_S / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±3000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (V+, V–)	Single supply	4.5		36	V
	Dual supply	±2.25		±18	
Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA1641-Q1, OPA1642-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9	n/a	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = 4.5 V to 36 (±2.25 V to ±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}		0.00005%		
				–126		dB
IMD	Intermodulation distortion	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz), G = 1, V_O = 3 V_{RMS}		0.00004%		
				–128		dB
		DIM 30 (3-kHz square wave and 15-kHz sine wave), G = 1, V_O = 3 V_{RMS}		0.00008%		
				–122		dB
		CCIF twin-tone (19 kHz and 20 kHz), G = 1, V_O = 3 V_{RMS}		0.00007%		
				–123		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1		11		MHz
SR	Slew rate	G = 1		20		V/µs
	Full-power bandwidth(1)	V_O = 1 V_P		3.2		MHz
	Overload recovery time(2)	G = –10		600		ns
	Channel separation (dual and quad)	f = 1 kHz		–126		dB
NOISE						
	Input voltage noise	f = 20 Hz to 20 kHz		4.3		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz		8		nV/√Hz
		f = 100 Hz		5.8		
		f = 1 kHz		5.1		
I_n	Input current noise density	f = 1 kHz		0.8		fA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±18 V		1	3.5	mV
PSRR	V_{OS} vs power supply	V_S = ±2.25 V to ±18 V		0.14	2	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±2	±20	pA
I_{OS}	Input offset current	V_{CM} = 0 V		±2	±20	pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V, V_S = ±18 V	120	126		dB
INPUT IMPEDANCE						
	Differential			10^{13} || 8		Ω || pF
	Common-mode	V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V		10^{13} || 6		Ω || pF

(1) Full power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) See Figure 19 and Figure 20.

Electrical Characteristics (continued)

at T_A = 25°C, V_S = 4.5 V to 36 (±2.25 V to ±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	OPA1641-Q1: (V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ	120	134		dB
		OPA1641-Q1: (V–) + 0.35 V ≤ V_O ≤ (V+) – 0.35 V, R_L = 2 kΩ	114	126		
		OPA1642-Q1: (V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ	114	134		
		OPA1642-Q1: (V–) + 0.35 V ≤ V_O ≤ (V+) – 0.35 V, R_L = 2 kΩ	111	126		
OUTPUT						
V_O	Voltage output swing from rail	R_L = 10 kΩ, A_{OL} ≥ 120 dB (OPA1641-Q1) A_{OL} ≥ 114 dB (OPA1642-Q1)	(V–) + 0.2		(V+) – 0.2	V
		R_L = 2 kΩ, A_{OL} ≥ 114 dB (OPA1641-Q1) A_{OL} ≥ 111 dB (OPA1642-Q1)	(V–) + 0.35		(V+) – 0.35	
I_{OUT}	Output current			See *Typical Characteristics*		
Z_O	Open-loop output impedance			See *Typical Characteristics*		
I_{SC}	Short-circuit current	Source		36		mA
		Sink		–30		
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current (per amplifier)	I_{OUT} = 0 A		1.8	2.3	mA
TEMPERATURE RANGE						
	Specified range		–40		125	°C
	Operating range		–55		125	°C

6.6 Typical Characteristics

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

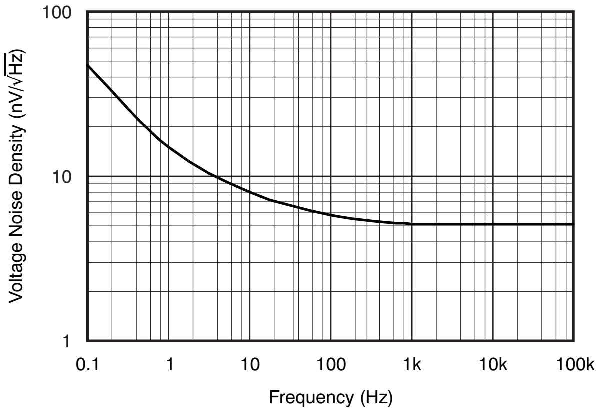


Figure 1. Input Voltage Noise Density vs Frequency

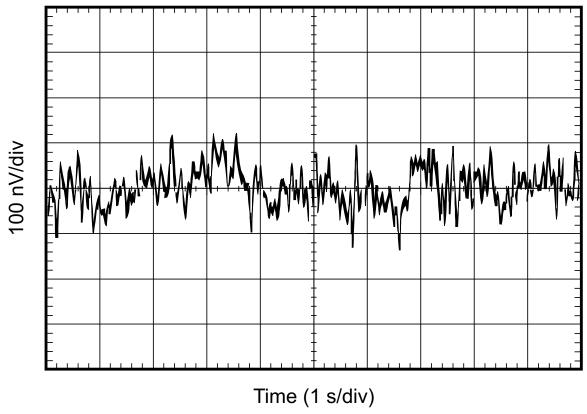


Figure 2. 0.1-Hz to 10-Hz Noise

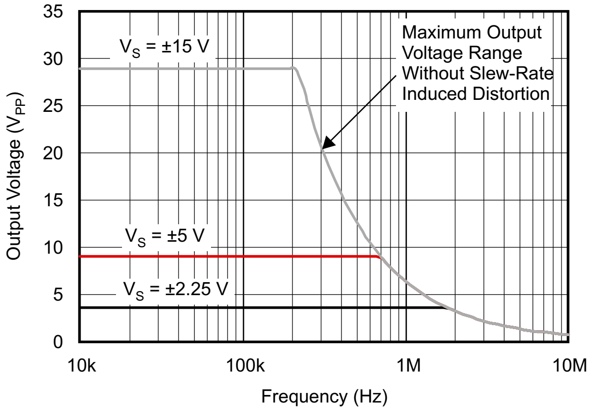


Figure 3. Maximum Output Voltage vs Frequency

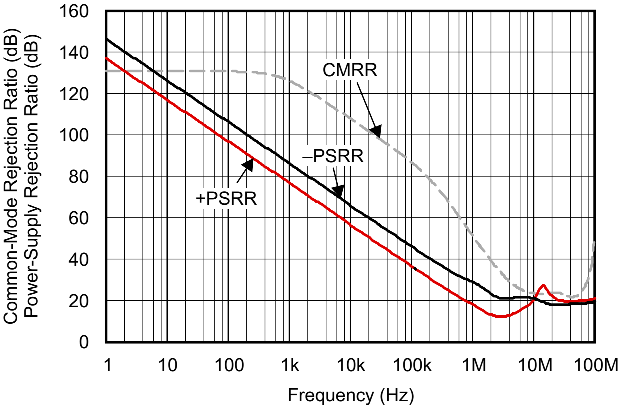


Figure 4. CMRR and PSRR vs Frequency (Referred to Input)

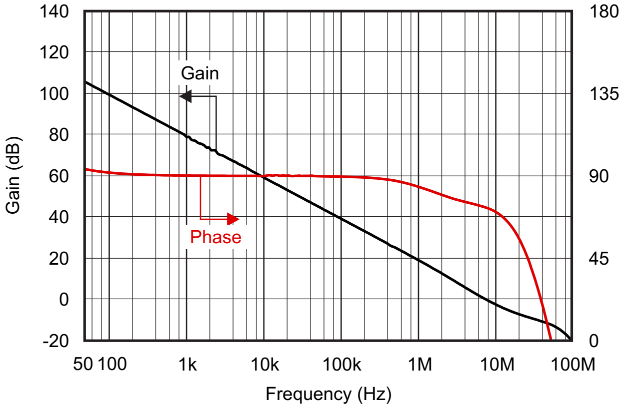


Figure 5. Gain and Phase vs Frequency

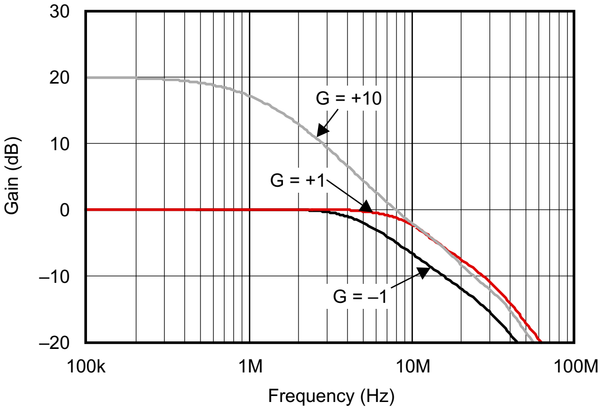
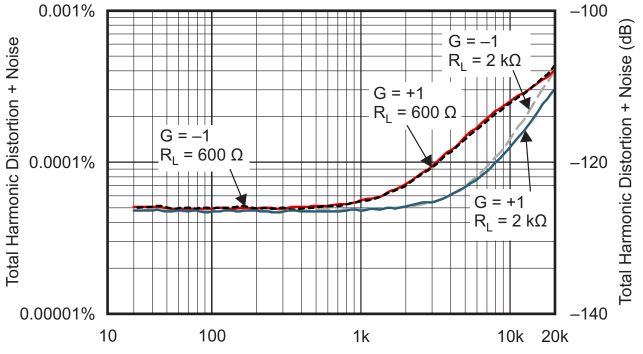


Figure 6. Closed-Loop Gain vs Frequency

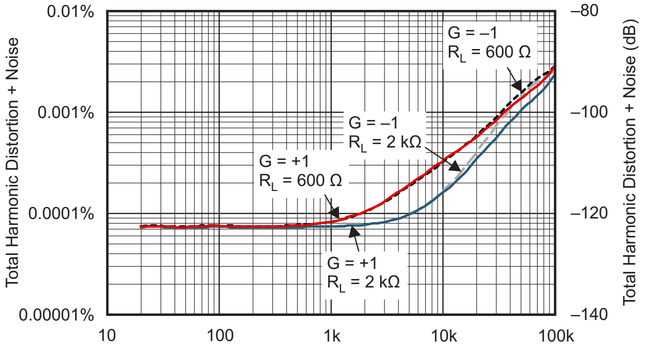
Typical Characteristics (continued)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



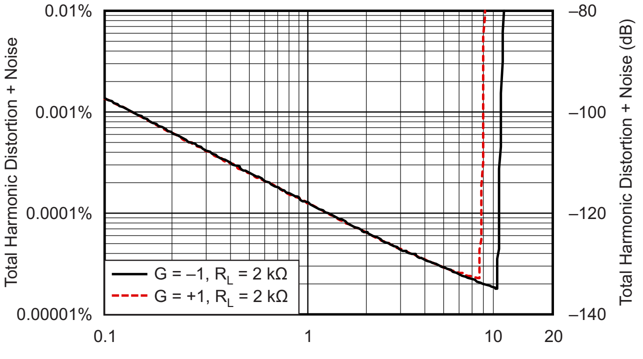
VOUT = 3 V_{RMS} BW = 80 kHz

Figure 7. THD+N Ratio vs Frequency



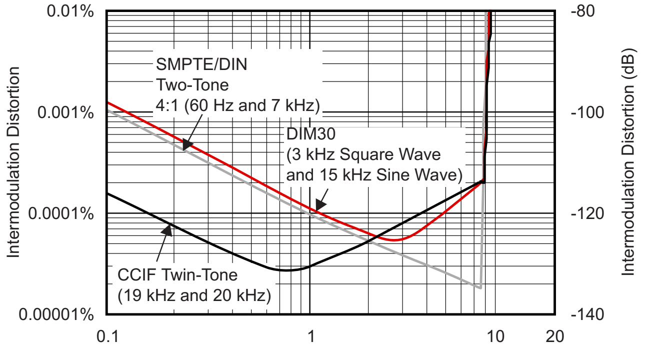
VOUT = 3 V_{RMS} BW > 500 kHz

Figure 8. THD+N Ratio vs Frequency



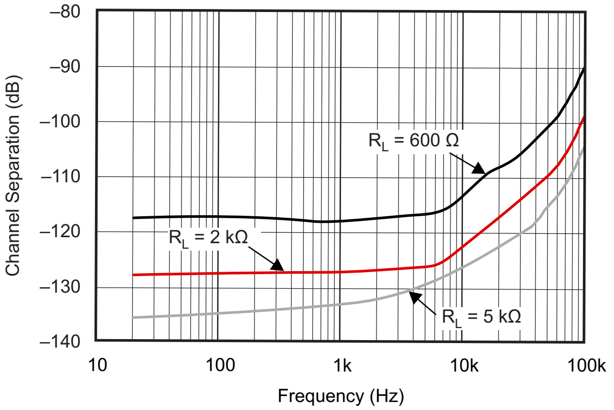
BW = 80 kHz 1 kHz Signal R_{SOURCE} = 0 Ω

Figure 9. THD+N Ratio vs Output Amplitude



G = 1

Figure 10. Intermodulation Distortion vs Output Amplitude



V_S = ±15 V V_{OUT} = 3 V_{RMS} G = 1

Figure 11. Channel Separation vs Frequency

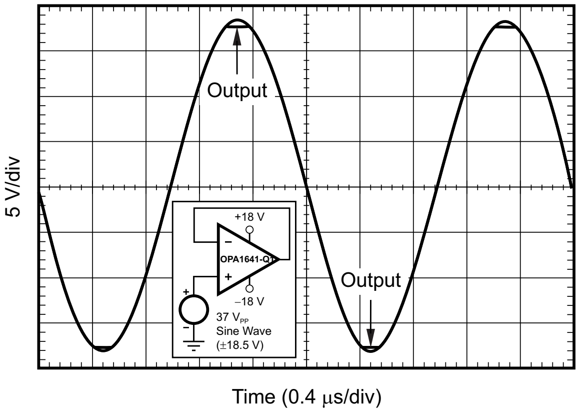
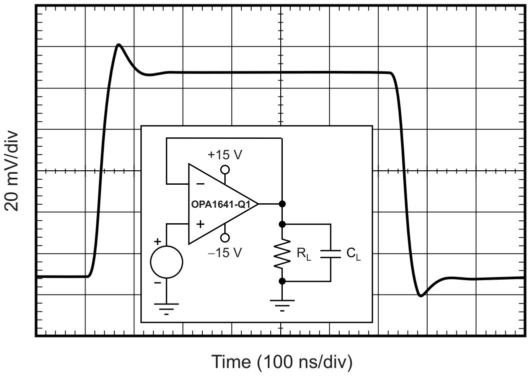


Figure 12. No Phase Reversal

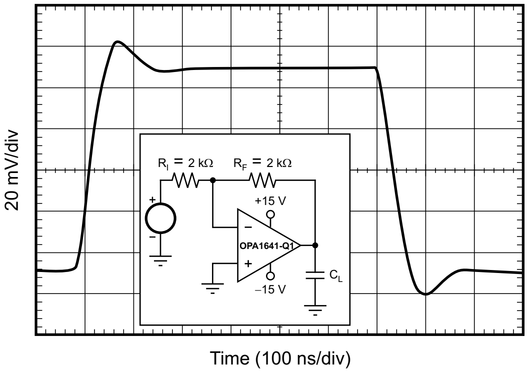
Typical Characteristics (continued)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



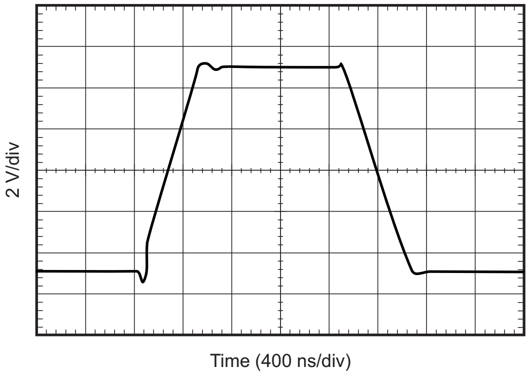
G = 1 C_L = 100 pF

Figure 13. Small-Signal Step Response (100 mV)



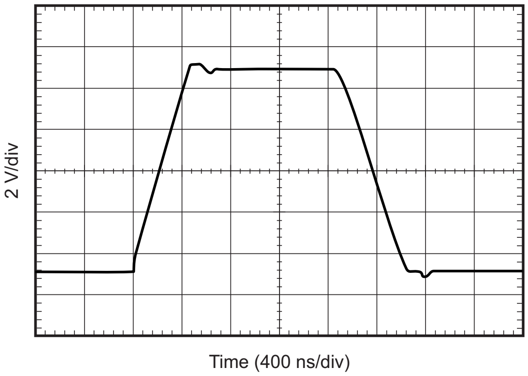
G = –1 C_L = 100 pF

Figure 14. Small-Signal Step Response (100 mV)



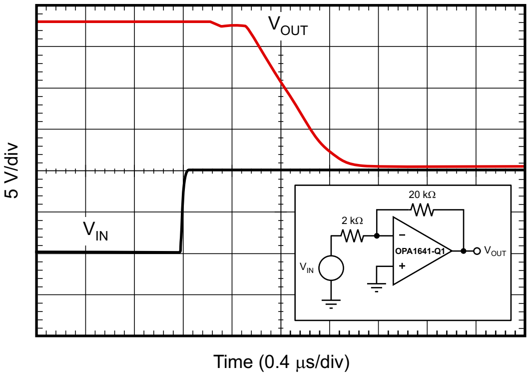
G = 1 C_L = 100 pF

Figure 15. Large-Signal Step Response



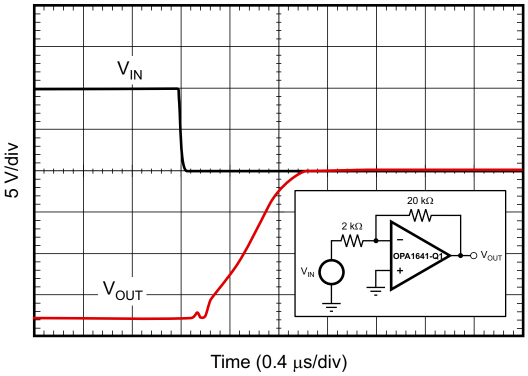
G = –1 C_L = 100 pF

Figure 16. Large-Signal Step Response



G = –10

Figure 17. Positive Overload Recovery

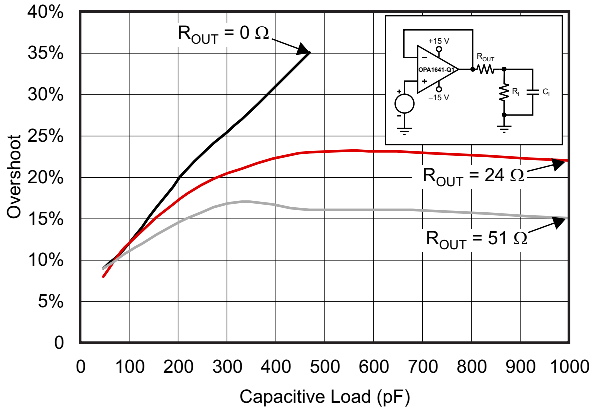


G = –10

Figure 18. Negative Overload Recovery

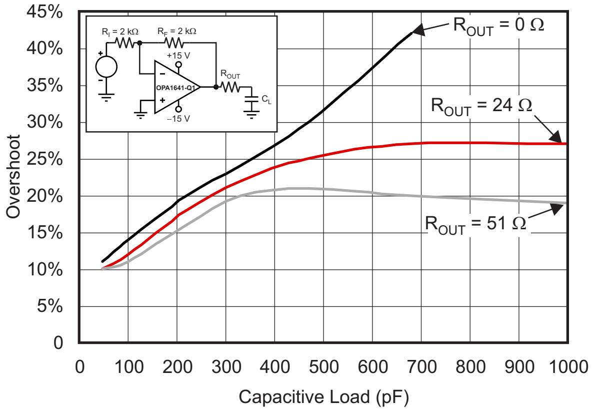
Typical Characteristics (continued)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



G = 1

Figure 19. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



G = –1

Figure 20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

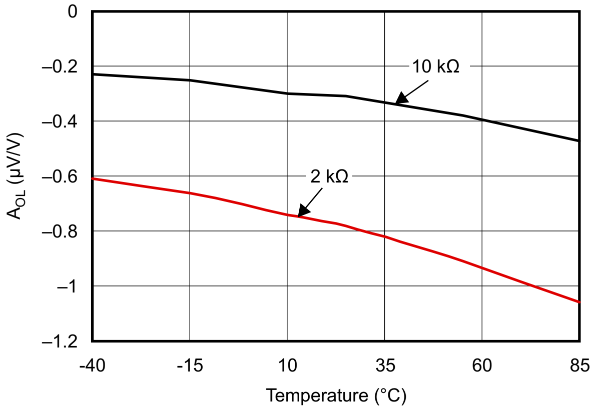


Figure 21. Open-Loop Gain vs Temperature

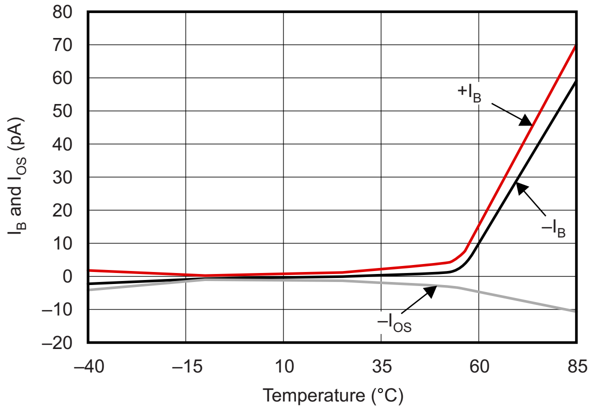
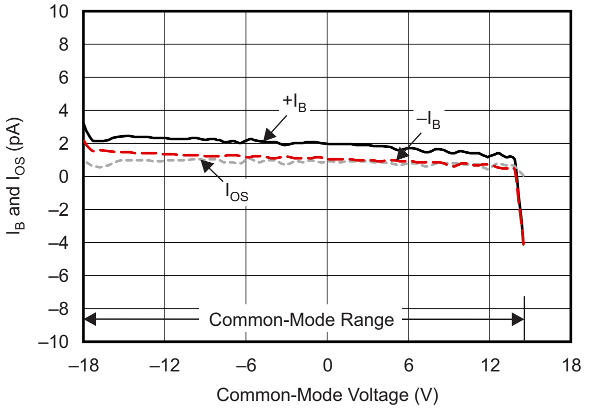


Figure 22. I_B and I_{OS} vs Temperature



V_S = ±18 V

Figure 23. I_B and I_{OS} vs Common-Mode Voltage

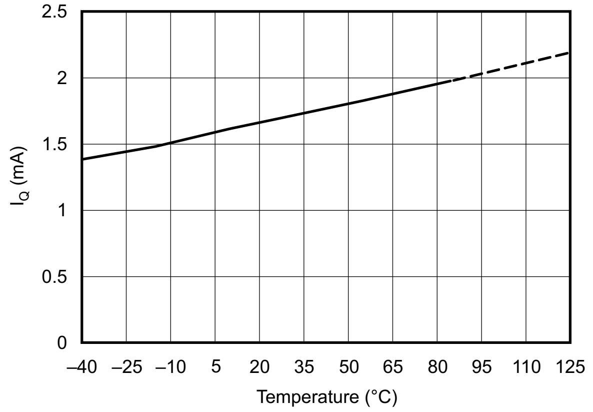


Figure 24. Quiescent Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

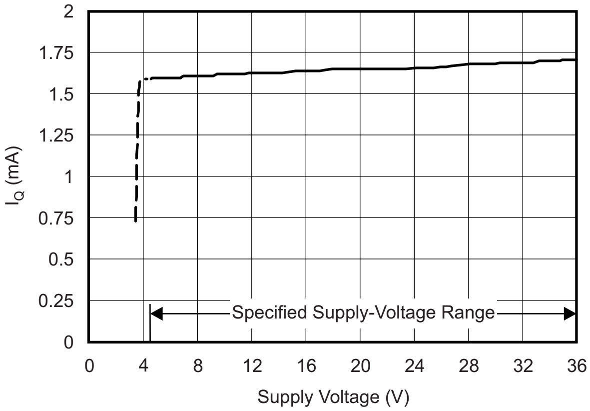
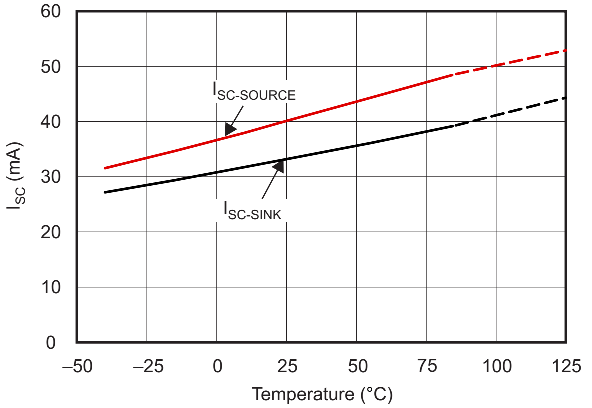


Figure 25. Quiescent Current vs Supply Voltage



V_{OUT} = Midsupply (includes self-heating)

Figure 26. Short-Circuit Current vs Temperature

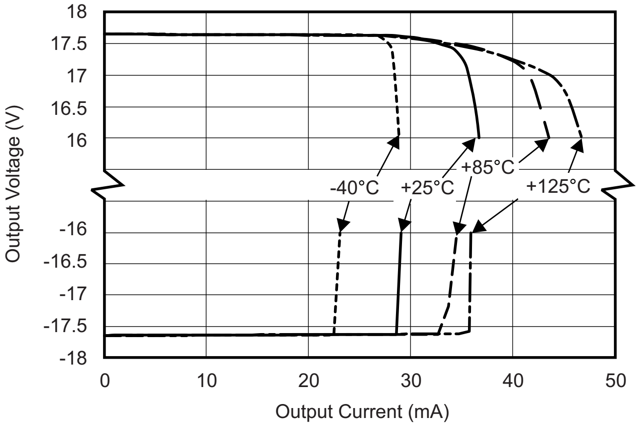


Figure 27. Output Voltage vs Output Current

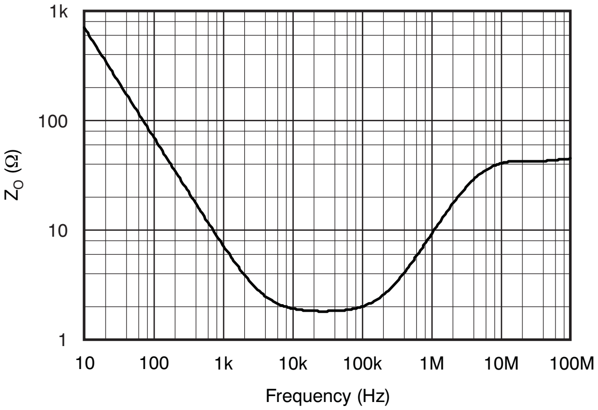


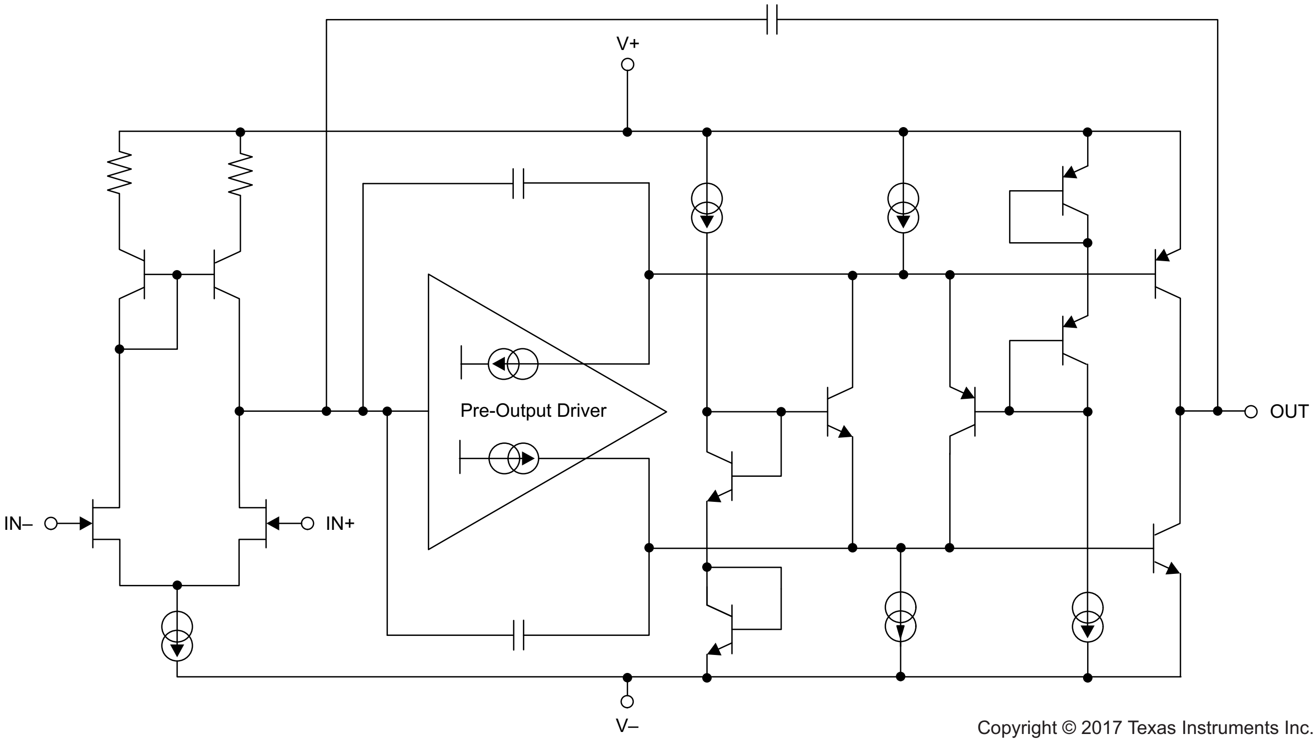
Figure 28. Open-Loop Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The OPA164x-Q1 family of operational amplifiers combine an ultra-low noise JFET input stage with a rail-to-rail output stage to provide high overall performance in audio applications. The internal topology is selected specifically to deliver extremely low distortion, consume limited power, and accommodate small packages. These amplifiers are well-suited for analog signal processing applications such as active filter circuits, pre-amplifiers, and tone controls. The unique input stage design and semiconductor processes used in this device deliver extremely high performance even in applications with high source impedance and wide common-mode voltage swings.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Phase Reversal Protection

The OPA164x-Q1 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA164x-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in Figure 29.

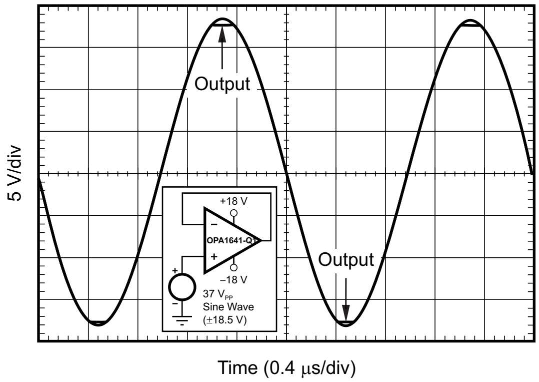


Figure 29. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

7.3.2 Output Current Limit

The output current of the OPA164x-Q1 series is limited by internal circuitry to 36 mA and –30 mA (sourcing and sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature; see Figure 26.

Although uncommon for most modern audio applications to require 600-Ω load drive capability, many audio operational amplifier applications continue to specify the total harmonic distortion (THD+N) at 600-Ω load for comparative purposes. Figure 7 and Figure 8 provide typical THD+N measurement curves for the OPA164x-Q1 series, where the output drives a 3-V_{RMS} signal into a 600-Ω load. However, correct device operation cannot be ensured when driving 600-Ω loads at full supply. Depending on supply voltage and temperature, this operating condition can possibly trigger the output current limit circuitry of the device.

7.3.3 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report *EMI Rejection Ratio of Operational Amplifiers*, available for download at www.ti.com.

Feature Description (continued)

The EMIRR IN+ of the OPA164x-Q1 is plotted versus frequency in Figure 30. If available, any dual and quad operational amplifier device versions have nearly identical EMIRR IN+ performance. The OPA164x-Q1 unity-gain bandwidth is 11 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

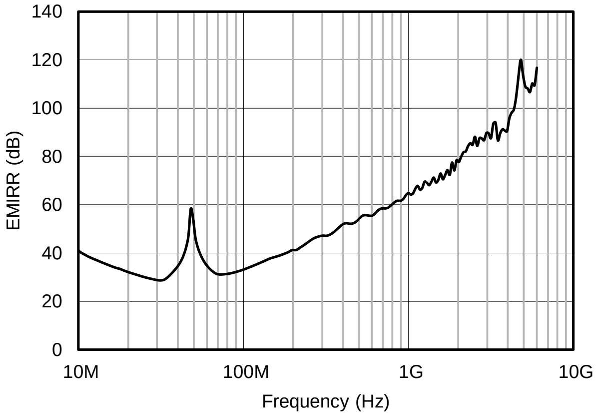


Figure 30. OPA164x-Q1 EMIRR vs Frequency

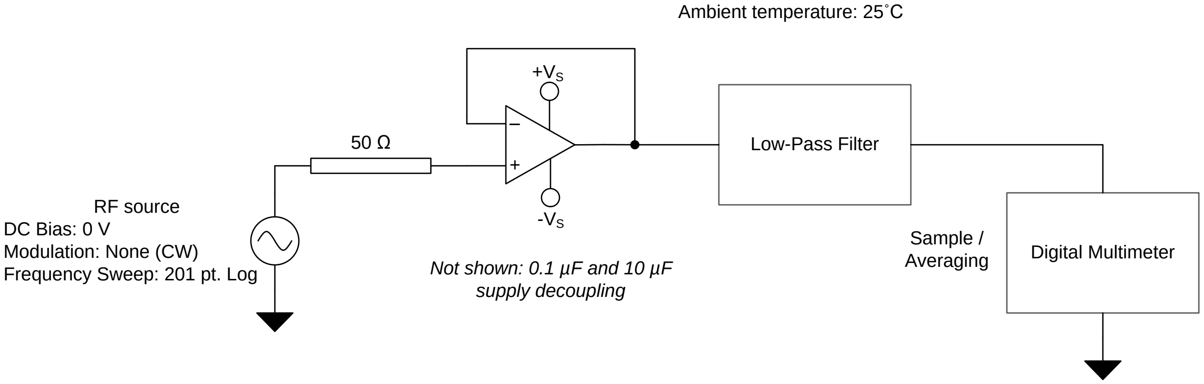
Table 1 lists the EMIRR IN+ values for the OPA164x-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPA164x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, UHF	53.1 dB
900 MHz	GSM, radio communication and navigation, GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	72.2 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	80.7 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio and satellite, S-band	86.8 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	91.7 dB
5 GHz	802.11a/n, aero communication and navigation, mobile communication, space and satellite operation, C-band	96.6 dB

7.3.3.1 EMIRR IN+ Test Configuration

Figure 31 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See *EMI Rejection Ratio of Operational Amplifiers* for more details.



Not shown: 0.1 µF and 10 µF supply decoupling

Figure 31. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

7.4.1 Operating Voltage

The OPA164x-Q1 series of operational amplifiers can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) and up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies; only a minimum supply voltage of 4.5 V (±2.25 V) is required. For V_S less than ±3.5 V, the common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device; see *Absolute Maximum Ratings* for more information. Key parameters are specified over the operating temperature range, T_A = –40°C to +85°C. Key parameters that vary over the supply voltage or temperature range are shown in *Typical Characteristics*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA164x-Q1 amplifiers are unity-gain stable, audio operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-μF capacitors are adequate. Figure 32 shows a simplified schematic of the OPA1641-Q1.

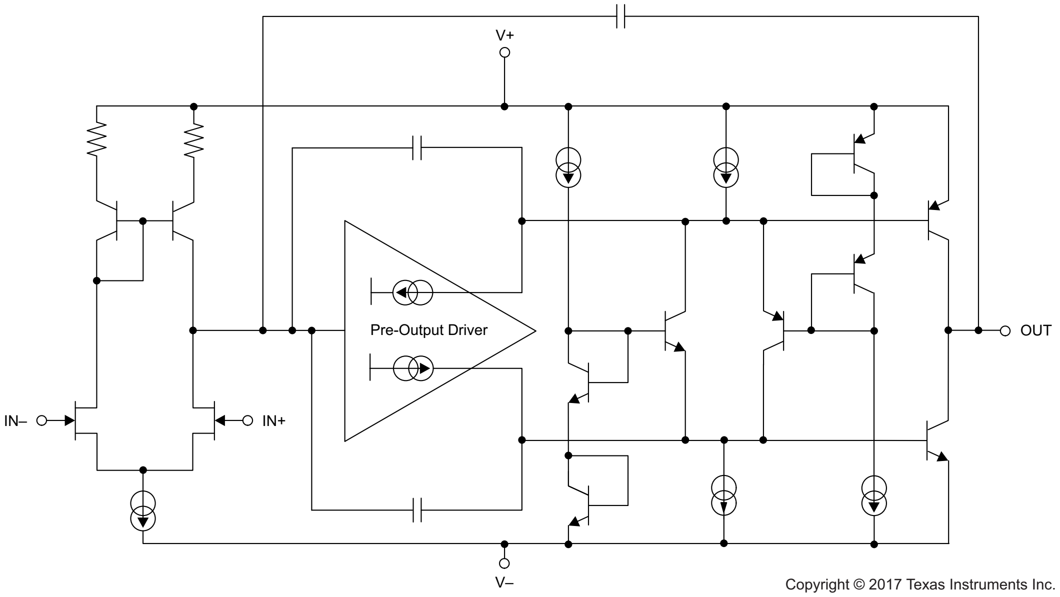


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Figure 32. Simplified Internal Schematic

Application Information (continued)

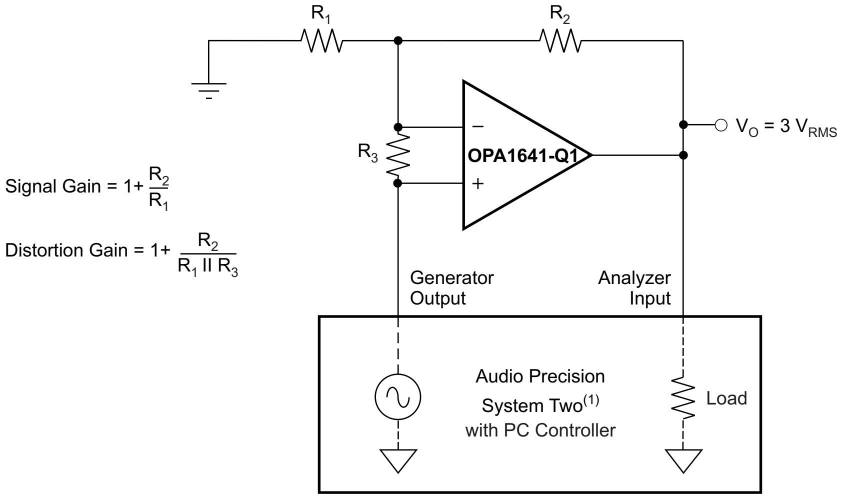
8.1.1 Total Harmonic Distortion Measurements

The OPA164x-Q1 series operational amplifiers have excellent distortion characteristics. THD + noise is below 0.00005% (G = 1, V_O = 3 V_{RMS}, BW = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see Figure 7).

The distortion produced by the OPA164x-Q1 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as shown in Figure 33) can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. Figure 33 shows a circuit that causes the operational amplifier distortion to be 101 times (or approximately 40 dB) greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, extending the resolution by 101. The input signal and load applied to the op amp are the same as with conventional feedback without R_3. Keep the value of R_3 small to minimize any effect on distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this document were made with an audio precision system two distortion and noise analyzer that greatly simplifies repetitive measurements. However, the measurement technique can be performed with manual distortion measurement instruments.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
1	101	∞	1 kΩ	10 Ω
11	101	100 Ω	1 kΩ	11 Ω

(1) For measurement bandwidth, see Figure 7 through Figure 10.

Figure 33. Distortion Test Circuit

8.1.2 Source Impedance and Distortion

In traditional JFET-input op amps, the impedance applied to the positive and negative inputs in noninverting applications must be matched for lowest distortion. Legacy methods for fabricating the JFETs in the FET input stage exhibit a varying input capacitance with applied common-mode input voltage. In inverting configurations, the input does not vary with input voltage because the inverting input is held at virtual ground. However, in noninverting applications, the inputs do vary, and the gate-to-source voltage is not constant. This effect produces increased distortion resulting from the varying capacitance for unmatched source impedances. However, the OPA164x-Q1 family of amplifiers is designed to maintain a constant input capacitance with varying common-mode voltage to prevent this mechanism of distortion. The variation of input capacitance with common-mode voltage for a traditional amplifier is compared to the OPA164x-Q1 family in Figure 34.

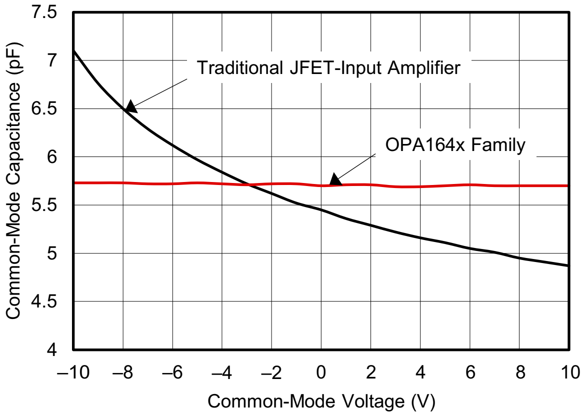


Figure 34. Input Capacitance of the OPA164x-Q1 Family of Amplifiers Compared to Traditional JFET-input Amplifiers

By stabilizing the input capacitance, the distortion performance of the amplifier is greatly improved for noninverting configurations with high source impedances. The measured performance of an OPA164x-Q1 amplifier is compared to a traditional JFET-input amplifier in Figure 35. The unity-gain configuration, high source impedance, and large-signal amplitude produce additional distortion in the traditional amplifier.

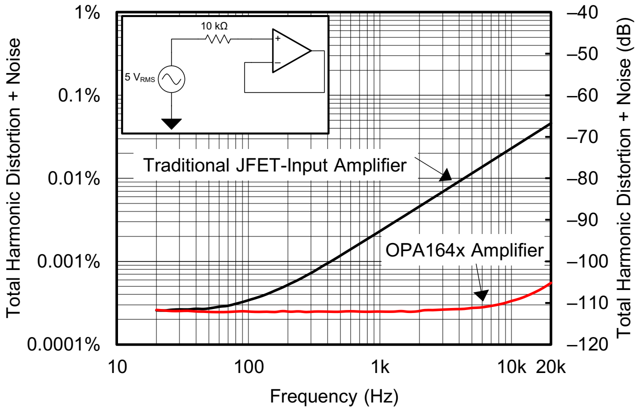


Figure 35. Measured THD+N of the OPA164x-Q1 Family of Amplifiers Compared to Traditional JFET-input Amplifiers

8.1.3 Capacitive Load and Stability

The dynamic characteristics of the OPA164x-Q1 are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω, for example) in series with the output.

Figure 19 and Figure 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT}. For details of analysis techniques and application circuits, see see *Feedback Plots Define Op Amp AC Performance* available for download at www.ti.com

8.1.4 Power Dissipation and Thermal Protection

The OPA164x-Q1 op amps are capable of driving 2-kΩ loads with power-supply voltages of up to ±18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8 kΩ at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance can be used, as long as the output current does not exceed 13 mA; otherwise, the device short-circuit current-protection circuit can activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA164x-Q1 series of devices improves heat dissipation compared to conventional materials. PCB layout can help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by functioning as an additional heat sink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to midsupply, the typical short-circuit current of 36 mA leads to an internal power dissipation of over 600 mW at a supply of ±18 V. In case of a dual OPA1642-Q1 in an VSSOP-8 package (thermal resistance $R_{\theta JA}$ = 180°C/W), such a power dissipation results in the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase destroys the device.

To prevent such excessive heating that can destroy the device, the OPA164x-Q1 series has an internal thermal shutdown circuit that shuts down the device if the die temperature exceeds approximately 180°C. When this thermal shutdown circuit activates, a built-in hysteresis of 15°C ensures that the die temperature must drop to approximately 165°C before the device switches on again.

8.1.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 36 illustrates the ESD circuits contained in the OPA164x-Q1 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines where an internal absorption device is connected. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger (or threshold voltage) that is above the normal operating voltage of the OPA164x-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

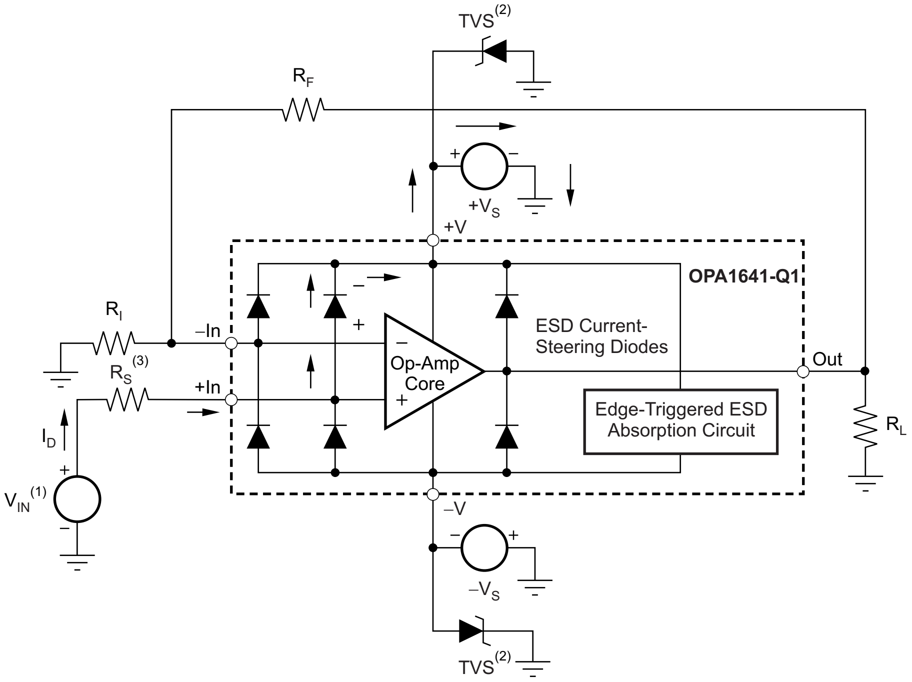
When the operational amplifier connects into a circuit as shown in Figure 36, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, some of the internal ESD protection circuits can be biased on and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 36 depicts a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies $+V_S$ and $–V_S$ are at 0 V. The amplifier behavior depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes can be added to the supply pins, as shown in Figure 36. The Zener voltage must be selected so the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



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(1) $V_{IN} = +V_S + 500$ mV.
(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$
(3) Suggested value is approximately 1 kΩ.

Figure 36. Equivalent Internal ESD Circuitry and the Relation to a Typical Circuit Application

8.2 Typical Application

8.2.1 Single-Supply Electret Microphone Preamplifier for Speech

Electret microphones are commonly used in automotive hands-free phone systems because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The low noise and distortion of the OPA1641-Q1 makes the device a good choice for preamplifier circuits for electret microphones. The circuit shown in Figure 37 is a single-supply preamplifier circuit for electret microphones with a bandwidth from 100 Hz to 3 kHz for capturing speech.

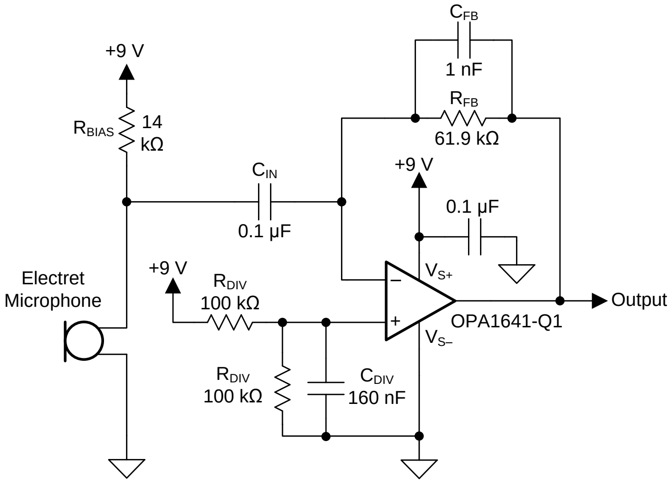


Figure 37. Preamplifier Circuit for Electret Microphones Using a Single Power Supply Voltage

8.2.1.1 Design Requirements

- 9-V single supply
- 1-V_{RMS} output for 100-dB_{SPL} input
- Approximately 100-Hz to 3-kHz, –3-dB Bandwidth
- Microphone sensitivity: 8 µA / Pa
- Microphone operating voltage: 2 V to 10 V
- Microphone bias current: 500 µA

8.2.1.2 Detailed Design Procedure

In this circuit, the op amp is configured as a transimpedance amplifier which converts the signal current of the microphone into an output voltage. The bandwidth of this circuit is limited to the vocal range as is common in telephony systems. The gain of the circuit is determined by the feedback resistor (R_{FB}), which must be calculated according to the microphone sensitivity. For this design, a microphone output current of 8 µA per Pascal (Pa) of air pressure was selected. Using this value, the output current for a sound pressure level of 100 dB_{SPL}, or 2 Pa air pressure, is calculated in Equation 1.

$$i_{mic} = \frac{8\ \mu A}{1\ Pa} \times 2\ Pa = 16\ \mu A \tag{1}$$

R_{FB} is then calculated from this current to produce 1-V_{RMS} output for a 100-dB_{SPL} input signal in Equation 2.

$$R_{FB} = \frac{V_O}{i_{mic}} = \frac{1\ V_{RMS}}{16\ \mu A} = 62500 \rightarrow 61.9\ k\Omega \tag{2}$$

The feedback capacitor (C_{FB}) is calculated to limit the bandwidth of the amplifier to 3 kHz in Equation 3.

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot R_{FB} \cdot f_H} = \frac{1}{2 \cdot \pi \cdot (61.9\ k\Omega) \cdot (3\ kHz)} = 857 \times 10^{-12} \rightarrow 1\ nF \tag{3}$$

Typical Application (continued)

R_{BIAS} is necessary to divert the microphone signal current through capacitor C_{IN} rather than flowing from the power supply (V_{CC}). Larger values of R_{BIAS} allow for a smaller capacitor to be used for C_{IN} and reduces the overall noise of the circuit. However, the maximum value for R_{BIAS} is limited by the microphone bias current and minimum operating voltage.

The value of R_{BIAS} is calculated in Equation 4.

$$R_{BIAS} = \frac{V_{CC} - V_{MIC}}{I_{BIAS}} = \frac{9\ \text{V} - 2\ \text{V}}{500\ \mu\text{A}} = 14\ \text{k}\Omega \tag{4}$$

Input capacitor C_{IN} forms a high-pass filter in combination with resistor R_{BIAS}. The filter corner frequency calculation is shown in Equation 5 to place the high-pass corner frequency at 100 Hz.

$$C_{IN} = \frac{1}{2 \cdot \pi \cdot R_{BIAS} \cdot f_L} = \frac{1}{2 \cdot \pi \cdot (14\ \text{k}\Omega) \cdot (100\ \text{Hz})} = 113.7 \times 10^{-9} \rightarrow 100\ \text{nF} \tag{5}$$

The voltage divider network at the op amp noninverting input is used to bias the op amp output to the midsupply point (V_{CC} / 2) to maximize the output voltage range of the circuit. This result is easily achieved by selecting the same value for both resistors in the divider. The absolute value of those resistors is limited by the acceptable power-supply current drawn by the voltage divider. Choosing 50 µA as an acceptable limit of supply current gives a value of 100 kΩ for the resistors in the divider, as Equation 6 shows.

$$R_{DIV} \geq \frac{V_{CC}}{2 \cdot I_{DIV}} \geq \frac{9\ \text{V}}{2 \cdot 50\ \mu\text{A}} \geq 90\ \text{k}\Omega \rightarrow 100\ \text{k}\Omega \tag{6}$$

Finally, to minimize the additional noise contribution from the voltage divider, a capacitor is placed at the op amp noninverting input. This capacitor forms a low-pass filter with the parallel combination of the voltage divider resistors. Selecting a filter corner frequency of 20 Hz minimizes the noise contribution of the voltage divider inside the amplifier passband; see Equation 7.

$$C_{DIV} = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{DIV}}{2}\right) \cdot f_L} = \frac{1}{2 \cdot \pi \cdot \left(\frac{100\ \text{k}\Omega}{2}\right) \cdot (20\ \text{Hz})} = 1.592 \times 10^{-7} \rightarrow 160\ \text{nF} \tag{7}$$

Typical Application (continued)

8.2.1.3 Application Curve

The transfer function of the microphone preamplifier circuit is shown in Figure 38. The nominal gain of the circuit is 95.46 dB, or 59,292.5 V per amp of input current. The –3-dB bandwidth limits of the circuit are 105.7 Hz and 2.77 kHz.

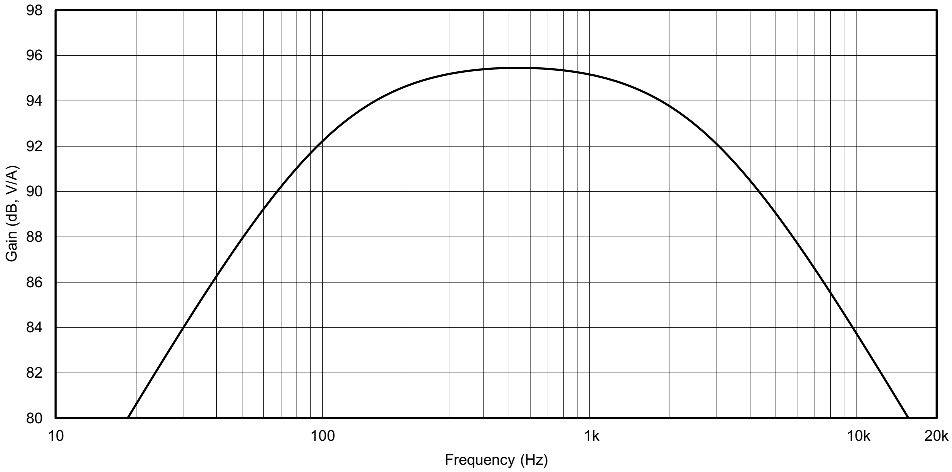


Figure 38. Microphone Preamplifier Transfer Function

9 Power Supply Recommendations

The OPA164x-Q1 devices are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

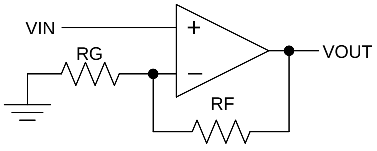
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in Figure 39, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



(Schematic Representation)

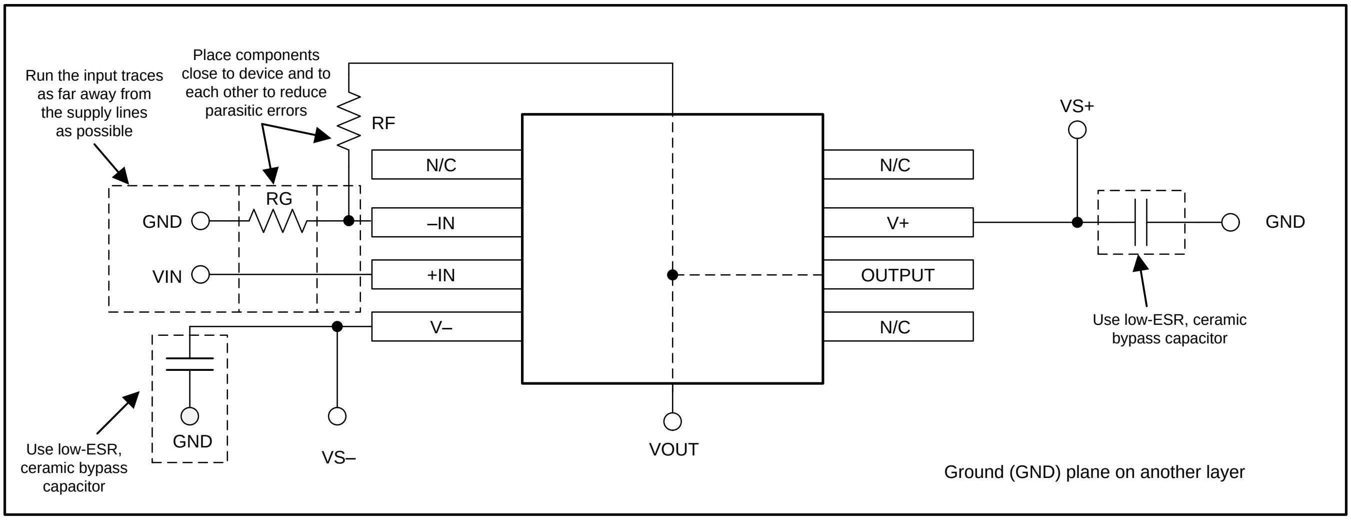


Figure 39. OPA1641-Q1 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/, are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets optimized filter designs to be created using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, the WEBENCH® Filter Designer allows complete multistage active filter solutions to be designed, optimized, and simulated within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- *Using infinite-gain, MFB filter topology in fully differential active filters*
- *Op Amp Performance Analysis*
- *Single-Supply Operation of Operational Amplifiers*
- *Tuning in Amplifiers*
- *Shelf-Life Evaluation of Lead-Free Component Finishes*

11.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA1641-Q1	Click here	Click here	Click here	Click here	Click here
OPA1642-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
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TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1641AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1641
OPA1641AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1641
OPA1642AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1642
OPA1642AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1642

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA1641-Q1, OPA1642-Q1 :

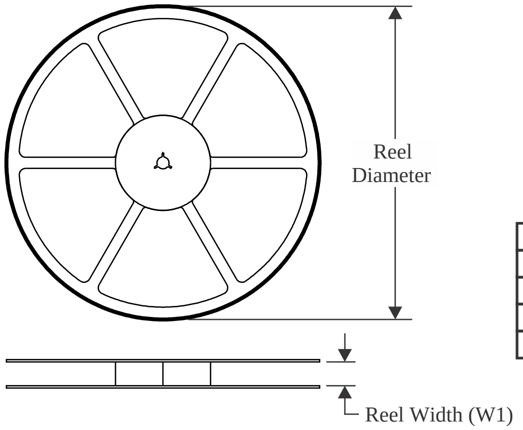
- Catalog : OPA1641, OPA1642

NOTE: Qualified Version Definitions:

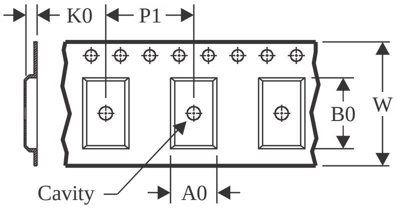
  - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

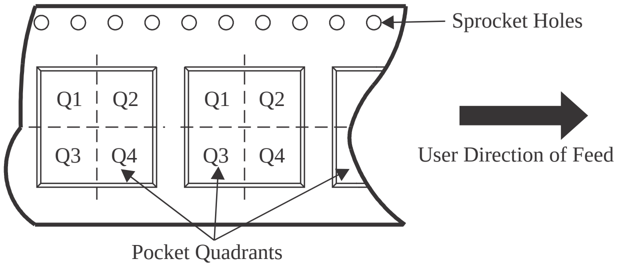


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

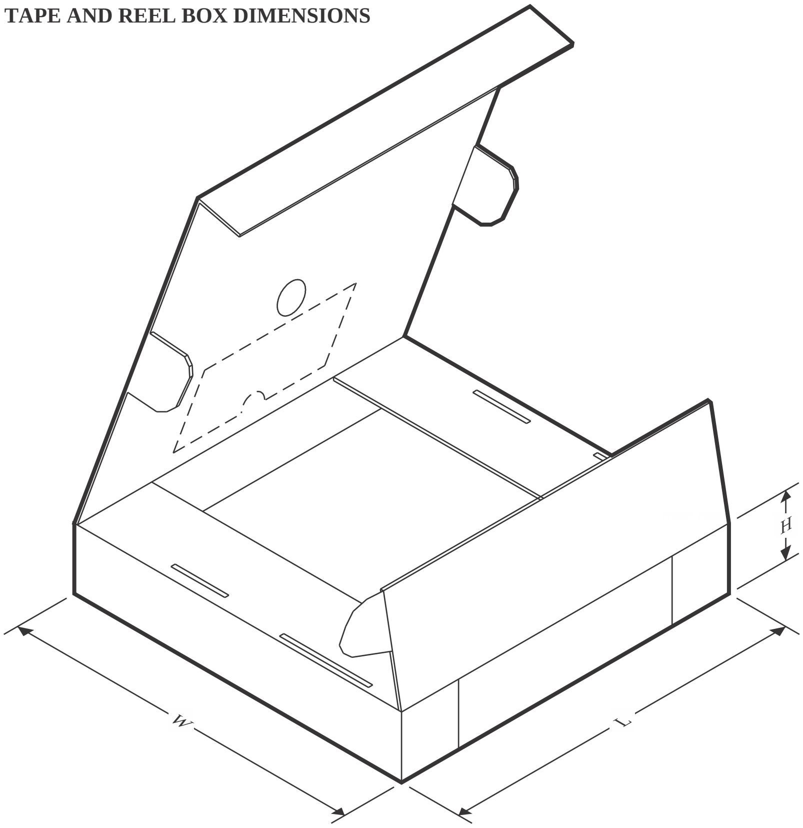
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

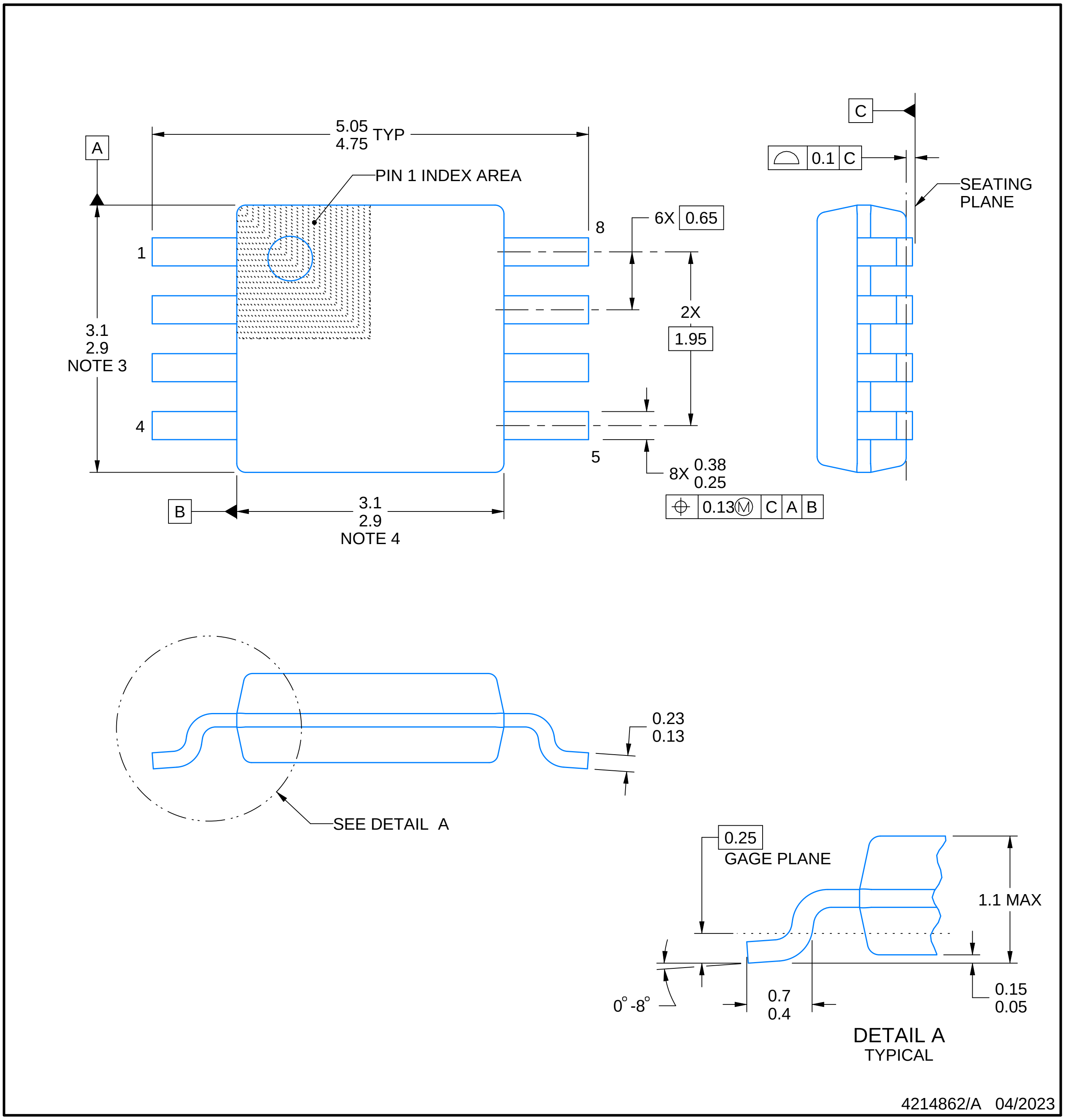
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1641AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

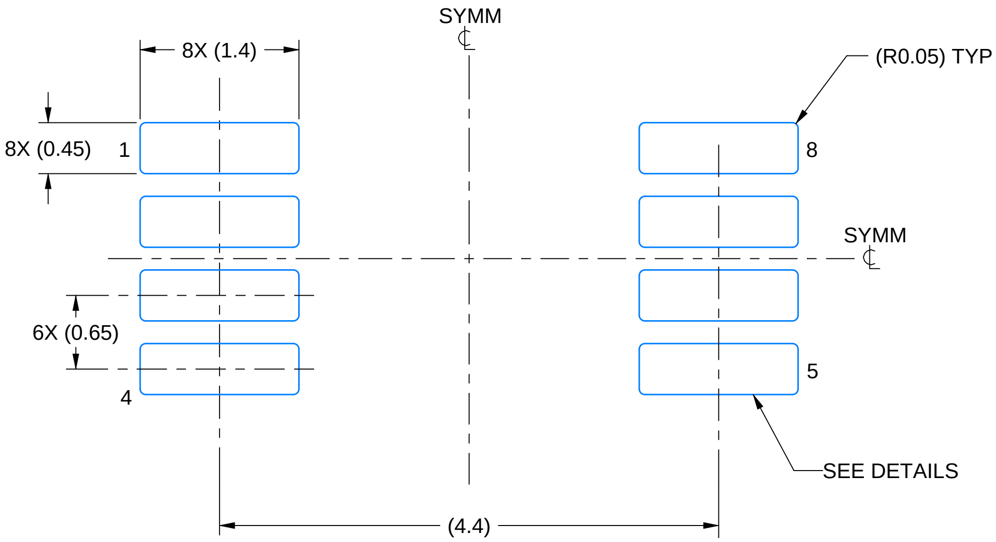
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1641AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

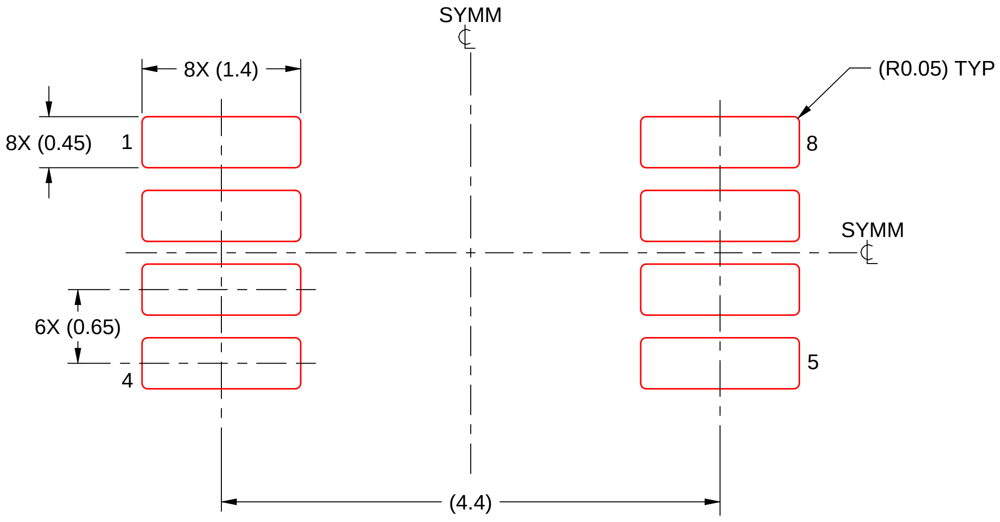
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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