# OPAx197-Q1 36V, Precision, Rail-to-Rail I/O, Low-Offset Voltage, Low-Input Bias Current e-trim™ Automotive Op Amps

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
- Low offset voltage: ±250µV (maximum)
- Low offset voltage drift: ±0.2 µV/°C
- Low noise: 5.5nV/√Hz at 1kHz
- High common-mode rejection: 140dB
- Low bias current: ±5pA
- Rail-to-rail input and output
- Wide bandwidth: 10MHz GBW
- High slew rate: 20V/µs
- Low quiescent current: 1mA per amplifier
- Wide supply: ±2.25V to ±18V, 4.5V to 36V
- EMI/RFI filtered inputs
- Differential input-voltage range to supply rail
- High capacitive load drive capability: 1nF
- Industry-standard packages:
  - Single and dual channel in very-small, 8-pin VSSOP
  - Quad channel in 14-pin TSSOP
  - Quad channel in 14 pin SOIC

## 2 Applications

- Inverter and motor control
- DC/DC converter
- On-board (OBC) and wireless charger
- Battery management system (BMS)

## 3 Description

The OPAx197-Q1 family (OPA197-Q1, OPA2197-Q1, and OPA4197-Q1) is part of a new generation of 36V, e-trim™ operational amplifiers. The OPAx197-Q1 family of e-trim operational amplifiers uses a proprietary method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding.

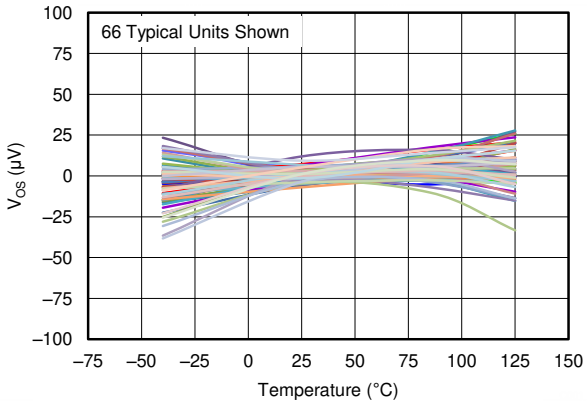
These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset (±5µV, typical), low offset drift (±0.2µV/°C, typical), and a 10MHz bandwidth.

Unique features such as differential input-voltage range to the supply rail, high output current (±65mA), high capacitive load drive of up to 1nF, and high slew rate (20V/µs) make the OPAx197-Q1 robust, high-performance op amps for high-voltage industrial applications.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| OPA197-Q1 | DGK, VSSOP (8) | 3.00mm × 3.00mm |
| OPA2197-Q1 | DGK, VSSOP (8) | 3.00mm × 3.00mm |
| OPA4197-Q1 | PW, TSSOP (14) | 5.00mm × 4.40mm |
| | D, SOIC (14) | 8.65mm × 3.9mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**The OPAx197-Q1 Maintains Ultra-Low Input Offset Voltage Over Temperature**

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# 4 Pin Configuration and Functions

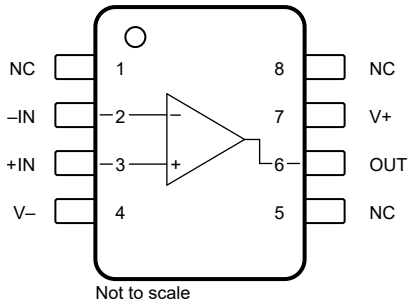


**Figure 4-1. OPA197-Q1 DGK Package, 8-Pin VSSOP, Top View**

**Pin Functions: OPA197-Q1**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| +IN | 3 | I | Noninverting input |
| –IN | 2 | I | Inverting input |
| NC | 1, 5, 8 | — | No internal connection (can be left floating) |
| OUT | 6 | O | Output |
| V+ | 7 | — | Positive (highest) power supply |
| V– | 4 | — | Negative (lowest) power supply |

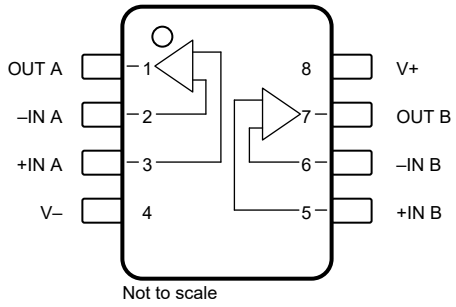


**Figure 4-2. OPA2197-Q1 DGK Package, 8-Pin VSSOP, Top View**

**Pin Functions: OPA2197-Q1**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | DGK (VSSOP) | | |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V+ | 8 | — | Positive (highest) power supply |
| V– | 4 | — | Negative (lowest) power supply |

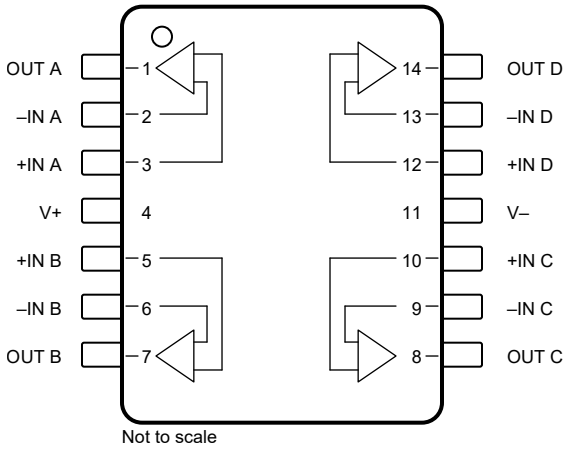


**Figure 4-3. OPA4197-Q1 PW Package, 14-Pin TSSOP, and D Package, 14-Pin SOIC, Top View**

**Pin Functions: OPA4197-Q1**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| +IN C | 10 | I | Noninverting input, channel C |
| +IN D | 12 | I | Noninverting input, channel D |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| –IN C | 9 | I | Inverting input, channel C |
| –IN D | 13 | I | Inverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V+ | 4 | — | Positive (highest) power supply |
| V– | 11 | — | Negative (lowest) power supply |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage | Single supply, $V_S$ = (V+) | | 40 | V |
| | | Dual supply, $V_S$ = (V+) – (V–) | | ±20 | |
| | Signal input voltage | Common-mode | (V–) – 0.5 | (V+) + 0.5 | V |
| | | Differential | | (V+) – (V–) + 0.2 | |
| | Signal input current | | | ±10 | mA |
| | Output short circuit[2] | | Continuous | | |
| | Latch-up per JESD78D | | Class IIA | | |
| $T_A$ | Operating temperature | | –55 | 150 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| **OPA197-Q1, OPA2197-Q1** | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002[1]<br>HBM ESD classification level 3A | ±4000 | V |
| | | Charge device model (CDM), per AEC Q100-011<br>CDM ESD classification level C4A | ±500 | |
| **OPA4197-Q1** | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002[1]<br>HBM ESD classification level 2 | ±2000 | V |
| | | Charge device model (CDM), per AEC Q100-011<br>CDM ESD classification level C5 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_S$ | Supply voltage | Single supply, $V_S$ = (V+) | 4.5 | | 36 | V |
| | | Dual supply, $V_S$ = (V+) – (V–) | ±2.25 | | ±18 | |
| $T_A$ | Operating temperature | | –40 | | 125 | °C |

## 5.4 Thermal Information: OPA197-Q1

| THERMAL METRIC(1) | | OPA197-Q1 DGK (VSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 180.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 67.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 102.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 100.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Thermal Information: OPA2197-Q1

| THERMAL METRIC(1) | | OPA2197-Q1 DGK (VSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 158 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 48.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 78.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 77.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.6 Thermal Information: OPA4197-Q1

| THERMAL METRIC(1) | | OPA4197-Q1 D (SOIC) 14 PINS | OPA4197-Q1 PW (TSSOP) 14 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 86.4 | 108.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 46.3 | 26.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 41.0 | 54.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 11.3 | 1.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.7 | 53.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.7 Electrical Characteristics: $V_S$ = ±4 V to ±18 V ($V_S$ = 8 V to 36 V)

at $T_A$ = +25°C, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | | | | ±25 | ±250 | µV |
| | | $T_A$ = 0°C to 85°C | | | ±30 | ±350 | |
| | | $T_A$ = –40°C to +125°C | | | ±50 | ±400 | |
| | | $V_{CM}$ = (V+) – 1.5 V | | | ±10 | ±250 | |
| | | | $T_A$ = 0°C to 85°C | | ±25 | ±350 | |
| | | | $T_A$ = –40°C to +125°C | | ±50 | ±500 | |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_A$ = 0°C to 85°C | | | ±0.5 | ±2.5 | µV/°C |
| | | $T_A$ = –40°C to +125°C | | | ±0.8 | ±4.5 | |
| PSRR | Power-supply rejection ratio | $T_A$ = –40°C to +125°C | | | ±0.3 | ±1.0 | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±5 | ±20 | pA |
| | | $T_A$ = –40°C to +125°C | | | | ±5 | nA |
| $I_{OS}$ | Input offset current | | | | ±2 | ±20 | pA |
| | | $T_A$ = –40°C to +125°C | | | | ±2 | nA |
| **NOISE** | | | | | | | |
| $E_n$ | Input voltage noise | (V–) – 0.1 V < $V_{CM}$ < (V+) – 3 V | f = 0.1 Hz to 10 Hz | | 1.3 | | $\mu V_{PP}$ |
| | | (V+) – 1.5 V < $V_{CM}$ < (V+) + 0.1 V | f = 0.1 Hz to 10 Hz | | 4 | | |
| $e_n$ | Input voltage noise density | (V–) – 0.1 V < $V_{CM}$ < (V+) – 3 V | f = 100 Hz | | 10.5 | | $nV/\sqrt{Hz}$ |
| | | | f = 1 kHz | | 5.5 | | |
| | | (V+) – 1.5 V < $V_{CM}$ < (V+) + 0.1 V | f = 100 Hz | | 32 | | |
| | | | f = 1 kHz | | 12.5 | | |
| $i_n$ | Input current noise density | f = 1 kHz | | | 1.5 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage | | | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | (V–) – 0.1 V < $V_{CM}$ < (V+) – 3 V | | 120 | 140 | | dB |
| | | (V–) < $V_{CM}$ < (V+) – 3 V, $T_A$ = –40°C to +125°C | | 114 | 126 | | |
| | | (V+) – 1.5 V < $V_{CM}$ < (V+) | | 100 | 120 | | |
| | | | $T_A$ = –40°C to +125°C | 86 | 100 | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $Z_{ID}$ | Differential | | | | 100 \|\| 1.6 | | MΩ \|\| pF |
| $Z_{IC}$ | Common-mode | | | | 1 \|\| 6.4 | | $10^{13}$Ω \|\| pF |

## 5.7 Electrical Characteristics: $V_S$ = ±4 V to ±18 V ($V_S$ = 8 V to 36 V) (continued)

at $T_A$ = +25°C, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | (V–) + 0.6 V < $V_O$ < (V+) – 0.6 V, $R_L$ = 2 kΩ | | 120 | 134 | | dB |
| | | | $T_A$ = –40°C to +125°C | 114 | 126 | | |
| | | (V–) + 0.3 V < $V_O$ < (V+) – 0.3 V, $R_L$ = 10 kΩ | | 126 | 140 | | |
| | | | $T_A$ = –40°C to +125°C | 120 | 134 | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Unity gain bandwidth | | | | 10 | | MHz |
| SR | Slew rate | G = 1, 10-V step | | | 20 | | V/µs |
| $t_s$ | Settling time | To 0.01% | G = 1, 10-V step | | 1.4 | | µs |
| | | | G = 1, 5-V step | | 0.9 | | |
| | | To 0.001% | G = 1, 10-V step | | 2.1 | | |
| | | | G = 1, 5-V step | | 1.8 | | µs |
| $t_{OR}$ | Overload recovery time | $V_{IN}$ × G = $V_S$ | | | 200 | | ns |
| THD+N | Total harmonic distortion + noise | G = 1, f = 1 kHz, $V_O$ = 3.5 $V_{RMS}$ | | | 0.00008% | | |
| | Crosstalk | OPA4197-Q1 at dc | | | 150 | | dB |
| | | OPA4197-Q1, f = 100 kHz | | | 130 | | dB |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing from rail | Positive rail | No load | | 5 | 15 | mV |
| | | | $R_L$ = 10 kΩ | | 95 | 110 | |
| | | | $R_L$ = 2 kΩ | | 430 | 500 | |
| | | Negative rail | No load | | 5 | 15 | |
| | | | $R_L$ = 10 kΩ | | 95 | 110 | |
| | | | $R_L$ = 2 kΩ | | 430 | 500 | |
| $I_{SC}$ | Short-circuit current | | | | ±65 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | | See Section 5.9 | | |
| $Z_O$ | Open-loop output impedance | f = 1 MHz, $I_O$ = 0 A; see Figure 5-29 | | | 375 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 A | | | 1 | 1.2 | mA |
| | | | $T_A$ = –40°C to +125°C | | | 1.5 | |
| **TEMPERATURE** | | | | | | | |
| | Thermal protection | | | | 140 | | °C |

## 5.8 Electrical Characteristics: $V_S$ = ±2.25 V to ±4 V ($V_S$ = 4.5 V to 8 V)

at $T_A$ = +25°C, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_{CM}$ = (V+) – 3 V | | | ±5 | ±250 | µV |
| | | | $T_A$ = 0°C to 85°C | | ±8 | ±350 | |
| | | | $T_A$ = –40°C to +125°C | | ±10 | ±400 | |
| | | (V+) – 3.5 V < $V_{CM}$ < (V+) – 1.5 V | | | See Section 6.3.6 | | |
| | | $V_{CM}$ = (V+) – 1.5 V | | | ±10 | ±250 | |
| | | | $T_A$ = 0°C to 85°C | | ±25 | ±350 | |
| | | | $T_A$ = –40°C to +125°C | | ±50 | ±500 | |
| $dV_{OS}/dT$ | Input offset voltage drift | $V_{CM}$ = (V+) – 3 V | $T_A$ = –40°C to +125°C | | ±0.5 | ±2.5 | µV/°C |
| $dV_{OS}/dT$ | Input offset voltage drift | $V_{CM}$ = (V+) – 1.5 V | | | ±0.8 | ±4.5 | |
| PSRR | Power-supply rejection ratio | $T_A$ = –40°C to +125°C | | | ±2 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±5 | ±20 | pA |
| | | $T_A$ = –40°C to +125°C | | | | ±5 | nA |
| $I_{OS}$ | Input offset current | | | | ±2 | ±20 | pA |
| | | $T_A$ = –40°C to +125°C | | | | ±2 | nA |
| **NOISE** | | | | | | | |
| $E_n$ | Input voltage noise | (V–) – 0.1 V < $V_{CM}$ < (V+) – 3 V, f = 0.1 Hz to 10 Hz | | | 1.3 | | $µV_{PP}$ |
| | | (V+) – 1.5 V < $V_{CM}$ < (V+) + 0.1 V, f = 0.1 Hz to 10 Hz | | | 4 | | |
| $e_n$ | Input voltage noise density | (V–) – 0.1 V < $V_{CM}$ < (V+) – 3 V | f = 100 Hz | | 10.5 | | $nV/\sqrt{Hz}$ |
| | | | f = 1 kHz | | 5.5 | | |
| | | (V+) – 1.5 V < $V_{CM}$ < (V+) + 0.1 V | f = 100 Hz | | 32 | | |
| | | | f = 1 kHz | | 12.5 | | |
| $i_n$ | Input current noise density | f = 1 kHz | | | 1.5 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | (V–) – 0.1 V < $V_{CM}$ < (V+) – 3 V | | 94 | 110 | | dB |
| | | | $T_A$ = –40°C to +125°C | 90 | 104 | | |
| | | (V+) – 1.5 V < $V_{CM}$ < (V+) | | 100 | 120 | | |
| | | | $T_A$ = –40°C to +125°C | 84 | 100 | | |
| | | (V+) – 3 V < $V_{CM}$ < (V+) – 1.5 V | | | See Section 5.9 | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $Z_{ID}$ | Differential | | | | 100 \|\| 1.6 | | MΩ \|\| pF |
| $Z_{IC}$ | Common-mode | | | | 1 \|\| 6.4 | | $10^{13}$Ω \|\| pF |

## 5.8 Electrical Characteristics: $V_S$ = ±2.25 V to ±4 V ($V_S$ = 4.5 V to 8 V) (continued)

at $T_A$ = +25°C, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | (V–) + 0.6 V < $V_O$ < (V+) – 0.6 V, $R_L$ = 2 kΩ | | 110 | 120 | | dB |
| | | | $T_A$ = –40°C to +125°C | 100 | 114 | | |
| | | (V–) + 0.3 V < $V_O$ < (V+) – 0.3 V, $R_L$ = 10 kΩ | | 110 | 126 | | dB |
| | | | $T_A$ = –40°C to +125°C | 110 | 120 | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Unity gain bandwidth | | | | 10 | | MHz |
| SR | Slew rate | G = 1, 5-V step | | | 20 | | V/µs |
| $t_s$ | Settling time | To 0.01%, $V_S$ = ±3 V, G = 1, 5-V step | | | 1 | | µs |
| $t_{OR}$ | Overload recovery time | $V_{IN}$ × G = $V_S$ | | | 200 | | ns |
| | Crosstalk | OPA4197-Q1 at dc | | | 150 | | dB |
| | | OPA4197-Q1, f = 100 kHz | | | 130 | | dB |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing from rail | Positive rail | No load | | 5 | 15 | mV |
| | | | $R_L$ = 10 kΩ | | 95 | 110 | |
| | | | $R_L$ = 2 kΩ | | 430 | 500 | |
| | | Negative rail | No load | | 5 | 15 | |
| | | | $R_L$ = 10 kΩ | | 95 | 110 | |
| | | | $R_L$ = 2 kΩ | | 430 | 500 | |
| $I_{SC}$ | Short-circuit current | | | | ±65 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | | See Section 5.9 | | |
| $Z_O$ | Open-loop output impedance | f = 1 MHz, $I_O$ = 0 A; see Figure 5-29 | | | 375 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 A | | | 1 | 1.2 | mA |
| | | | $T_A$ = –40°C to +125°C | | | 1.5 | |
| **TEMPERATURE** | | | | | | | |
| | Thermal protection | | | | 140 | | °C |

## 5.9 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)

**Table 5-1. Table of Graphs**

| DESCRIPTION | FIGURE |
|---|---|
| Offset Voltage Production Distribution | Figure 5-1 to Figure 5-6 |
| Offset Voltage Drift Distribution | Figure 5-7 to Figure 5-8 |
| Offset Voltage vs Temperature | Figure 5-9 |
| Offset Voltage vs Common-Mode Voltage | Figure 5-10 to Figure 5-12 |
| Offset Voltage vs Power Supply | Figure 5-13 |
| Open-Loop Gain and Phase vs Frequency | Figure 5-14 |
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## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)

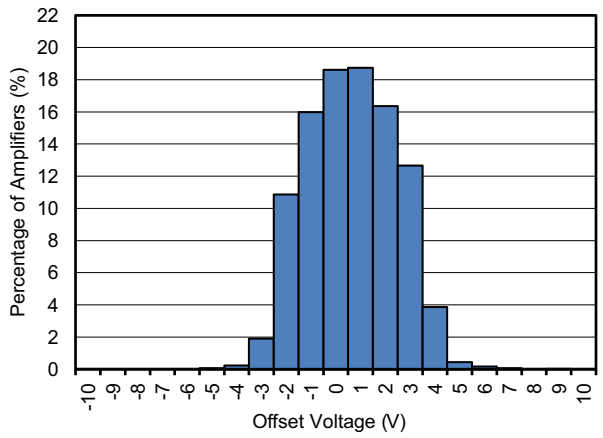
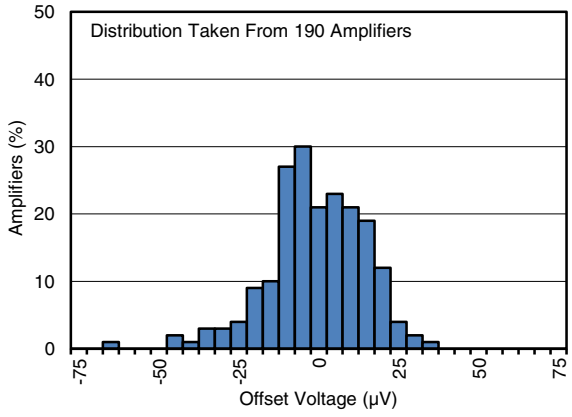
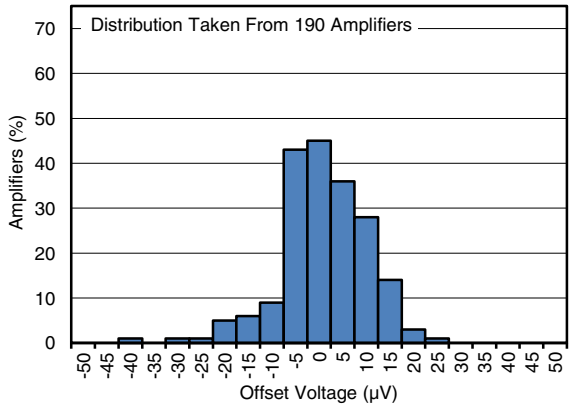



**Figure 5-1. Offset Voltage Production Distribution at 25°C**



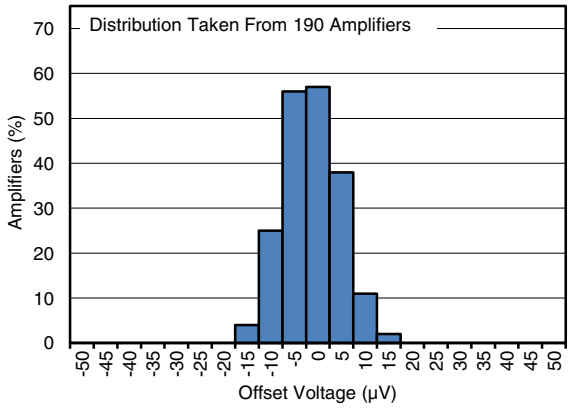

$T_A$ = 125°C

**Figure 5-2. Offset Voltage Production Distribution at 125°C**



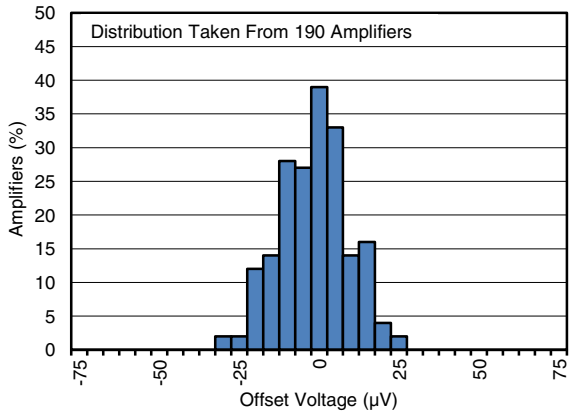

$T_A$ = 85°C

**Figure 5-3. Offset Voltage Production Distribution at 85°C**



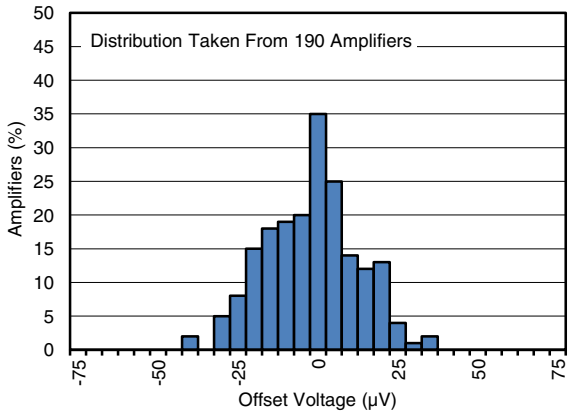

$T_A$ = 0°C

**Figure 5-4. Offset Voltage Production Distribution at 0°C**




$T_A$ = –25°C

**Figure 5-5. Offset Voltage Production Distribution at –25°C**




$T_A$ = –40° C

**Figure 5-6. Offset Voltage Production Distribution at –40°C**

## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)

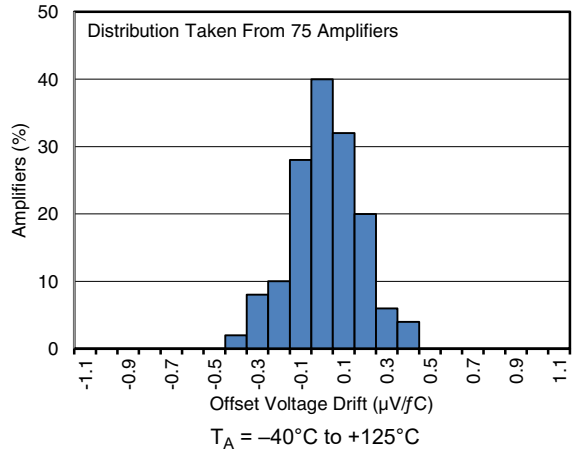



**Figure 5-7. Offset Voltage Drift Distribution from –40°C to +125°C**

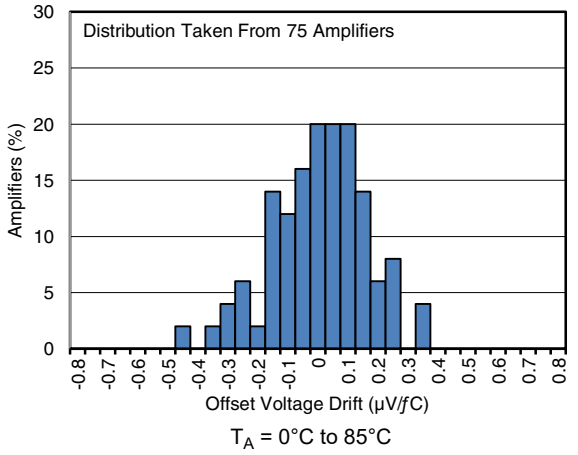



**Figure 5-8. Offset Voltage Drift Distribution from 0°C to 85°C**

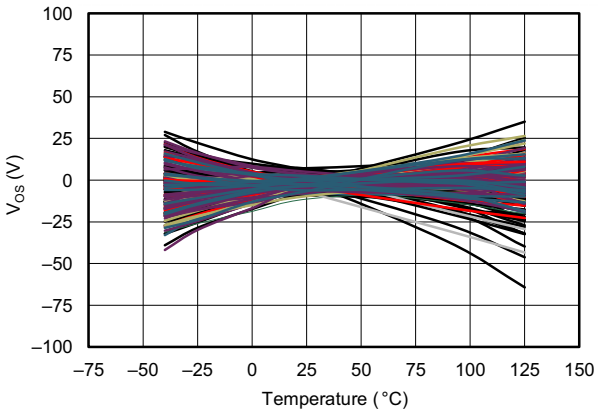



**Figure 5-9. Offset Voltage vs Temperature**

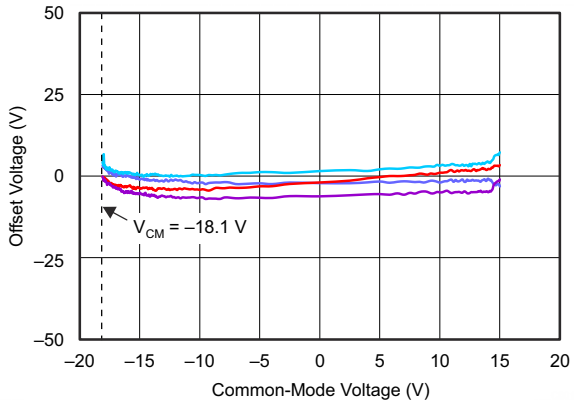



**Figure 5-10. Offset Voltage vs Common-Mode Voltage**

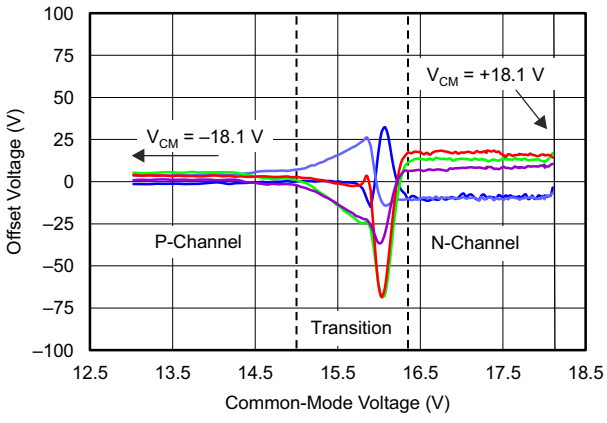



**Figure 5-11. Offset Voltage vs Common-Mode Voltage**

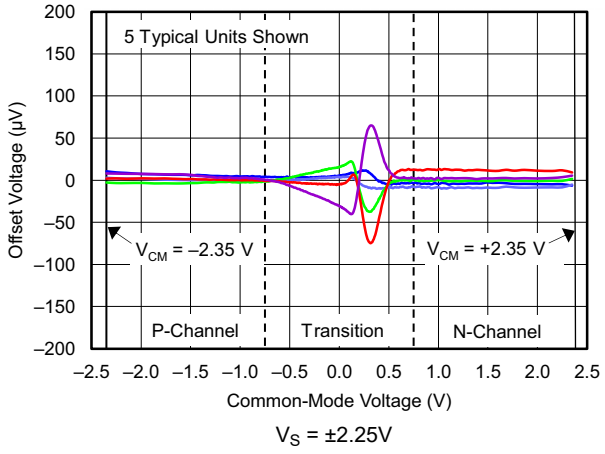
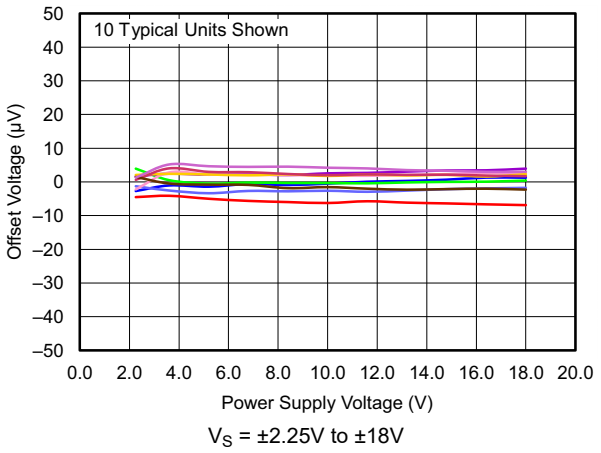



**Figure 5-12. Offset Voltage vs Common-Mode Voltage**

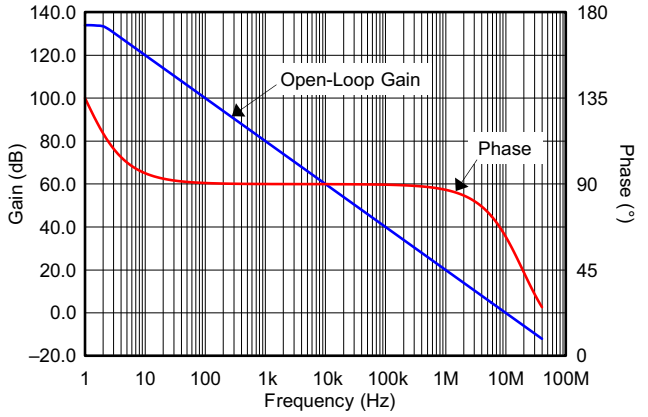
## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)




$V_S$ = ±2.25V to ±18V

**Figure 5-13. Offset Voltage vs Power Supply**




$C_{LOAD}$ = 15pF

**Figure 5-14. Open-Loop Gain and Phase vs Frequency**

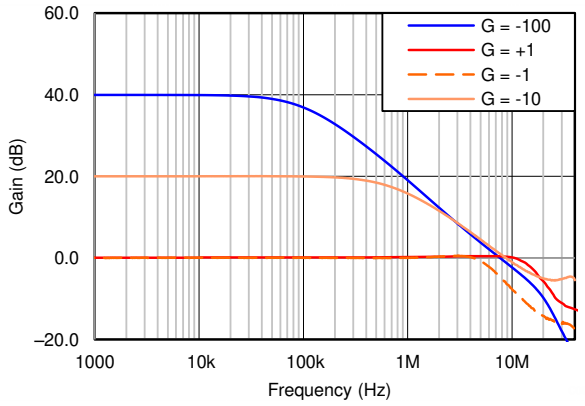



**Figure 5-15. Closed-Loop Gain and Phase vs Frequency**

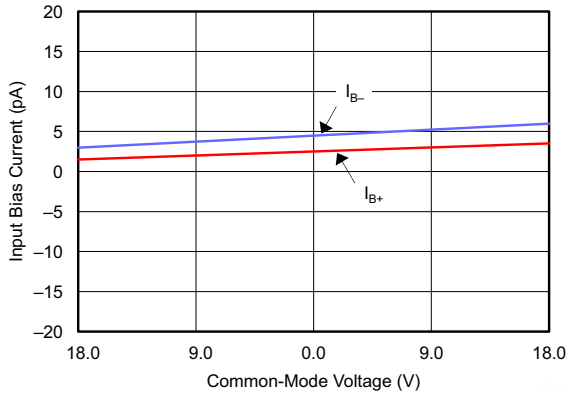



**Figure 5-16. Input Bias Current vs Common-Mode Voltage**

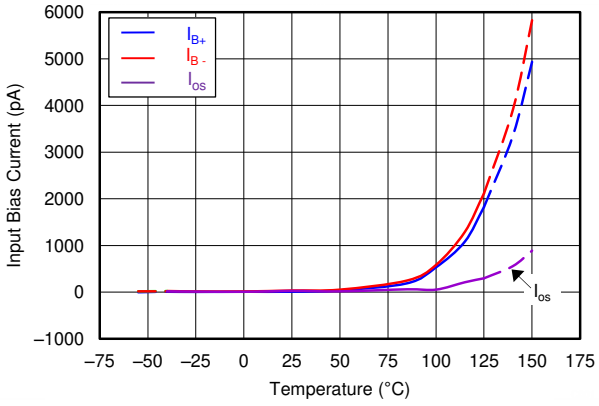



**Figure 5-17. Input Bias Current vs Temperature**

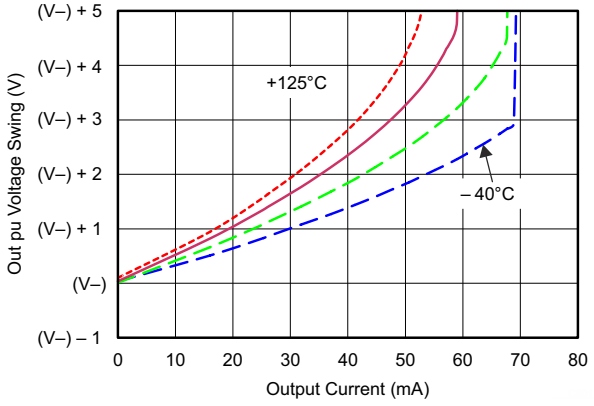



**Figure 5-18. Output Voltage Swing vs Output Current (Maximum Supply)**

## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)

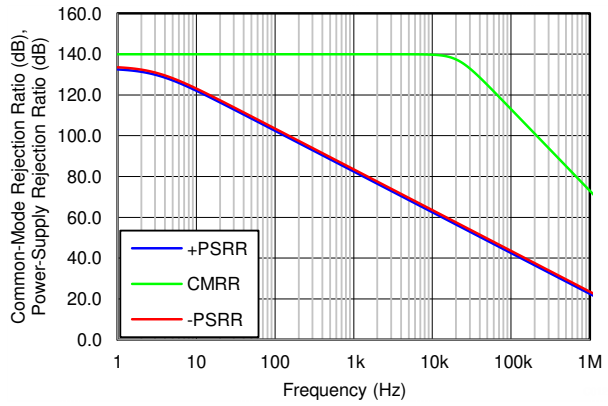



**Figure 5-19. CMRR and PSRR vs Frequency**

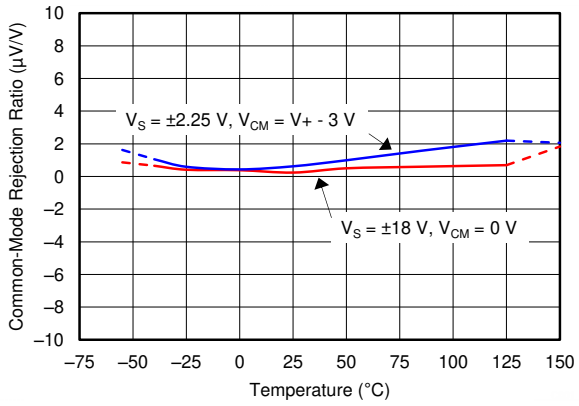



**Figure 5-20. CMRR vs Temperature**

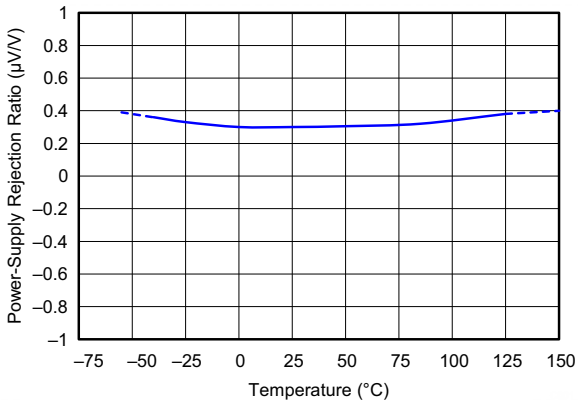



**Figure 5-21. PSRR vs Temperature**

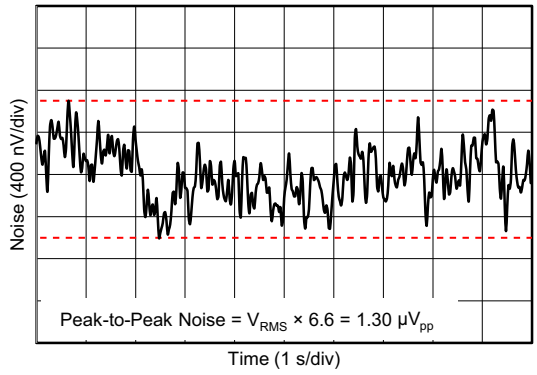



**Figure 5-22. 0.1Hz to 10Hz Noise**

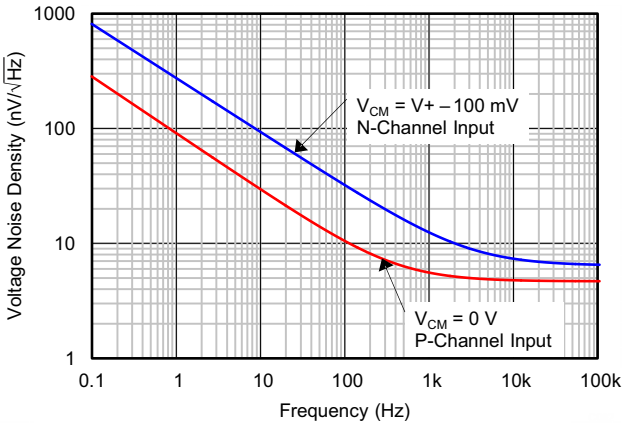



**Figure 5-23. Input Voltage Noise Spectral Density vs Frequency**

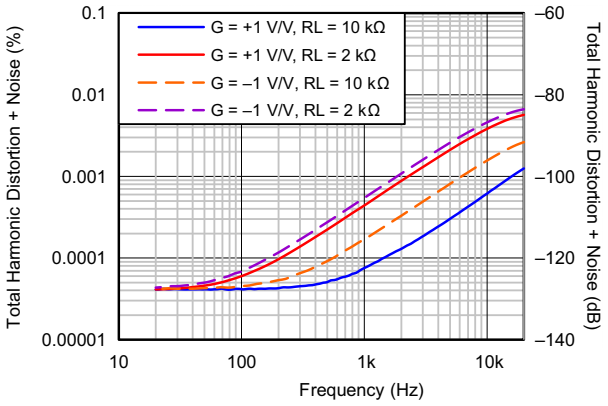



**Figure 5-24. THD+N Ratio vs Frequency**

## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)

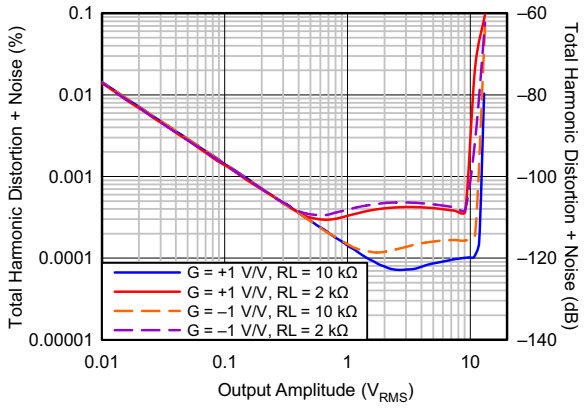



**Figure 5-25. THD+N vs Output Amplitude**

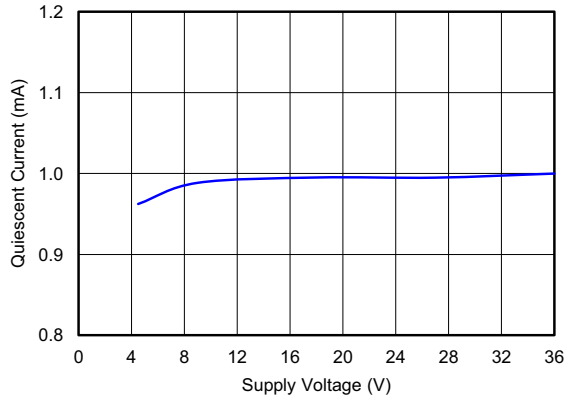



**Figure 5-26. Quiescent Current vs Supply Voltage**

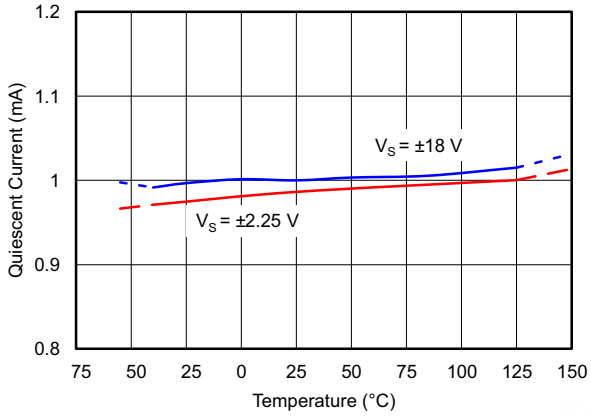



**Figure 5-27. Quiescent Current vs Temperature**

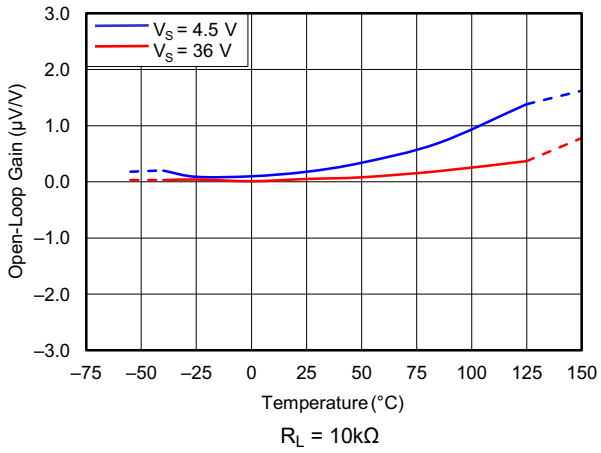



**Figure 5-28. Open-Loop Gain vs Temperature**

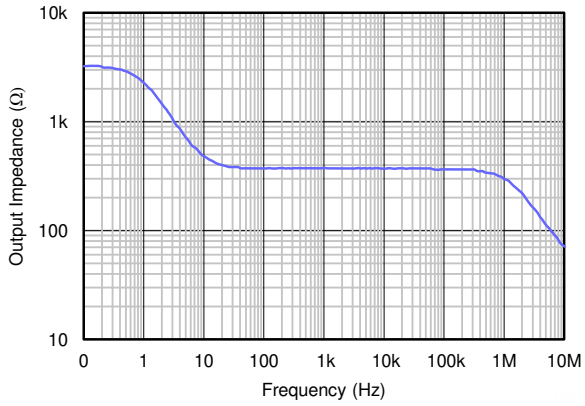



**Figure 5-29. Open-Loop Output Impedance vs Frequency**

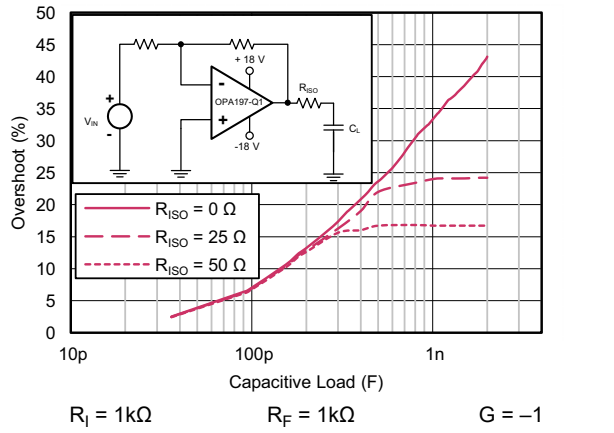
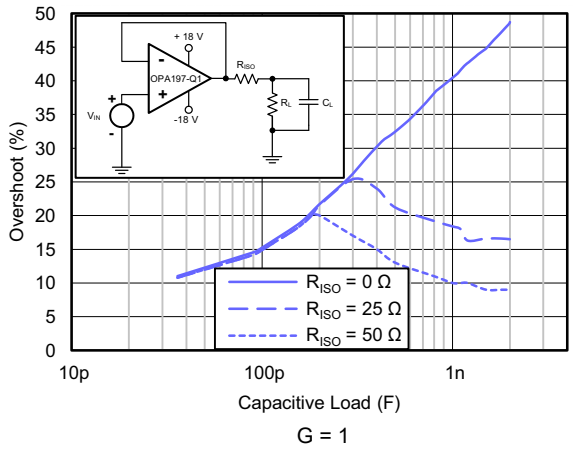



**Figure 5-30. Small-Signal Overshoot vs Capacitive Load (100mV Output Step)**

## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)




G = 1

**Figure 5-31. Small-Signal Overshoot vs Capacitive Load (100mV Output Step)**

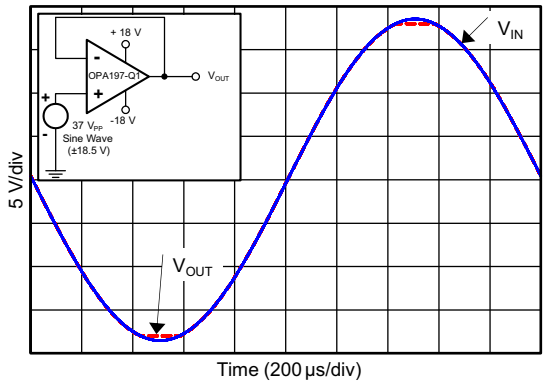
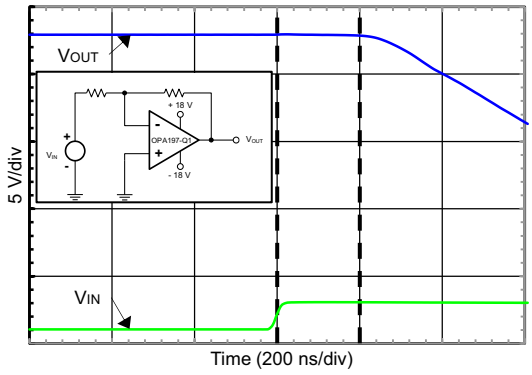
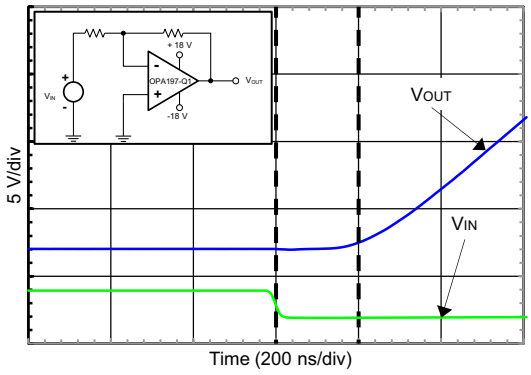



**Figure 5-32. No Phase Reversal**



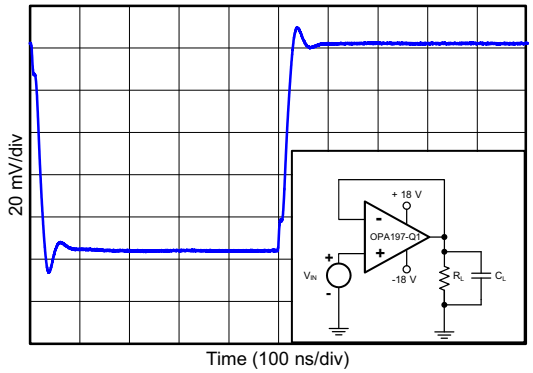

RI = 1kΩ RF = 10kΩ G = –10

**Figure 5-33. Positive Overload Recovery**



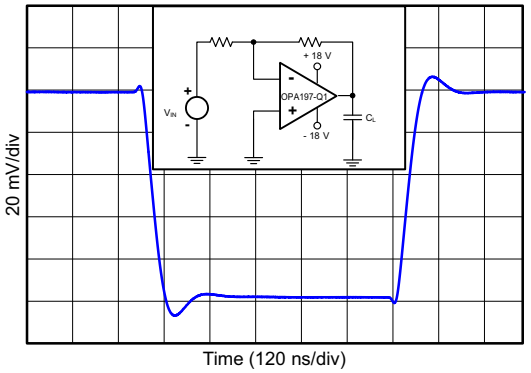

RI = 1kΩ G = –10 RF = 10kΩ

**Figure 5-34. Negative Overload Recovery**




CL = 10pF G = 1

**Figure 5-35. Small-Signal Step Response (100mV)**




RL = 1kΩ CL = 10pF G = –1

**Figure 5-36. Small-Signal Step Response (100mV)**

## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)

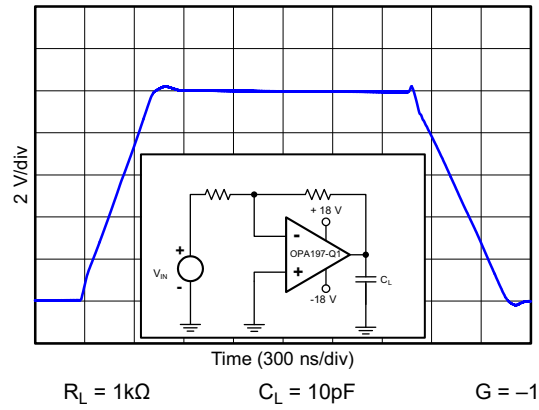



**Figure 5-37. Large-Signal Step Response**

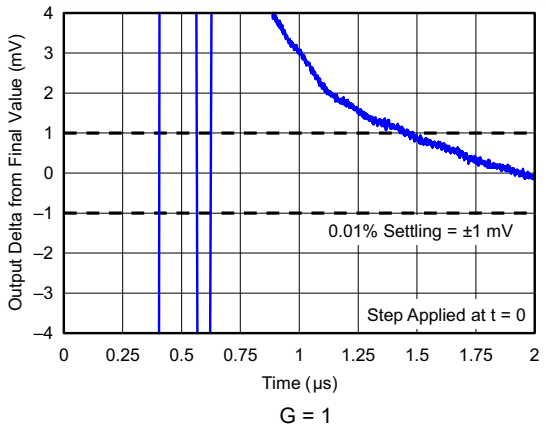



**Figure 5-38. Settling Time (10V Positive Step)**

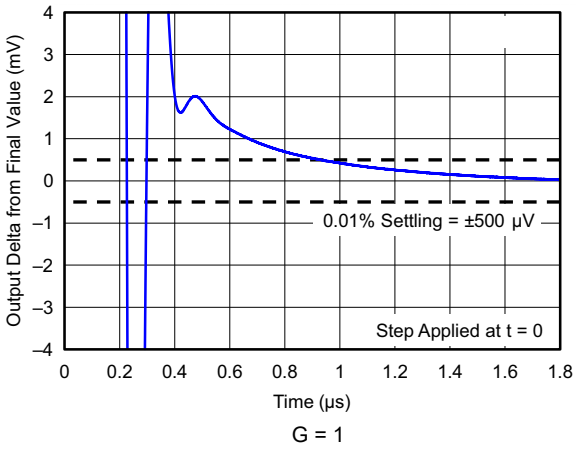



**Figure 5-39. Settling Time (5V Positive Step)**

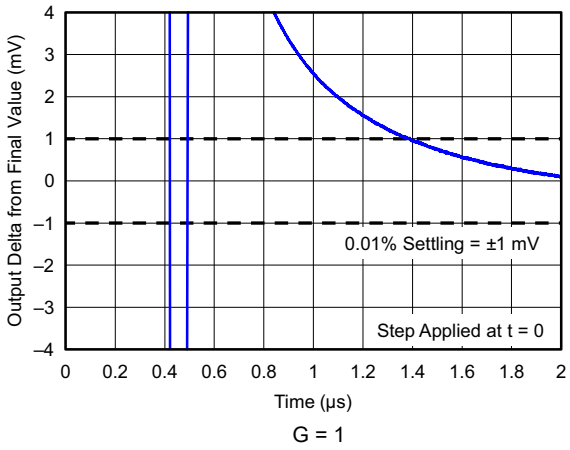



**Figure 5-40. Settling Time (10V Negative Step)**

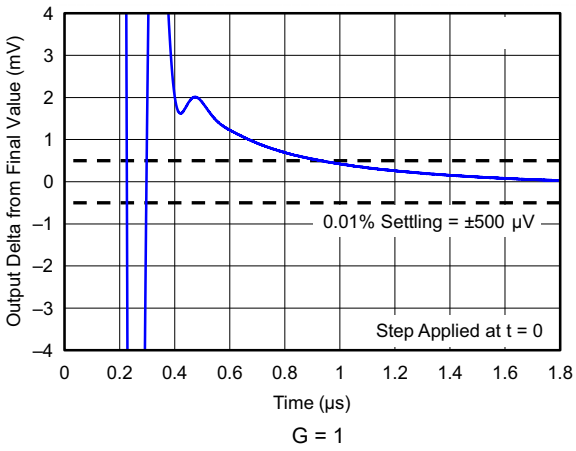



**Figure 5-41. Settling Time (5V Negative Step)**

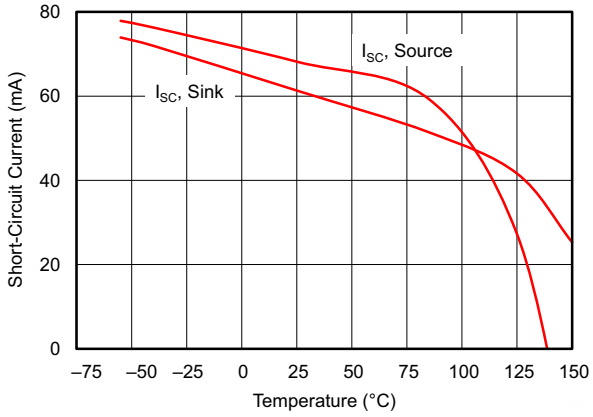



**Figure 5-42. Short-Circuit Current vs Temperature**

## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2, and $C_L$ = 100pF, (unless otherwise noted)

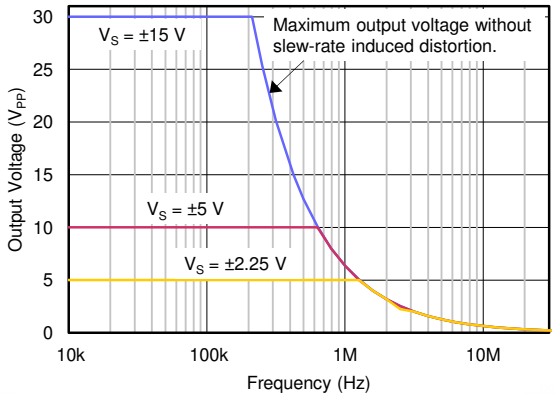



**Figure 5-43. Maximum Output Voltage vs Frequency**

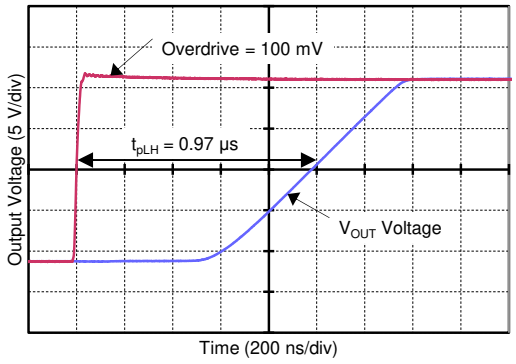



**Figure 5-44. Propagation Delay Rising Edge**

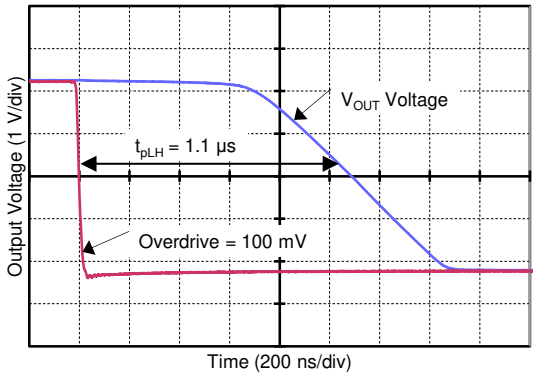



**Figure 5-45. Propagation Delay Falling Edge**

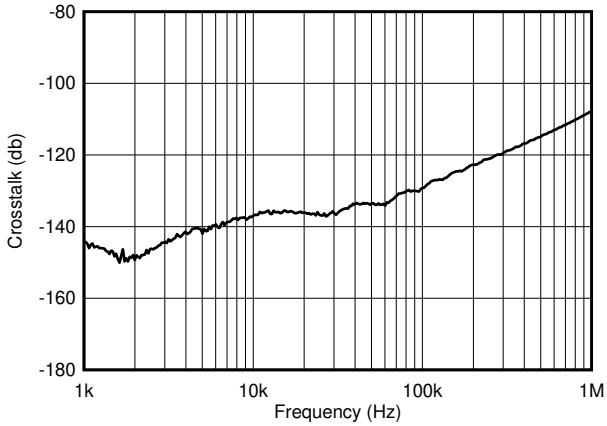



**Figure 5-46. Crosstalk vs Frequency**

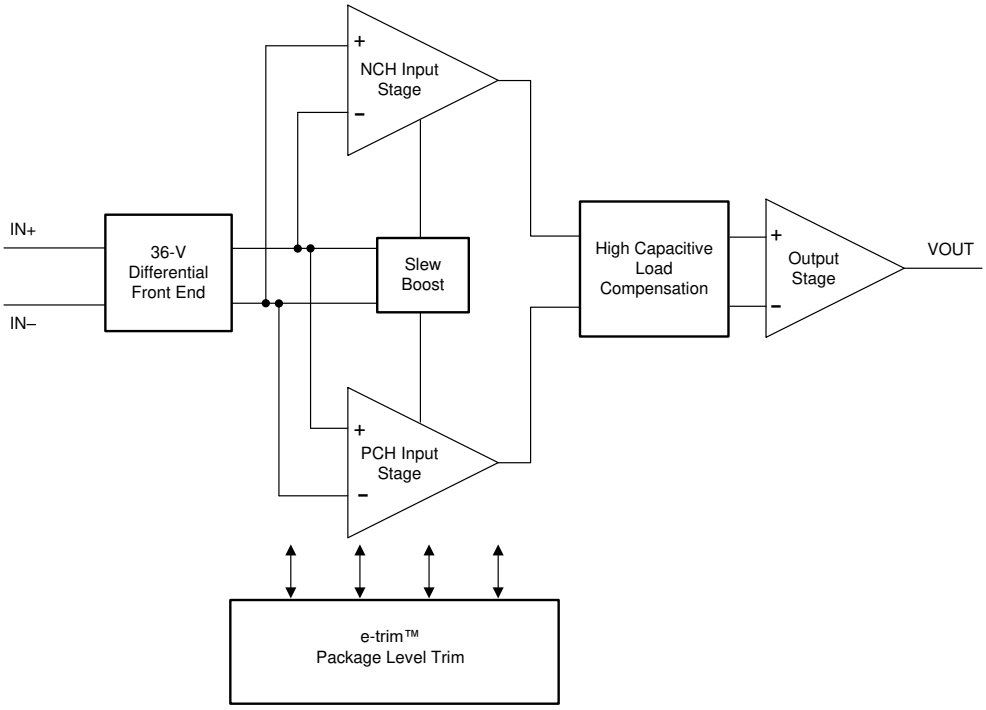
# 6 Detailed Description

## 6.1 Overview

The OPAx197-Q1 family of e-trim operational amplifiers use a proprietary method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. *Section 6.2* shows the simplified diagram of the OPAx197-Q1.

Unlike previous e-trim op amps, the OPAx197-Q1 uses a patented two-temperature trim architecture to achieve a very-low offset voltage of 25µV (maximum) and low voltage offset drift of 0.5µV/°C (maximum) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers especially useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### *6.3.1 Input Protection Circuitry*

The OPAx197-Q1 use a unique input architecture to eliminate the need for input protection diodes but still provide robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 6-1 can be activated by fast transient step responses, and can introduce signal distortion and settling-time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current, and resulting in extended settling time, as shown in Figure 6-3.

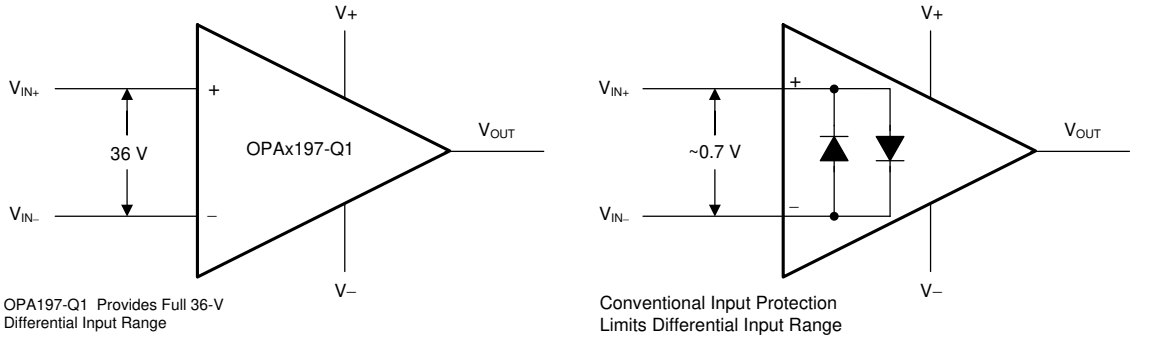





**Figure 6-1. OPAx197-Q1 Input Protection Does Not Limit Differential Input Capability**

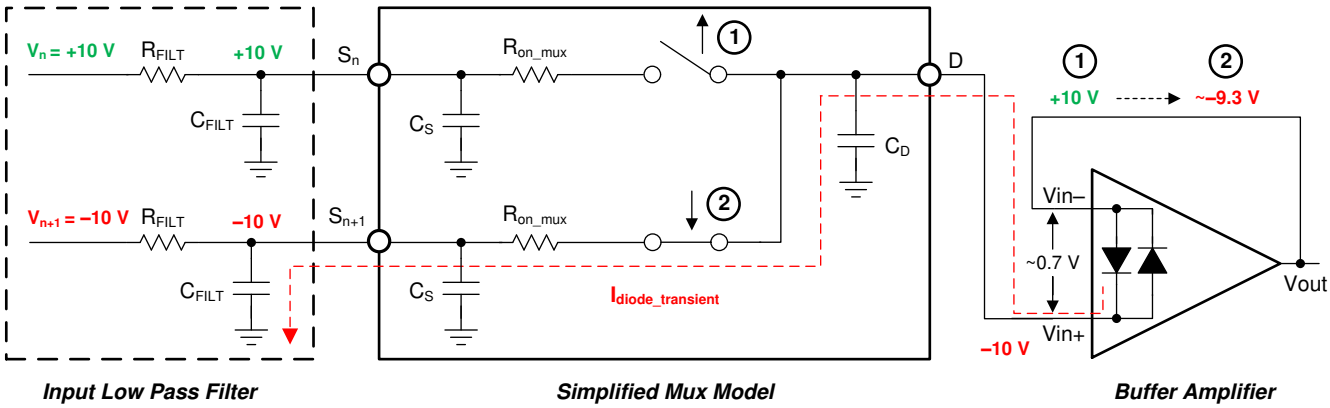



**Figure 6-2. Back-to-Back Diodes Create Settling Issues**

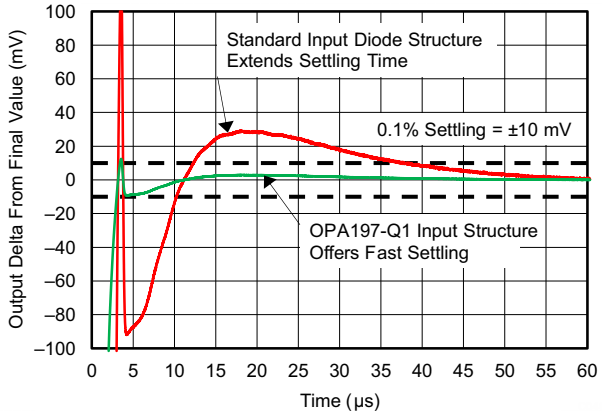



**Figure 6-3. OPAx197-Q1 Protection Circuit Maintains Fast-Settling Transient Response**

The OPAx197-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making these devices the optimal op amps for multichannel, high-switched, input applications. The OPAx197-Q1 tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36V, making these devices an excellent choice for use as comparators or in applications with fast-ramping input signals, such as multiplexed data-acquisition systems; see Figure 7-1.

### *6.3.2 EMI Rejection*

The OPAx197-Q1 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx197-Q1 benefit from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-4 shows the results of this testing on the OPAx197-Q1. Table 6-1 shows the EMIRR IN+ values for the OPAx197-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 6-1 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the TI application report *EMI Rejection Ratio of Operational Amplifiers* available for download from www.ti.com.

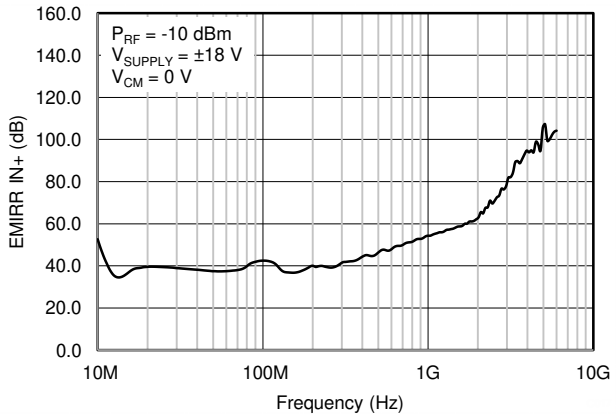



**Figure 6-4. EMIRR Testing**

**Table 6-1. OPAx197-Q1 EMIRR IN+ For Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|---|---|---|
| 400MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 44.1dB |
| 900MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications | 52.8dB |
| 1.8GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz) | 61.0dB |
| 2.4GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz) | 69.5dB |
| 3.6GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 88.7dB |
| 5GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz) | 105.5dB |

### 6.3.3 Phase Reversal Protection

The OPAx197-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx197-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 6-5.

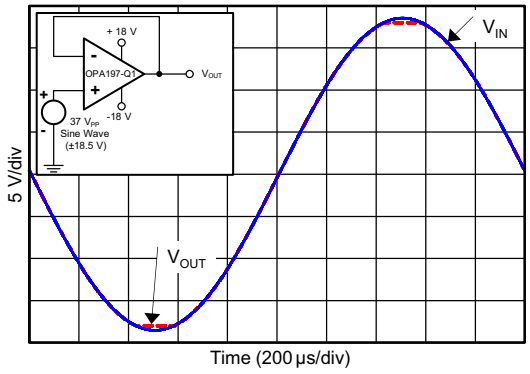



**Figure 6-5. No Phase Reversal**

### 6.3.4 Thermal Protection

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx197-Q1 is 150°C and exceeding this maximum temperature causes damage to the device. The OPAx197-Q1 have a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 6-6 shows an application example for the OPAx197-Q1 that has significant self heating (159°C) because of the power dissipation (0.81W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 6-6 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

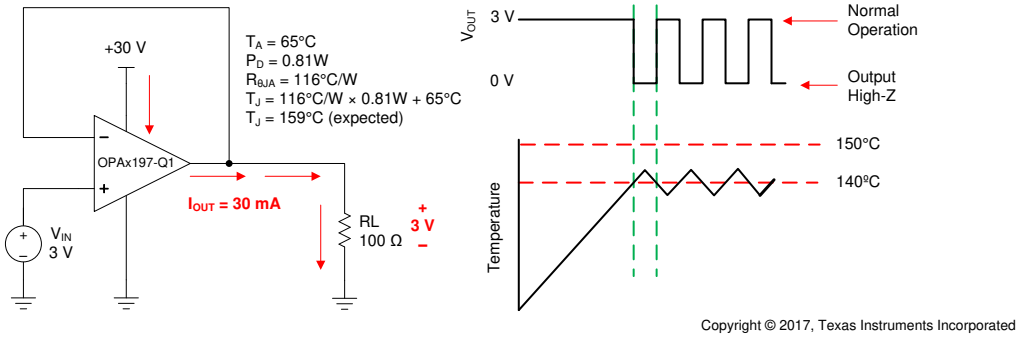



**Figure 6-6. Thermal Protection**

### 6.3.5 Capacitive Load and Stability

The OPAx197-Q1 feature a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drive up to 1nF of pure capacitive load. Increasing the gain enhances the ability of these amplifiers to drive greater capacitive loads; see Figure 6-7 and Figure 6-8. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

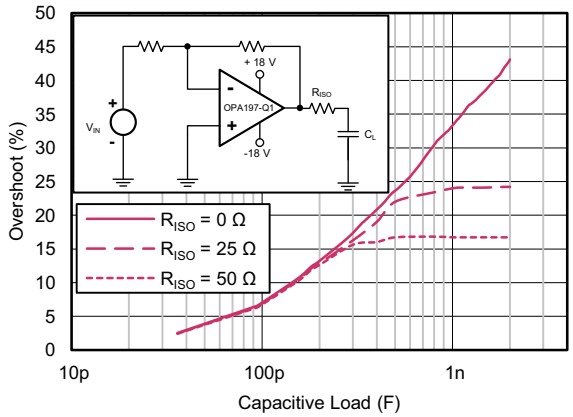



**Figure 6-7. Small-Signal Overshoot vs Capacitive Load (100mV Output Step)**

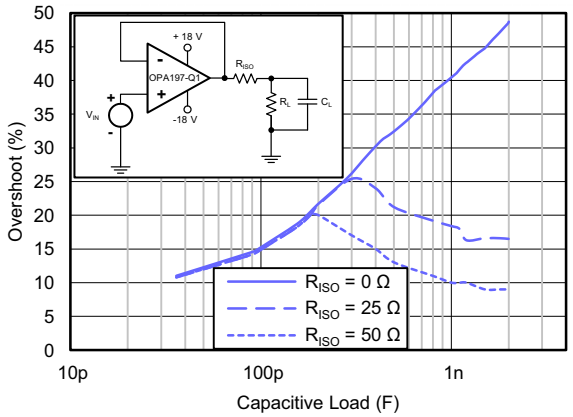



**Figure 6-8. Small-Signal Overshoot vs Capacitive Load (100mV Output Step)**

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10Ω to 20Ω) resistor, $R_{ISO}$, in series with the output, as shown in Figure 6-9. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_{ISO}$ / $R_L$, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx197-Q1 a great choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 6-9 uses an isolation resistor, $R_{ISO}$, to stabilize the output of an op amp. $R_{ISO}$ modifies the open-loop gain of the system for increased phase margin, and results using the OPAx197-Q1 are summarized in Table 6-2. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIPD128 details complete design goals, simulation, and test results.

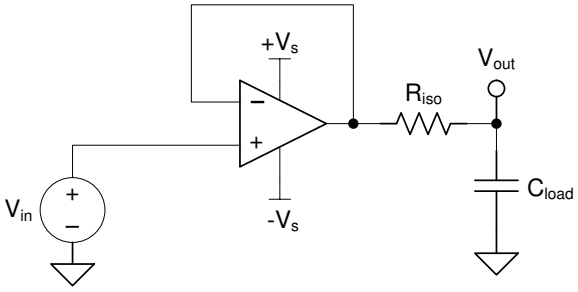



**Figure 6-9. Extending Capacitive Load Drive With the OPAx197-Q1**

**Table 6-2. OPAx197-Q1 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results**

| PARAMETER | VALUE | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Capacitive Load** | 100pF | | 1000pF | | 0.01µF | | 0.1µF | | 1µF | |
| **Phase Margin** | 45° | 60° | 45° | 60° | 45° | 60° | 45° | 60° | 45° | 60° |
| **$R_{ISO}$ (Ω)** | 47 | 360 | 24 | 100 | 20 | 51 | 6.2 | 15.8 | 2 | 4.7 |
| **Measured Overshoot (%)** | 23.2 8.6 | 10.4 | 22.5 | 9 | 22.1 | 8.7 | 23.1 | 8.6 | 21 | 8.6 |
| **Calculated PM** | 45.1° | 58.1° | 45.8° | 59.7° | 46.1° | 60.1° | 45.2° | 60.2° | 47.2° | 60.2° |

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, see TI Precision Design TIPD128*Capacitive Load Drive Solution using an Isolation Resistor*.

### *6.3.6 Common-Mode Voltage Range*

The OPAx197-Q1 are 36V, true rail-to-rail input operational amplifiers with an input common-mode range that extends 100mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6-10. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3V to 100mV above the positive supply. The P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+) – 1.5V. There is a small transition region, typically ( V+) –3V to (V+) – 1.5V, in which both input pairs are on. This transition region can vary modestly with process variation, and within this region, PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

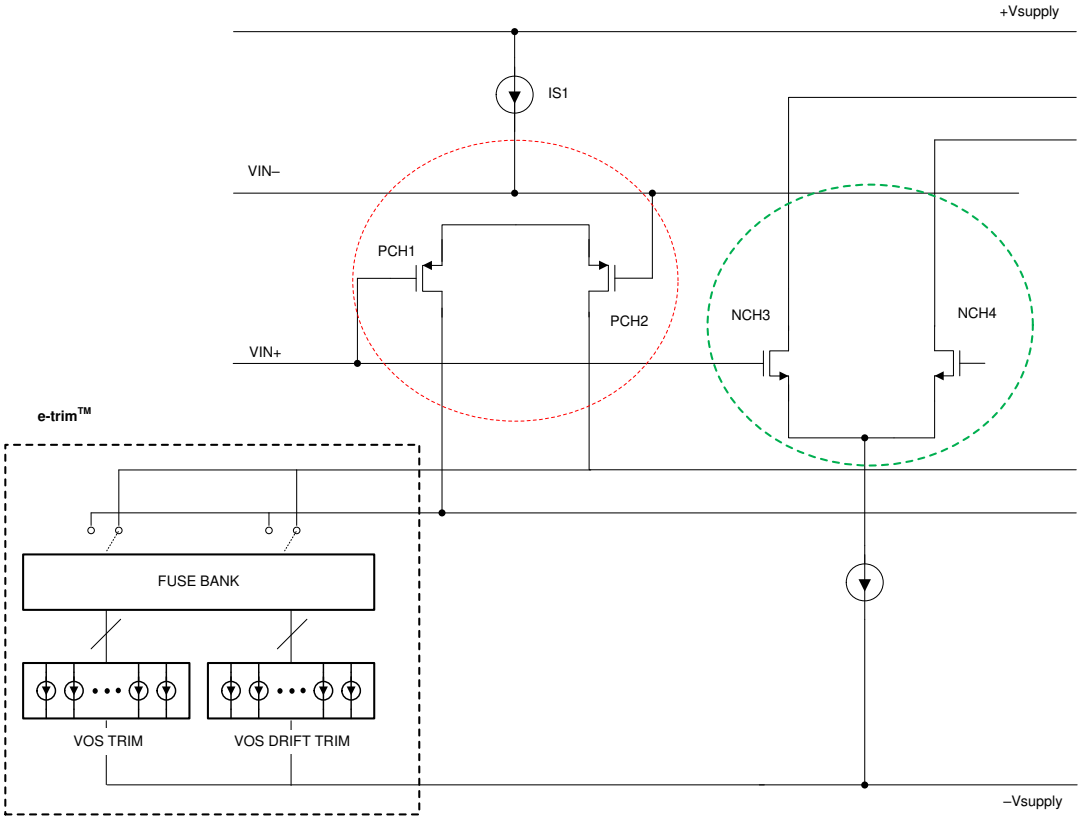



**Figure 6-10. Rail-to-Rail Input Stage**

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx197-Q1 use a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 6-11.

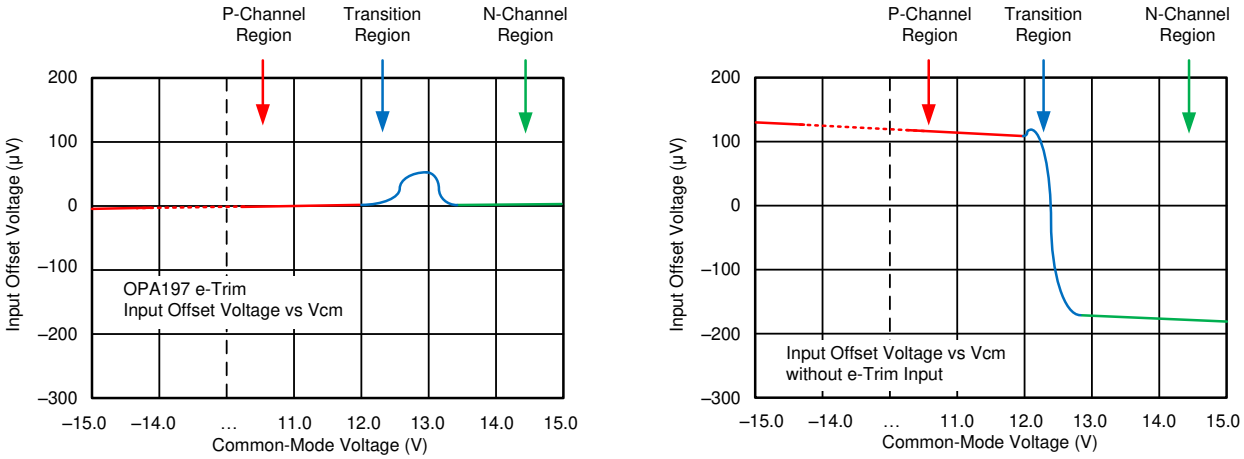



**Figure 6-11. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers**

### *6.3.7 Electrical Overstress*

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-12 shows an illustration of the ESD circuits contained in the OPAx197-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

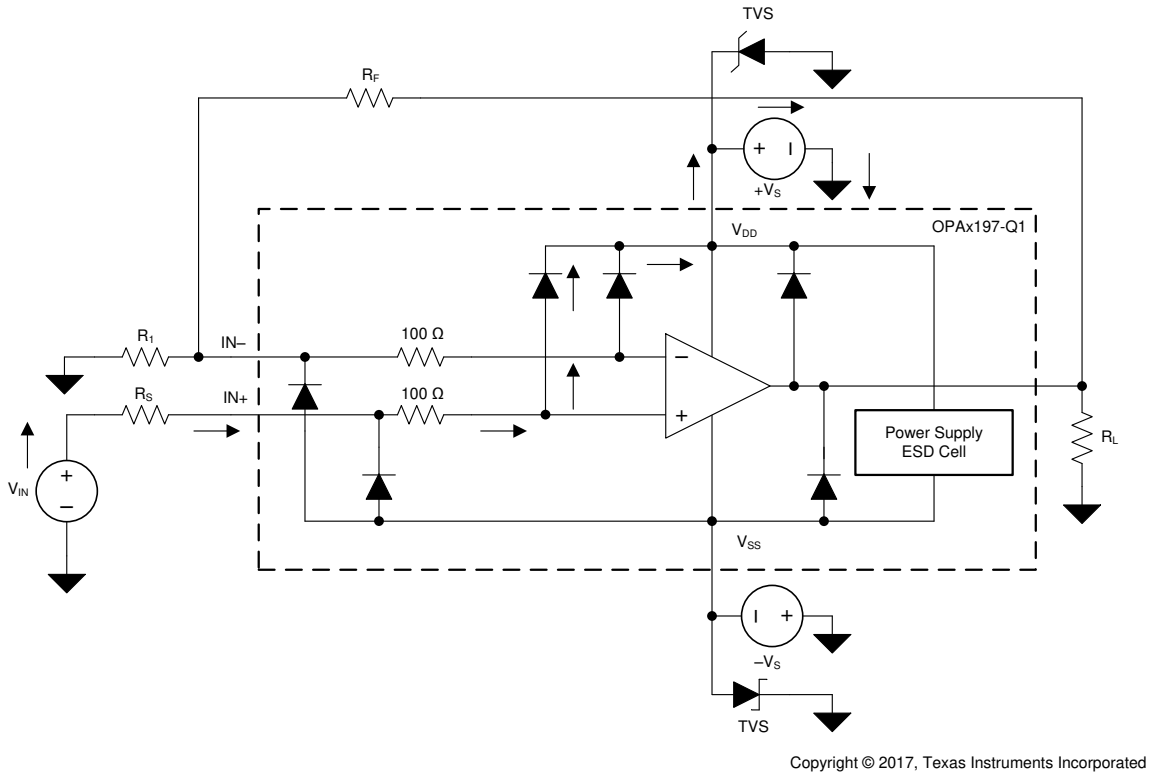





**Figure 6-12. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event is very short in duration and very high voltage (for example, 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example, 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

### *6.3.8 Overload Recovery*

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx197-Q1 is approximately 200ns.

## 6.4 Device Functional Modes

The OPAx197-Q1 have a single functional mode and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The maximum power supply voltage for the OPAx197-Q1 is 36V (±18V).

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The OPAx197-Q1 family offers outstanding dc precision and ac performance. These devices operate up to 36V supply rails and offer true rail-to-rail input and output, ultra-low offset voltage and offset voltage drift, as well as 10MHz bandwidth and high capacitive load drive. These features make the OPAx197-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

## 7.2 Typical Applications

### *7.2.1 16-Bit Precision Multiplexed Data-Acquisition System*

Figure 7-1 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the OPAx197-Q1 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

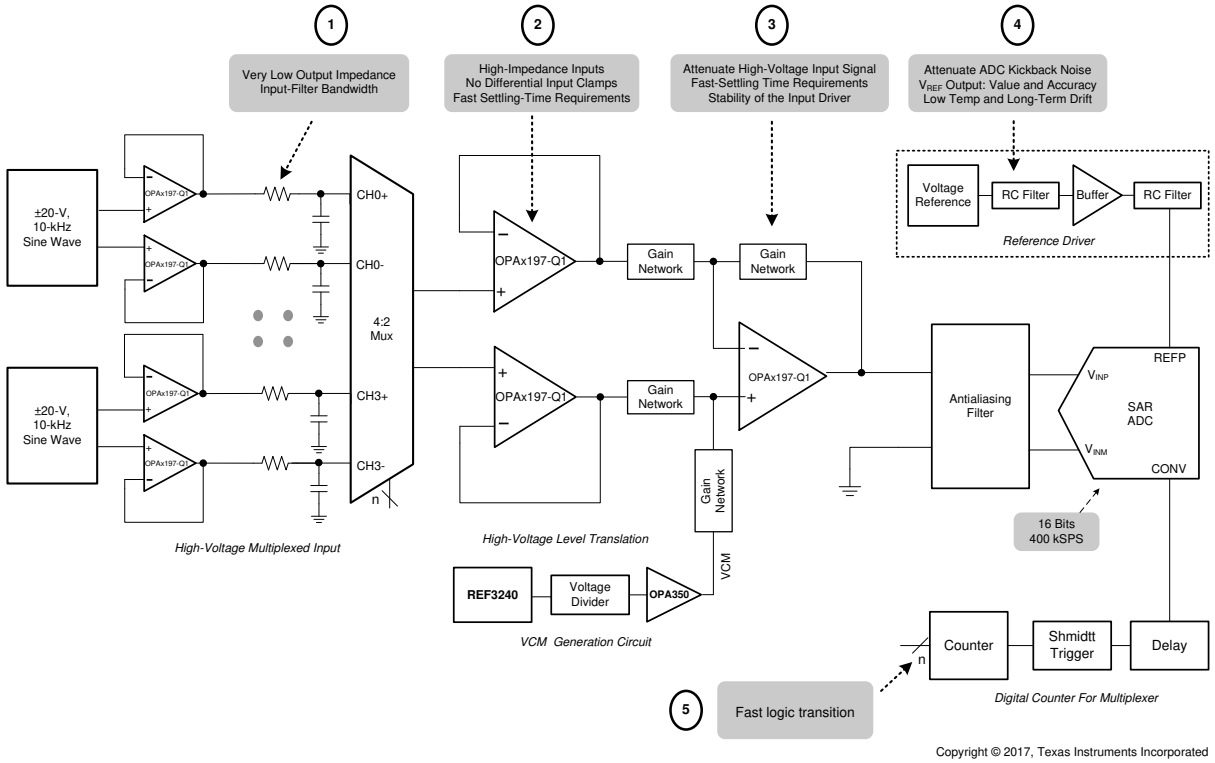



**Figure 7-1. OPAx197-Q1 in 16-Bit, 400kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion**

#### 7.2.1.1 Design Requirements

The primary objective is to design a ±20V, differential, 4-channel, multiplexed data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400kSPS for a 10kHz, full-scale, pure sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15V
- ADC supply voltage: 3.3V
- ADC sampling rate: 400kSPS
- ADC reference voltage (REFP): 4.096V
- System input signal: A high-voltage differential input signal with a peak amplitude of 10V and frequency ($f_{IN}$) of 10kHz are applied to each differential input of the multiplexer.

#### 7.2.1.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal high voltage multiplexed data acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in Figure 7-1. The circuit is a multichannel data acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, attenuating SAR ADC driver, digital counter for mux and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision multiplexed data acquisition system are the mux input analog front-end and the high-voltage level translation SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. Figure 7-1 includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely low impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input when maintaining amplifier stability. The next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

> For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD151, *16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion*.

#### 7.2.1.3 Application Curve

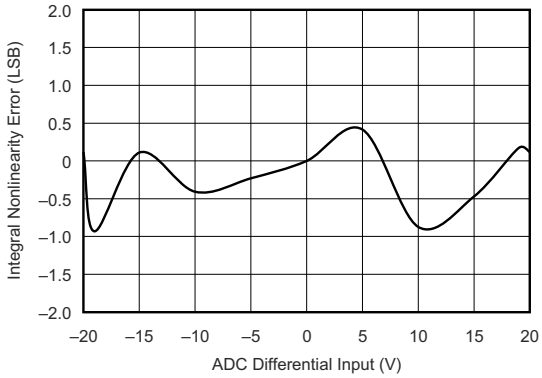



**Figure 7-2. ADC 16-Bit Linearity Error for the Multiplexed Data Acquisition Block**

### 7.2.2 Slew-Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx197-Q1 make these devices the optimal amplifiers to achieve slew-rate control for both dual- and single-supply systems.Figure 7-3 shows the OPAx197-Q1 in a slew-rate limit design.

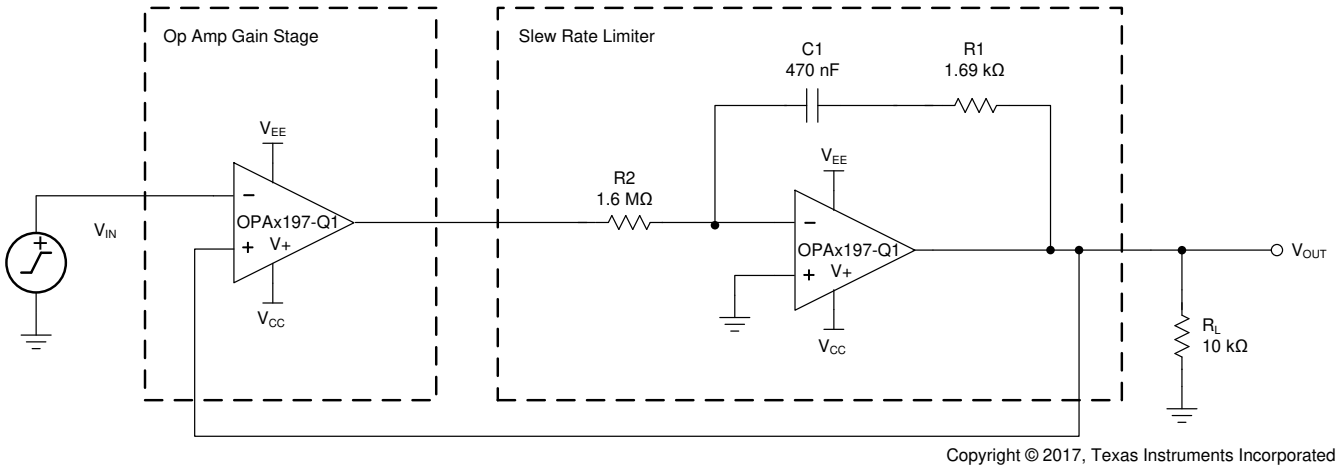





**Figure 7-3. Slew-Rate Limiter Uses One Op Amp**

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see TI Precision Design TIPD140, *Slew Rate Limiter Uses One Op Amp*.

### 7.2.3 Precision Reference Buffer

The OPAx197-Q1 feature high output-current-drive capability and low input offset voltage, making these devices an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10µF ceramic capacitor shown in Figure 7-4, a 37.4Ω isolation resistor ($R_{ISO}$), provides separation of two feedback paths for optimal stability. Feedback path number one is through $R_F$ and is directly at the output ($V_{OUT}$). Feedback path number two is through $R_{Fx}$ and $C_F$ and is connected at the output of the op amp. The optimized stability components shown for the 10µF load give a closed-loop signal bandwidth at $V_{OUT}$ of 4kHz and still provide a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: $R_F$, $R_{Fx}$ , $C_F$ , and $R_{ISO}$.

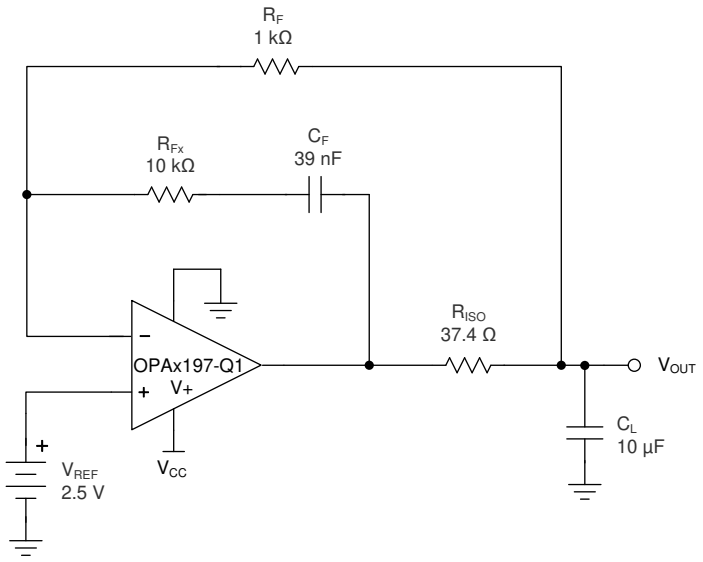





**Figure 7-4. Precision Reference Buffer**

## 7.3 Power Supply Recommendations

The OPAx197-Q1 are specified for operation from 4.5V to 36V (±2.25V to ±18V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 5.9*.

**CAUTION**

Supply voltages larger than 40V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 7.4*.

## 7.4 Layout

### 7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.

  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 7-6, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

### 7.4.2 Layout Examples

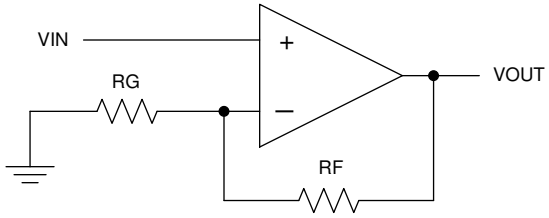



**Figure 7-5. Schematic Representation**

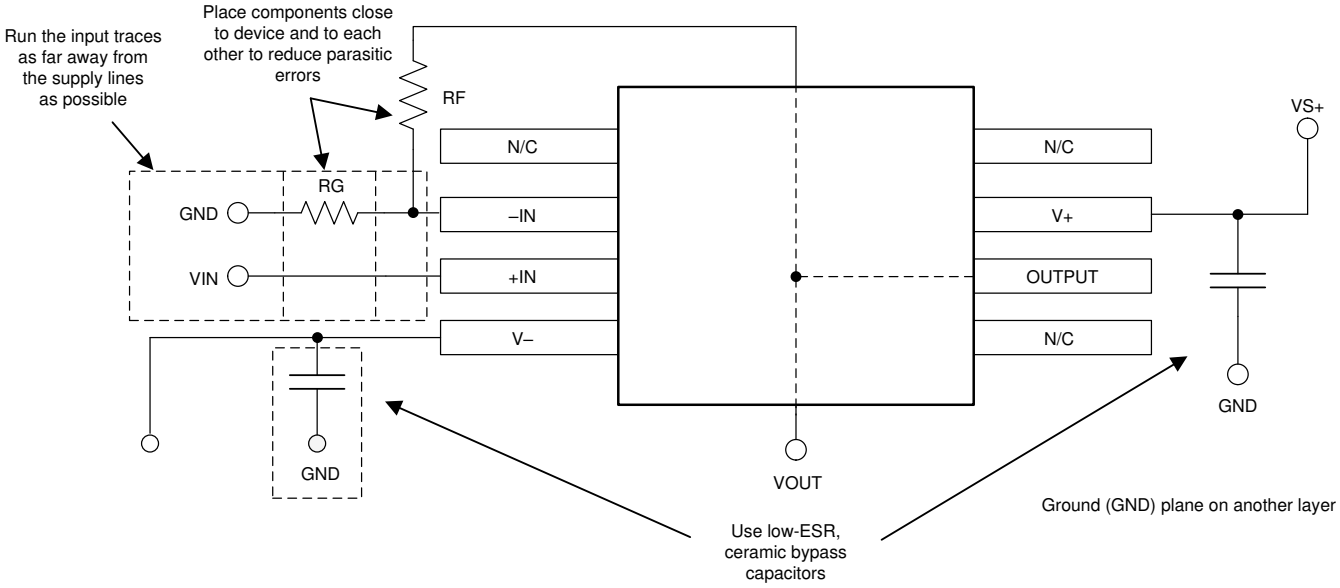



**Figure 7-6. Operational Amplifier Board Layout for Noninverting Configuration**

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

#### 8.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ simulation software is a free, fully functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**Note**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

#### 8.1.1.2 TI Precision Designs

The OPA197 is featured in several Texas Instruments (TI) Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

## 8.2 Documentation Support

### *8.2.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Capacitive Load Drive Solution using an Isolation Resistor* reference design

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

### 8.5 Trademarks

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### 8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (January 2021) to Revision B (June 2026) | Page |
|---|---|
| • Added OPA4197-Q1 D package, 14-pin SOIC, production data | 1 |

| Changes from Revision * (March 2018) to Revision A (January 2021) | Page |
|---|---|
| • Added OPA4197-Q1 and associated content | 1 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| OPA197QDGKRQ1 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 197 |
| OPA197QDGKRQ1.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 197 |
| OPA2197QDGKRQ1 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2197 |
| OPA2197QDGKRQ1.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2197 |
| OPA4197QDRQ1 | Active | Production | SOIC (D) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O4197QD |
| OPA4197QPWRQ1 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | O4197Q |
| OPA4197QPWRQ1.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | O4197Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF OPA197-Q1, OPA2197-Q1, OPA4197-Q1 :**

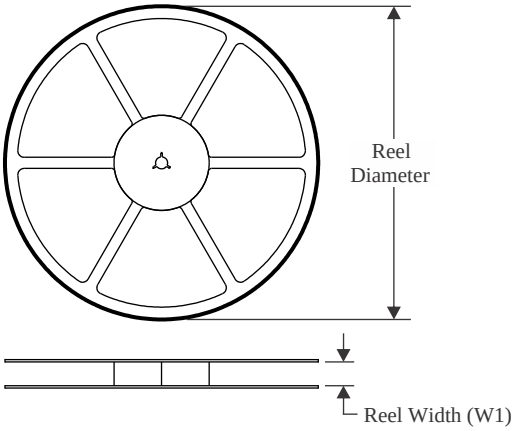
- Catalog : OPA197, OPA2197, OPA4197

NOTE: Qualified Version Definitions:

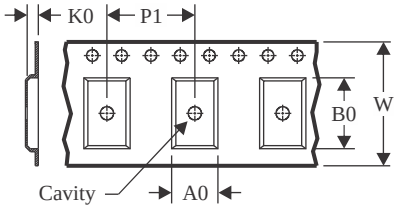
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

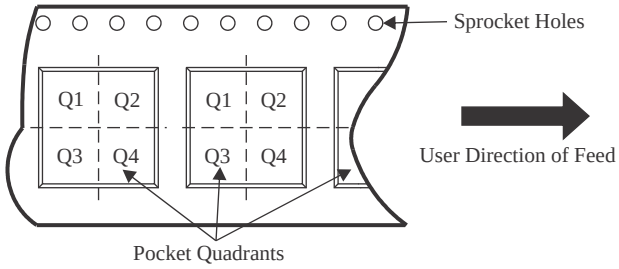



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

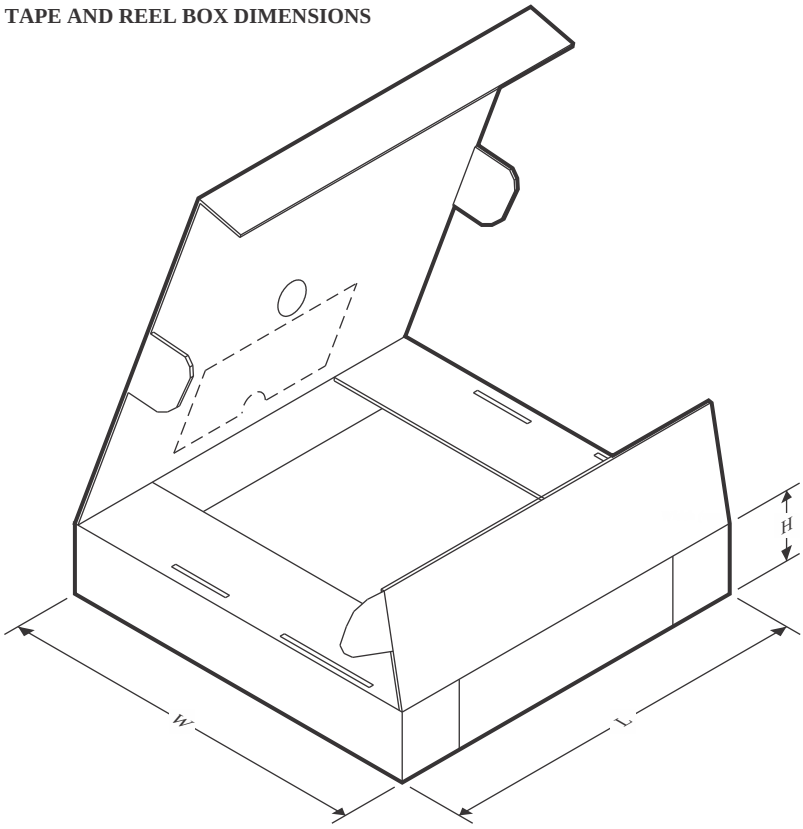
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA197QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2197QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA4197QDRQ1 | SOIC | D | 14 | 3000 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| OPA4197QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

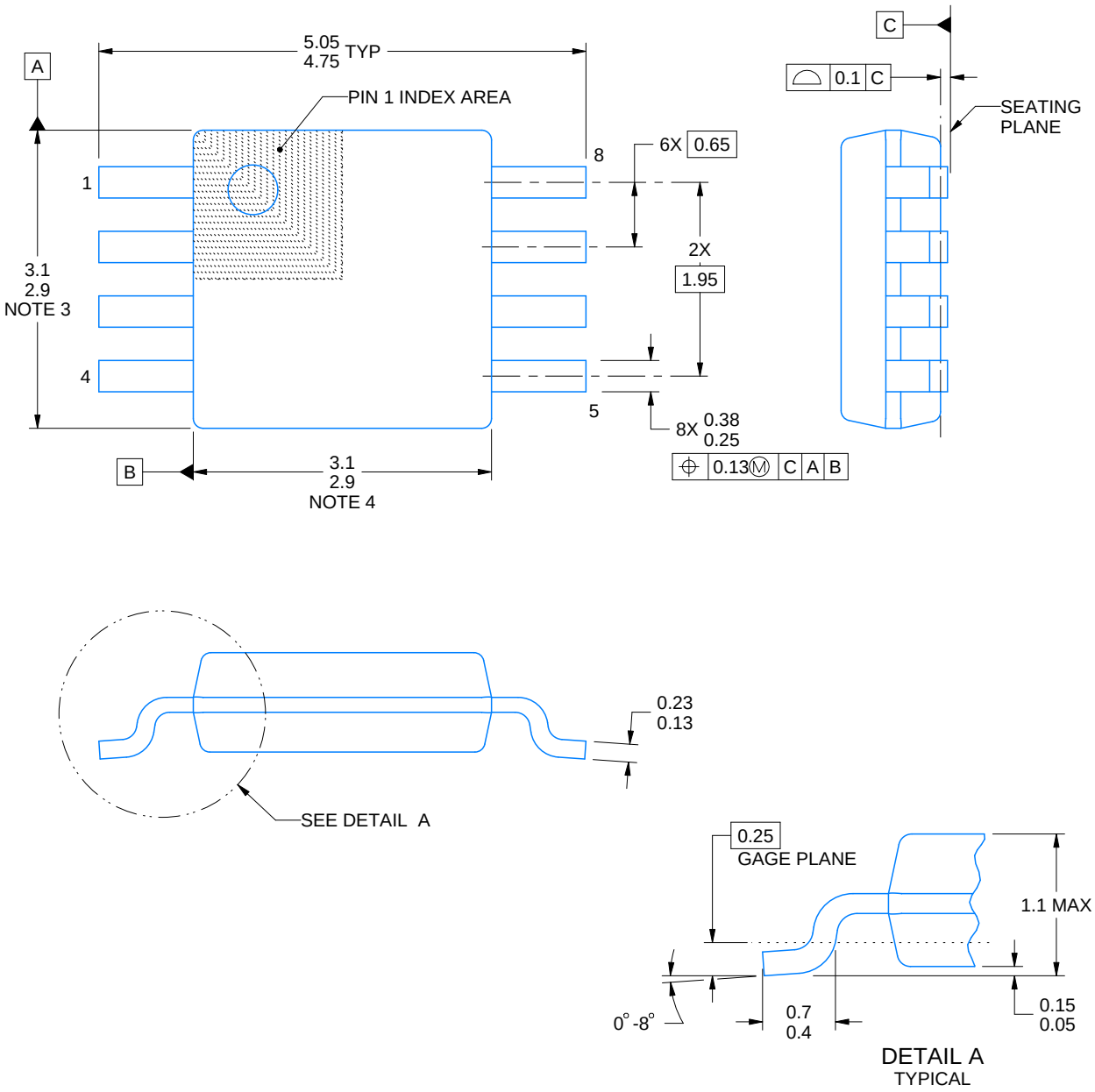
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA197QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2197QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA4197QDRQ1 | SOIC | D | 14 | 3000 | 353.0 | 353.0 | 32.0 |
| OPA4197QPWRQ1 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

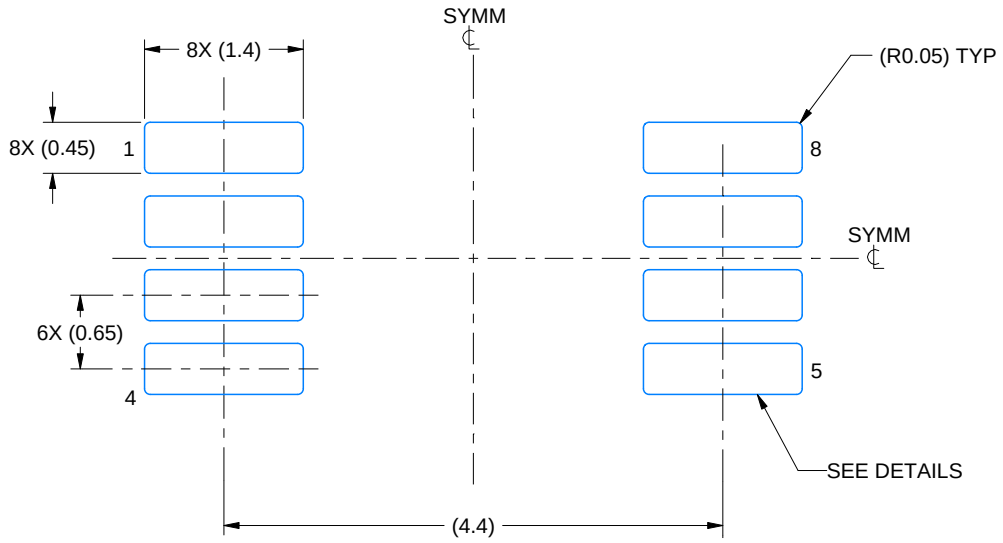
SMALL OUTLINE PACKAGE



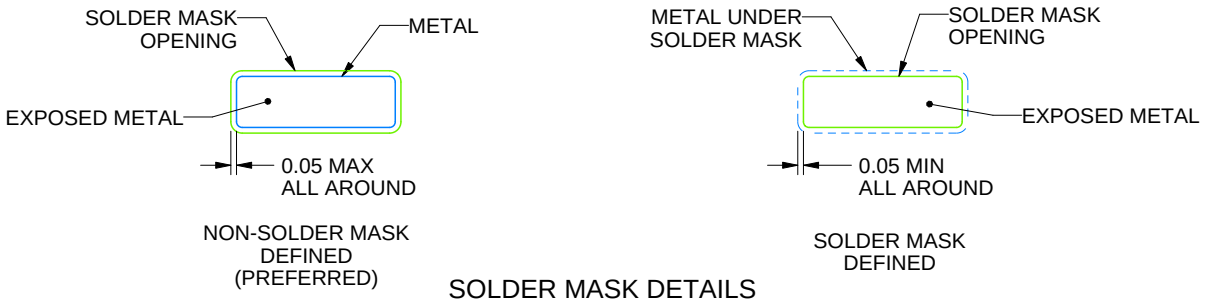

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

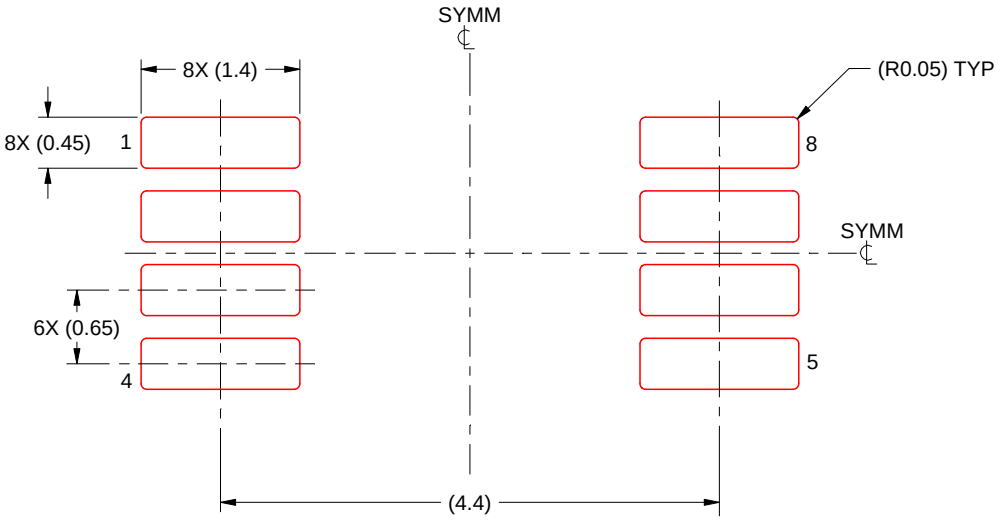



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

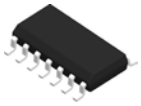



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

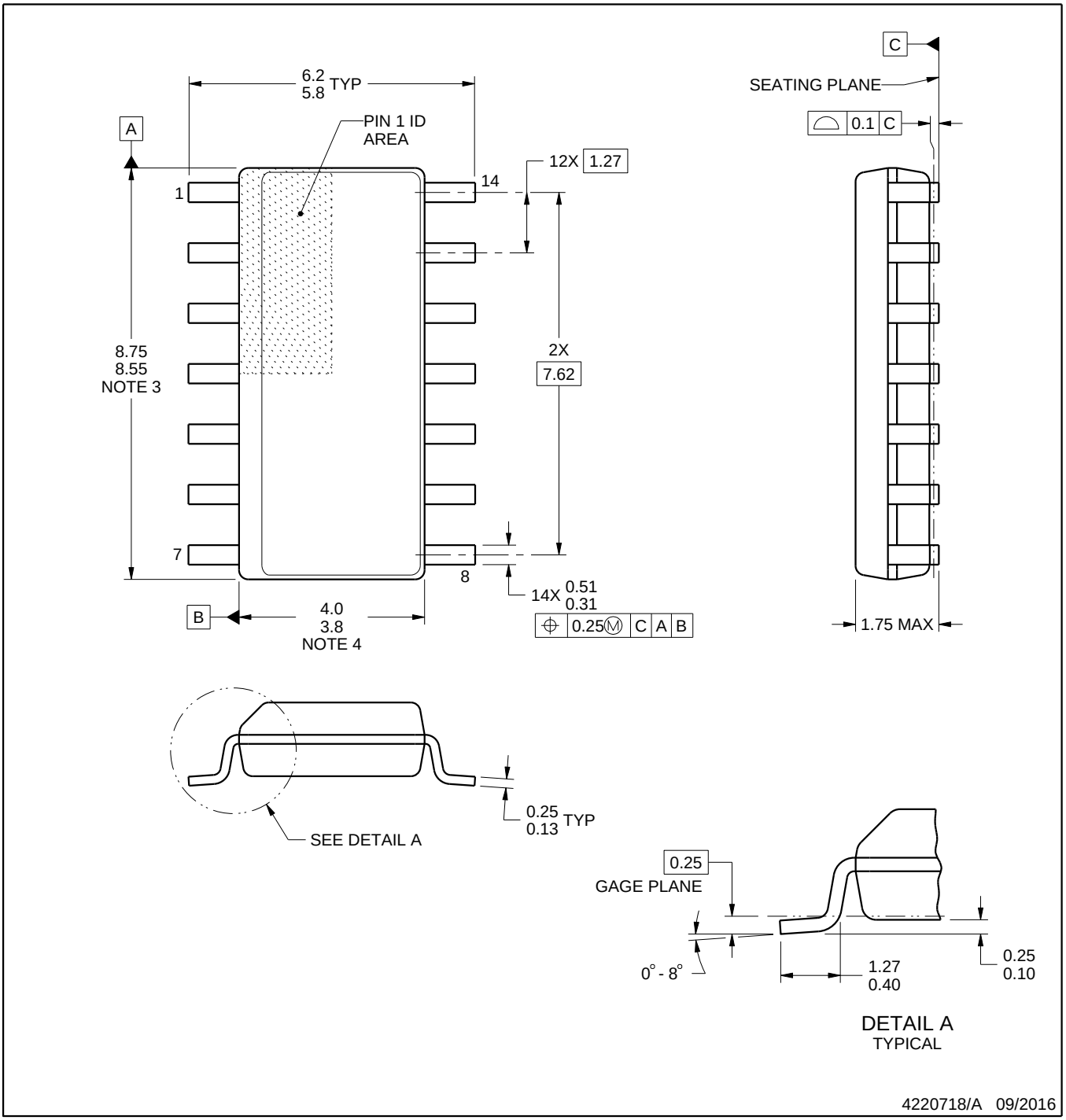


# PACKAGE OUTLINE

## D0014A

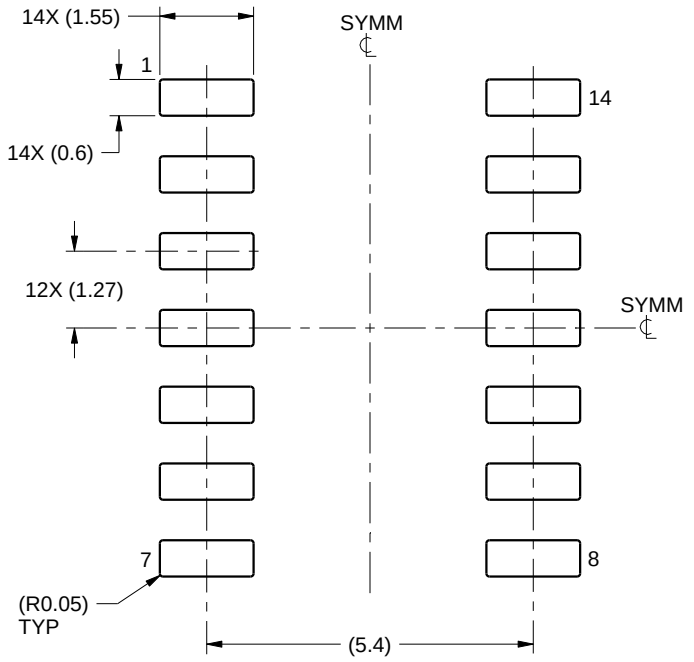
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

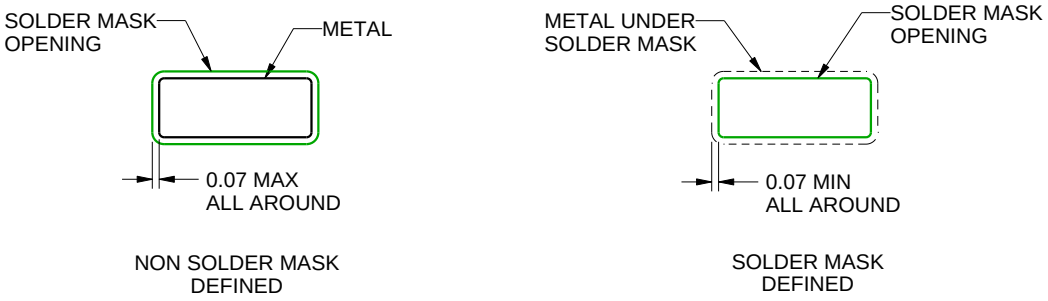



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

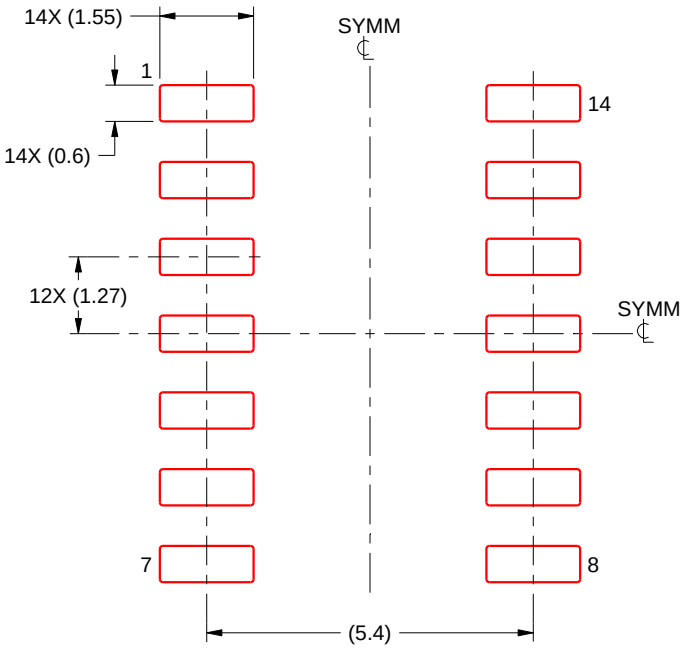
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

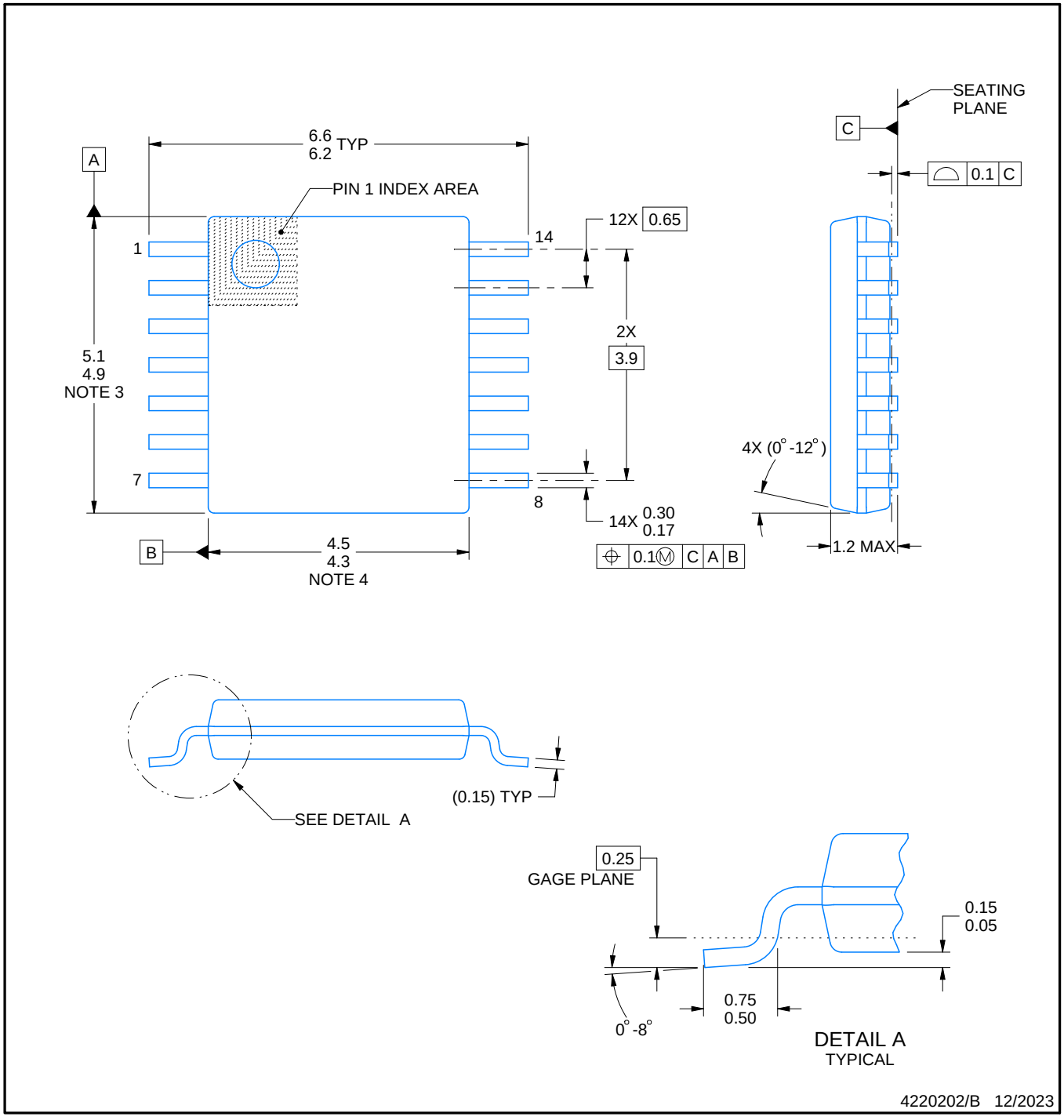
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0014A

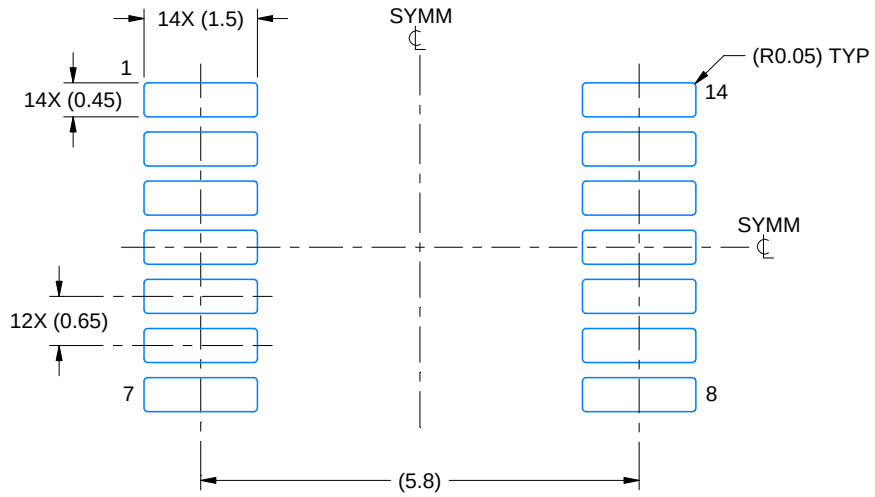
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

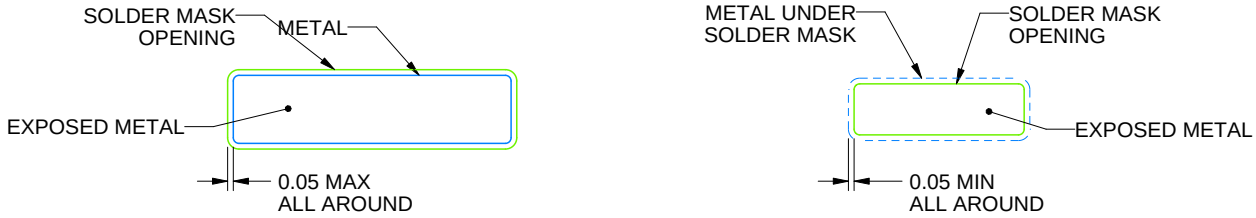



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

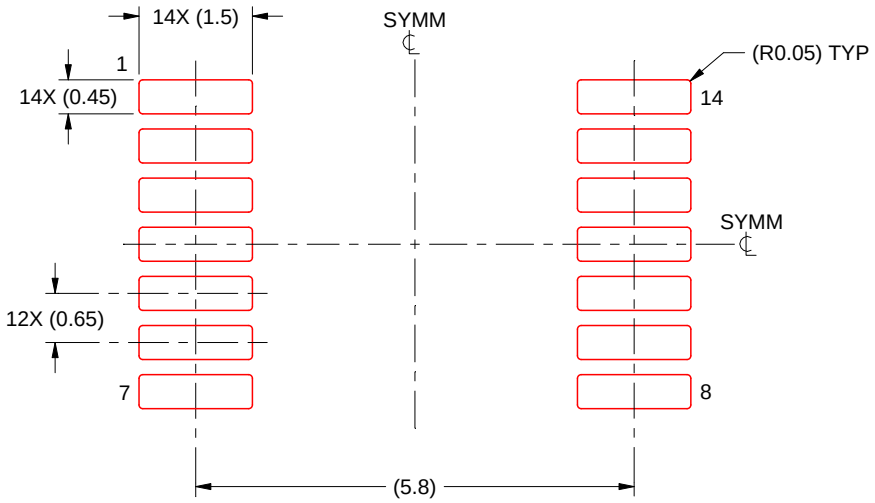



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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