OPAx30x Low-Noise, Fast-Settling, 150MHz CMOS Operational Amplifiers

1 Features

- High bandwidth: 150MHz
- 16-bit settling in 150ns
- Low noise: 3nV/√Hz
- Low distortion: 0.003%
- Low power: 9.5mA (typical) on 5.5V
- Shutdown to 5μA
- Unity-gain stable
- Excellent output swing:
  - (V+) − 100mV to (V−) + 100mV
- Single supply: +2.7V to +5.5V
- Tiny packages: VSSOP and SOT23

2 Applications

- 16-bit ADC input driver
- Low-noise preamplifier
- IF/RF amplifier
- Active filtering

3 Description

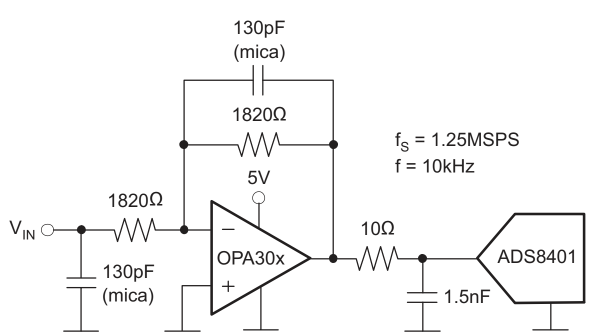
The OPA300, OPA301, OPA2300, and OPA2301 (OPAx30x) series high-speed, voltage-feedback, CMOS operational amplifiers are designed for 16-bit resolution systems. The OPAx30x series are unity-gain stable and feature excellent settling and harmonic distortion specifications. Low power applications benefit from low quiescent current. The OPA300 and OPA2300 feature a digital shutdown (enable) function to provide additional power savings during idle periods. Optimized for single-supply operation, the OPA30x series offer high output swing and excellent common-mode range.

The OPAx30x series op amps have 150MHz of unity-gain bandwidth, low 3nV/√Hz voltage noise, and 0.1% settling within 30ns. Single-supply operation from 2.7V (±1.35V) to 5.5V (±2.75V) and an available shutdown function that reduces supply current to 5μA are useful for portable low-power applications. The OPAx30x are available in SO-8 and SOT-23 packages. The OPA2300 is available in VSSOP-10, and the OPA2301 is available in SO-8 and VSSOP-8. All versions are specified over the industrial temperature range of −40°C to +125°C.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE[(1)]
OPA300	Single	SO-8
		SOT23-6
OPA301	Single	SO-8
		SOT23-6
OPA2300	Dual	VSSOP−10
OPA2301	Dual	SO-8
		VSSOP−8

(1) For all available packages, see Section 10.



Typical Application

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4 Pin Configuration and Functions

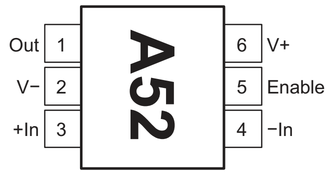

Figure 4-1. OPA300, SOT- 23 Package, 6-pin (Top View)

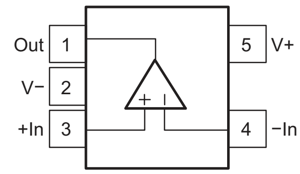

Figure 4-2. OPA301, SOT23-5 Package, 10-pin (Top View)

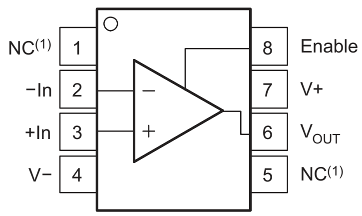

Figure 4-3. OPA300, SO- 8 Package, 8-pin (Top View)

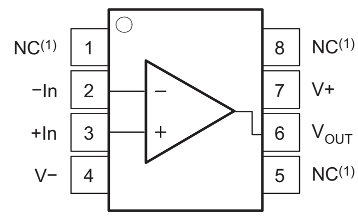

Figure 4-4. OPA301, MSOP Package, 10-pin (Top View)

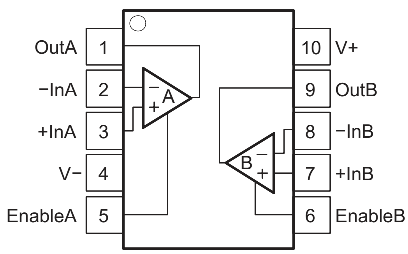

Figure 4-5. OPA2300, MSOP Package, 10-pin (Top View)

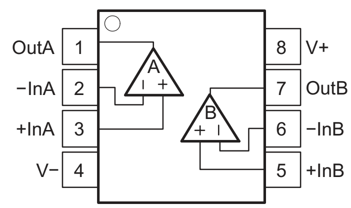

Figure 4-6. OPA301, SO- 8, MSOP- 8 Package, 10-pin (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Enable	8	Input	Enable pin
+In	3	Input	Positive input voltage
–In	2	Input	Negative input voltage
V_{OUT}	6	Output	Output voltage
V+	7	Power	Positive supply voltage
V–	4	Power	Negative supply voltage
NC	1,5	-	No connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
	Power supply		7	V
V_S	Operating voltage range	2.7	5.5	V
	Signal input terminals, voltage [2]	0.5	$(V_S) + 0.5$	V
	Signal input terminals, current		±10	mA
	Open short circuit current [3]		Continuous	
	Operating temperature range	–55	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground; one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2]	500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Power supply voltage	2.7		5.5	V
T_A	Ambient temperature	–40	25	125	°C

5.4 Electrical Characteristics

at T_A = 25°C, R_L = 2kΩ connected to $V_S/2$, $V_{OUT} = V_S/2$, and $V_{CM} = V_S/2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5V			1	5	mV
			T_A= –40°C to +125°C			7	
dV_{OS}/dT	Drift offset voltage				2.5		µV/°C
PSRR	Offset voltage vs power supply	V_S = 2.7V to 5.5V, V_{CM} < (V+) – 0.9V			50	200	µV/V
	Channel separation, dc				140		dB
		f = 5MHz			100		dB
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) – 0.9	V
CMRR	Common-mode rejection ratio	(V–) –0.2V < V_{CM} < (V+) – 0.9V		66	80		dB

5.4 Electrical Characteristics (continued)

at T_A = 25°C, R_L = 2kΩ connected to V_S/2, V_{OUT} = V_S/2, and V_{CM} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT							
I_B	Input bias current				±0.1	±5	pA
I_{OS}	Input offset current				±0.5	±5	pA
INPUT IMPEDANCE							
	Differential				10^{13} || 3		Ω||pF
	Common-mode				10^{13} || 3		Ω||pF
NOISE							
	Input voltage noise	f = 0.1Hz to 1MHz			40		μV_{PP}
e_n	Input voltage noise density	f > 1MHz			3		nV/√Hz
i_n	Input current noise density	f < 1kHz			1.5		fA/√Hz
	Differential gain error	NTSC, R_L = 150Ω			0.01		%
	Differential phase error	NTSC, R_L = 150Ω			0.1		°
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5V, R_L = 2kΩ, 0.1V < V_O < 4.9V		95	106		dB
			T_A= –40°C to +125°C	90			
		V_S = 5V, R_L = 100Ω, 0.5V < V_O< 4.5V		95	106		
			T_A= –40°C to +125°C	90			
OUTPUT							
	Voltage output swing from rail	R_L= 2kΩ, A_{OL} > 95dB			75	100	mV
		R_L= 100Ω, A_{OL} > 95dB			300	500	
I_{SC}	Short-circuit current				70		mA
R_O	Open-loop output impedance	I_O = 0, f = 1MHz			20		Ω
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				150		MHz
SR	Slew rate	G = +1			80		V/μs
t_s	Settling time	V_S = 5V, 2V step, G = +1, 0.01%			90		ns
		V_S = 5V, 2V step, G = +1, 0.1%			30		
	Overload recovery time	Gain = –1			30		ns
THD+N	Total harmonic distortion + noise	V_S = 5V, V_O = $3V_{PP}$, G = +1, f = 1kHz			0.003		%
POWER SUPPLY							
V_S	Specified voltage range			2.7		5.5	V
I_Q	Quiescent current (per amplifier)	I_O = 0mA			9.5	12	mA
			T_A= –40°C to +125°C			13	
SHUTDOWN							
t_{OFF}	Turn-off time				40		ns
t_{ON}	Turn-off time				5		μs
	V_L(Shutdown)			(V–) – 0.2		(V–) + 0.8	V
	V_H(amplifier is active)			(V–) + 2.5		(V+) + 0.2	V
	I_{QSD}(per amplifier)				3	10	μA

5.5 Typical Characteristics

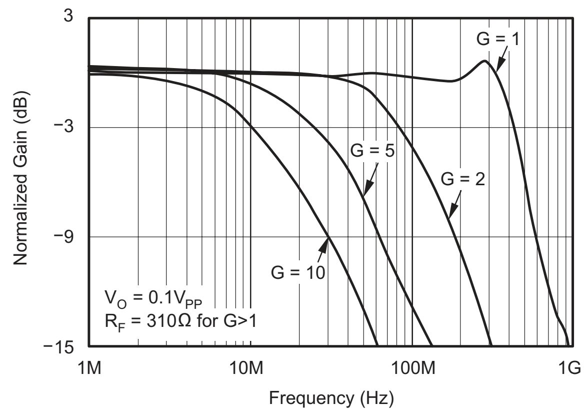

Figure 5-1. Non-Inverting Gain Small Signal Frequency Response

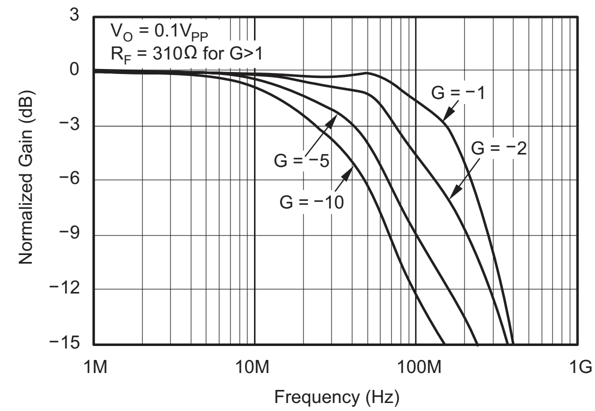

Figure 5-2. Inverting Gain Small Signal Frequency Response

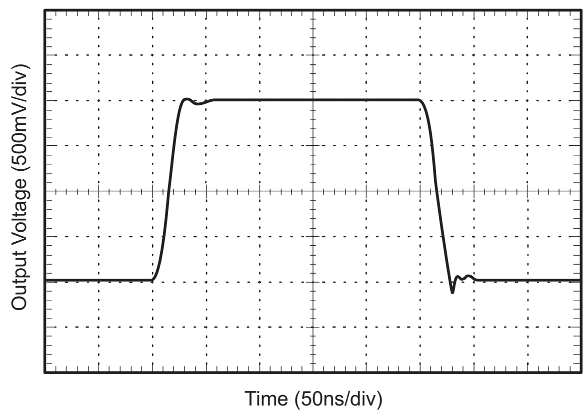

Figure 5-3. Large Signal Step Response

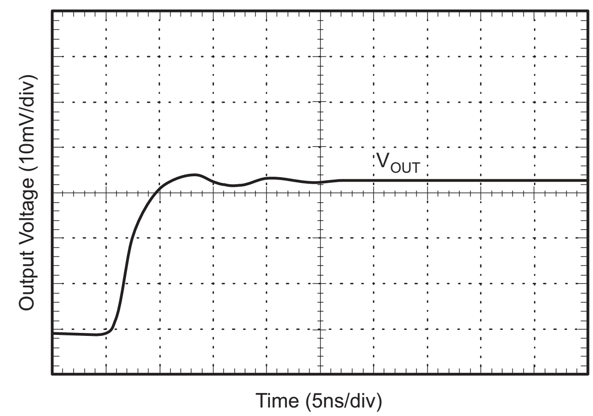

Figure 5-4. Small Signal Step Response

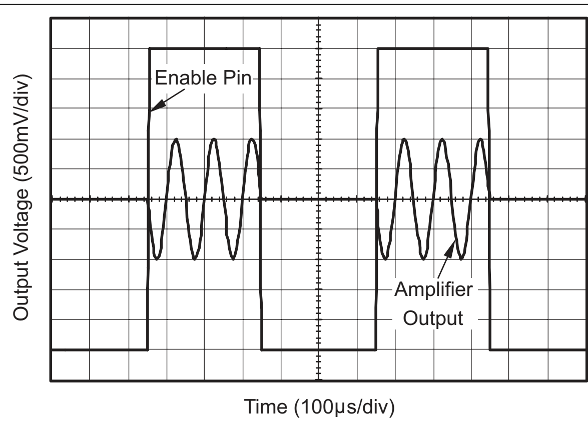

Figure 5-5. Large Signal Enable Disable Response

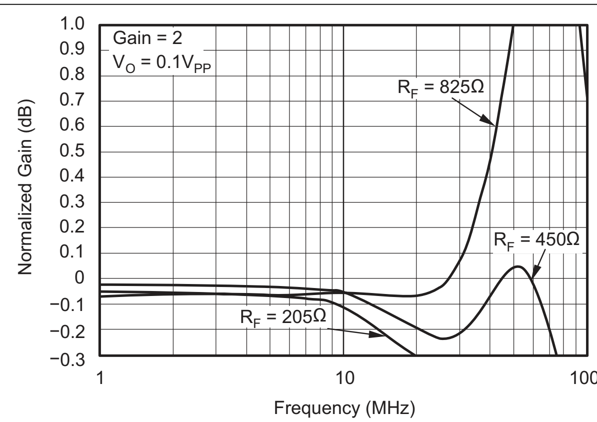

Figure 5-6. 0.1dB Gain Flatness For Various R_F

5.5 Typical Characteristics (continued)

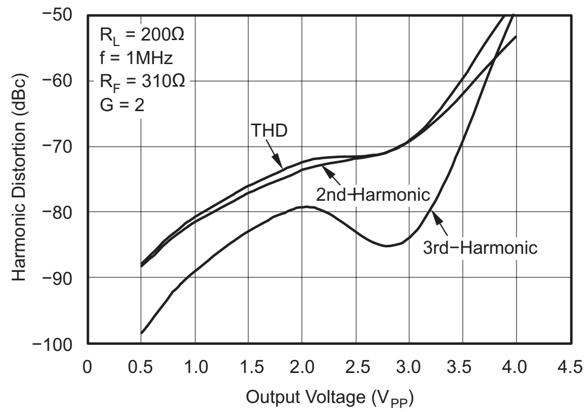

Figure 5-7. Harmonic Distortion vs Output Voltage

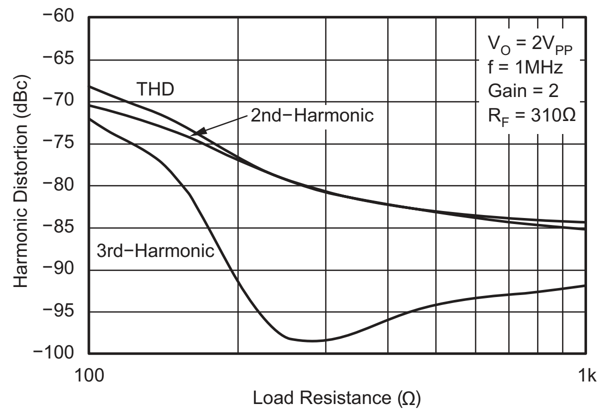

Figure 5-8. Harmonic Distortion vs Load Resistance

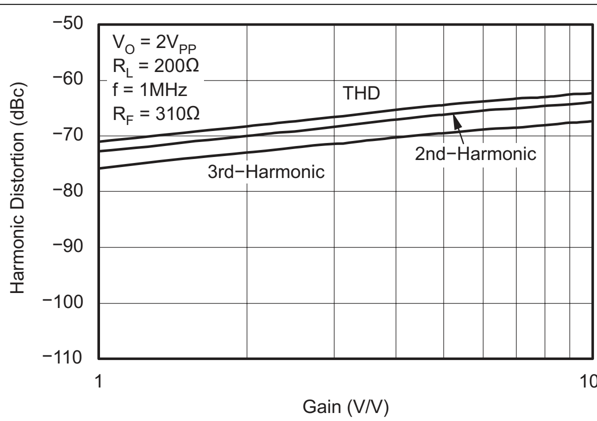

Figure 5-9. Harmonic Distortion vs Inverting Gain

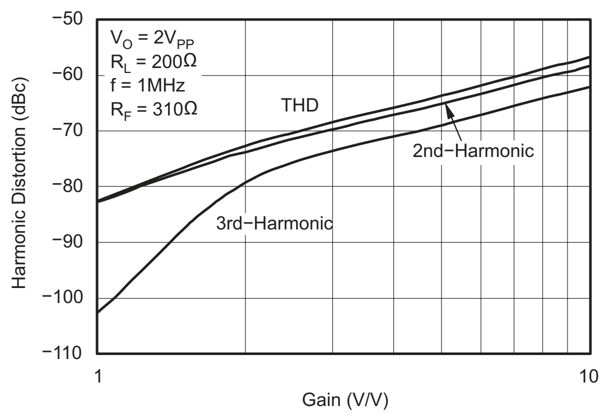

Figure 5-10. Harmonic Distortion vs Non-Inverting Gain

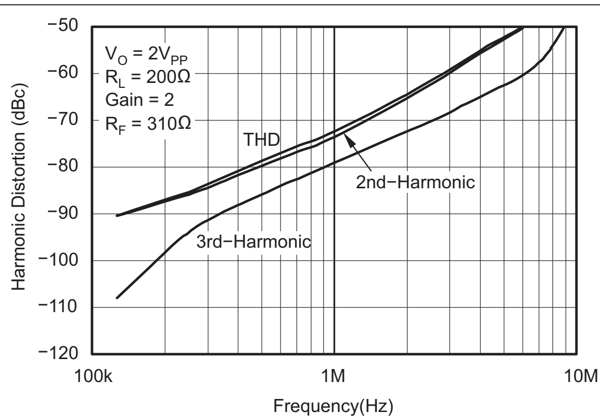

Figure 5-11. Harmonic Distortion vs Frequency

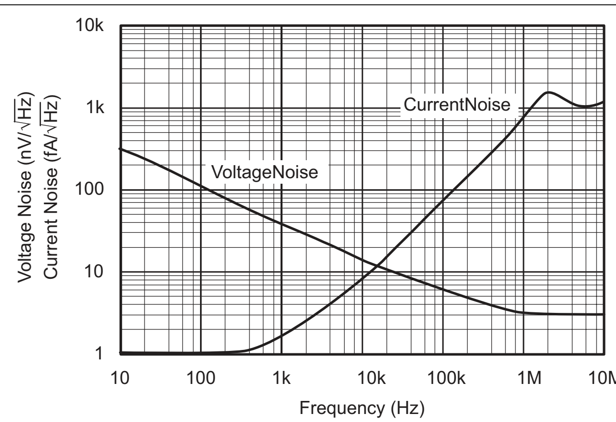

Figure 5-12. Input Voltage And Current Noise Spectral Density vs Frequency

5.5 Typical Characteristics (continued)

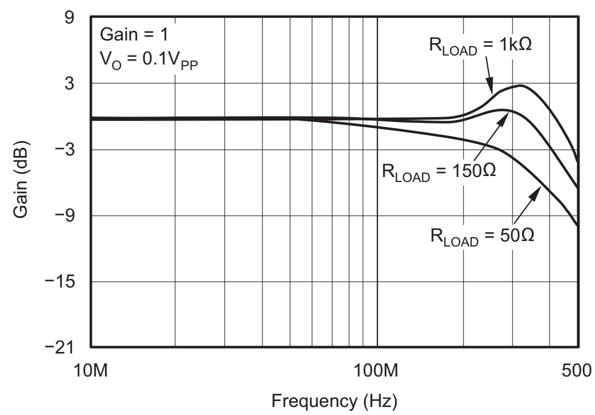

Figure 5-13. Frequency Response For Various R_L

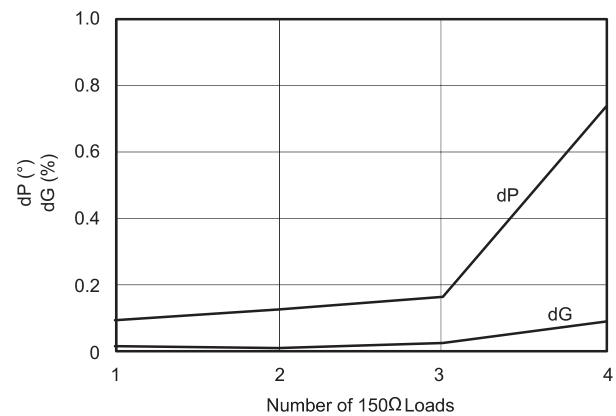

Figure 5-14. Composite Video Differential Gain And Phase

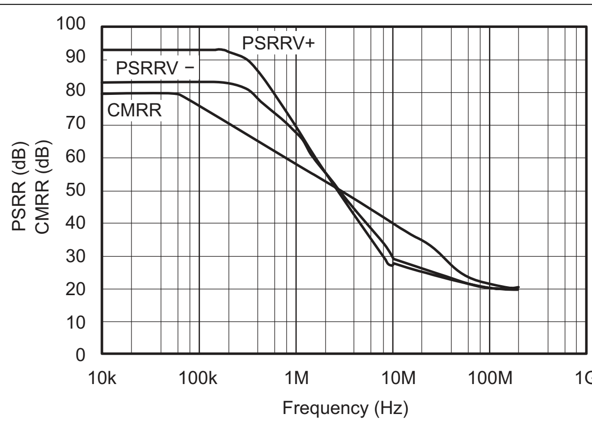

Figure 5-15. Common-Mode Rejection Ration and Power-Supply Rejection Ratio vs Frequency

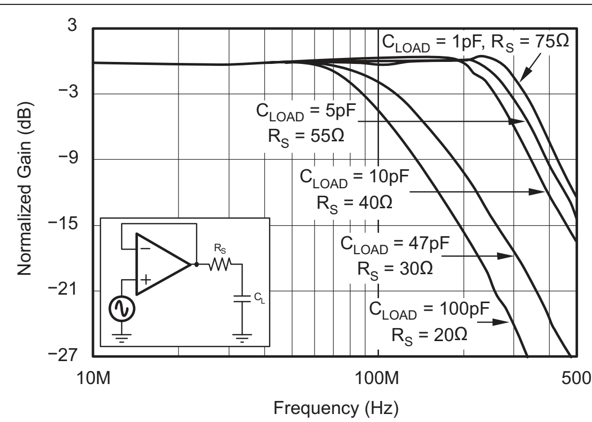

Figure 5-16. Frequency Response vs Capacitive Load

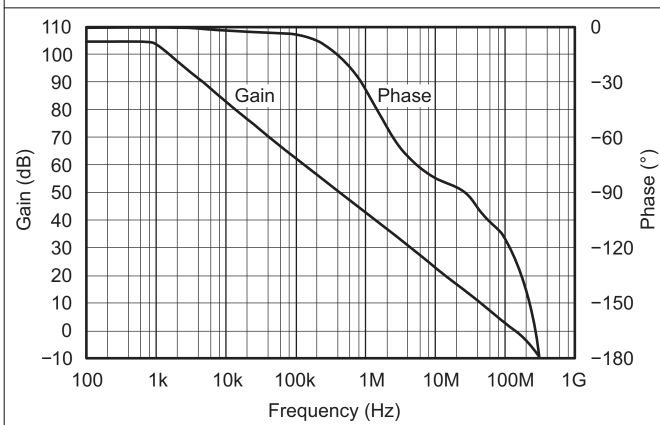

Figure 5-17. Open-Loop Gain and Phase vs Frequency

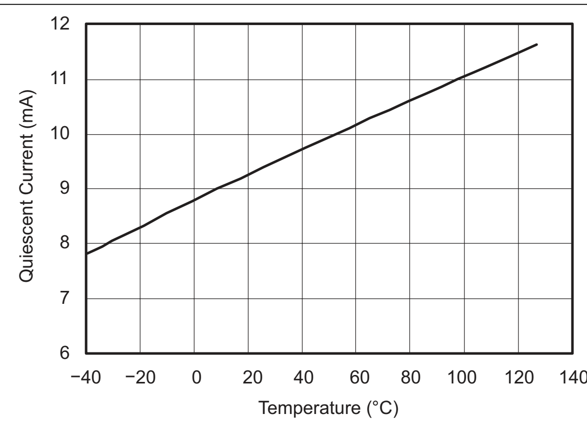

Figure 5-18. Quiescent Current vs Temperature

5.5 Typical Characteristics (continued)

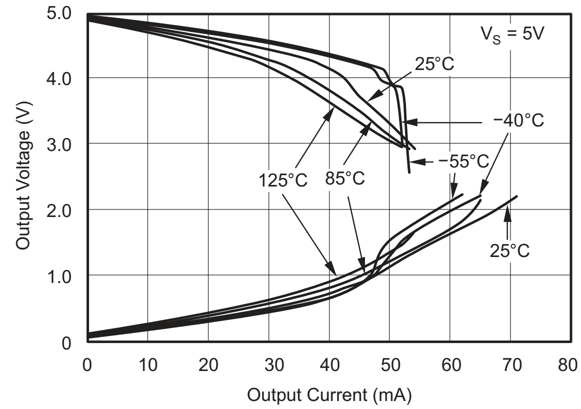

Figure 5-19. Output Voltage Swing vs Output Current

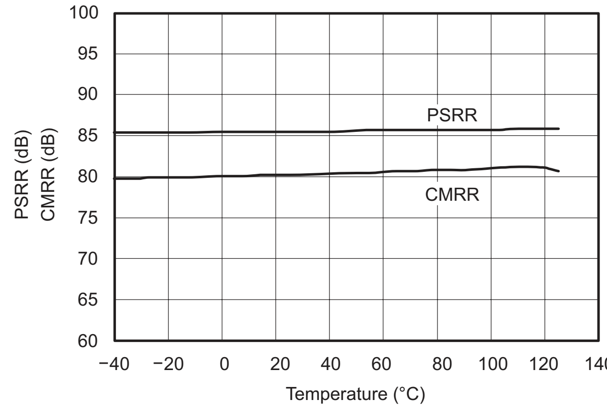

Figure 5-20. Open-loop Gain and Phase vs Frequency

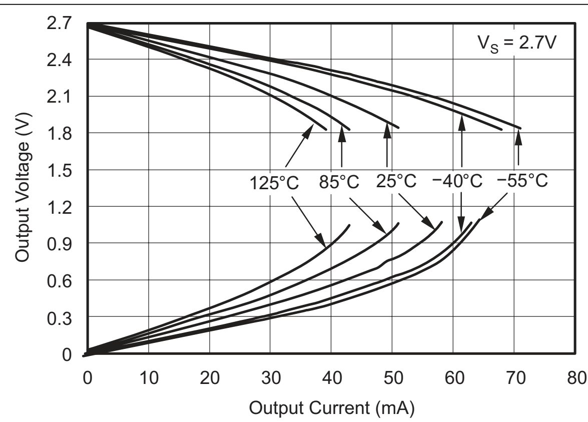

Figure 5-21. Output Voltage Swing vs Output Current

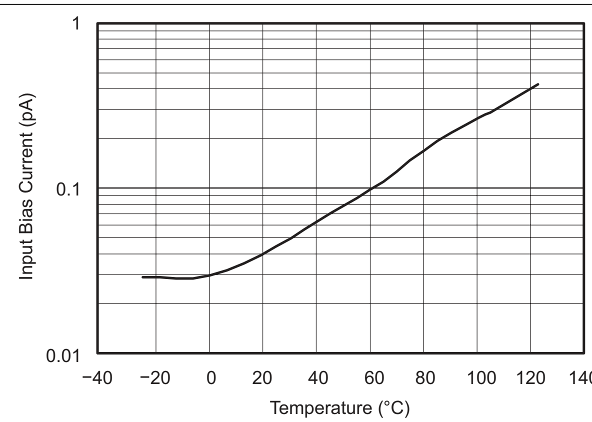

Figure 5-22. Input Bias Current vs Temperature

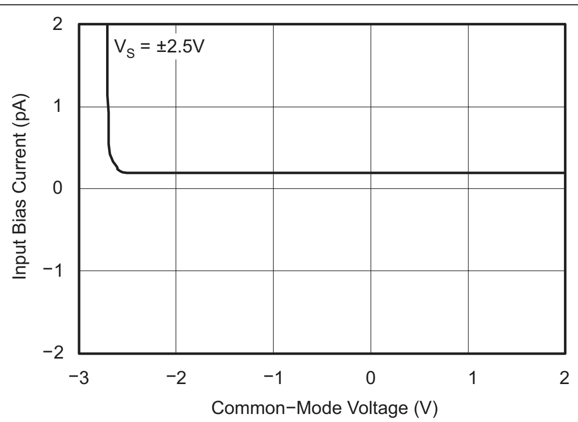

Figure 5-23. Input Bias Current vs Common-Mode Voltage

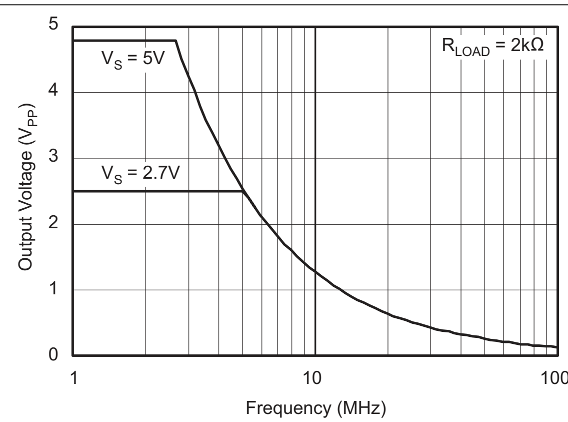

Figure 5-24. Maximum Output Voltage vs Frequency

5.5 Typical Characteristics (continued)

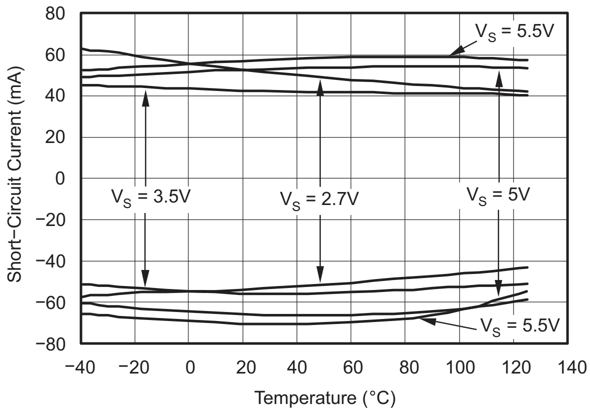

Figure 5-25. Short Circuit Current vs Temperature

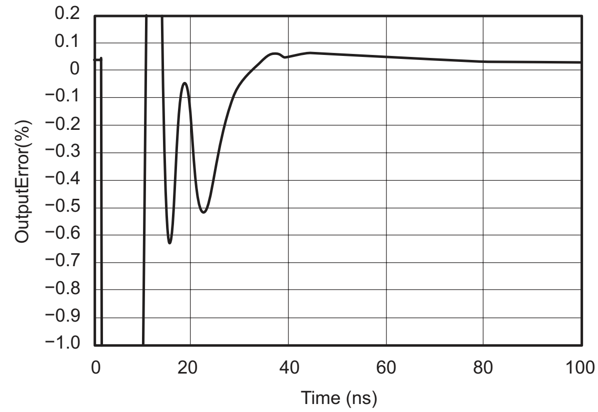

Figure 5-26. Output Settling Time 0.1%

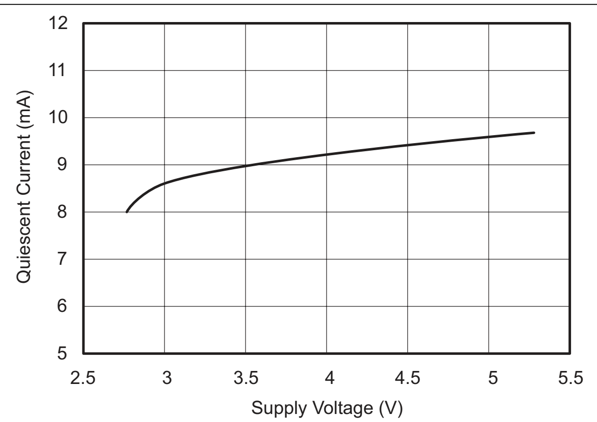

Figure 5-27. Quiescent Current vs Supply Voltage

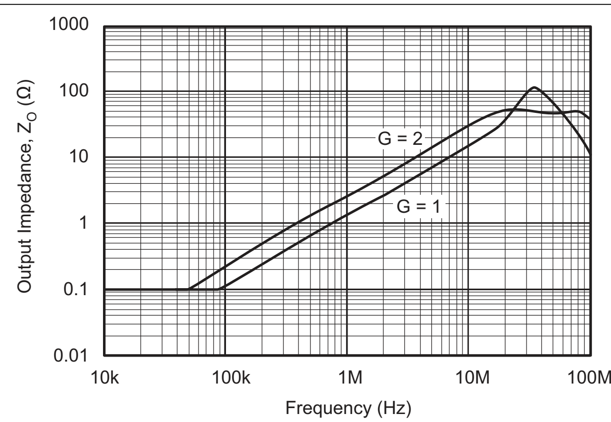

Figure 5-28. Output Impedance vs Frequency

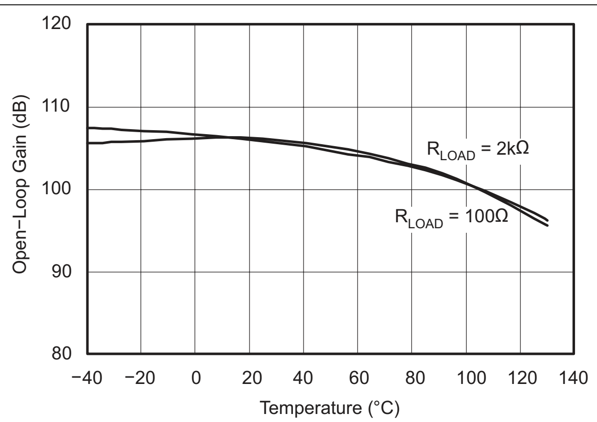

Figure 5-29. Open Gain Loop vs Temperature

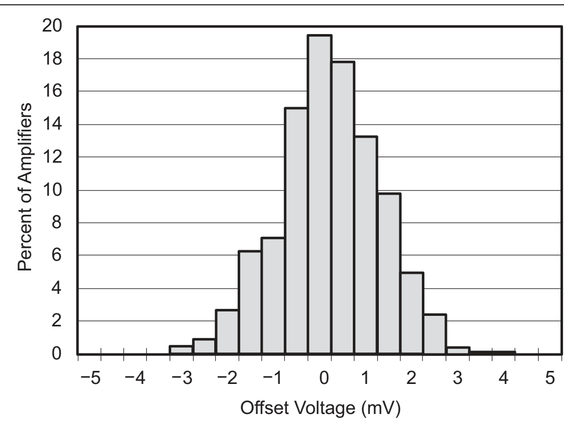

Figure 5-30. Offset Voltage Production Distribution

5.5 Typical Characteristics (continued)

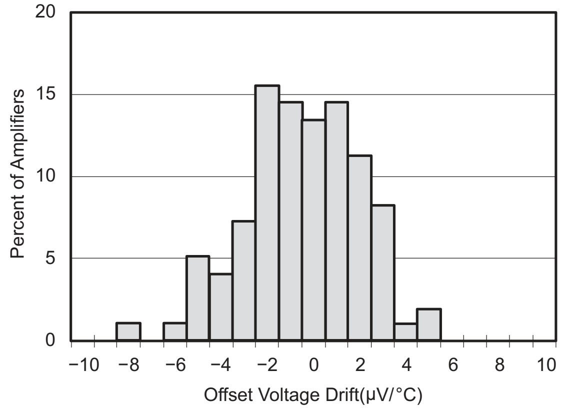

Figure 5-31. Offset Voltage Drift Production Distribution

6 Detailed Description

6.1 Overview

The OPAx30x series op amps use a classic two-stage topology, shown in Figure 6-1. The differential input pair is biased to maximize slew rate without compromising stability or bandwidth. The folded cascode adds the signal from the input pair and presents a differential signal to the class AB output stage. The class AB output stage allows rail- to-rail output swing, with high-impedance loads (> 2kΩ), typically 100mV from the supply rails. With 10Ω loads, a useful output swing is achieved and still maintains high open-loop gain. See the typical characteristic Figure 5-19

6.2 Functional Block Diagram

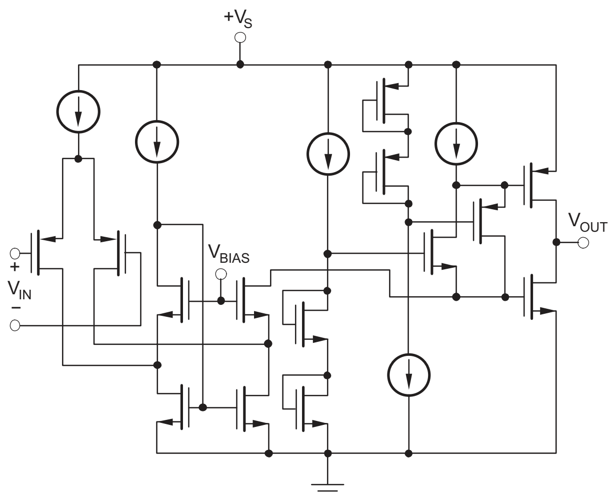

Figure 6-1. OPA30x Classic Two-Stage Topology

6.3 Feature Description

6.4 Operating Voltage

The OPAx30x series op amp parameters are fully specified from +2.7V to +5.5V. Supply voltages higher than 5.5V (absolute maximum) are able to cause permanent damage to the amplifier. Many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

6.5 Input and ESD Protection

All OPAx30x series op amps pins are static protected with internal ESD protection diodes tied to the supplies; see Figure 6-2. These diodes provide overdrive protection if the current is externally limited to 10mA, as stated in the Section 5.1. Any input current beyond the *Absolute Maximum Ratings*, or long-term operation at maximum ratings, shortens the lifespan of the amplifier.

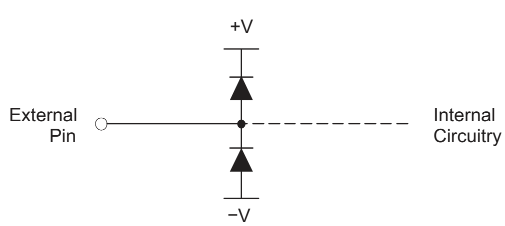

Figure 6-2. ESD Protection Diodes

6.6 Enable Function

The shutdown function of the OPA300 and OPA2300 is referenced to the negative supply voltage of the operational amplifier. A logic level high enables the op amp. A valid logic high is defined as 2.5V greater than the negative supply applied to the enable pin. A valid logic low is defined as < 0.8V greater than the negative supply pin. If dual or split power supplies are used, ensure that logic input signals are properly referred to the negative supply voltage. If this pin is not connected to a valid high or low voltage, the internal circuitry pulls the node high and enables the device to function

The logic input is a high-impedance CMOS input. For battery-operated applications, this feature is used to greatly reduce the average current and extend battery life. The enable time is 10µs, and the disable time is 1µs. When disabled, the output assumes a high-impedance state. This state allows the OPA300 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPA300 and OPA301 series of single-supply CMOS op amps are designed to interface with high-speed 16-bit analog-to-digital converters (ADCs). Featuring wide 150MHz bandwidth, fast 150ns settling time to 16 bits, and high open loop gain, this series offers excellent performance in a small SO-8 and tiny SOT23 packages.

7.2 Typical Application

7.2.1 Driving Capacitive Loads

When using high-speed operational amplifiers, it is extremely important to consider the effects of capacitive loading on amplifier stability. Capacitive loading will interact with the output impedance of the operational amplifier, and depending on the capacitor value, may significantly decrease the gain bandwidth, as well as introduce peaking. To reduce the effects of capacitive loading and allow for additional capacitive load drive, place a series resistor between the output and the load. This will reduce available bandwidth, but permit stable operation with capacitive loading.Figure 7-1 illustrates the recommended relationship between the resistor and capacitor values.

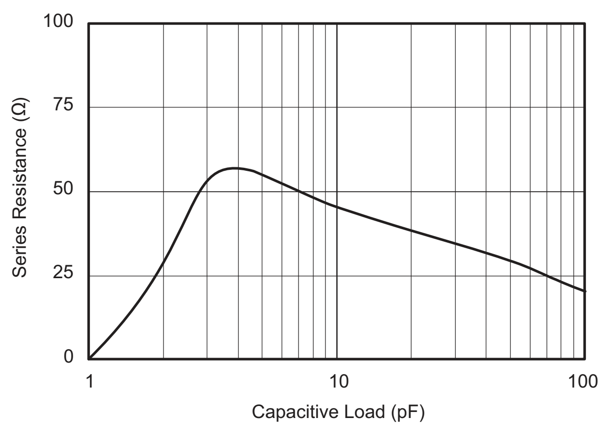

Figure 7-1. Recommended RS and CL Combinations

Amplifiers configured in unity gain are most susceptible to stability issues. The typical characteristic, Figure 5-16 describes the relationship between capacitive load and stability for the OPA300/OPA301 series. In unity gain, the OPA300/OPA301 series is capable of driving a few pico farads of capacitive load without compromising stability. Board level parasitic capacitance can often fall into the range of a pico farad or more, and should be minimized through good circuit-board layout practices to avoid compromising the stability of the OPA300/OPA301. For more information on detecting parasitics during testing, see the Application Note Measuring Board Parasitics in High-Speed Analog Design , available at the TI web site www.ti.com.

7.2.2 Driving 16 Bit ADC

The OPA300/OPA301 series feature excellent THD+noise, even at frequencies greater than 1MHz, with a 16-bit settling time of 150ns.Figure 7-2 shows a total single supply solution for high-speed data acquisition. The OPA300/OPA301 directly drives the ADS8401, a 1.25 mega sample per second (MSPS) 16-bit data converter. The OPA300/OPA301 is configured in an inverting gain of 1, with a 5V single supply. Results of the OPA300/OPA301 performance are summarized in Table 7-1

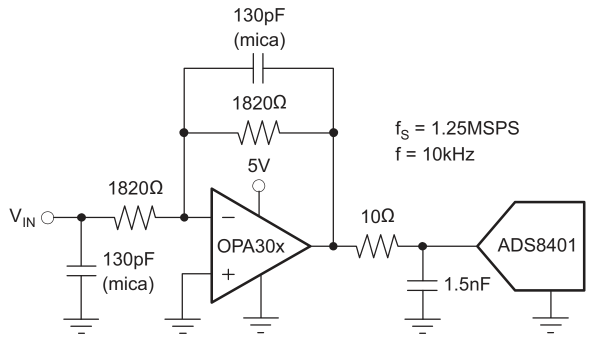

Figure 7-2. The OPA30x Drives the 16-Bit ADS8401

Table 7-1. OPA30x Performance Results Driving a 1.25MSPS ADS8401

PARAMETER	RESULTS f = 10kHz
THD	–99.3dB
SFDR	101.2dB
THS+N	84.2dB
SNR	84.3dB

7.3 Layout

7.3.1 Layout Guidelines

As with most high-speed operational amplifiers, board layout requires special attention to maximize AC and DC performance. Extensive use of ground planes, short lead lengths, and high-quality bypass capacitors will minimize leakage that can compromise signal quality. Guard rings applied with potential as near to the input pins as possible help minimize board leakage.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2007) to Revision E (July 2025)	Page
• Updated data sheet to new format	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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