# Ultra-Wideband, Fixed Gain Video BUFFER AMPLIFIER with Disable

## FEATURES

- VERY HIGH BANDWIDTH (G = +2): 700MHz
- FLEXIBLE SUPPLY RANGE:
  +5V to +12V Single Supply
  ±2.5V to ±6V Dual Supplies
- INTERNALLY FIXED GAIN: +2 or ±1
- LOW SUPPLY CURRENT: 13mA
- LOW DISABLED CURRENT: 120µA
- HIGH OUTPUT CURRENT: ±120mA
- OUTPUT VOLTAGE SWING: ±4.1V
- SOT23-6 AVAILABLE

## APPLICATIONS

- BROADBAND VIDEO LINE DRIVERS
- MULTIPLE LINE VIDEO DA
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- HIGH FREQUENCY ACTIVE FILTERS
- HFA1112 IMPROVED DROP-IN

### OPA693 RELATED PRODUCTS

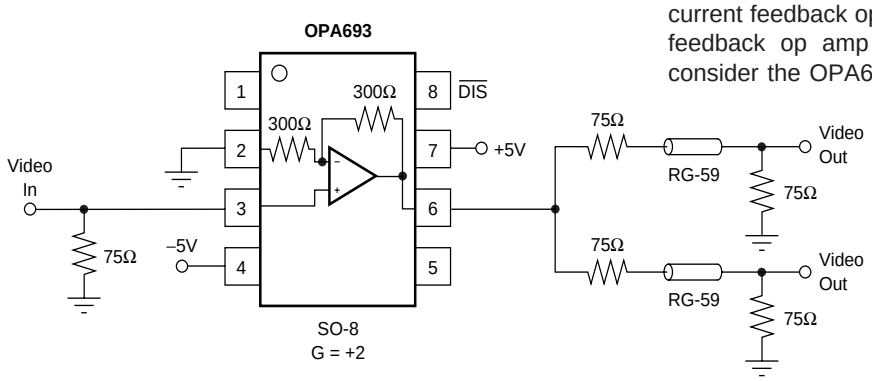
| | SINGLES | DUALS | TRIPLES |
|---|---|---|---|
| Voltage Feedback | OPA690 | OPA2690 | OPA3690 |
| Current Feedback | OPA691 | OPA2691 | OPA3691 |
| Fixed Gain | OPA692 | — | OPA3692 |
| > 900MHz | OPA695 | — | — |

## DESCRIPTION

The OPA693 provides an easy to use, broadband, fixed gain buffer amplifier. Depending on the external connections, the internal resistor network may be used to provide either a fixed gain of +2 video buffer or a gain of ±1 voltage buffer. Operating on a low 13mA supply current, the OPA693 offers a slew rate (2500V/µs) and bandwidth (> 700MHz) normally associated with a much higher supply current. A new output stage architecture delivers high output current with a minimal headroom and crossover distortion. This gives exceptional single-supply operation. Using a single +5V supply, the OPA693 can deliver a $2.5V_{PP}$ swing with over 90mA drive current and 500MHz bandwidth at a gain of +2. This combination of features makes the OPA693 an ideal RGB line driver or single-supply undersampling Analog-to-Digital Converter (ADC) input driver.

The OPA693's low 13mA supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, ensures lower maximum supply current than competing products that report only a room temperature nominal supply current. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, gives normal operation. This optional disable allows the OPA693 to fit into existing video buffer layouts where the disable pin is unconnected to get improved performance with no board changes. If pulled LOW, the OPA693 supply current drops to less than 170µA while the output goes into a high impedance state. This feature may be used for power savings.

The low gain stable current-feedback architecture used in the OPA693 is particularly suitable for high full-power bandwidth cable driving requirements. Where the additional flexibility of an op amp is required, consider the OPA695 ultra-wideband current feedback op amp. Where a unity gain stable voltage feedback op amp with very high slew rate is required, consider the OPA690.




**700MHz, 2-Output Component Video DA**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Power Supply | $\pm 6.5V_{DC}$ |
| Internal Power Dissipation[2] | See Thermal Information |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | $\pm V_S$ |
| Storage Temperature Range: D, DVB | –65°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature ($T_J$) | +150°C |
| ESD Rating (Human Body Model) | 2000V |
| (Charge Device Model) | 1000V |
| (Machine Model) | 100V |

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

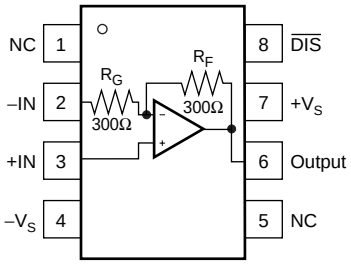
## PACKAGE/ORDERING INFORMATION[1]

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| OPA693 | SO-8 | D | –40°C to +85°C | OPA693D | OPA693ID | Rails, 100 |
| " | " | " | " | " | OPA693IDR | Tape and Reel, 2500 |
| OPA693 | SOT23-6 | DBV | –40°C to +85°C | C59 | OPA693IDBVT | Tape and Reel, 250 |
| " | " | " | " | " | OPA693IDBVR | Tape and Reel, 3000 |

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

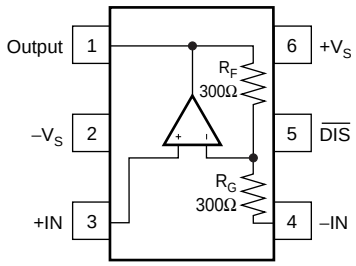
## PIN CONFIGURATION

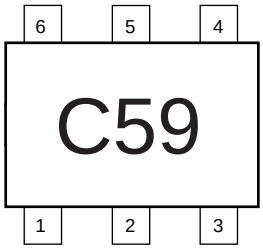
**Top View** **SO**




NC = No Connection

**Top View** **SOT23**




Pin Orientation/Package Marking

# ELECTRICAL CHARACTERISTICS: $V_S$ = ±5V

**Boldface** limits are tested at **25°C.**

G = +2 (–IN grounded) and $R_L$ = 100Ω (see Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA693ID, IDBV | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE[1] | | | | | |
| | | +25°C | +25°C | 0°C to 70°C | –40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL[2] |
| **AC PERFORMANCE (see Figure 1)** | | | | | | | | |
| Small-Signal Bandwidth ($V_O$ < 1.0$V_{PP}$) | G = +1 | 1400 | | | | MHz | typ | C |
| | G = +2 | 700 | 510 | 490 | 480 | MHz | min | B |
| | G = –1 | 700 | 510 | 490 | 480 | MHz | typ | C |
| Bandwidth for 0.2dB Gain Flatness | G = +2, $V_O$ < 1.0$V_{PP}$, $R_L$ = 150Ω | 400 | 122 | 112 | 108 | MHz | min | B |
| Peaking at a Gain of +1 | $V_O$ < 1.0$V_{PP}$ | 2.5 | 3.8 | 4.8 | 5.2 | dB | max | B |
| Large-Signal Bandwidth | G = +2, $V_O$ = 4$V_{PP}$ | 400 | | | | MHz | typ | C |
| Slew Rate | G = +2, 4V Step | 2500 | 2200 | 2100 | 2000 | V/µs | min | B |
| Rise-and-Fall Time | G = +2, $V_O$ = 0.5V Step | 0.6 | 0.8 | 0.8 | 0.8 | ns | max | B |
| | G = +2, $V_O$ = 5V Step | 1.2 | 1.3 | 1.3 | 1.4 | ns | max | B |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | 16 | | | | ns | typ | C |
| Settling Time to 0.1% | G = +2, $V_O$ = 2V Step | 12 | | | | ns | typ | C |
| Harmonic Distortion | G = +2, f = 10MHz, $V_O$ = 2$V_{PP}$ | | | | | | | |
| 2nd-Harmonic | $R_L$ = 100Ω | –69 | –66 | –65 | –64 | dBc | max | B |
| | $R_L$ ≥ 500Ω | –82 | –80 | –79 | –78 | dBc | max | B |
| 3rd-Harmonic | $R_L$ = 100Ω | –83 | –80 | –70 | –69 | dBc | max | B |
| | $R_L$ ≥ 500Ω | –96 | –86 | –85 | –82 | dBc | max | B |
| Input Voltage Noise | f > 1MHz | 1.8 | 2 | 2.7 | 2.9 | nV/√Hz | max | B |
| Noninverting Input Current Noise | f > 1MHz | 18 | 19 | 21 | 22 | pA/√Hz | max | B |
| Inverting Input Current Noise (internal) | f > 1MHz | 22 | 24 | 26 | 27 | pA/√Hz | max | B |
| Differential Gain | NTSC, $R_L$ = 150Ω | 0.03 | | | | % | typ | C |
| | NTSC, $R_L$ = 37.5Ω | 0.03 | | | | % | typ | C |
| Differential Phase | NTSC, $R_L$ = 150Ω | 0.01 | | | | deg | typ | C |
| | NTSC, $R_L$ = 37.5Ω | 0.1 | | | | deg | typ | C |
| **DC PERFORMANCE[3]** | | | | | | | | |
| Gain Error | G = +1 | ±0.2 | | | | % | typ | C |
| | G = +2 | ±0.3 | **±0.9** | ±1.0 | ±1.1 | % | max | A |
| | G = –1, $R_S$ = 0Ω | ±0.2 | ±0.8 | ±0.9 | ±1.0 | % | max | B |
| DC Linearity | $V_O$ = ±2, $R_L$ = 100Ω, G = +2 | 0.0016 | | | | % | typ | C |
| Internal $R_F$ and $R_G$ | | | | | | | | |
| Maximum | | 300 | **341** | 345 | 346 | Ω | max | A |
| Minimum | | 300 | **264** | 260 | 259 | Ω | min | A |
| Average Drift | | | | 0.03 | 0.03 | %/C° | max | B |
| Input Offset Voltage | $V_{CM}$ = 0V | ±0.3 | **±2.0** | ±2.3 | ±2.5 | mV | max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | ±5 | ±8 | µV/°C | max | B |
| Noninverting Input Bias Current | $V_{CM}$ = 0V | +15 | **±35** | ±43 | ±45 | µA | max | A |
| Average Noninverting Input Bias Current Drift | $V_{CM}$ = 0V | | | 170 | 170 | nA/°C | max | B |
| Inverting Input Bias Current (internal) | $V_{CM}$ = 0V | ±20 | **±50** | ±52 | ±54 | µA | max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 0V | | | 50 | 60 | nA°C | max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range | | ±3.4 | **±3.3** | ±3.2 | ±3.2 | V | min | B |
| Noninverting Input Impedance | | 300 \|\| 1.2 | | | | kΩ \|\| pF | typ | C |
| **OUTPUT** | | | | | | | | |
| Voltage Output Swing | No Load | ±4.1 | **±3.9** | ±3.9 | ±3.8 | V | min | A |
| | 100Ω Load | ±3.8 | **±3.7** | ±3.7 | ±3.6 | V | min | A |
| Current Output, Sourcing | | +120 | **+90** | +80 | +70 | mA | min | A |
| Current Output, Sinking | | –120 | **–90** | –80 | –70 | mA | min | A |
| Closed-Loop Output Impedance | G = +2, f = 100kHz | 0.18 | | | | Ω | typ | C |

(1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +20°C at high temperature limit specifications.

(2) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation.
(B) Limits set by characterization and simulation.
(C) Typical value only for information.

(3) Current is considered positive out-of-node. $V_{CM}$ is the input common-mode voltage.

# ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

**Boldface** limits are tested at **25°C.**

G = +2 (–IN grounded) and $R_L = 100\Omega$ (see Figure 1 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA693ID, IDBV | | | | | | TEST LEVEL(2) |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE(1) | | | | | |
| | | +25°C | +25°C | 0°C to 70°C | –40°C to +85°C | UNITS | MIN/ MAX | |
| **DISABLE/POWER DOWN ($\overline{DIS}$ Pin)** | | | | | | | | |
| Power-Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0V | –70 | **–170** | –186 | –192 | µA | max | A |
| Disable Time | $V_{IN}$ = +1$V_{DC}$ | 3 | | | | µs | typ | C |
| Enable Time | $V_{IN}$ = +1$V_{DC}$ | 25 | | | | ns | typ | C |
| Off Isolation | G = +2, 5MHz | 70 | | | | dB | typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | typ | C |
| Turn-On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 0$V_{DC}$ | ±100 | | | | mV | typ | C |
| Turn-Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 0$V_{DC}$ | ±20 | | | | mV | typ | C |
| Enable Voltage | +$V_S$ = +5V | 3.3 | **3.5** | 3.6 | 3.7 | V | min | A |
| Disable Voltage | +$V_S$ = +5V | 1.8 | **1.7** | 1.6 | 1.5 | V | max | A |
| Control Pin Input Bias Current | $V_{\overline{DIS}}$ = 0V | 75 | **130** | 143 | 149 | µA | max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | typ | C |
| Maximum Operating Voltage Range | | | **±6** | ±6 | ±6 | V | max | A |
| Max Quiescent Current | $V_S$ = ±5V | 13 | **13.3** | 13.7 | 14.1 | mA | max | A |
| Min Quiescent Current | $V_S$ = ±5V | 13 | **12.5** | 11.6 | 11.0 | mA | min | A |
| Power-Supply Rejection Ratio (+PSRR) | Input Referred | 58 | **54** | 52 | 51 | dB | min | A |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: D, DBV | | –40 to +85 | | | | °C | typ | C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| D SO-8 | | 125 | | | | °C/W | typ | C |
| DBV SOT23-6 | | 150 | | | | °C/W | typ | C |

(1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +20°C at high temperature limit specifications.

(2) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation.
(B) Limits set by characterization and simulation.
(C) Typical value only for information.

(3) Current is considered positive out-of-node. $V_{CM}$ is the input common-mode voltage.

# ELECTRICAL CHARACTERISTICS: $V_S$ = +5V

**Boldface** limits are tested at **+25°C.**

G = +2 (–IN grounded though 0.001µF) and $R_L$ = 100Ω to $V_S$/2 (see Figure 4 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA693ID, IDBV | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| | | +25°C | +25°C(1) | 0°C to 70°C | –40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL(2) |
| **AC PERFORMANCE (see Figure 4)** | | | | | | | | |
| Small-Signal Bandwidth ($V_O$ < 1.0$V_{PP}$) | G = +1 | 634 | | | | MHz | typ | C |
| | G = +2 | 526 | 400 | 390 | 380 | MHz | min | B |
| | G = –1 | 512 | | | | MHz | typ | C |
| Bandwidth for 0.2dB Gain Flatness | G = +2, $V_O$ < 1.0$V_{PP}$ | 210 | 110 | 100 | 96 | MHz | min | B |
| Peaking at a Gain of +1 | $V_O$ < 1.0$V_{PP}$ | 1.9 | 2.6 | 3.6 | 3.9 | dB | max | B |
| Large-Signal Bandwidth | G = +2, $V_O$ = 2$V_{PP}$ | 400 | | | | MHz | typ | C |
| Slew Rate | G = +2, 2V Step | 1500 | 1200 | 1100 | 1000 | V/µs | min | B |
| Rise-and-Fall Time | G = +2, $V_O$ = 0.5V Step | 0.8 | | | | ns | typ | C |
| | G = +2, $V_O$ = 2V Step | 1.0 | | | | ns | typ | C |
| Settling Time to 0.02% | G = +2, $V_O$ = 2V Step | 16 | | | | ns | typ | C |
| Settling Time to 0.1% | G = +2, $V_O$ = 2V Step | 12 | | | | ns | typ | C |
| Harmonic Distortion | G = +2, f = 10MHz, $V_O$ = 2$V_{PP}$ | | | | | | | |
| 2nd-Harmonic | $R_L$ = 100Ω to $V_S$/2 | –66 | –62 | –62 | –61 | dBc | max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –75 | –69 | –68 | –68 | dBc | max | B |
| 3rd-Harmonic | $R_L$ = 100Ω to $V_S$/2 | –70 | –64 | –63 | –62 | dBc | max | B |
| | $R_L$ ≥ 500Ω to $V_S$/2 | –69 | –63 | –62 | –61 | dBc | max | B |
| Input Voltage Noise | f > 1MHz | 1.8 | 2 | 2.7 | 2.9 | nV/√Hz | max | B |
| Noninverting Input Current Noise | f > 1MHz | 18 | 19 | 21 | 22 | pA/√Hz | max | B |
| Inverting Input Current Noise | f > 1MHz | 22 | 24 | 26 | 27 | pA/√Hz | max | B |
| **DC PERFORMANCE(3)** | | | | | | | | |
| Gain Error | G = +1 | ±0.2 | | | | % | typ | C |
| | G = +2 | ±0.5 | **±1.2** | ±1.3 | ±1.4 | % | max | A |
| | G = –1 | ±0.4 | ±1.1 | ±1.2 | ±1.3 | % | max | B |
| Internal $R_F$ and $R_G$ | | | | | | | | |
| Maximum | | 300 | 341 | 345 | 346 | Ω | max | B |
| Minimum | | 300 | 264 | 260 | 259 | Ω | min | B |
| Average Drift | | | 0.03 | 0.03 | 0.03 | %/C° | max | B |
| Input Offset Voltage | $V_{CM}$ = 2.5V | ±0.3 | **±2.5** | ±2.8 | ±3.0 | mV | max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 2.5V | | | ±5 | ±8 | µV/°C | max | B |
| Noninverting Input Bias Current | $V_{CM}$ = 2.5V | +5 | **±25** | ±33 | ±35 | µA | max | A |
| Average Noninverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | ±170 | ±170 | nA/°C | max | B |
| Inverting Input Bias Current | $V_{CM}$ = 2.5V | ±20 | **±50** | ±52 | ±54 | µA | max | A |
| Average Inverting Input Bias Current Drift | $V_{CM}$ = 2.5V | | | ±50 | ±60 | nA°C | max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage | | 1.6 | 1.7 | 1.8 | 1.8 | V | max | B |
| Most Positive Input Voltage | | 3.4 | 3.3 | 3.2 | 3.2 | V | min | B |
| Noninverting Input Impedance | | 300 ‖ 1.2 | | | | kΩ ‖ pF | typ | C |
| **OUTPUT** | | | | | | | | |
| Most Positive Output Voltage | No Load | 4.1 | **3.9** | 3.9 | 3.8 | V | min | A |
| | $R_L$ = 100Ω | 3.9 | **3.8** | 3.8 | 3.7 | V | min | A |
| Least Positive Output Voltage | No Load | 0.9 | **1.1** | 1.1 | 1.2 | V | max | A |
| | $R_L$ = 100Ω | 1.1 | **1.2** | 1.2 | 1.3 | V | max | A |
| Current Output, Sourcing | | +120 | **+90** | +80 | +70 | mA | min | A |
| Current Output, Sinking | | –120 | **–90** | –80 | –70 | mA | min | A |
| Output Impedance | G = +2, f = 100kHz | 0.18 | | | | Ω | typ | C |

(1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications.

(2) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation.
(B) Limits set by characterization and simulation.
(C) Typical value only for information.

(3) Current is considered positive out-of-node. $V_{CM}$ is the input common-mode voltage.

# ELECTRICAL CHARACTERISTICS: $V_S$ = +5V (Cont.)

**Boldface** limits are tested at **+25°C.**

G = +2 (–IN grounded though 0.001µF) and $R_L$ = 100Ω to $V_S$/2 (see Figure 4 for AC performance only), unless otherwise noted.

| PARAMETER | CONDITIONS | OPA693ID, IDBV | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| | | +25°C(1) | +25°C | 0°C to 70°C | –40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL(2) |
| **DISABLE/POWER DOWN ($\overline{DIS}$ Pin)** | | | | | | | | |
| Power-Down Supply Current (+$V_S$) | $V_{\overline{DIS}}$ = 0 | –95 | **–155** | –172 | –180 | µA | typ | A |
| Off Isolation | G = +2, 5MHz | 65 | | | | dB | typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | typ | C |
| Turn-On Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 2.5V | ±20 | | | | mV | typ | B |
| Turn-Off Glitch | G = +2, $R_L$ = 150Ω, $V_{IN}$ = 2.5V | ±20 | | | | mV | typ | B |
| Enable Voltage | | 3.3 | 3.5 | 3.6 | 3.7 | V | min | B |
| Disable Voltage | | 1.8 | 1.7 | 1.6 | 1.5 | V | max | B |
| Control Pin Input Bias Current ($\overline{DIS}$) | $V_{\overline{DIS}}$ = 0 | 80 | **137** | 153 | 160 | µA | typ | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Single-Supply Operating Voltage | | 5 | | | | V | typ | C |
| Maximum Single-Supply Operating Voltage | | | **+12** | +12 | +12 | V | max | A |
| Maximum Quiescent Current | $V_S$ = +5V | 11.5 | **12.0** | 12.5 | 12.9 | mA | max | A |
| Minimum Quiescent Current | $V_S$ = +5V | 11.5 | **11.0** | 9.5 | 9.2 | mA | min | A |
| Power-Supply Rejection Ratio (+PSRR) | Input Referred | 57 | | | | dB | typ | C |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification: D, DBV | | –40 to +85 | | | | °C | typ | C |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | |
| D SO-8 | | 125 | | | | °C/W | typ | C |
| DBV SOT23-6 | | 150 | | | | °C/W | typ | C |

(1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications.

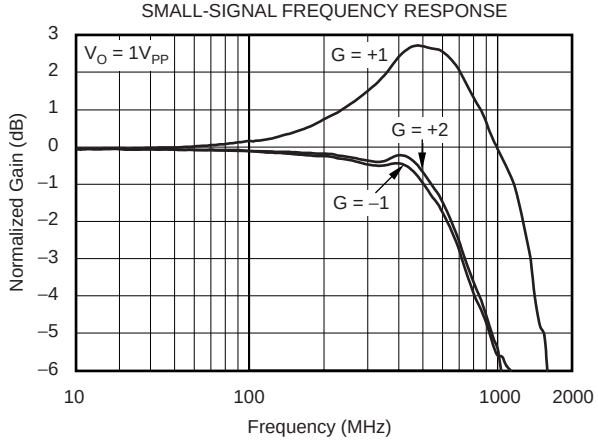
(2) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation.
(B) Limits set by characterization and simulation.
(C) Typical value only for information.

(3) Current is considered positive out-of-node. $V_{CM}$ is the input common-mode voltage.

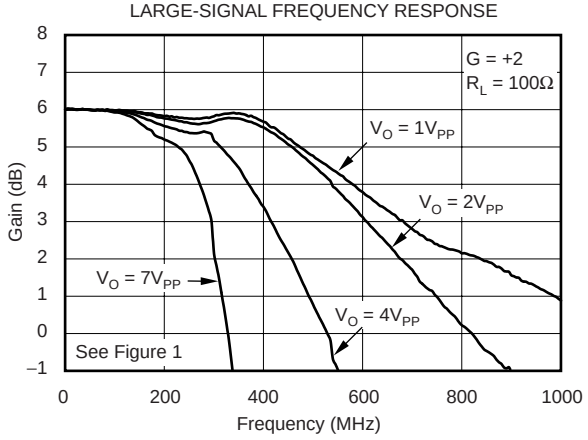
# TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

At $T_A$ = +25°C, G = +2, and $R_L$ = 100Ω, unless otherwise specified.

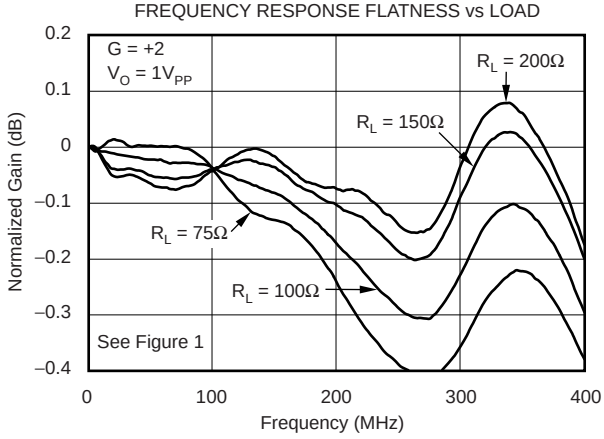
SMALL-SIGNAL FREQUENCY RESPONSE



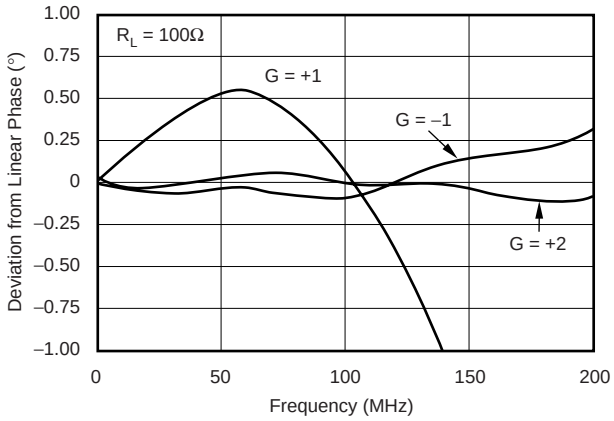

LARGE-SIGNAL FREQUENCY RESPONSE



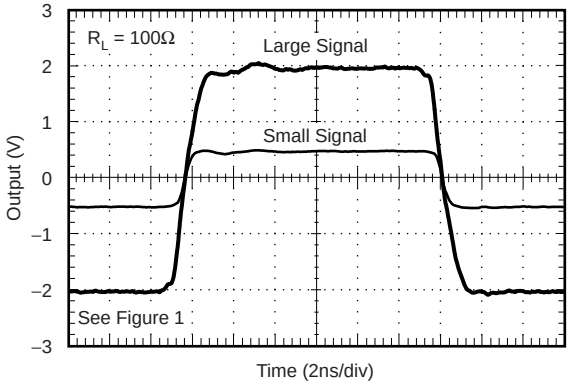

FREQUENCY RESPONSE FLATNESS vs LOAD



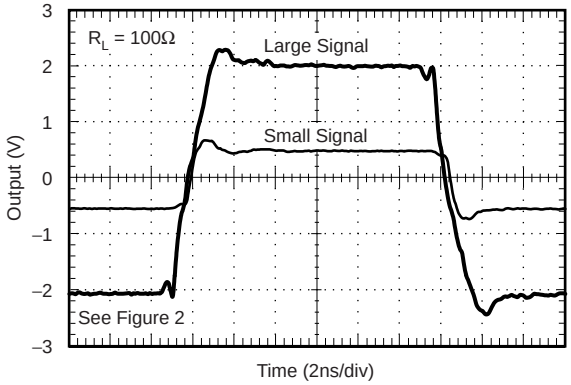

DEVIATION FROM LINEAR PHASE




GAIN OF +2 PULSE RESPONSE



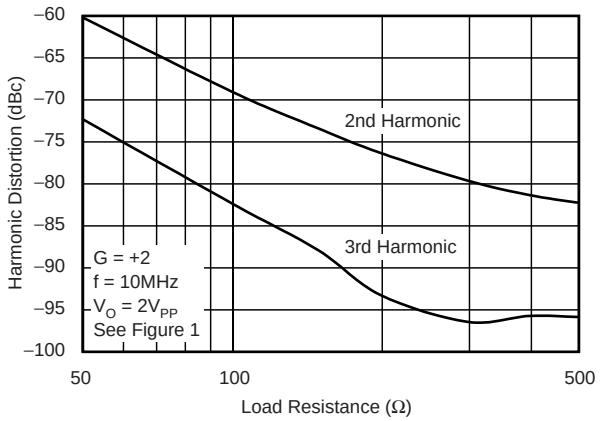

GAIN OF +1 PULSE RESPONSE



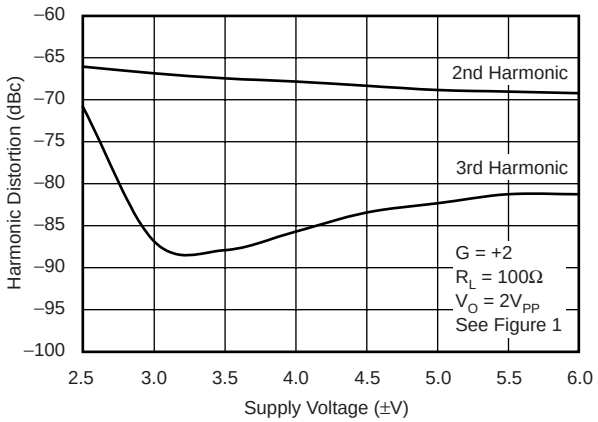
# TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A$ = +25°C, G = +2, and $R_L$ = 100Ω, unless otherwise specified.

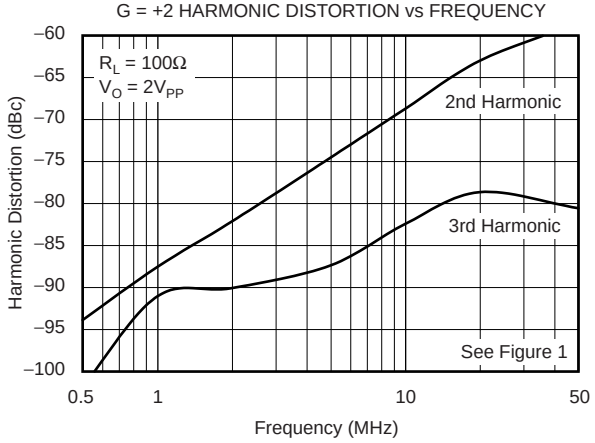
10MHz HARMONIC DISTORTION vs LOAD RESISTANCE



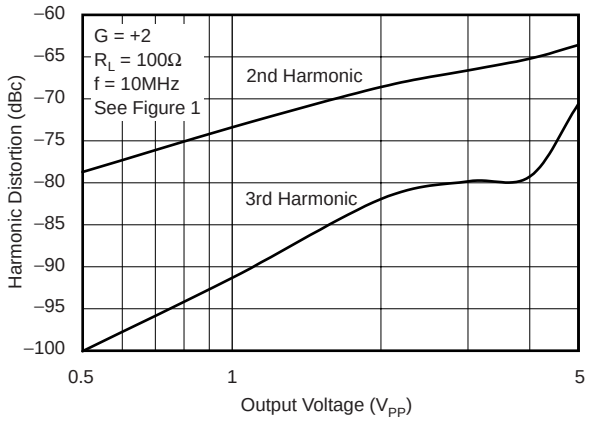

10MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



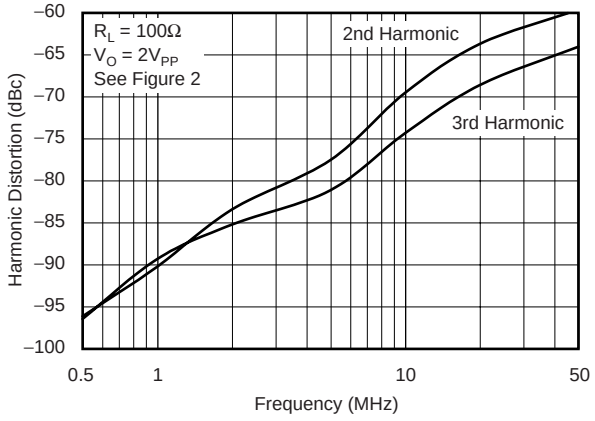

G = +2 HARMONIC DISTORTION vs FREQUENCY



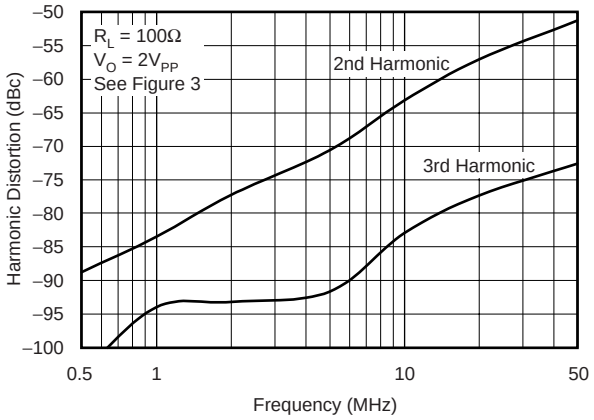

10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE




G = +1 HARMONIC DISTORTION vs FREQUENCY



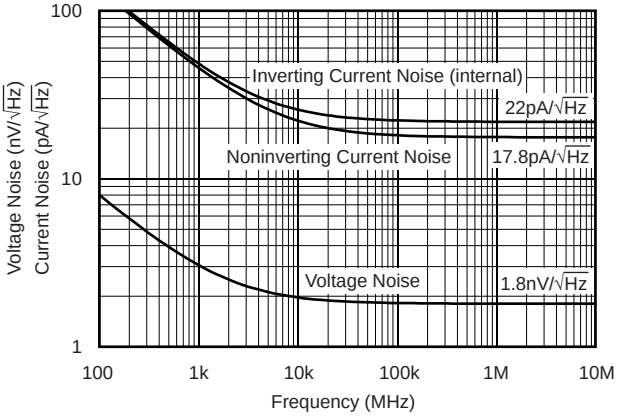

G = –1 HARMONIC DISTORTION vs FREQUENCY



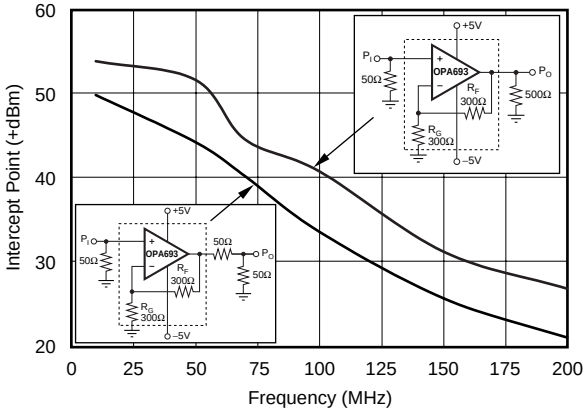
# TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A$ = +25°C, G = +2, and $R_L$ = 100Ω, unless otherwise specified.

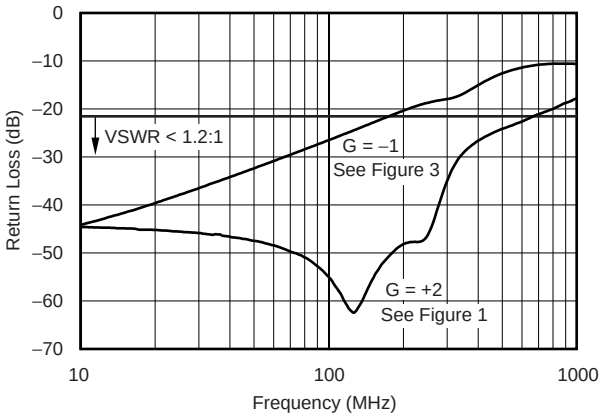
INPUT VOLTAGE vs CURRENT NOISE DENSITY



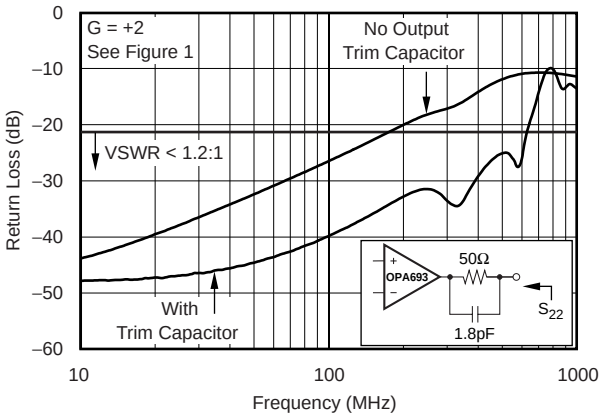

2-TONE, 3RD-ORDER
INTERMODULATION INTERCEPT



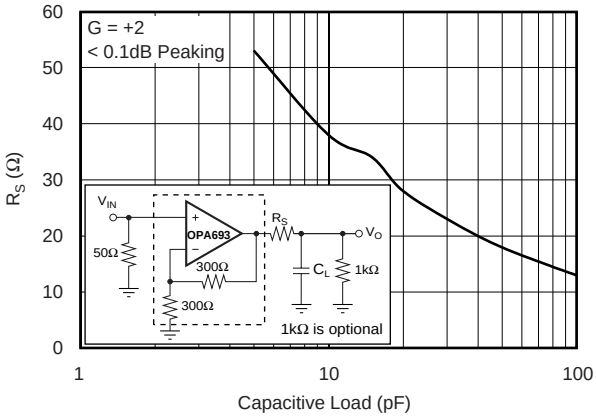

INPUT RETURN LOSS vs FREQUENCY ($S_{11}$)



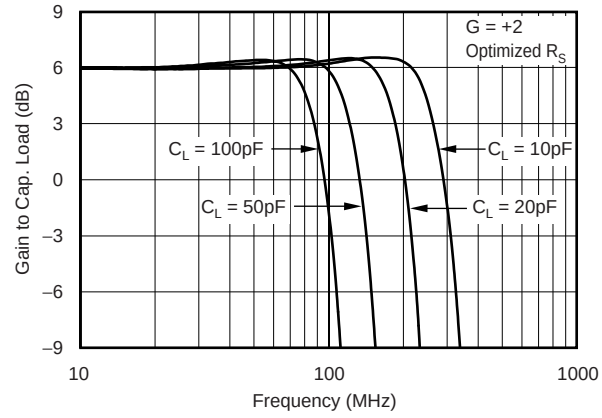

OUTPUT RETURN LOSS vs FREQUENCY ($S_{22}$)




RECOMMENDED $R_S$ vs CAPACITIVE LOAD



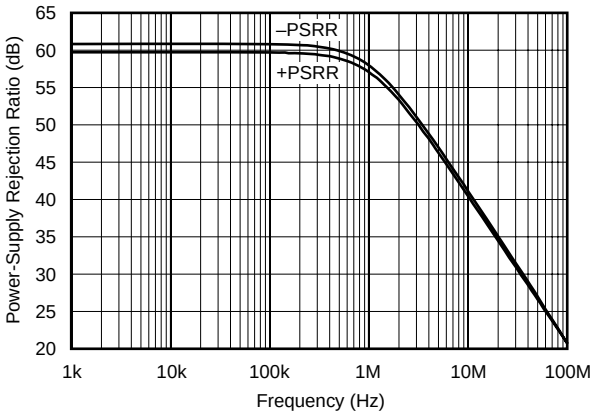

SMALL-SIGNAL FREQUENCY RESPONSE
vs CAPACITIVE LOAD



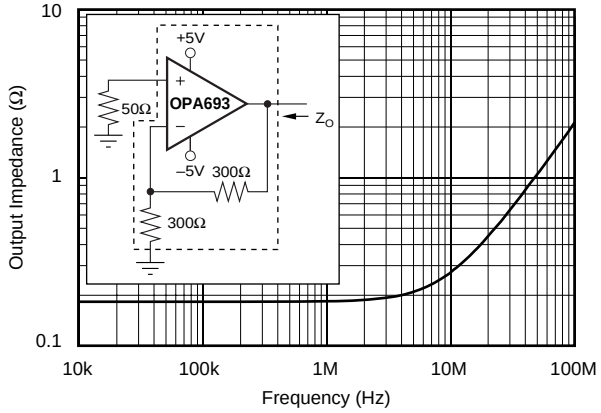
# TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A$ = +25°C, G = +2, and $R_L$ = 100Ω, unless otherwise specified.

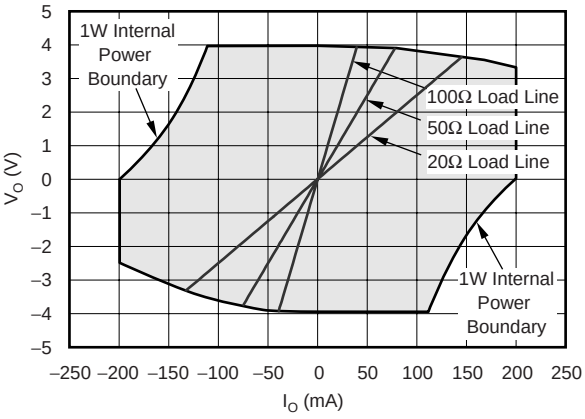
PSRR vs FREQUENCY



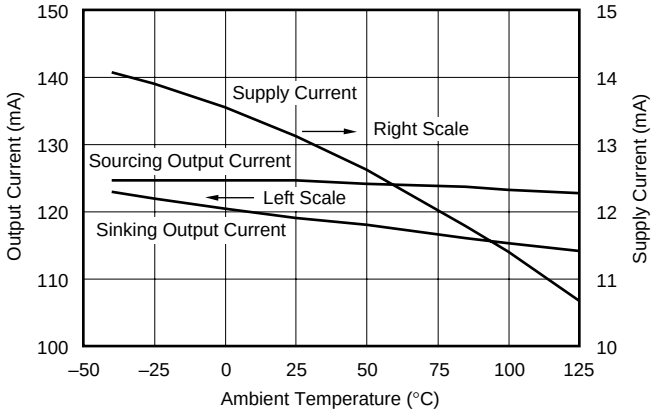

CLOSED-LOOP OUTPUT IMPEDANCE



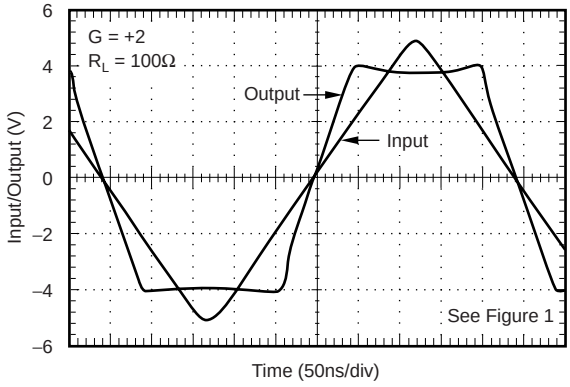

OUTPUT VOLTAGE AND CURRENT LIMITATIONS



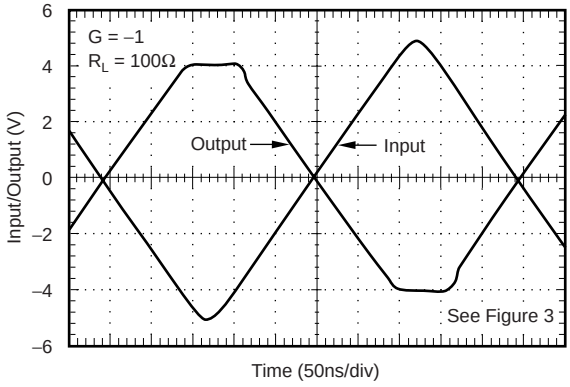

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE




NONINVERTING OVERDRIVE RECOVERY



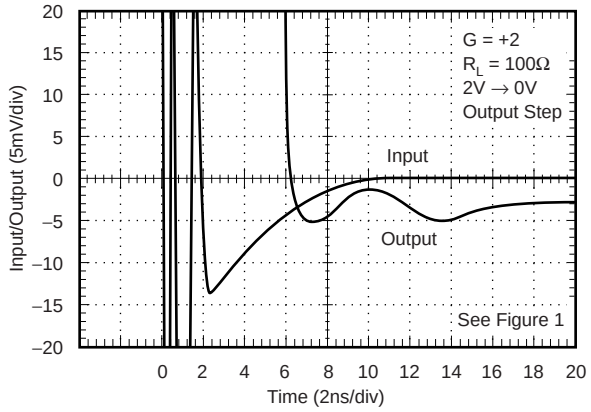

INVERTING OVERDRIVE RECOVERY



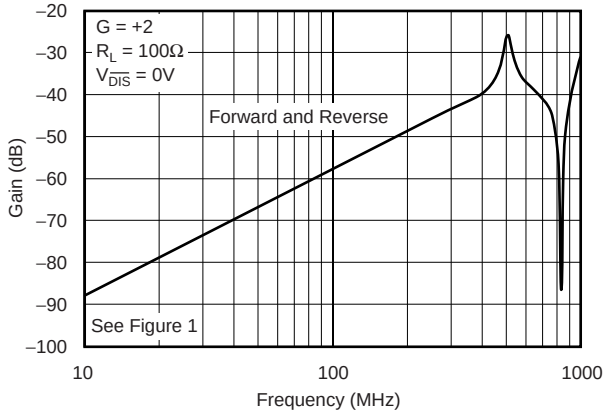
# TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A$ = +25°C, G = +2, and $R_L$ = 100Ω, unless otherwise specified.

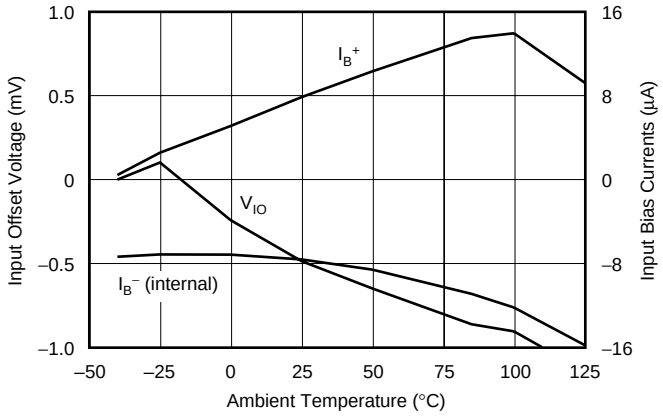
SETTLING TIME



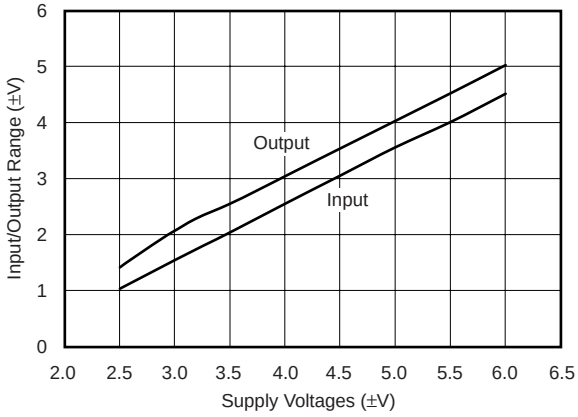

DISABLED FEEDTHRU vs FREQUENCY



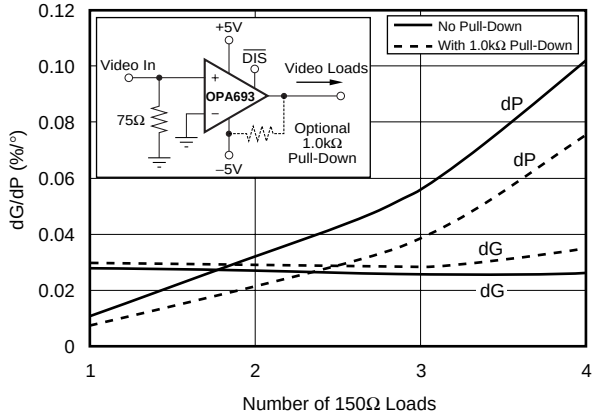

TYPICAL DC DRIFT OVER TEMPERATURE



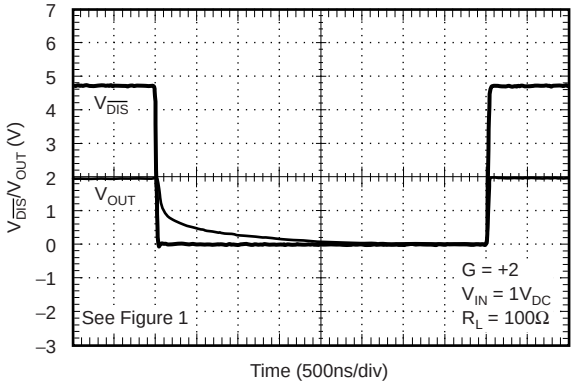

COMMON-MODE INPUT AND OUTPUT SWING vs SUPPLY VOLTAGE




COMPOSITE VIDEO dG/dP



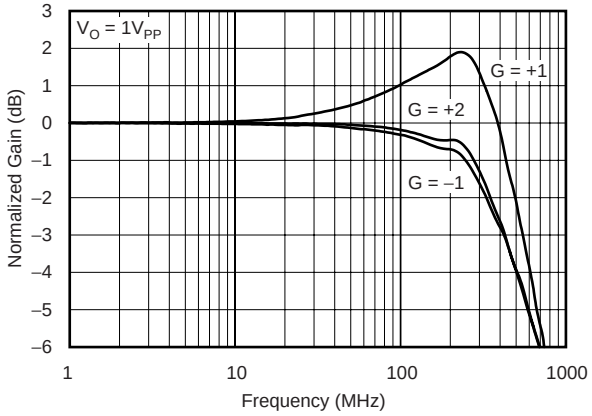

LARGE-SIGNAL DISABLE/ENABLE RESPONSE



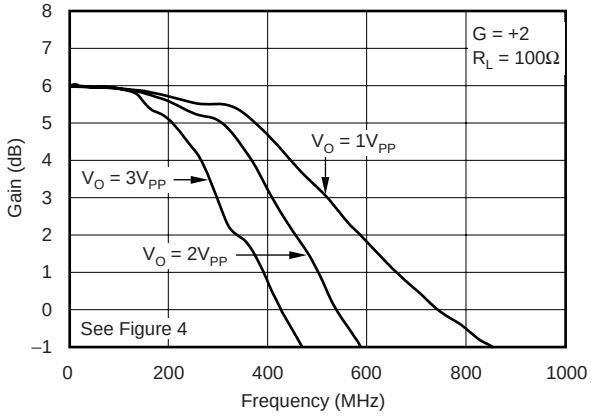
# TYPICAL CHARACTERISTICS: $V_S$ = +5V

At $T_A$ = +25°C, G = +2, and $R_L$ = 100Ω to $V_S$/2, unless otherwise specified.

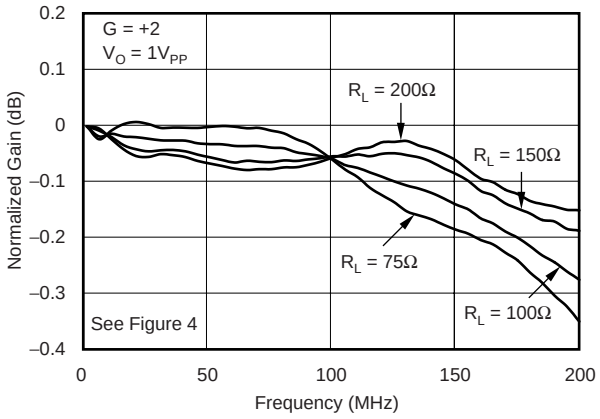
SMALL-SIGNAL FREQUENCY RESPONSE



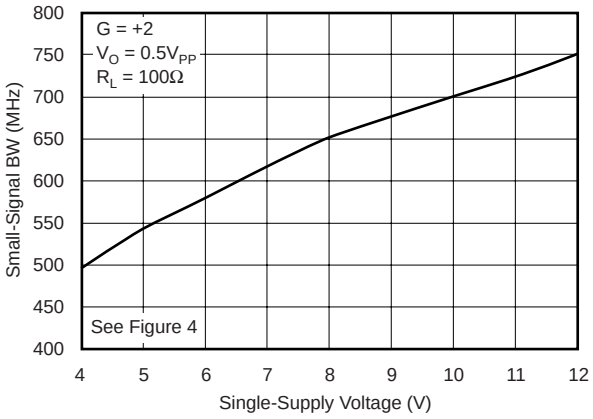

LARGE-SIGNAL FREQUENCY RESPONSE



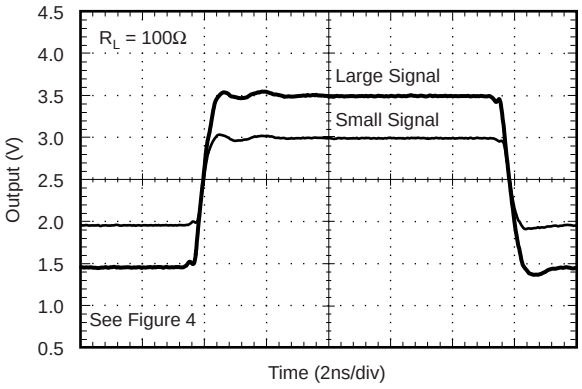

FREQUENCY RESPONSE FLATNESS vs LOAD



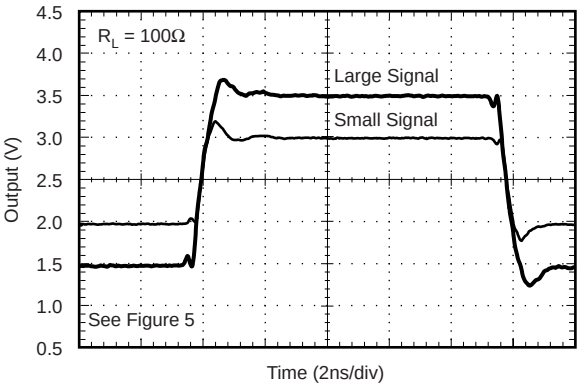

SMALL-SIGNAL BANDWIDTH
vs SINGLE-SUPPLY VOLTAGE




GAIN OF +2 PULSE RESPONSE



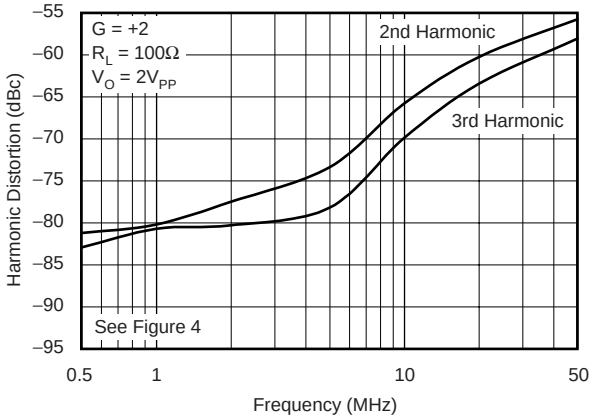

GAIN OF +1 PULSE RESPONSE



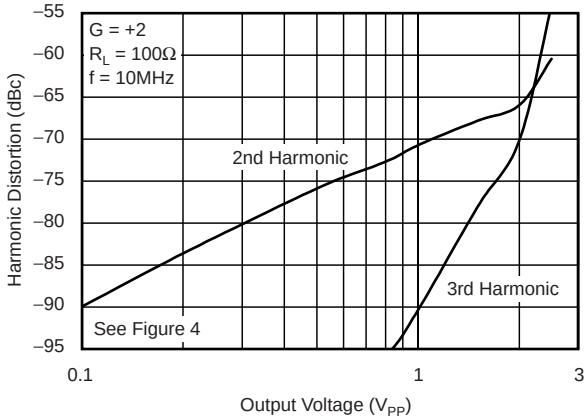
# TYPICAL CHARACTERISTICS: $V_S$ = +5V (Cont.)

At $T_A$ = +25°C, G = +2, and $R_L$ = 100Ω to $V_S$/2, unless otherwise specified.

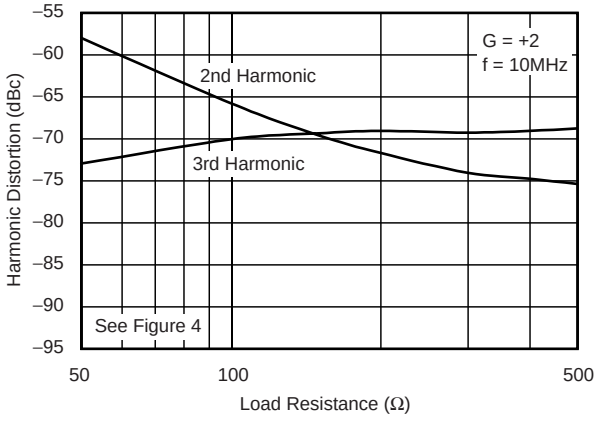
HARMONIC DISTORTION vs FREQUENCY



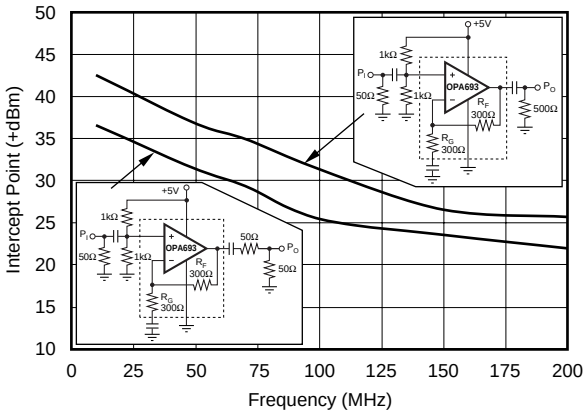

HARMONIC DISTORTION vs OUTPUT VOLTAGE




HARMONIC DISTORTION
vs LOAD RESISTANCE




2-TONE, 3RD-ORDER
INTERMODULATION INTERCEPT



# APPLICATION INFORMATION

## WIDEBAND BUFFER OPERATION

The OPA693 gives the exceptional AC performance of a wideband current-feedback op amp with a highly linear output stage. It features internal $R_F$ and $R_G$ resistors, making it a simple matter to select a gain of +2, +1 or –1 with no external resistors. Requiring only 13mA supply current, the OPA693's output swings to within 1V of either supply with > 700MHz small signal bandwidth and > 300MHz delivering $7V_{PP}$ into a 100Ω load. This low output headroom in a very high-speed amplifier gives remarkable single +5V operation. The OPA693 delivers $2V_{PP}$ swing with > 500MHz bandwidth operating on a single +5V supply. The primary advantage of a current-feedback fixed gain video buffer, as opposed to a slew-enhanced low-gain stable voltage-feedback implementation, is a higher slew rate with lower quiescent power and output noise.

Figure 1 shows the DC-coupled, gain of +2V/V, dual power-supply circuit configuration used as the basis for the ±5V Electrical Characteristics table and Typical Characteristics curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 600Ω = 85.7Ω. The disable control line ($\overline{DIS}$) is typically left open to ensure normal amplifier operation. In addition to the usual power supply decoupling capacitors to ground, a 0.01µF capacitor can be included between the two power-supply pins. This optional added capacitor will typically improve the 2nd harmonic distortion performance by 3dB to 6dB.

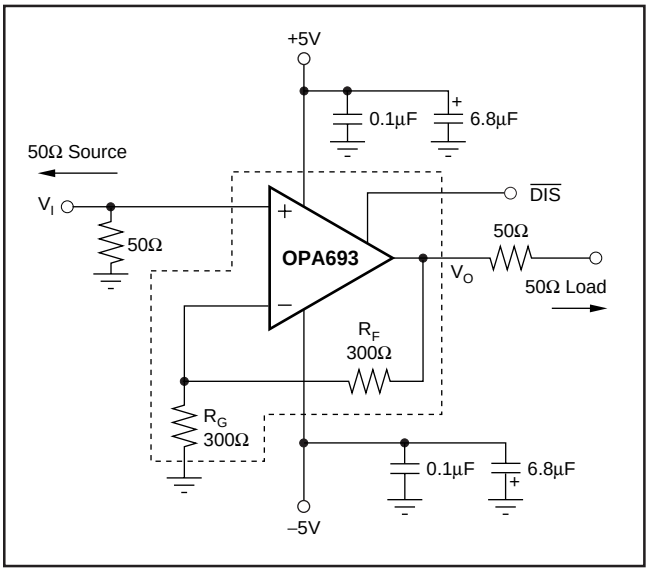



Figure 1. DC-Coupled, G = +2, Bipolar-Supply, Specification and Test Circuit.

Figure 2 shows the DC-coupled, gain of +1V/V buffer configuration used as a starting point for the gain of +1V/V Typical Characteristic curves. In this case, the inverting input resistor, $R_G$, is left open giving a very broadband gain of +1 performance. While the test circuit shows a 50Ω input resistor, a buffer application is typically transforming from a source that cannot drive a heavy load to a 100Ω load, such as shown in Figure 2. The noninverting input impedance of the OPA693 is typically 100kΩ || 2pF. Driving directly into the noninverting input will provide this very light load to the source. However, the source must still provide the noninverting input bias current required by the input stage to operate. An alternative approach to a gain of +1 buffer is described in the Wideband Unity Gain Buffers section of this data sheet.

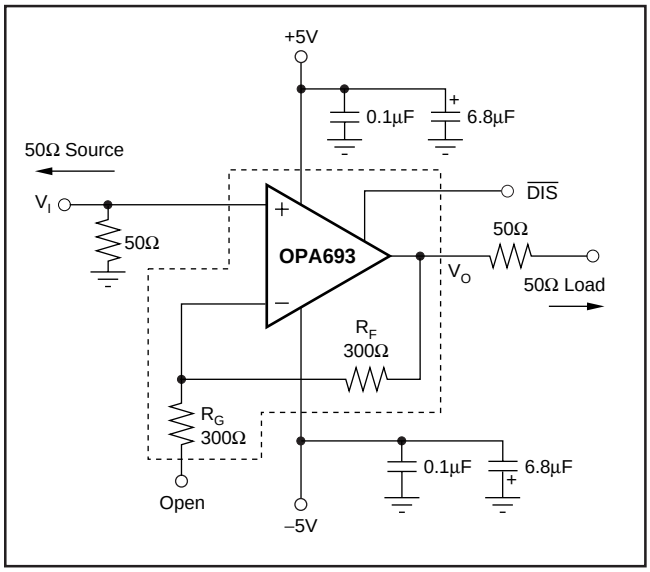



Figure 2. DC-Coupled, G = +1V/V, Bipolar-Supply, Specification and Test Circuit.

Figure 3 shows the DC-coupled, gain of –1V/V buffer configuration used as a starting point for the gain of –1V/V Typical Characteristic curves. The input impedance is set to 50Ω using the parallel combination of an external 60.4Ω resistor and the internal 300Ω $R_G$ resistor. The noninverting input is tied directly to ground. Since the internal design for the OPA693 is current-feedback, trying to get improved DC accuracy by including a resistor on the noninverting input to ground is ineffective. Using a direct short to ground on the noninverting input reduces both the contribution of the DC bias current and noise current to the output error. While the external 60.4Ω is used here to match to the 50Ω source from the test equipment, the maximum input impedance in this configuration is limited to the 300Ω $R_G$ resistor even with the $R_M$ resistor removed. Unlike the noninverting unity gain buffer application, removing $R_M$ does not strongly impact the DC operating point because the short on the noninverting input of Figure 3 provides the DC operating voltage. This application of the OPA693 provides a very broadband, high-output, signal inverter.

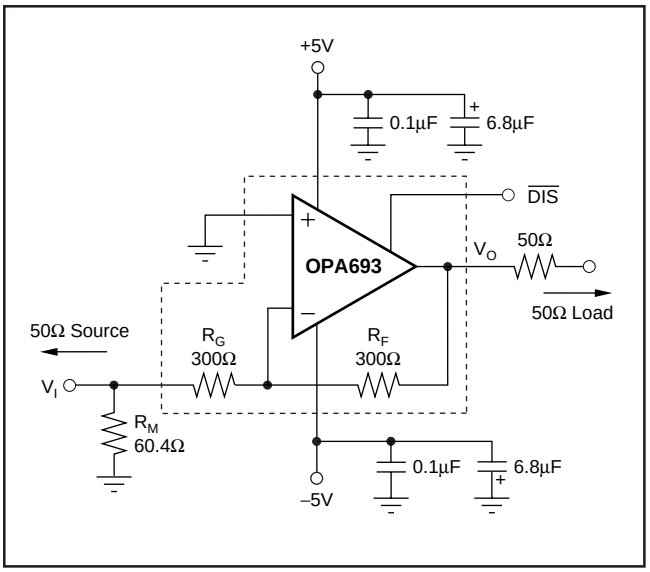



Figure 3. DC-Coupled, G = –1V/V, Bipolar-Supply Specification and Test Circuit.

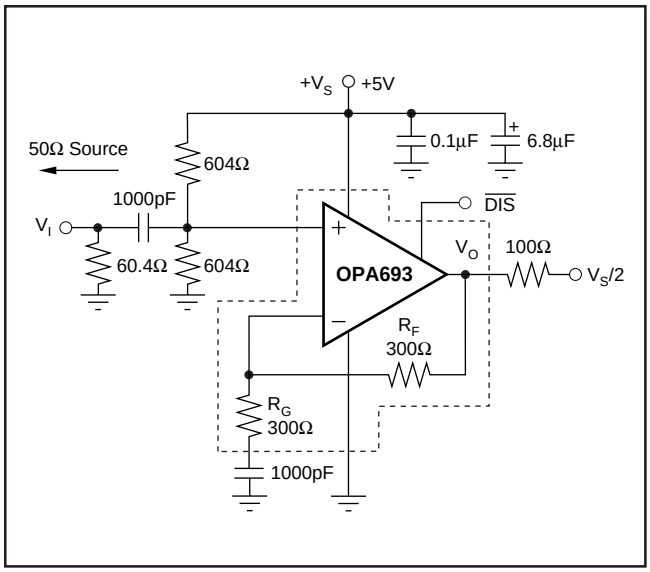



Figure 4. AC-Coupled, G = +2V/V, Single-Supply Specification and Test Circuit.

## SINGLE-SUPPLY OPERATION

The OPA693 may be used over a single-supply range of +5V to +12V. Though not a rail-to-rail output design, the OPA693 requires minimal input and output voltage headroom compared to other very-wideband video buffer amplifiers. As shown in the single +5V Typical Characteristic curves, the OPA693 provides > 300MHz bandwidth driving a $3V_{PP}$ swing into a 100Ω load. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output.

The circuit of Figure 4 shows the AC-coupled, gain of +2V/V, video buffer circuit used as the basis for the Electrical Characteristics table and Typical Characteristics curves. The circuit of Figure 4 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 604Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.7V of either supply pin, giving a $1.6V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (60.4Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor ($R_G$) is AC-coupled, giving the circuit a DC gain of +1, which puts the input DC bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 90mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA693 can deliver large bipolar output current into this midpoint load with minimal crossover distortion, as shown by the +5V supply, 3rd-harmonic distortion plots.

While the circuit of Figure 4 shows +5V single-supply operation, this same circuit may be used for single supplies ranging as high as +12V nominal. The noninverting input bias resistors are relatively low in Figure 4 to minimize output DC offset due to noninverting input bias current. At higher signal-supply voltage, these should be increased to limit the added supply current drawn through this path.

Figure 5 shows the AC-coupled, G = +1V/V, single-supply specification and test circuit. In this case, the gain setting resistor, $R_G$, is simply left open to get a gain of +1V for AC signals. Once again, the noninverting input is DC biased at mid-supply, putting that same $V_S/2$ at the output pin. The signal is AC-coupled into this midpoint with an added termination resistor on the source side of the blocking capacitor.

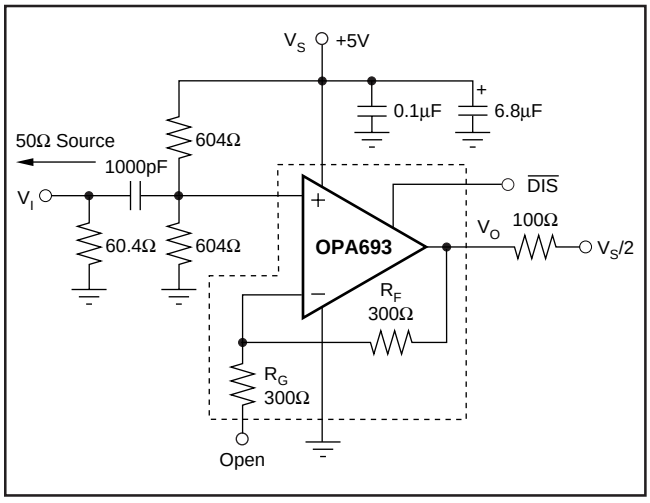



Figure 5. AC-Coupled, G = +1V/V, Single-Supply Specification and Test Circuit.

## SINGLE-SUPPLY ADC INTERFACE

Most modern, high-performance ADCs (such as the Texas Instruments ADS8xx series) operate on a single +5V (or lower) power supply. It has been a considerable challenge for single-supply op amps to deliver a low distortion input signal at the ADC input for signal frequencies exceeding 5MHz. The high slew rate, exceptional output swing, and high linearity of the OPA693 make it an ideal single-supply ADC driver. Figure 6 shows an example input interface to a very high-performance, 10-bit, 75MSPS CMOS converter.

The OPA693 in the circuit of Figure 6 provides > 500MHz bandwidth at an operating gain of +2V/V delivering $1V_{PP}$ at the output for a $0.5V_{PP}$ input. This broad bandwidth provides adequate margin to deliver low distortion to the maximum 20Mhz analog input frequency intended for the circuit of Figure 6. A 40MHz low-pass filter is provided as part of the converter interface to both limit broadband noise and reduce harmonics as the signal frequency exceeds 15MHz. The noninverting input bias voltage is referenced to the midpoint of the ADC signal range by dividing off the top and bottom of the internal ADC reference ladder.

## WIDEBAND UNITY GAIN BUFFER WITH IMPROVED FLATNESS

As shown in the Typical Characteristic curves, the unity gain buffer configuration of Figure 2 shows a peaking in the frequency response exceeding 2dB. This gives the slight amount of overshoot and ringing apparent in the gain of +1V/V pulse response curves. A similar circuit that holds a flatter frequency response, giving improved pulse fidelity, is shown in Figure 7.

This circuit removes the peaking by bootstrapping out any parasitic effects on $R_G$. The input impedance is still set by $R_M$ as the apparent impedance looking into $R_G$ is very high. $R_M$ may be increased to show a higher input impedance, but larger values will start to impact DC output offset voltage. This circuit creates an additional input offset voltage as the difference in the two input bias currents times the impedance to ground at $V_I$. Figure 8 shows a comparison of small-signal frequency response for the unity gain buffer of Figure 2 compared to the improved approach shown in Figure 7.

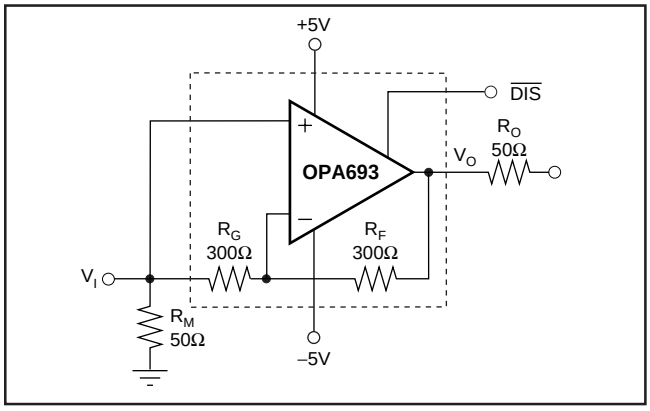



Figure 7. Improved Unity Gain Buffer.

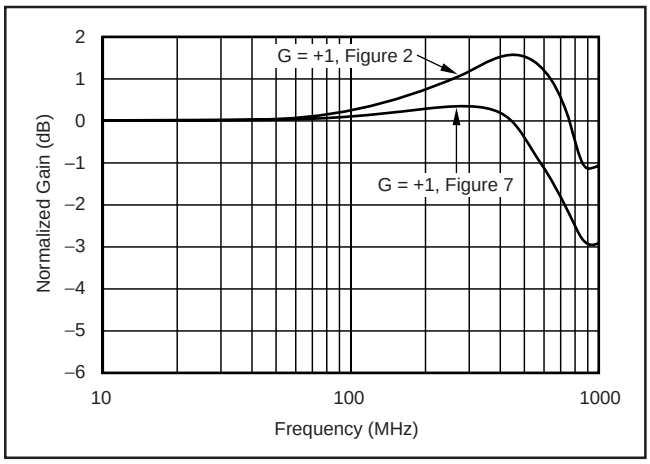



Figure 8. Buffer Frequency Response Comparison.

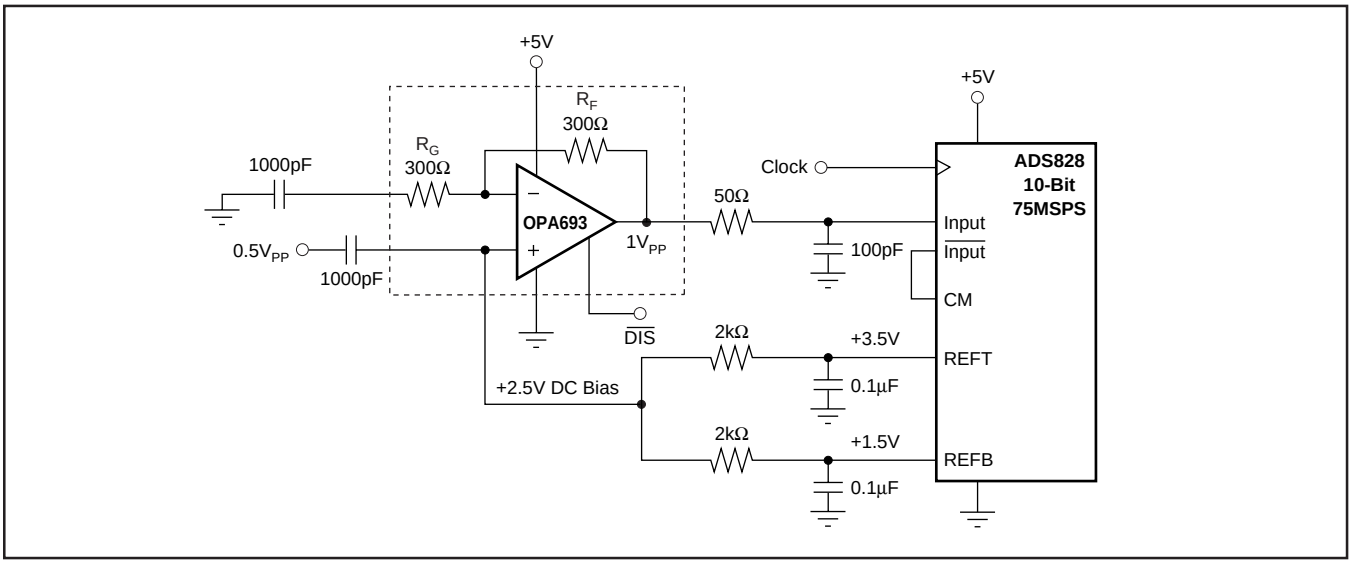



Figure 6. Wideband, AC-Coupled, Single-Supply ADC Driver.

## WIDEBAND, DC-COUPLED, SINGLE-TO-DIFFERENTIAL CONVERSION

The frequency response shown in Figure 7 for the improved gain of +1V/V buffer closely matches the inverting gain of –1V/V frequency response. Combining two OPA693s to give a +1 and –1 response will give a very broadband, DC-coupled, single-ended input to differential output conversion. Figure 9 shows this implementation where the input match is now set by $R_M$ in parallel with the $R_G$ resistor of the inverting stage. This circuit is essentially providing a DC to 700MHz 1:1 transformer operation. A 50Ω input match is shown, but this may be increased by increasing $R_M$. For instance, targeting a 200Ω input impedance requires an $R_M$ = 600Ω to get the parallel combination of $R_M$ and $R_G$ = 200Ω.

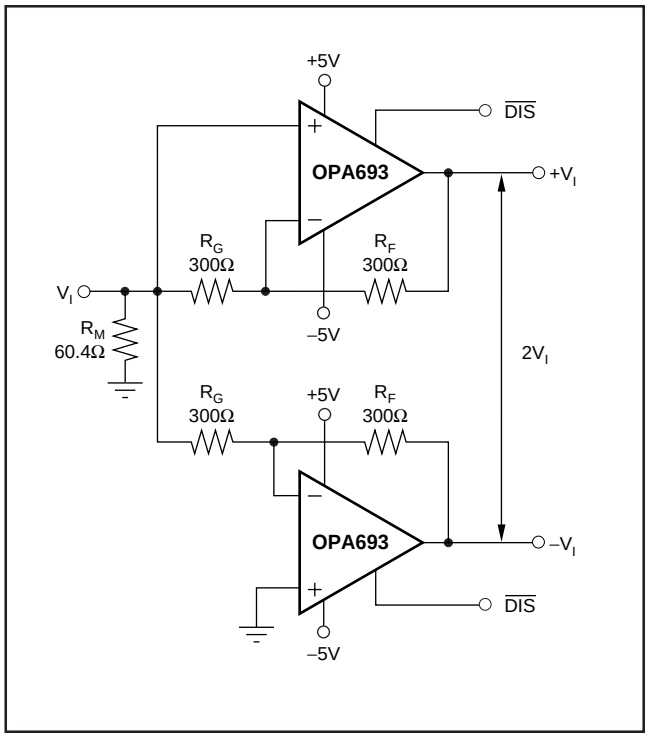



Figure 9. DC → 700MHz, Single-to-Differential Conversion.

## HIGH-FREQUENCY ACTIVE FILTERS

The extremely wide bandwidth of the OPA693 allows a wide range of active filter topologies to be implemented with minimal amplifier bandwidth interaction in the filter shape. Sallen-Key filters, using either a gain of 1 or gain of 2 amplifier, may be easily implemented with no external gain setting elements. In general, given a desired filter $W_O$, the amplifier should have at least 20X that $W_O$ to minimize filter interaction with the amplifier frequency response. Figure 10 shows an example gain of +2 line driver using the OPA693 that incorporates a 40MHz low-pass Butterworth response with just a few external components. The filter resistor values have been adjusted slightly here from an ideal filter analysis to account for parasitic effects.

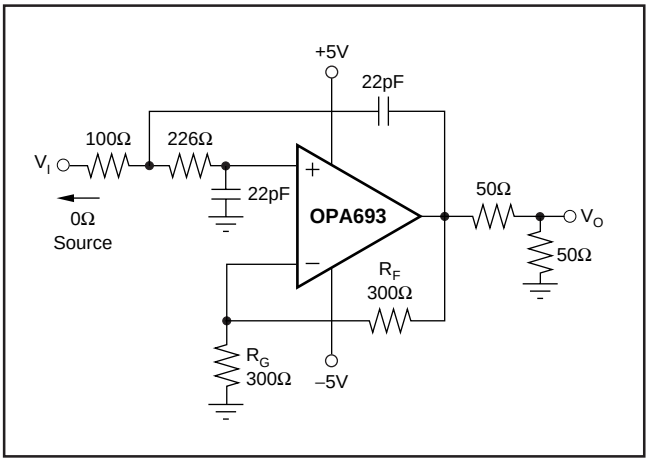



Figure 10. Line Driver with 40 MHz Low-Pass Active Filter.

This type of filter depends on a low output impedance from the amplifier through very high frequencies to continue to provide an increasing attenuation with frequency. As the amplifier output impedance rises with frequency, any input signal or noise starts to feed directly through to the output via the feedback capacitor. Since the OPA693 used in Figure 10 has a 700MHz bandwidth, the active filter will continue to roll off through frequencies exceeding 200MHz. Figure 11 shows the frequency response for the filter of Figure 10, where the desired 40MHz cutoff is achieved and a 40dB/dec rolloff is held through very high frequencies.

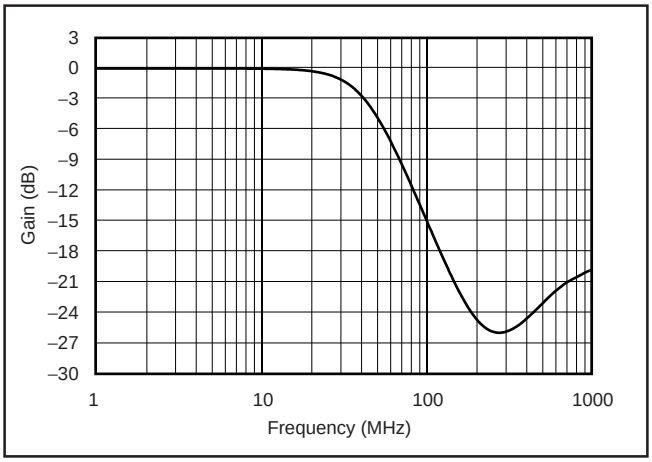



Figure 11. 40MHz Low-Pass Active Filter Response.

# DESIGN-IN TOOLS

## DEMONSTRATION BOARDS

Two printed circuit (PC) boards are available to assist in the initial evaluation of the circuit performance using the OPA693 in its two package styles. Both are available free as unpopulated PC boards delivered with descriptive documentation. The summary information for these boards is shown in Table I.

| PRODUCT | PACKAGE | DEMO BOARD PART NUMBER | LITERATURE REQUEST NUMBER |
|---|---|---|---|
| OPA693ID | SO-8 | DEM-OPA68xU | SBOU009 |
| OPA693IDBV | SOT23-6 | DEM-OPA6xxN | SBOU010 |

TABLE I. Demo Board Ordering Information.

To request either of these boards, check the Texas Instruments web site at www.ti.com.

# OPERATING SUGGESTIONS

## GAIN SETTING

Setting the gain for the OPA693 is very easy. For a gain of +2, ground the –IN pin and drive the +IN pin with the signal. For a gain of +1, either leave the –IN pin open and drive the +IN pin or drive both the +IN and –IN pins as shown in Figure 7. For a gain of –1, ground the +IN pin and drive the –IN pin with the input signal. An external resistor may be used in series with the –IN pin to reduce the gain. However, since the internal resistors ($R_F$ and $R_G$) have a tolerance and temperature drift different than the external resistor, the absolute gain accuracy and gain drift over temperature will be relatively poor compared to the previously described standard gain connections using no external resistor.

## OUTPUT CURRENT AND VOLTAGE

The OPA693 provides output voltage and current capabilities that can easily support multiple video loads and/or 100Ω loads with very low distortion. Under no-load conditions at 25°C, the output voltage typically swings to 1V of either supply rail; the tested swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±90mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or V-I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA693's output drive capabilities, noting that the graph is bounded by a "Safe Operating Area" of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA693 can drive ±3.4V into 20Ω or ±3.7V into 50Ω without exceeding either the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test-circuit load) shows full ±3.8V output swing capability, as shown in the Typical Characteristics.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the over-temperature min/max specifications. As the output transistors deliver power, their junction temperatures increase, which decreases their $V_{BE}$'s (increasing the available output voltage swing) and increases their current gains (increasing the available output current). In steady state operation, the available output voltage and current will always be greater than that shown in the over-temperature characteristics since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem, since most applications include a series matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to an adjacent positive power supply pin will, in most cases, destroy the amplifier. If additional protection to a power-supply short is required, consider a small series resistor in the power supply leads. Under heavy output loads, this will reduce the available output voltage swing. A 5Ω series resistor in each supply lead will limit the internal power dissipation to < 1W for an output short while decreasing the available output voltage swing only 0.5V, for up to 100mA desired load currents. Always place the 0.1μF power supply decoupling capacitors after these supply current limiting resistors directly on the device supply pins.

## DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC, including additional external capacitance, which may be recommended to improve ADC linearity. A high-speed, high open-loop gain, amplifier like the OPA693 can be very susceptible to decreased stability and may give closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show a Recommended $R_S$ vs Capacitive Load curve to help the designer pick a value to give < 0.1dB peaking to the load. The resulting frequency response curves show a 0.1dB peaked response for several selected capacitive loads and recommended $R_S$ combinations. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA693. Long PC board traces, unmatched cables, and connections to other amplifier inputs can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA693 output pin (see the Board Layout Guidelines section).

The criterion for setting this $R_S$ resistor is a maximum bandwidth, flat frequency response at the load (< 0.1dB peaking). For the OPA693 operating in a gain of +2, the frequency response at the output pin is very flat to begin with, allowing relatively small values of $R_S$ to be used for low capacitive loads.

## DISTORTION PERFORMANCE

The OPA693 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, the OPA693 holds much lower distortion at higher frequencies (> 20Mhz) than alternative solutions. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd harmonic will dominate the distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration it is just $R_F$ (see Figure 3). Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

The OPA693 has an extremely low 3rd-order harmonic distortion. This also produces a high 2-tone, 3rd-order intermodulation intercept. Two graphs for this intercept are given in the in the Typical Characteristics; one for ±5V and one for +5V. The lower curve shown in each graph is defined at the 50Ω load when driven through a 50Ω matching resistor, to allow direct comparisons to RF MMIC devices. The higher curve in each graph shows the intercept if the output is taken directly at the output pin with a 500Ω load, to allow prediction of the 3rd-order spurious level when driving a lighter load, such as an ADC input. The output matching resistor attenuates the voltage swing from the output pin to the load by 6dB. If the OPA693 drives directly into the input of a high-impedance device, such as an ADC, this 6dB attenuation is not taken and the intercept will increase a minimum of 6dB, as shown in the 500Ω load typical characteristic.

The intercept is used to predict the intermodulation spurious levels for two closely-spaced frequencies. If the two test frequencies (f1 and f2) are specified in terms of average and delta frequency, $f_O = (f1 + f2)/2$ and $\Delta f = |f2 - f1|/2$, then the two, 3rd-order, close-in spurious tones will appear at $f_O \pm 3 \times \Delta f$. The difference between two equal test tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \times (IM3 - P_O)$, where IM3 is the intercept taken from the Typical Characteristics and $P_O$ is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. For instance, at 50MHz, the OPA693 at a gain of +2 has an intercept of 44dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$ at this load, this requires each tone to be 4dBm ($1V_{PP}$). The 3rd-order intermodulation spurious tones will then be $2 \times (44 - 4) = 80$dBc below the test tone power level (–76dBm). If this same $2V_{PP}$ 2-tone envelope were delivered directly into a lighter 500Ω load, the intercept would increase to the 52dBm shown in the Typical Characteristics. With the same output signal and gain conditions, but now driving directly into a light load with no matching loss, the 3rd-order spurious tones will then be at least $2 \times (52 - 4) = 96$dBc below the 4dBm test tone power levels centered on 50MHz (–92dBm). We are still using a 4dBm for the $1V_{PP}$ output swing into this 500Ω load. While not strictly correct from a power standpoint, this does give the correct prediction for spurious level. The class AB output stage for the OPA693 is much more voltage swing dependent on output distortion than strictly power dependent. To use the 500Ω intercept curve, use the single-tone voltage swing as if it were driving a 50Ω load to compute the $P_O$ used in the intercept equation.

## GAIN ACCURACY AND LINEARITY

The OPA693 provides improved absolute gain accuracy and DC linearity over earlier fixed gain of two line drivers. Operating at a gain of +2V/V by tying the –IN pin to ground, the OPA693 shows a maximum gain error of ±0.9% at 25°C. The DC gain will therefore lie between 1.982V/V and 2.018V/V at room temperature. Over the specified temperature ranges, this gain tolerance expands only slightly due to the matched temperature drift for $R_F$ and $R_G$. Achieving this gain accuracy requires a very low impedance ground at –IN. Typical production lots show a much tighter distribution in gain than this ±0.9% specification. Figure 12 shows a typical distribution in measured gain at the gain of +2V/V configuration, in this case showing a slight drop in the mean (0.25%) from the nominal but with a very tight distribution.

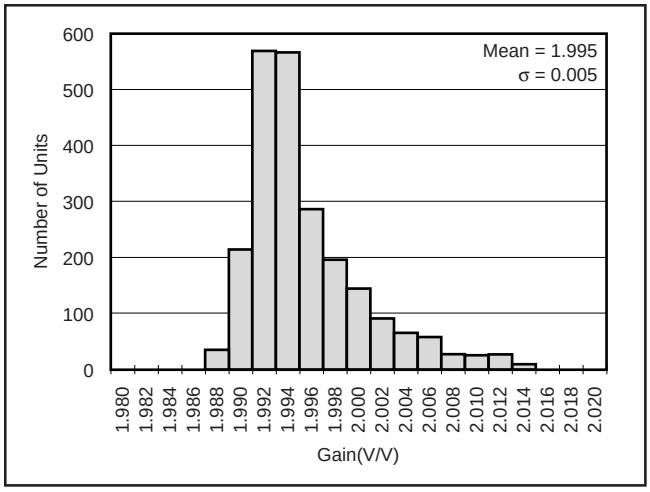



Figure 12. Typical +2V/V Gain Distribution.

The exceptionally linear output stage (as illustrated by the high 3rd-order intermodulation intercept) and low thermal gradient induced errors for the OPA693 give an extremely linear output over large voltage swings and heavy loads. Figure 13 shows the tested deviation (in % of peak to peak) from linearity for a range of symmetrical output swings and loads. Below $4V_{PP}$, for either a 100Ω or a 500Ω load, the OPA693 delivers > 14-bit linear output response.

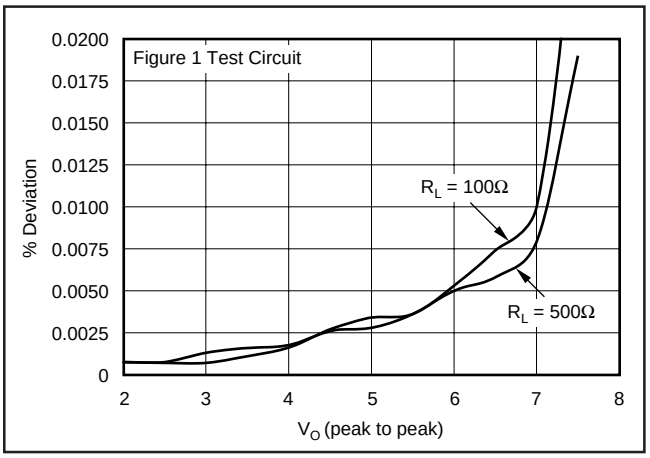



Figure 13. DC Linearity vs Output Swing and Loads.

## NOISE PERFORMANCE

The OPA693 offers an excellent balance between voltage and current noise terms to achieve a low output noise under a variety of operating conditions. The inverting node noise current (internal) will appear at the output multiplied by the relatively low 300Ω feedback resistor. The input noise voltage (1.8nV/$\sqrt{Hz}$) is extremely low for a unity gain stable amplifier. This low input voltage noise was achieved at the price of higher noninverting input current noise (17.8pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting input is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise for the each of the three gain settings available using the OPA693. Figure 14 shows the op amp noise analysis model with all of the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

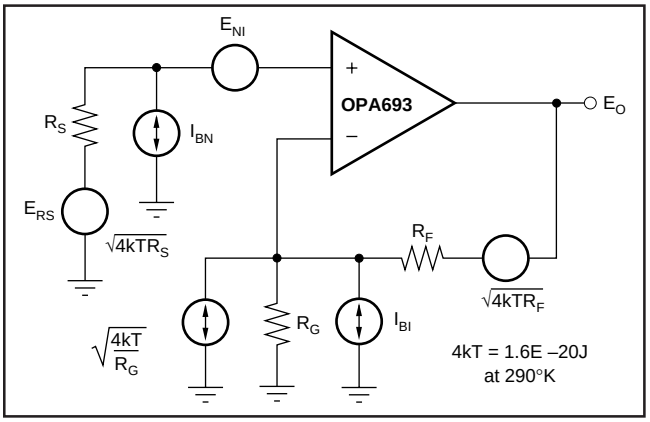



Figure 14. Op Amp Noise Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 14.

(1)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression through by noise gain ($NG = 1 + R_F/R_G$) will give the equivalent input-referred spot noise voltage at the non-inverting input, as shown in Equation 2.

(2)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating the output noise and input noise expressions for the two noninverting gain configurations, and with two different values for the noninverting source impedance, gives output and input referred spot noise voltages of Table II.

| CONFIGURATION | $R_S$ (Ω) | OUTPUT SPOT NOISE $E_O$ (nV/$\sqrt{Hz}$) | TOTAL INPUT SPOT NOISE $E_N$ (nV/$\sqrt{Hz}$) |
|---|---|---|---|
| G = +2 (Figure 1) | 25 | 8.3 | 4.15 |
| G = +2 (Figure 1) | 300 | 14 | 7 |
| G = +1 (Figure 2) | 25 | 7.3 | 7.3 |
| G = +1 (Figure 2) | 300 | 9.2 | 9.2 |

TABLE II. Total Output and Input Referred Noise.

The output noise is being dominated by the inverting current noise times the internal feedback resistor. This gives a total input referred noise voltage that exceeds the 1.8nV voltage term for the amplifier itself.

## DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA693 provides exceptional bandwidth and slew rate giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm(NG \times V_{OS}) + (I_{BN} \times R_S/2 \times NG) \pm (I_{BI} \times R_F)$

$= \pm(2 \times 2.0mV) \pm (35\mu A \times 25\Omega \times 2) \pm (50\mu A \times 300\Omega)$

$= \pm 4mV \pm 1.75mV \pm 15mV$

$= \pm 30.75mV$

where NG = noninverting signal gain.

Minimizing the resistance seen by the noninverting input will minimize the output DC error. For improved DC precision in a wideband low-gain amplifier, consider the OPA842 where a bipolar input is acceptable (low source resistance) or the OPA656 where a JFET input is required.

## DISABLE OPERATION

The OPA693 provides an optional disable feature that can be used to reduce system power. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA693 will operate normally. This shutdown is intended only as a power-savings feature. Forward path isolation when disabled is very good for small signals for gains of +1 or +2. Large-signal isolation is not ensured. Using this feature to multiplex two or more outputs together is not recommended. Large signals applied to the disabled output stages can turn on parasitic devices degrading signal linearity for the desired channel.

Turn-on time is very quick from the shutdown condition, typically < 60ns. Turn-off time is strongly dependent on the selected gain configuration and load, but is typically 3µs for the circuit of Figure 1.

To shutdown, the control pin must be asserted low. This logic control is referenced to the positive supply, as shown in the simplified circuit of Figure 15.

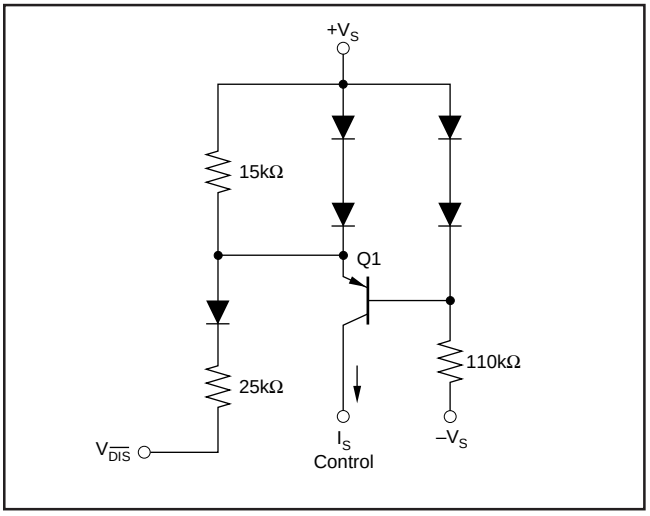



Figure 15. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 15kΩ, eventually turning on these two diodes (≈80µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the shutdown mode is only that required to operate the circuit of Figure 15.

The shutdown feature for the OPA693 is a positive supply referenced, current-controlled, interface. Open collector (or drain) interfaces are most effective, as long as the controlling logic can sustain the resulting voltage (in the open mode) that will appear at the $V_{\overline{DIS}}$ pin. That voltage will be one diode below the positive supply voltage applied to the OPA693. For voltage output logic interfaces, the on/off voltage levels described in the Electrical Characteristics apply only for a +5V positive supply on the OPA693. An open-drain interface is recommended for shutdown operation using a higher positive supply for the OPA693 and/or logic families with inadequate high-level voltage swings.

## THERMAL ANALYSIS

The OPA693 does not require heatsinking or airflow in most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described here. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature ($T_J$) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation ($P_D$) is the sum of quiescent power ($P_{DQ}$) and additional power dissipated in the output stage ($P_{DL}$) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. $P_{DL}$ will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$ where $R_L$ includes feedback network loading. This is the absolute highest power that can be dissipated for a given $R_L$. All actual applications will dissipate less power in the output stage.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum $T_J$ using an OPA693IDBV (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load. Maximum internal power is:

$P_D = 10V \times 14.1mA + 5^2 /(4 \times (100\Omega + || \ 600\Omega)) = 214mW$

Maximum $T_J = +85°C + (0.21W \times 150°C/W) = 117°C$.

All actual applications will operate at a lower junction temperature than the 117°C computed above. Compute your actual output stage power to get an accurate estimate of maximum junction temperature, or use the results shown here as an absolute maximum.

## BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA693 requires careful attention to PC board layout parasitics and external component types. Recommendations that will optimize performance include:

**a) Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, create a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

**b) Minimize the distance** (< 0.25") from the power supply pins to high frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

**c) Careful selection and placement of external components will preserve the high frequency performance of the OPA693.** Use resistors that have low reactance at high frequencies. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Since the inverting input node is internal for the OPA693, it is more robust to layout issues than amplifiers with similar speed but external feedback and gain resistors. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Good axial metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 2.0kΩ, this parasitic capacitance can add a pole and/or zero below 400MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations.

**d) Connections to other wideband devices** on the PC board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set $R_S$ from the plot of *Recommended $R_S$ vs Capacitive Load*. Low parasitic capacitive loads (< 4pF) may not need an $R_S$ since the OPA693 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA693 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Recommended $R_S$ vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

**e) Socketing a high-speed part like the OPA693 is not recommended**. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA693 directly onto the board.

## INPUT AND ESD PROTECTION

The OPA693 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 16.

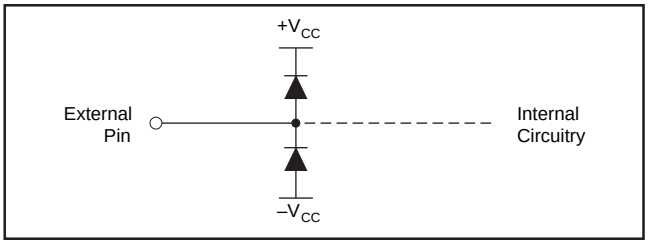



Figure 16. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA693), current limiting series resistors may be added on the noninverting input. Keep this resistor value as low as possible since high values degrade both noise performance and frequency response. The inverting input already has a 300Ω resistor from the external pin to the internal summing junction for the op amp. This provides considerable protection for that node.

## Revision History

| DATE | REVISION | PAGE | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 7/08 | A | 2 | Abs Max Ratings | Changed Storage Temperature Range from –40°C to +125C to –65°C to +125C. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA693ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 693 | Samples |
| OPA693IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | C59 | Samples |
| OPA693IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | C59 | Samples |
| OPA693IDG4 | ACTIVE | SOIC | D | 8 | 75 | TBD | Call TI | Call TI | -40 to 85 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

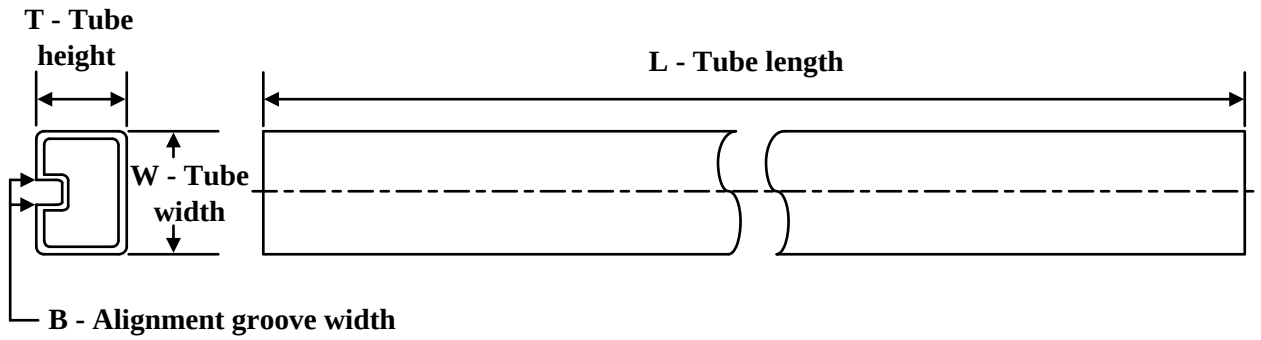
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

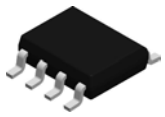
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| OPA693ID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

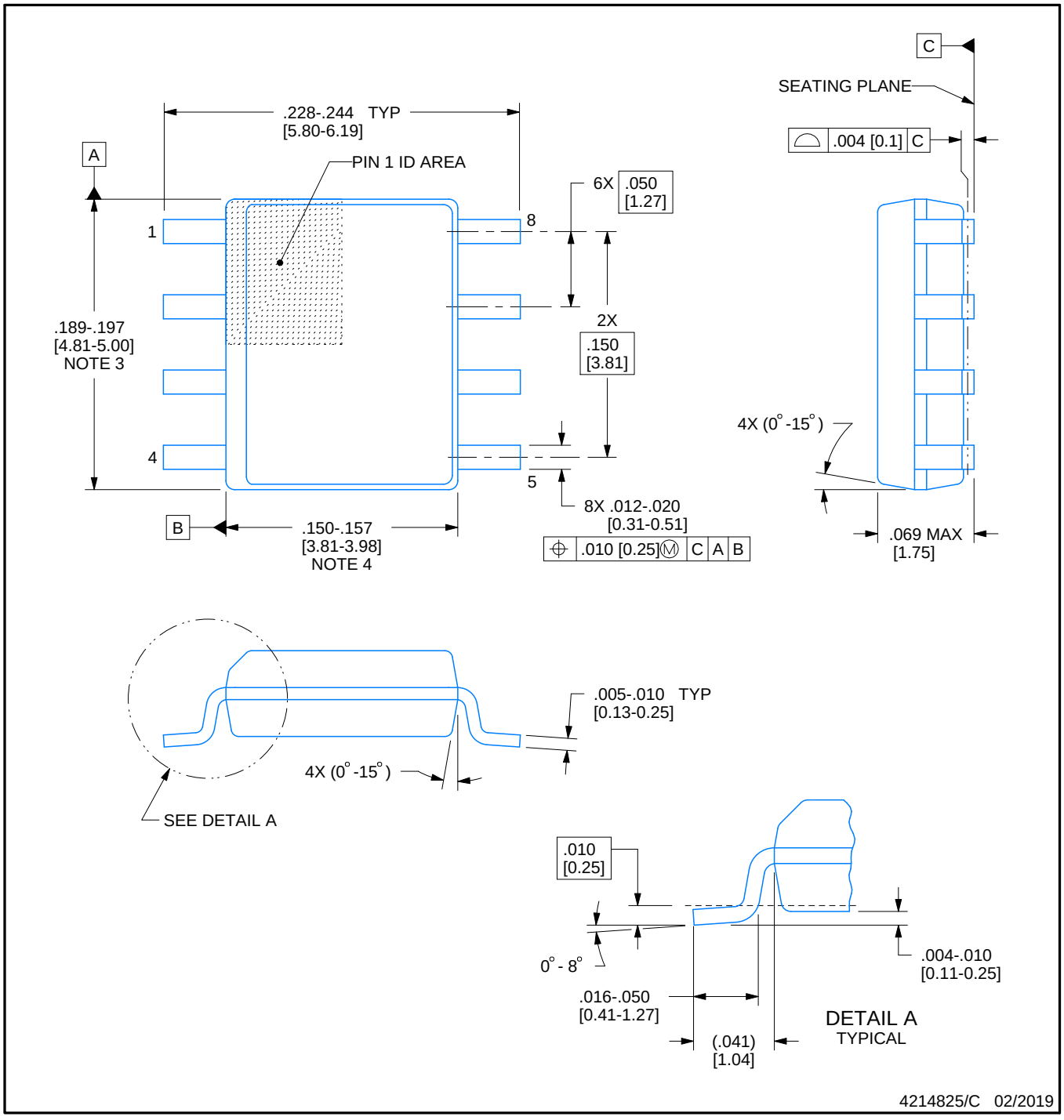


# PACKAGE OUTLINE

## D0008A

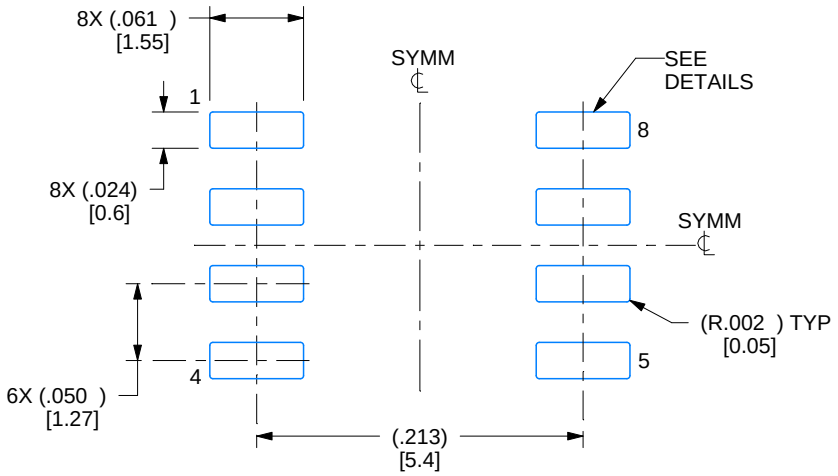
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

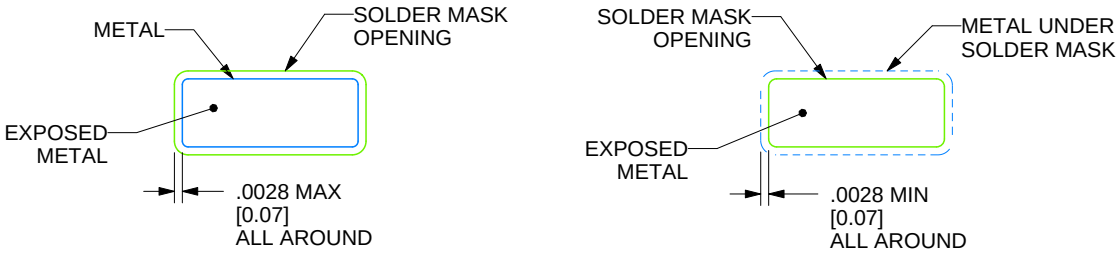



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

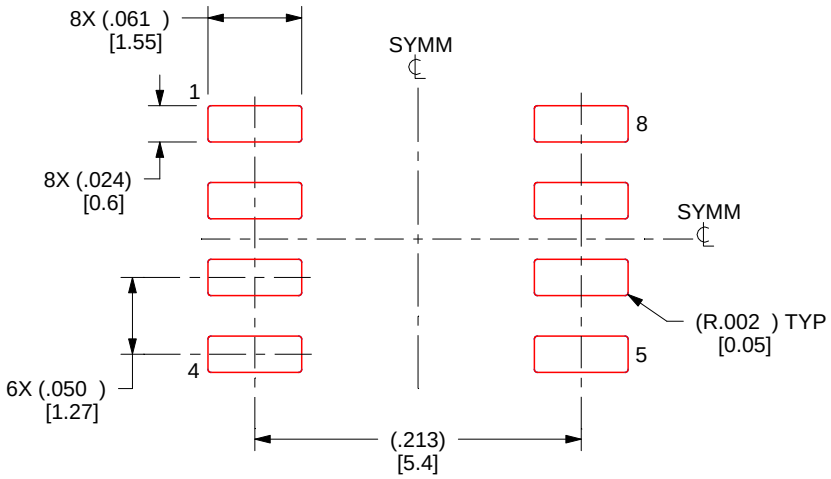
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

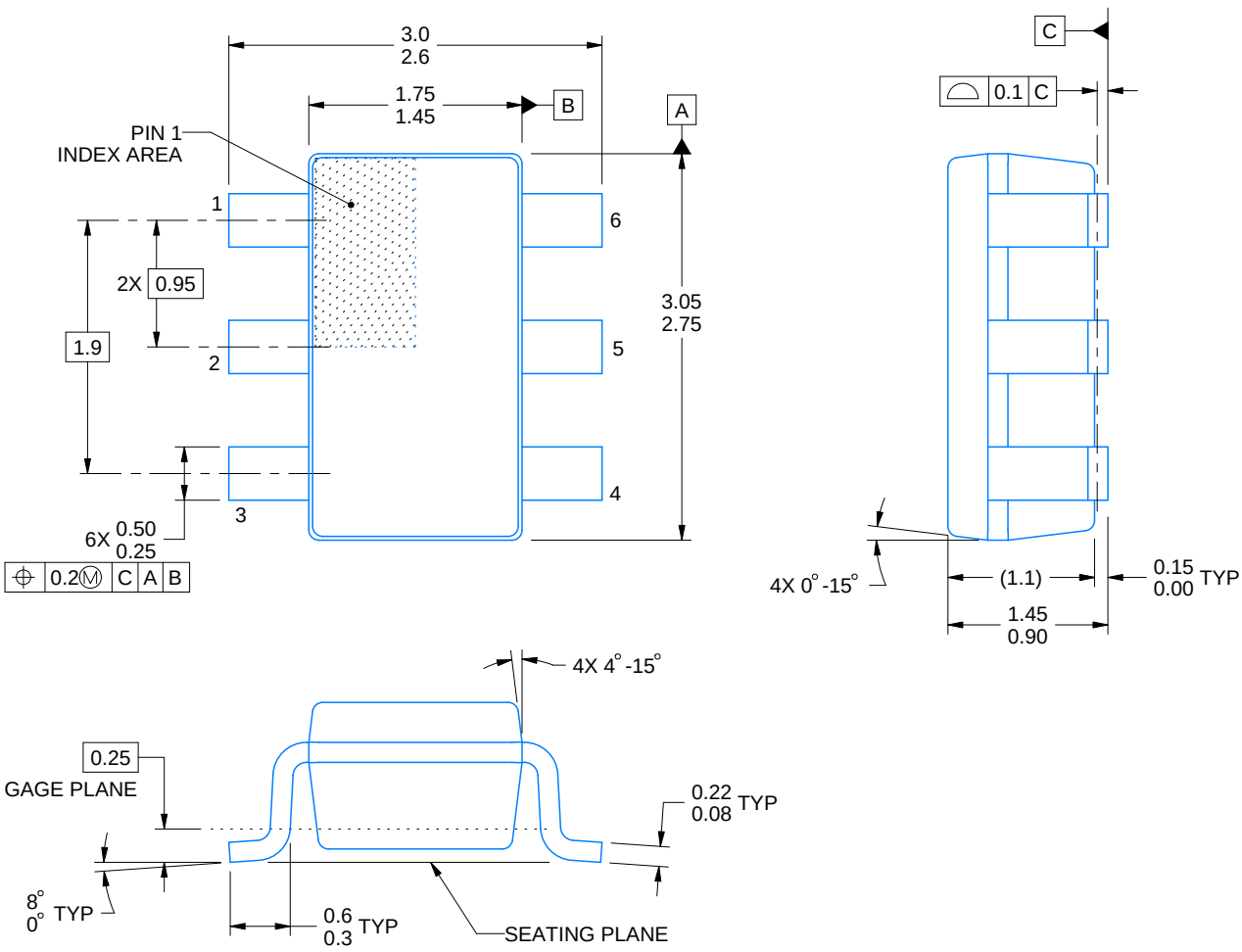
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

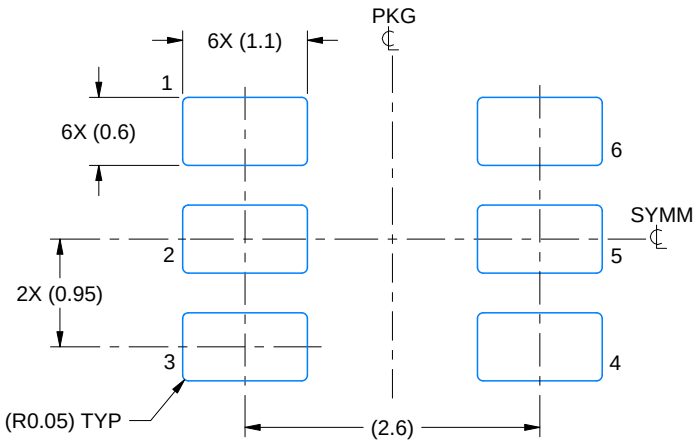
SMALL OUTLINE TRANSISTOR



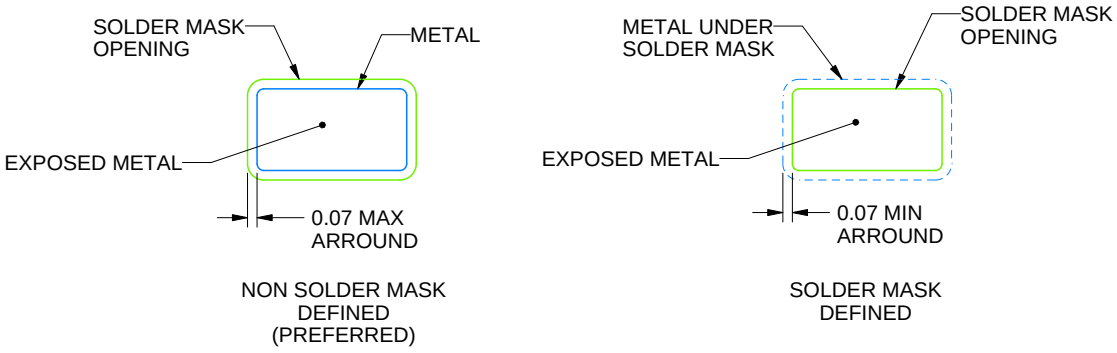

4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

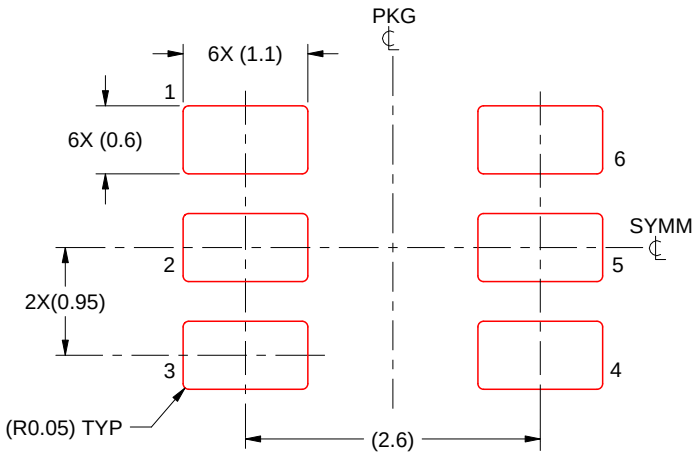



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265