OPA955 11GHz Gain Bandwidth Product, Gain of 7V/V Stable, Bipolar Input Amplifier

1 Features

- High gain bandwidth product: 11GHz
- Decompensated, gain ≥ 7V/V (stable)
- Ultra low input voltage noise: 0.79nV/√Hz
- Slew rate: 3750V/µs
- Low input capacitance:
  - Common-mode: 0.9pF
  - Differential: 0.2pF
- Wide input common-mode range:
  - 0.4V from positive supply
  - 1.1V from negative supply
- $3V_{PP}$ total output swing
- Supply voltage range: 3.3V to 5.25V
- Quiescent current: 20.2mA
- Package: 8-pin WSON
- Temperature range: –40°C to +125°C

2 Applications

- Optical time domain reflectometry (OTDR) front-end
- ToF LiDAR front-end
- Active probe design
- Optical In-vitro diagnostics (IVD) front-end
- Solid-state scanning LiDAR front-end
- Silicon photomultiplier (SiPM) buffer amplifier
- Photomultiplier tube post amplifier
- High-speed data acquisition (DAQ)

3 Description

The OPA955 is a wideband, ultra-low noise operational amplifier with bipolar inputs for wideband transimpedance and voltage feedback amplifier applications. When the device is configured as a transimpedance amplifier (TIA), the 11GHz gain bandwidth product (GBWP) enables high closed-loop bandwidths at transimpedance gains up to tens of kilohms. The following graphs show the transimpedance bandwidth and transimpedance pulse response performance of the OPA955 in low-capacitance photodiode (PD) applications.

The OPA955 is a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require ultra-low noise and high-gain front ends. For example, the OPA955 can operate in optical time-of-flight (ToF) systems along with time-to-digital converters, such as the TDC7201, and integrated laser drivers, such as the LMH13000. The OPA955 can also be used to drive a high-speed analog-to-digital converter (ADC) in high-resolution LiDAR systems with a differential output amplifier, such as the THS4541 or LMH5401 devices. For optimized frequency respone, the OPA955 package has a feedback pin (FB) that simplifies the feedback network connection between the input and output.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA955	DSG (WSON, 8)	2mm × 2mm

(1) See the *Device Comparison Table*.
(2) For more information, see Section 12.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.

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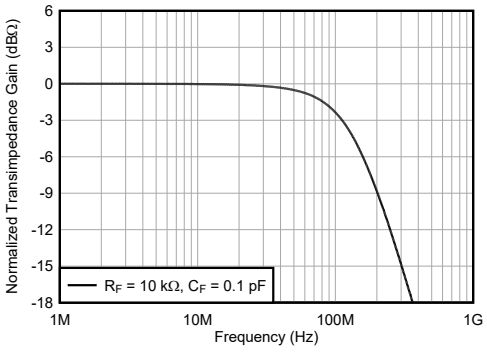
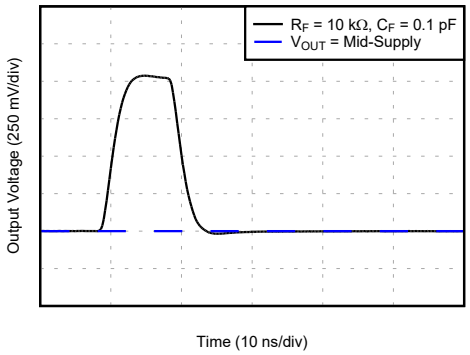


I_{IN} = 20 μA_{PP}, C_{IN} = 4.7pF

Transimpedance Bandwidth vs Frequency



I_{IN} = 100 µA Pulse, C_{IN} = 4.7pF

Transimpedance Pulse Response

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4 Device Comparison Table

DEVICE	INPUT TYPE	MINIMUM STABLE GAIN (V/V)	VOLTAGE NOISE (nV/√Hz)	CURRENT NOISE (pA/√Hz)	INPUT CAPACITANCE (pF)	GAIN BANDWIDTH (GHz)
OPA955	Bipolar	7	0.79	0.55	1.1	11
OPA855	Bipolar	7	0.98	2.5	0.8	8
OPA856	Bipolar	1	0.9	2.5	1.1	1.1
OPA858	CMOS	7	2.5	0.055	0.8	5.5
OPA859	CMOS	1	3.3	0.055	0.8	0.9
LMH6629	Bipolar	10	0.69	2.6	2.1	4
OPA818	JFET	7	2.2	0.145	2.4	2.7

5 Pin Configuration and Functions

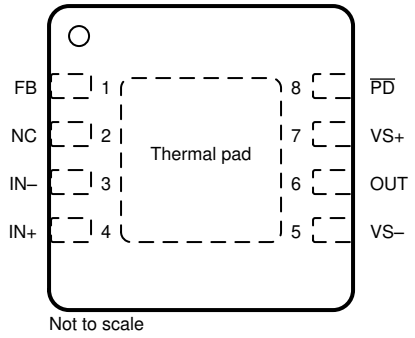

**Figure 5-1. DSG Package,
8-Pin WSON With Exposed Thermal Pad
(Top View)**

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
FB	1	Input	Feedback connection to output of amplifier
IN–	3	Input	Inverting input
IN+	4	Input	Noninverting input
NC	2	—	Do not connect
OUT	6	Output	Amplifier output
$\overline{PD}$	8	Input	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VS–	5	—	Negative voltage supply
VS+	7	—	Positive voltage supply
Thermal pad		—	Connect the thermal pad to a heat-spreading power or ground plane.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)		5.5	V
V_{IN+}, $V_{IN–}$	Input voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
V_{ID}	Differential input voltage		1	V
VOUT	Output voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current(2)		±50	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)	3.3	5	5.25	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA955 DSG (WSON) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	45	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	6.8	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	45.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at V_{S+} = 5 V, V_{S-} = 0 V, G = 7 V/V, R_F = 453 Ω, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		2.8		GHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		1.2		GHz
GBWP	Gain-bandwidth product			11		GHz
	Bandwdith for 0.1-dB flatness			800		MHz
SR	Slew rate (10%-90%)	V_{OUT} = 2-V step		3750		V/µs
t_r	Rise time	V_{OUT} = 100-mV step		0.13		ns
t_f	Fall time	V_{OUT} = 100-mV step		0.13		ns
	Settling time to 0.1%	V_{OUT} = 2-V step		2.3		ns
	Settling time to 0.01%	V_{OUT} = 2-V step		10		ns
	Overshoot or undershoot	V_{OUT} = 2-V step		10		%
	Overdrive recovery	2x output overdrive		3		ns
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		-79		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		-62		
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		-88		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		-74		
e_n	Input-referred voltage noise	f = 1 MHz		0.79		nV/√Hz
e_i	Input-referred current noise	f = 1 MHz		0.55		pA/√Hz
z_O	Closed-loop output impedance	f = 1 MHz		0.06		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain		70	76		dB
V_{OS}	Input offset voltage	T_A = 25°C	–1.5	±0.2	1.5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = –40°C to 125°C		1		µV/°C
I_B	Input bias current (1)	T_A = 25°C	–5	-2	–0.1	µA
$\Delta I_B/\Delta T$	Input bias current drift	T_A = –40°C to +125°C		–0.08		µA/°C
I_{BOS}	Input offset current	T_A = 25°C	–0.6	±0.2	0.6	µA
$\Delta I_{BOS}/\Delta T$	Input offset current drift	T_A = –40°C to +125°C		1		nA/°C
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V referred to midsupply	80	86		dB
INPUT						
	Common-mode input resistance			2.3		MΩ
C_{CM}	Common-mode input capacitance			0.9		pF
	Differential input resistance			50		kΩ
C_{DIFF}	Differential input capacitance			0.2		pF
V_{IH}	Common-mode input range (high)	CMRR > 80 dB, V_{S+} = 3.3 V	2.7	2.9		V
V_{IL}	Common-mode input range (low)	CMRR > 80 dB, V_{S+} = 3.3 V		0.9	1.4	V
V_{IH}	Common-mode input range (high)	CMRR > 80 dB	4.4	4.6		V
V_{IH}	Common-mode input range (high)	T_A = –40°C to +125 °C, CMRR > 80 dB		4.55		V
V_{IL}	Common-mode input range (low)	CMRR > 80 dB		1.1	1.35	V
V_{IL}	Common-mode input range (low)	T_A = –40°C to +125°C, CMRR > 80 dB		1.3		V

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at V_{S+} = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, R_F = 453 Ω, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OH}	Output voltage (high)(2)	T_A = 25°C, V_{S+} = 3.3 V	2.35	2.4		V
V_{OH}	Output voltage (high)(2)	T_A = 25°C	3.95	4.1		V
		T_A = –40°C to +125°C		4		
V_{OL}	Output voltage (low)(2)	T_A = 25°C, V_{S+} = 3.3 V		1.05	1.15	V
V_{OL}	Output voltage (low)(2)	T_A = 25°C		1.05	1.15	V
		T_A = –40°C to +125°C		1.0		
I_{O_LIN}	Linear output drive (sink and source)	R_L = 10 Ω, A_{OL} > 60 dB	65	80		mA
		T_A = –40°C to +125°C, R_L = 10 Ω, A_{OL} > 60 dB		70		
I_{SC}	Output short-circuit current		80	105		mA
POWER SUPPLY						
I_Q	Quiescent current		18	20.2	22	mA
		T_A = –40°C		18.7		
		T_A = 125°C		22		
PSRR+	Positive power-supply rejection ratio		80	86		dB
PSRR–	Negative power-supply rejection ratio		70	80		
POWER DOWN						
	Disable voltage threshold	Amplifier OFF below this voltage	0.65	0.95		V
	Enable voltage threshold	Amplifier ON above this voltage		1	1.8	V
	Power-down quiescent current			465	520	µA
	$\overline{PD}$ bias current			30	50	µA
	Turnon time delay	Time to V_{OUT} = 90% of final value		120		ns
	Turnoff time delay			30		ns

(1) Current flowing into the input pin is considered negative
(2) Amplifier output saturated

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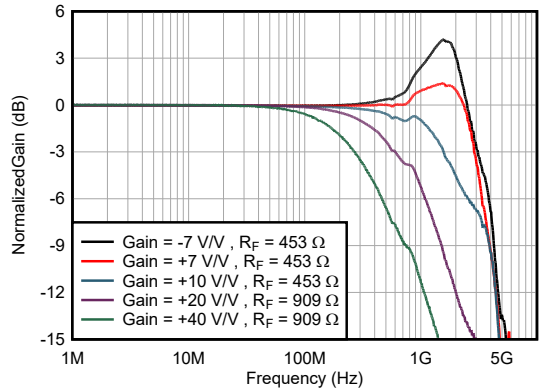
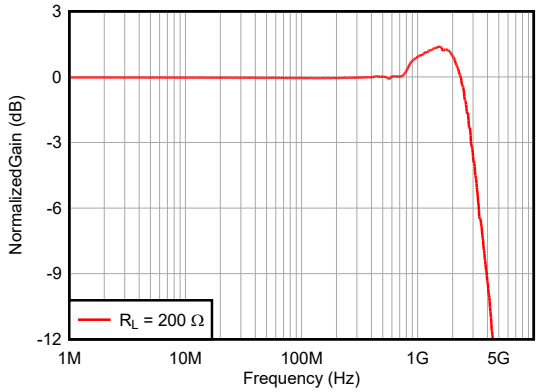
6.6 Typical Characteristics

at T_A = 25°C, V_{S+} = 2.5V, $V_{S–}$ = –2.5V, V_{IN+} = 0V, R_F = 453Ω, gain = 7 V/V, R_L = 200Ω, and output load referenced to midsupply (unless otherwise noted)



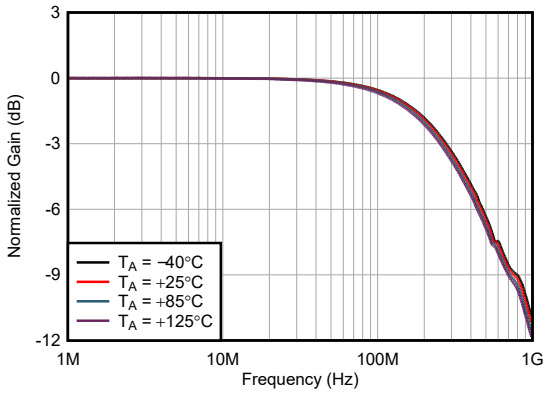
V_{OUT} = 100mV_{PP}; for circuit configuration, see Section 7

Figure 6-1. Small-Signal Frequency Response vs Gain



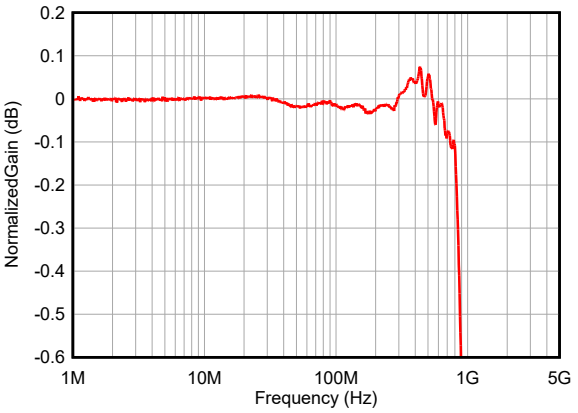
V_{OUT} = 100mV_{PP}

Figure 6-2. Small-Signal Frequency Response vs Output Load



Gain = 40V/V, R_F = 909Ω, V_{OUT} = 100mV_{PP}

Figure 6-3. Small-Signal Frequency Response vs Ambient Temperature



V_{OUT} = 2V_{PP}

Figure 6-4. Large-Signal Response for 0.1dB Gain Flatness

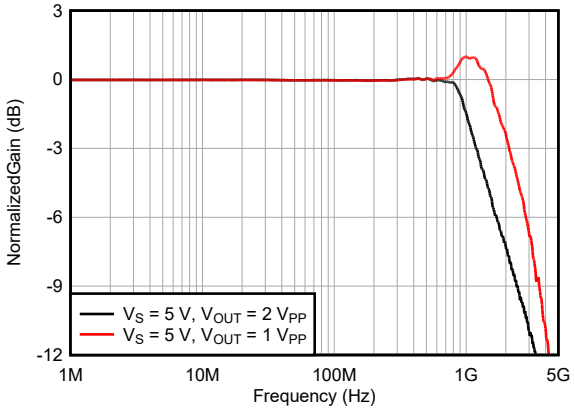
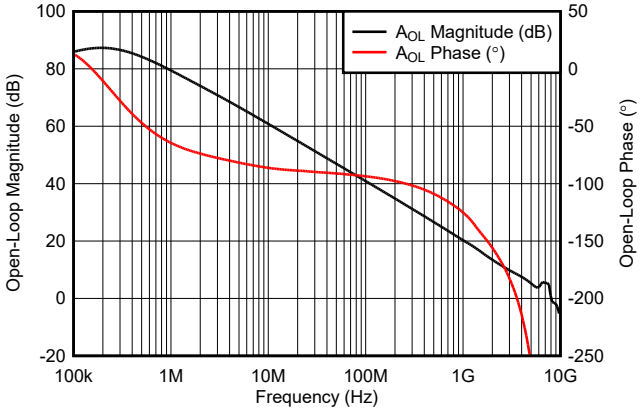


Figure 6-5. Large-Signal Frequency Response vs Voltage Supply



Small-signal response

Figure 6-6. Open-Loop Magnitude and Phase vs Frequency

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5V, $V_{S–}$ = –2.5V, V_{IN+} = 0V, R_F = 453Ω, gain = 7 V/V, R_L = 200Ω, and output load referenced to midsupply (unless otherwise noted)

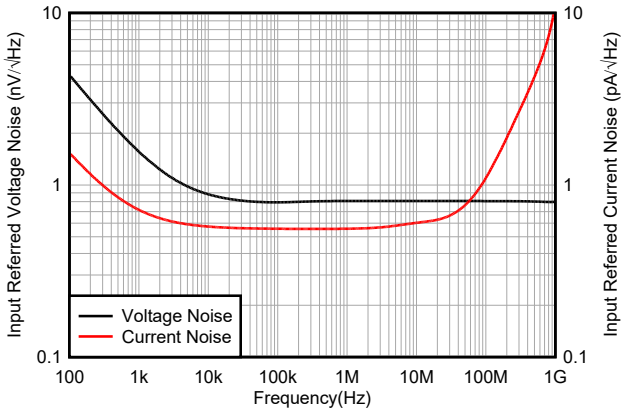

Figure 6-7. Voltage and Current Noise Density vs Frequency

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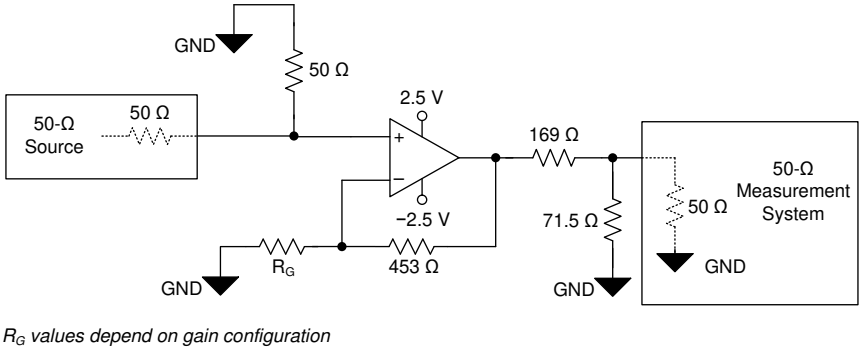
7 Parameter Measurement Information

The various test setup configurations for the OPA955 are shown in Figure 7-1, Figure 7-2, and Figure 7-3. When configuring the OPA955 in a gain of +20V/V and +40V/V, set the feedback resistor R_F to 909Ω.

Figure 6-1 shows 5dB of peaking with the amplifier in an inverting configuration of –7V/V with the amplifier configured as shown in Figure 7-2. The 50Ω matched termination of this circuit configuration results in the amplifier being configured in a noise gain of 5.3V/V, which is lower than the recommended +7V/V.



R_G values depend on gain configuration

Figure 7-1. Noninverting Configuration

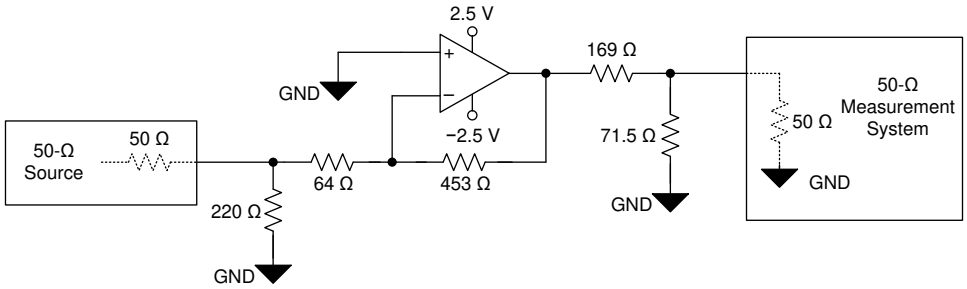


Figure 7-2. Inverting Configuration (Gain = –7V/V)

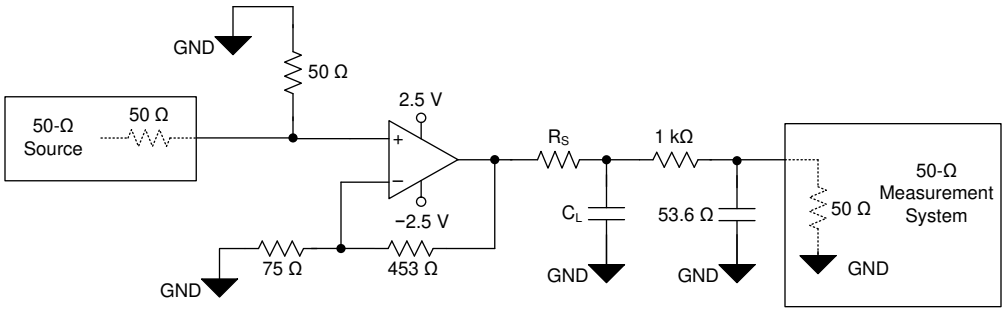


Figure 7-3. Capacitive Load Driver Configuration

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8 Detailed Description

8.1 Overview

The ultra-wide, 11GHz gain bandwidth product (GBWP) of the OPA955, combined with the ultra-low broadband voltage noise of 0.79nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA955 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA955 has 1.2GHz of large-signal bandwidth ($2V_{PP}$), and a slew rate of 3750V/µs, making the device a viable option for high-speed pulsed applications.

8.2 Functional Block Diagram

The OPA955 is a classic voltage-feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, such as the two basic options in Figure 8-1 and Figure 8-2.The resistor on the noninverting pin is used for bias current cancellation to minimize the output offset voltage. In a noninverting configuration, the additional resistors on the noninverting pin add noise to the system; therefore, if SNR is critical, the resistor can be eliminated. In an inverting configuration, the noninverting node is typically connected to a dc voltage; therefore, the high-frequency noise contribution from the bias cancellation resistor can be bypassed by adding a large 1-µF capacitor in parallel to the resistor to shunt the noise. The dc operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

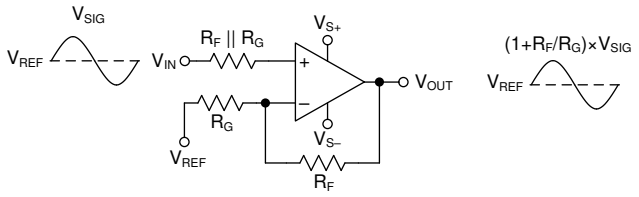

Figure 8-1. Noninverting Amplifier

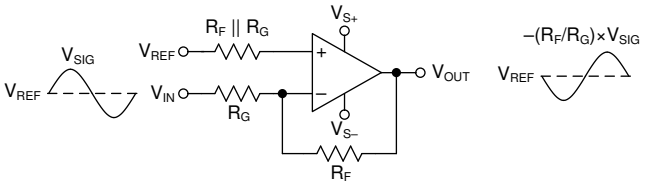

Figure 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA955 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as Figure 8-3 shows. There are two anti-parallel diodes between the inputs of the amplifier that clamp the inputs during an over-range or fault condition.

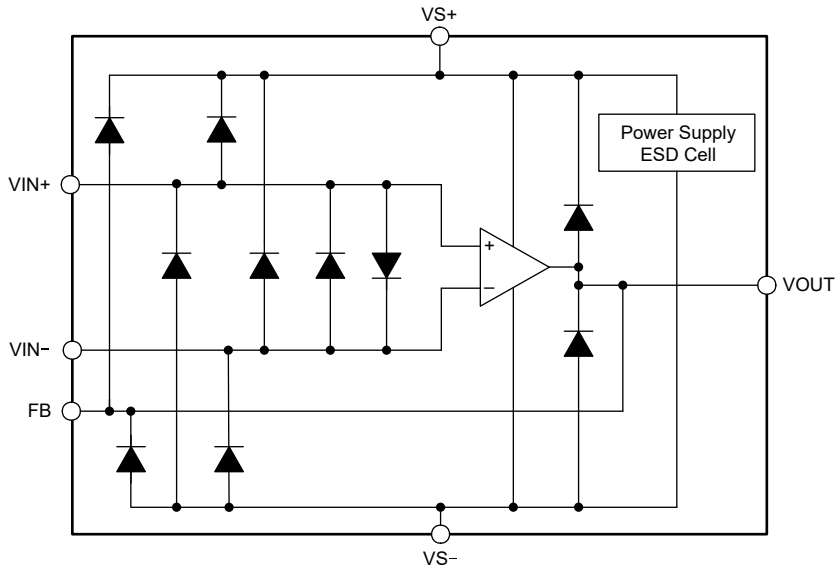

Figure 8-3. Internal ESD Structure

8.3.2 Feedback Pin

The OPA955 pin layout is optimized to minimize parasitic inductance and capacitance, which is a critical care about in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN– pin on the same side of the package (see Figure 8-4) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins by increasing the physical separation between the pins.

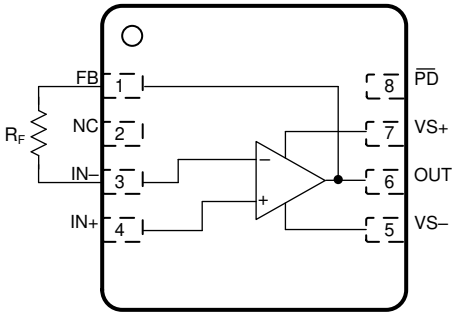

Figure 8-4. R_F Connection Between FB and IN– Pins

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8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA955 can be configured with single-sided supplies or split supplies; see also Figure 9-1. Split-supply operation using balanced supplies with the input common-mode set to ground can help ease lab testing (because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground). In split-supply operation, connect the thermal pad to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA955 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. In single-supply operation, level shift the dc input and output reference voltages by half the difference between the power supply rails. This configuration maintains the input common-mode and output load reference at midsupply. To eliminate gain errors, the source driving the reference input common-mode voltage must have low output impedance across the frequency range of interest. In this case, connect the thermal pad to ground.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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9.1 Power Supply Recommendations

The OPA955 operates on supplies from 3.3V to 5.25V. The OPA955 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA955 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3V supplies.

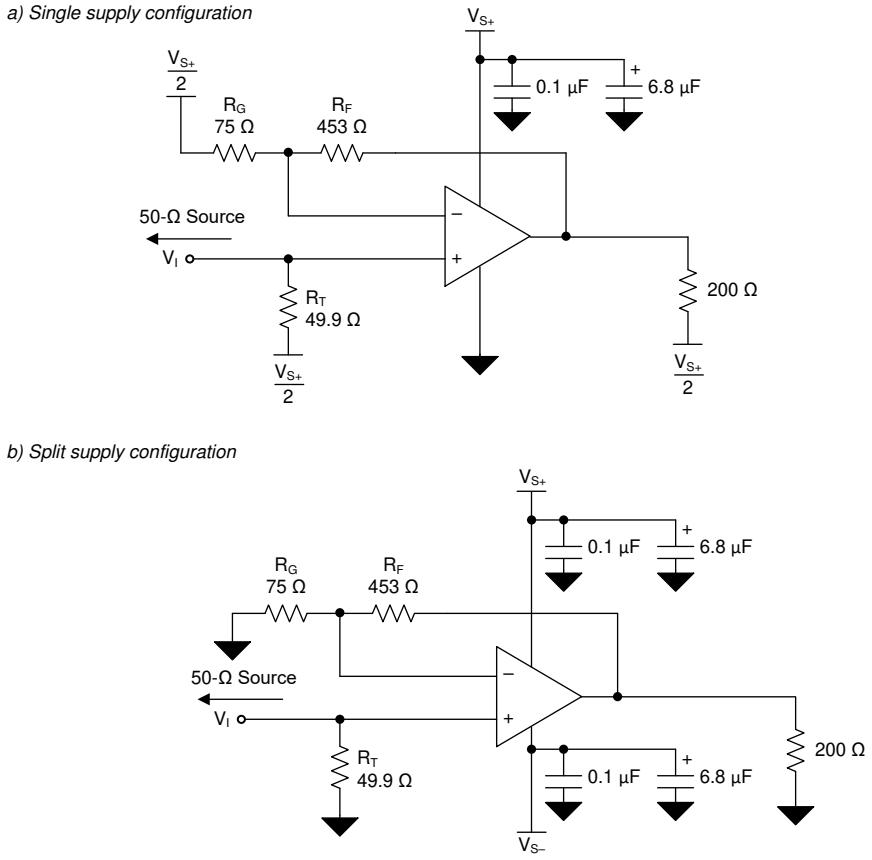

Figure 9-1. Split and Single Supply Circuit Configuration

ADVANCE INFORMATION

9.2 Layout

9.2.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA955 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
- **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- **Careful selection and placement of external components preserves the high-frequency performance of the OPA955.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wire-wound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA955 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

9.2.2 Layout Example

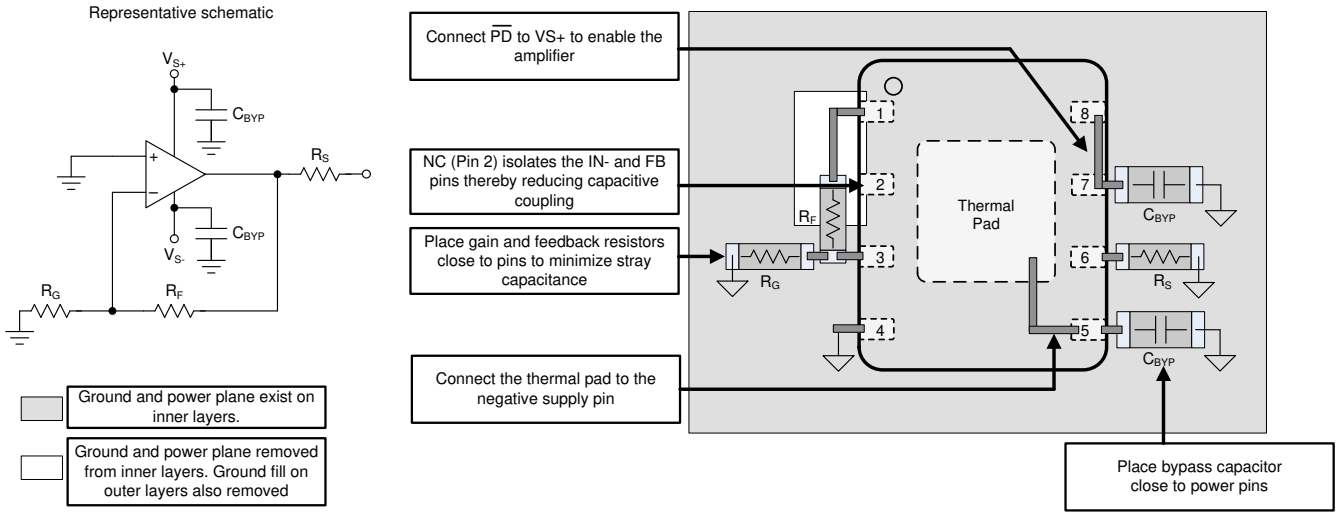

Figure 9-2. Layout Recommendation

When configuring the OPA955 as a transimpedance amplifier, take care to minimize the inductance between the avalanche photodiode (APD) and the amplifier. Always place the photodiode on the same side of the PCB as the amplifier. Placing the amplifier and the APD on opposite sides of the PCB increases the parasitic effects due to via inductance. APD packaging can be quite large, which often requires the APD to be placed further away from the amplifier than ideal. Figure 9-3 shows that the added distance between the two device results in increased inductance between the APD and op amp feedback network. The added inductance is detrimental to a decompensated amplifiers stability because this inductance isolates the APD capacitance from the noise-gain transfer function. The noise gain is given by Equation 1. The added PCB trace inductance between the feedback network increases the denominator in Equation 1 thereby reducing the noise gain and the phase margin. In cases where a leaded APD in a TO-can package is used, further minimize inductance by cutting the leads of the TO-can package as short as possible.

$$\text{Noise Gain} = \left(1 + \frac{Z_F}{Z_{IN}}\right) \quad (1)$$

where

- Z_F is the total impedance of the feedback network.
- Z_{IN} is the total impedance of the input network.

The layout shown in Figure 9-3 is improved by following some of the guidelines in Figure 9-4. The two key rules to follow are:

1. Add an isolation resistor R_{ISO} as close as possible to the inverting input of the amplifier. Select the value of R_{ISO} to be between 10Ω and 20Ω. The resistor dampens the potential resonance caused by the trace inductance and the amplifiers internal capacitance.
2. Close the loop between the feedback elements (R_F and C_F) and R_{ISO} as close to the APD pins as possible. This closure provides a more balanced layout and reduces the inductive isolation between the APD and the feedback network.

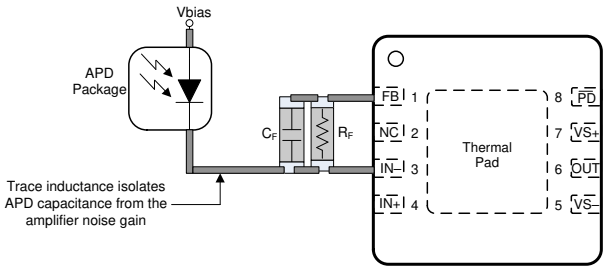

Figure 9-3. Non-Ideal TIA Layout

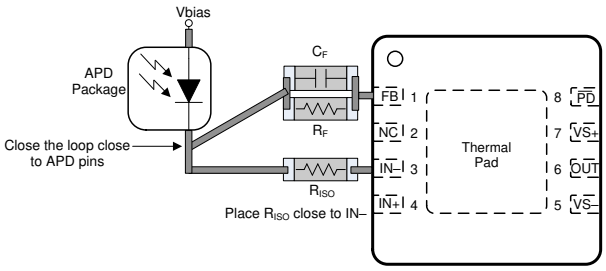

Figure 9-4. Improved TIA Layout

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- *LIDAR Pulsed Time of Flight Reference Design*
- *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters*
- *Wide Bandwidth Optical Front-end Reference Design*

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DEM-OPA-WSON8-EVM*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers application report*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XOPA955DSGR	Active	Preproduction	WSON (DSG) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

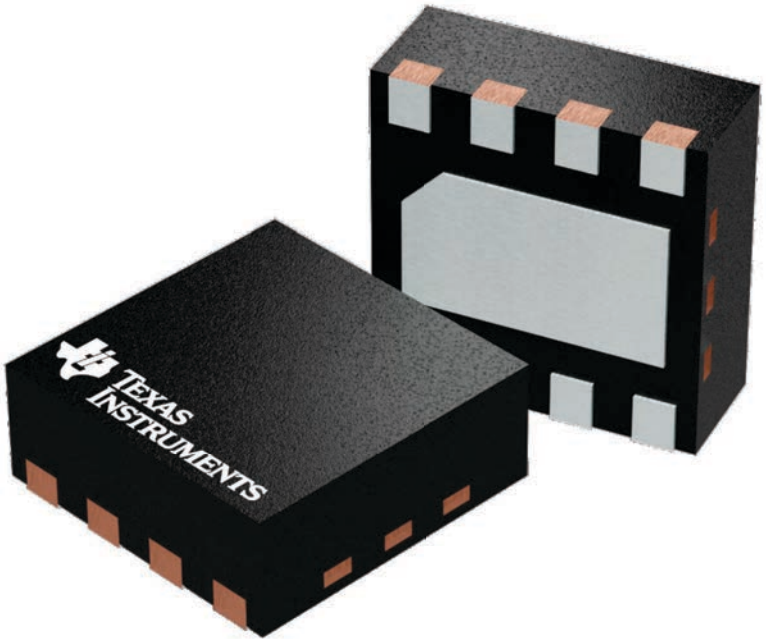
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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