PGA848 Low-Noise, Wide-Bandwidth, Scope Gain, Single-Ended Output, Programmable Gain Instrumentation Amplifier

1 Features

- Differential to single-ended conversion
- Eight pin-programmable decade (scope) gains
  - G (V/V) = ½, 1, 2, 5, 10, 20, 50, and 100
- Low gain error drift: ±2ppm/°C (maximum)
- Faster signal processing:
  - Wide bandwidth: 6.2MHz (G < 10), 2.4MHz (G = 50, 100)
  - High slew rate: 43V/µs at all gains
  - Settling time: 710ns to 0.01% (G < 20)
  - Input stage noise: 8.5nV/√Hz at G > 10V/V
  - Filter option to achieve better SNR
- Input overvoltage protection to ±40V beyond supplies
- Input-stage supply range:
  - Single supply: 9V to 36V
  - Dual supply: ±4.5V to ±18V
- Independent output power-supply pins
- Output-stage supply range:
  - Single supply: 4.5V to 36V
  - Dual supply: ±2.25V to ±18V
- Specified temperature range: –40°C to +125°C
- Small package: 3mm × 3mm VQFN

2 Applications

- Factory automation and controls
- Analog input modules
- Data acquisition (DAQ)
- Test and measurement
- Parametric measurement units (PMU)

3 Description

The PGA848 is a wide-bandwidth, low-noise programmable gain instrumentation amplifier for differential-to-single-ended conversion. The PGA848 is equipped with eight decade (scope) gain settings, from an attenuating gain of 0.5V/V to a maximum of 100V/V. Gain is set using three digital gain selection pins.

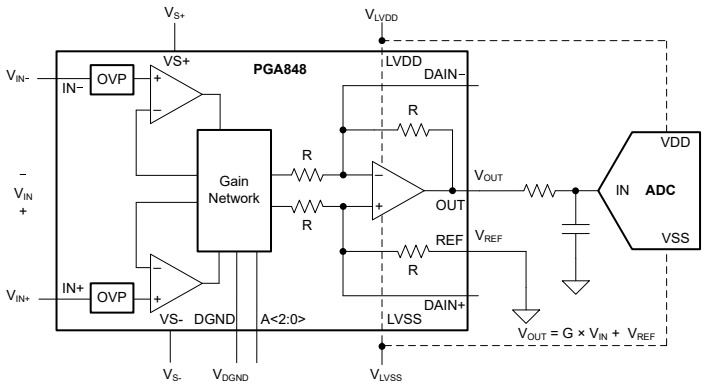
The PGA848 architecture is optimized to drive inputs of high-resolution, precision analog-to-digital converters (ADCs) with sampling rates up to 1MSPS without additional ADC drivers. The output-stage power supplies are decoupled from the input stage to protect the ADC or downstream devices against overdrive damage.

The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of 0.3pA/√Hz. This capability makes the PGA848 a versatile choice for virtually any sensor type. The low-noise current-feedback front-end architecture offers exceptional gain flatness even at high frequencies, making the PGA848 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages of up to ±40V beyond the power-supply voltages.

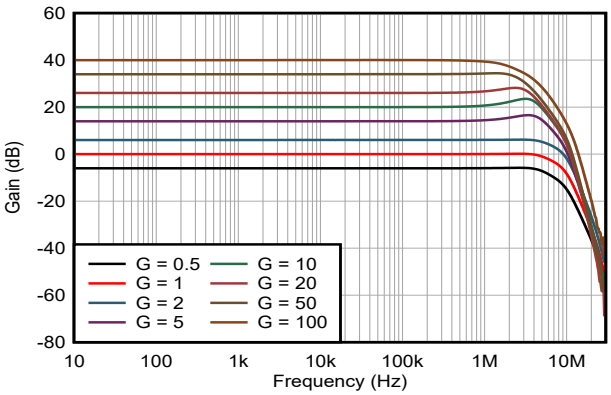
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
PGA848	RGT (VQFN, 16)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



PGA848 Simplified Application



Gain vs Frequency

Table of Contents

4 Device Comparison Table

DEVICE	OUTPUT TYPE	GAIN (V/V)	BANDWIDTH (MHz)	SLEW RATE (V/µs)	NOISE (nV/√Hz)
PGA849	Single-ended	⅛, ¼, ½, 1, 2, 4, 8, 16	10	35	8.6
INA849	Single-ended	G = 1 + 6kΩ / R_G	28	35	1
PGA848	Single-ended	½, 1, 2, 5, 10, 20, 50, 100	6.2	43	8.5
PGA854	Differential	½, 1, 2, 5, 10, 20, 50, 100	6.2	45	8.8
PGA855	Differential	⅛, ¼, ½, 1, 2, 4, 8, 16	10	35	7.8
INA851	Differential	G = 1 + 6kΩ / R_G	22	37	3.2
INA821	Single-ended	G = 1 + 49.4kΩ / R_G	4.7	2	7
INA819	Single-ended	G = 1 + 50kΩ / R_G	2	0.9	8

5 Pin Configuration and Functions

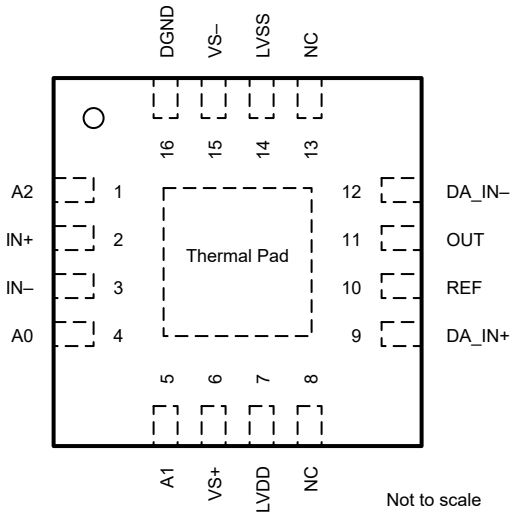


Figure 5-1. RGT Package, 16-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	4	Input	Gain-setting pin 0
A1	5	Input	Gain-setting pin 1
A2	1	Input	Gain-setting pin 2
DA_IN+	9	Input	Connection to output difference amplifier summing node
DA_IN–	12	Input	Connection to output difference amplifier summing node
DGND	16	Power	Ground reference for digital-logic and gain-setting pins
IN–	3	Input	Negative (inverting) input
IN+	2	Input	Positive (noninverting) input
LVDD	7	Power	Output-driver positive supply
LVSS	14	Power	Output-driver negative supply
NC	8, 13	—	Do not connect
OUT	11	Output	Output
REF	10	Input	Reference input. Drive this pin with a low-impedance source
VS–	15	Power	Input-stage negative supply
VS+	6	Power	Input-stage positive supply
Thermal Pad	Thermal pad	—	Solder the thermal pad to the printed-circuit board (PCB). Connect the thermal pad to a plane or large copper pour that is either floating or electrically connected to VS–. Make this connection even for applications that have low power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage on VS+, VS– pins; $V_S = (V_{S+}) – (V_{S–})$	0	40	V
V_{SOUT}	Supply voltage on LVDD, LVSS pins; $V_{SOUT} = V_{LVDD} – V_{LVSS}$	0	40	V
	Voltage on power pins LVDD, LVSS	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Voltage on signal-input pins IN+, IN–	$(V_{S–}) – 40$	$(V_{S+}) + 40$	V
	DGND, DA_IN+, DA_IN– pin voltage	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Voltage on gain-select pins A2, A1, A0	$V_{DGND} – 0.5$	$(V_{S+}) + 0.5$	V
V_{OUT}	Voltage on output pin OUT	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
V_{REF}	Reference input voltage on REF pin	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
I_O	Output pin OUT current	–100	100	mA
I_{SC}	Output short-circuit current(2)	Continuous		
T_A	Operating temperature	–50	150	°C
T_J	Junction temperature		175	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_{SOUT} / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Input stage supply voltage	Single supply	9	36	V
		Dual supply	±4.5	±18	
V_{SOUT}	Output stage supply voltage	Single supply	4.5	36	V
		Dual supply	±2.25	±18	
T_A	Specified temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		PGA848 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

at T_A = 25 °C, V_S = V_{SOUT} = ±15V, V_{ICM} = 0V, V_{REF} = 0V, R_L = 10kΩ connected to ground, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage (RTI)	G = 5 to 100			±50	±300	µV
		G = 0.5, 1, 2			±100 / G	±700 / G	
	Offset voltage drift RTI)	T_A = –40°C to +125°C	G > 1		±0.1	±1.0	µV/°C
			G = 0.5, 1		±0.2	±2.0	
PSRR	Power-supply rejection ratio	±4.5V ≤ V_S ≤ ±18V, RTI	G = 0.5	108	124		dB
			G = 1	114	128		
			G = 2	118	130		
			G ≥ 5	120	134		
z_{id}	Differential input impedance				100 || 1		GΩ || pF
		TA = –40°C to +125°C		10 || 1			
z_{ic}	Common-mode input impedance				100 || 4.4		
V_{ICM}	Common-mode input voltage	V_S = ±4.5V to ±18V, T_A = –40°C to +125°C		($V_{S–}$) + 3		(V_{S+}) – 3	V
V_{IN}	Differential input voltage[1]			–16		+16	V
CMRR	Common-mode rejection ratio	At dc to 60Hz, V_{ICM} = ±10V, T_A = –40°C to +125°C, RTI	G = 0.5	69	82		dB
			G = 1	75	88		
			G = 2	80	94		
			G = 5	88	100		
			G = 10	95	106		
			G = 20	100	112		
			G = 50	108	116		
			G = 100	116	124		
BIAS CURRENT							
I_B	Input bias current				±0.5	±2	nA
		T_A = –40°C to +125°C			±1	±3.6	
	Input bias current drift	T_A = –40°C to +125°C				±5	pA/°C
I_{OS}	Input offset current				±0.5	±1	nA
		T_A = –40°C to +125°C			±1	±2	
	Input offset current drift	T_A = –40°C to +125°C				±5	pA/°C

6.5 Electrical Characteristics (continued)

at T_A = 25 °C, V_S = V_{SOUT} = ±15V, V_{ICM} = 0V, V_{REF} = 0V, R_L = 10kΩ connected to ground, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE VOLTAGE							
e_{NI}	Voltage noise density (RTI)	f = 1kHz	G = 100		8.5		nV/√Hz
			G = 50		8.5		
			G = 20		8.5		
			G = 10		8.5		
			G = 5		10.5		
			G = 2		19.5		
			G = 1		39.5		
			G = 0.5		78.5		
E_{NI}	Voltage noise (RTI)	f_B = 0.1Hz to 10Hz	G = 100		0.29		μV_{PP}
			G = 50		0.29		
			G = 20		0.29		
			G = 10		0.29		
			G = 5		0.29		
			G = 2		0.47		
			G = 1		0.78		
			G = 0.5		1.55		
i_N	Input current noise density	f = 1kHz			0.19		pA/√Hz
I_N	Input current noise	f_B = 0.1Hz to 10Hz			7.5		pA_{PP}
GAIN							
	Gain			0.5		100	V/V
GE	Gain error	G = 0.5, 1, 2			±0.005	±0.035	%
		G = 5, 10, 20, 50			±0.015	±0.045	
		G = 100			±0.025	±0.055	
	Gain drift	T_A = –40°C to +125°C	G = 2		±0.05	±1	ppm/°C
			G ≠ 2		±0.2	±2	
	Gain nonlinearity	G = 0.5, V_{OUT} = 8V G = 1 to 20, V_{OUT} = 10V			±2	±6	ppm
		G = 50, 100, V_{OUT} = 10V			±15	±35	
		T_A = –40°C to +125°C, G = 0.5, V_{OUT} = 8V G = 1 to 100, V_{OUT} = 10V	G ≤ 20		±3	±6	
			G = 50, 100		±15	±35	
OUTPUT							
V_{OUT}	Output voltage[2]	No load, V_{SOUT} = ±2.25V		V_{LVSS} + 0.1		V_{LVDD} – 0.1	V
		R_L = 10kΩ	V_{SOUT} = ±2.25V	V_{LVSS} + 0.2		V_{LVDD} – 0.2	
			V_{SOUT} = ±18V	V_{LVSS} + 0.4		V_{LVDD} – 0.4	
C_L	Load capacitance	Stable operation for capacitive load			100		pF
I_{SC}	Short-circuit current	Continuous to V_{SOUT} / 2			±45		mA
			T_A = –40°C to +125°C	±20		±60	

6.5 Electrical Characteristics (continued)

at T_A = 25 °C, V_S = V_{SOUT} = ±15V, V_{ICM} = 0V, V_{REF} = 0V, R_L = 10kΩ connected to ground, and G = 1V/V (unless otherwise noted)

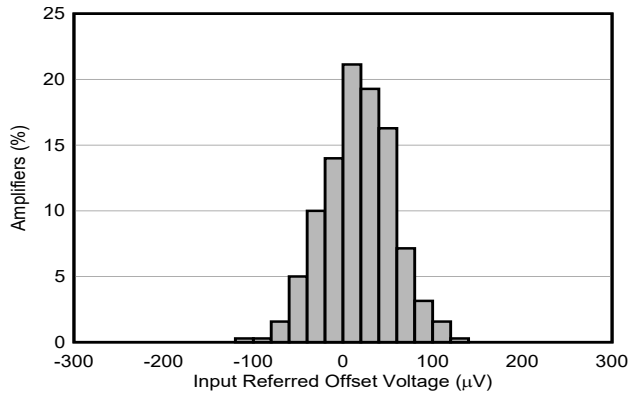
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	G < 10			6.5		MHz
		G = 10, 20			5.0		
		G = 50, 100			2.5		
SR	Slew rate	G = 0.5, V_{OUT} = 8V G = 1 to 20, V_{OUT} = 10V			43		V/µs
t_S	Settling time	G = 0.5, V_{IN} = 10V step or G= 1 to 20, V_{OUT} = 10V step	To 0.01%		0.71		µs
			To 0.0015%		0.88		µs
		G = 50 V_{OUT} = 10V step	To 0.01%		1.21		µs
			To 0.0015%		1.40		µs
		G = 100 V_{OUT} = 10V step	To 0.01%		2.01		µs
			To 0.0015%		2.20		µs
	Gain switching time				1.5		µs
THD+N	Total harmonic distortion and Noise	Differential input, f = 10kHz, V_{OUT} = 10V_{PP}			–97		dB
		Single-ended input, f = 10kHz, V_{OUT} = 10V_{PP}			–99		
HD2	Second-order harmonic distortion	Differential input, f = 10kHz, V_{OUT} = 10V_{PP}			–132		
		Single-ended input, f = 10kHz, V_{OUT} = 10V_{PP}			–112		
HD3	Third-order harmonic distortion	Differential input, f = 10kHz, V_{OUT} = 10V_{PP}			–106		
		Single-ended input, f = 10kHz, V_{OUT} = 10V_{PP}			–106		
REFERENCE INPUT							
	Reference input voltage			V_{LVSS}		V_{LVDD}	V
	Reference input impedance				10		kΩ
	Reference input current	V_{IN} = 0V			140		µA
	Reference gain to output				1		V/V
	Reference gain error	V_{OUT} = ±10V, within the linear operating range			0.01	0.05	%
INPUT STAGE POWER SUPPLY							
I_{Q_input}	Input stage quiescent current VS+, VS–	V_{IN} = 0V, V_{ICM} = 0V			3.2	3.9	mA
			T_A = –40°C to +125°C			4.9	
OUTPUT STAGE POWER SUPPLY							
I_{Q_output}	Output stage quiescent current LVDD, LVSS	V_{IN} = 0V, V_{REF} = 0V			1.3	1.8	mA
			T_A = –40°C to +125°C			2.2	
DIGITAL LOGIC							
V_{IL}	Digital input logic low	A0, A1, A2 pins, referred to DGND		V_{DGND}		V_{DGND} + 0.8	V
V_{IH}	Digital input logic high	A0, A1, A2 pins, referred to DGND		V_{DGND} + 1.8		V_{S+}	V
	Digital input pin current	A0, A1, A2 pins			1.5	3	µA
V_{DGND}	DGND voltage			$V_{S–}$		(V_{S+}) – 4	V
	DGND reference current				4	10	µA

(1) Differential Input voltage of the PGA848 amplifier (V_{IN} = V_{IN+} – V_{IN-}). The valid input range depends on input common-mode voltage V_{ICM}, gain G, and reference voltage V_{REF}. See Section 8.1.1

(2) Output voltage V_{OUT} = G × V_{IN} + V_{REF} if V_{IN}, V_{ICM}, and V_{REF} are in valid linear operating range. See Section 8.1.1

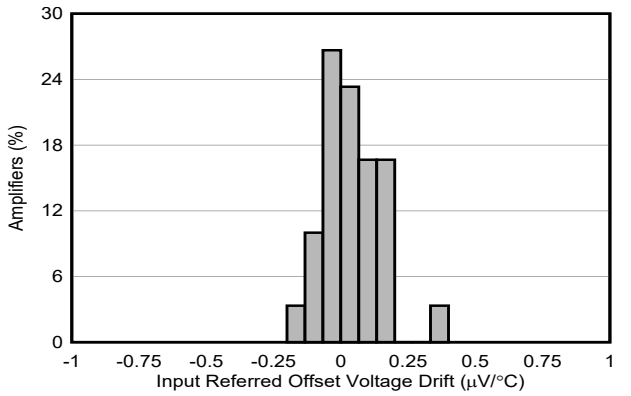
6.6 Typical Characteristics

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



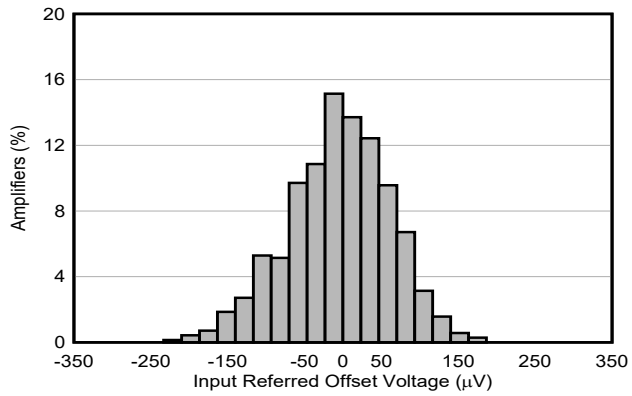
N = 700 Mean = 17.29µV Std. dev. = 38.32µV
G = 100V/V

Figure 6-1. Distribution of Offset Voltage (RTI)



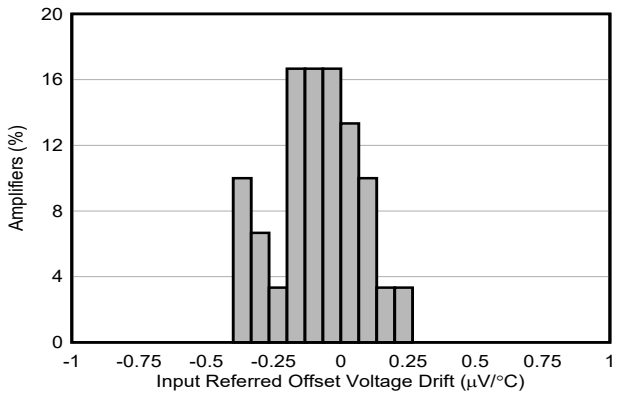
N = 30 Mean = –0.03µV/°C Std. dev. = 0.105µV/°C
G = 100V/V

Figure 6-2. Distribution of Offset Voltage Drift (RTI)



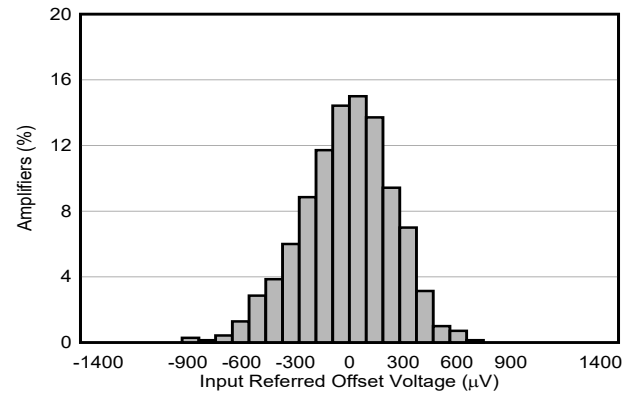
N = 700 Mean = –3.23µV Std. dev. = 67.1µV
G = 2V/V

Figure 6-3. Distribution of Offset Voltage (RTI)



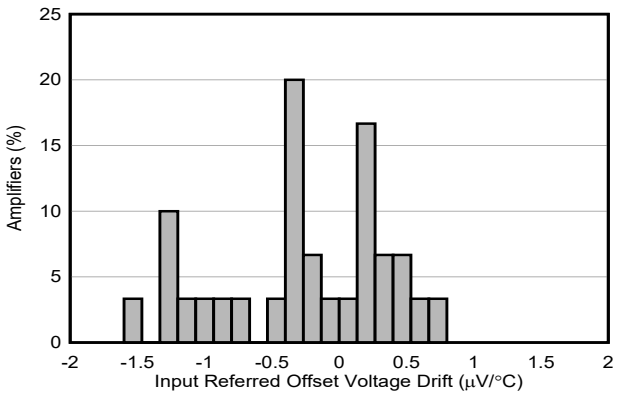
N = 30 Mean = –0.091µV/°C Std. dev. = 0.030µV/°C
G = 2V/V

Figure 6-4. Distribution of Offset Voltage Drift (RTI)



N = 700 Mean = 1.45µV Std. dev. = 253.2µV
G = 0.5V/V

Figure 6-5. Distribution of Offset Voltage (RTI)

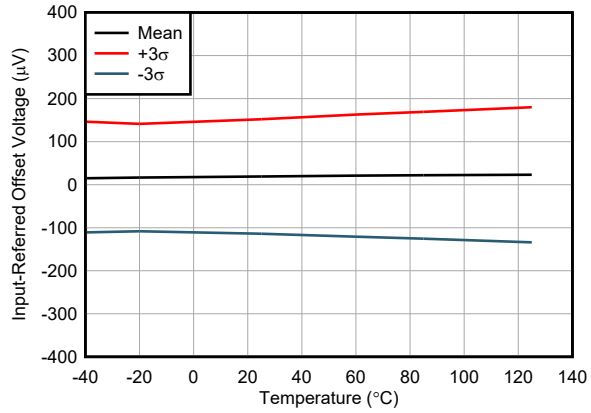


N = 30 Mean = –0.253µV/°C Std. dev. = 0.606µV/°C
G = 0.5V/V

Figure 6-6. Distribution of Offset Voltage Drift (RTI)

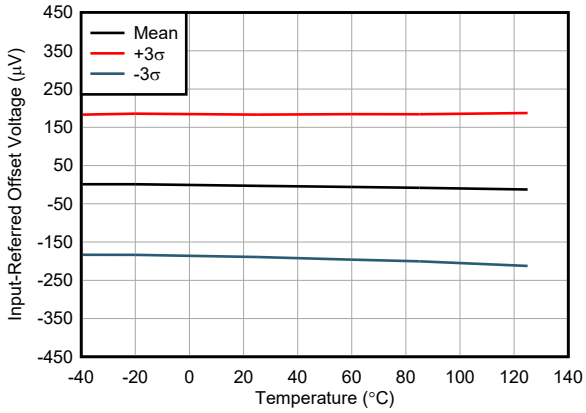
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



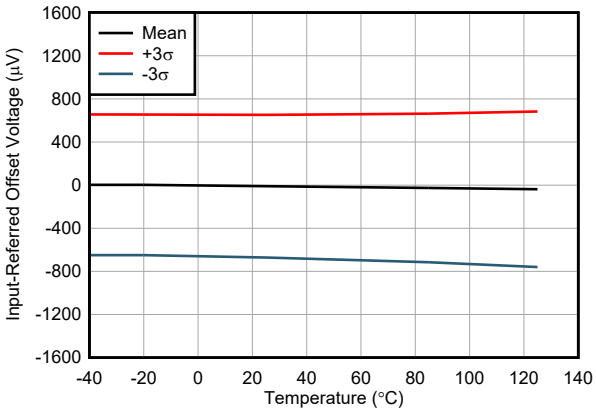
N = 36 1 wafer lot
G = 100V/V

Figure 6-7. Offset Voltage (RTI) vs Temperature



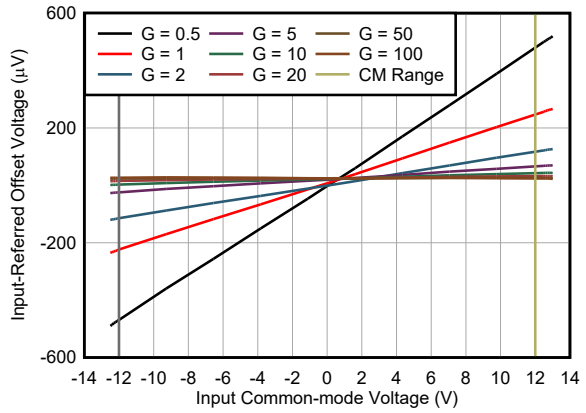
N = 36 1 wafer lot
G = 2V/V

Figure 6-8. Offset Voltage (RTI) vs Temperature



N = 36 1 wafer lot
G = 0.5V/V

Figure 6-9. Offset Voltage (RTI) vs Temperature



Typical unit shown
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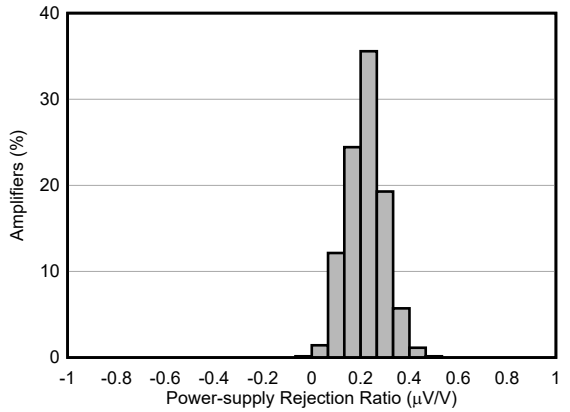
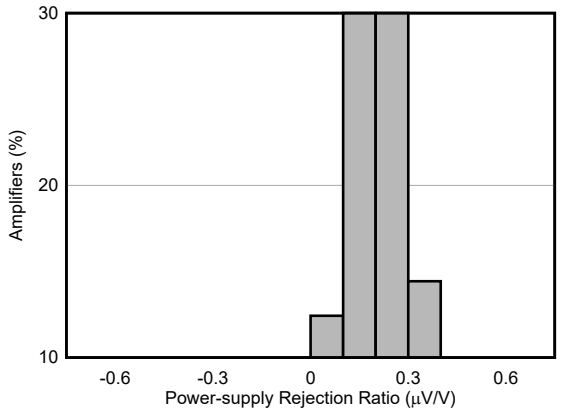
Figure 6-10. Offset Voltage (RTI) vs V_{ICM}



N = 700 Mean = 0.219µV/V Std. dev. = 0.0765µV/V
G = 100V/V

Figure 6-11. PSRR Distribution

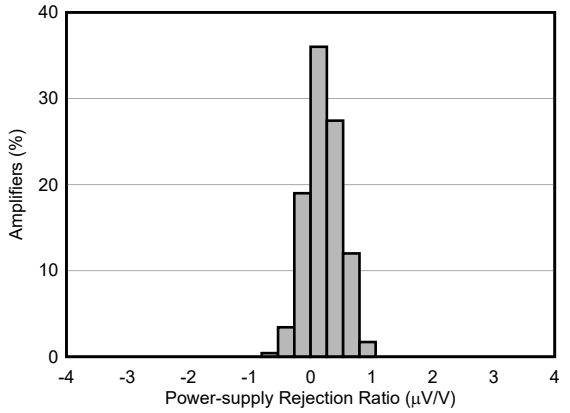


N = 700 Mean = 0.203µV/V Std. dev. = 0.101µV/V
G = 2V/V

Figure 6-12. PSRR Distribution

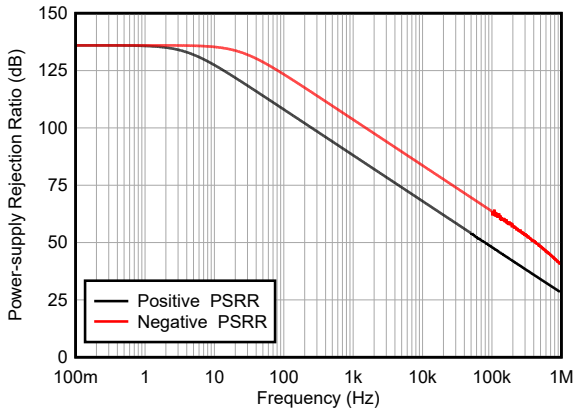
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



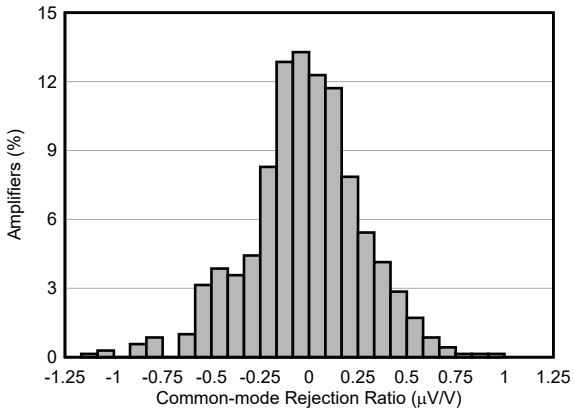
N = 700 Mean = 0.204µV/V Std. dev. = 0.0278µV/V
G = 0.5V/V

Figure 6-13. PSRR Distribution



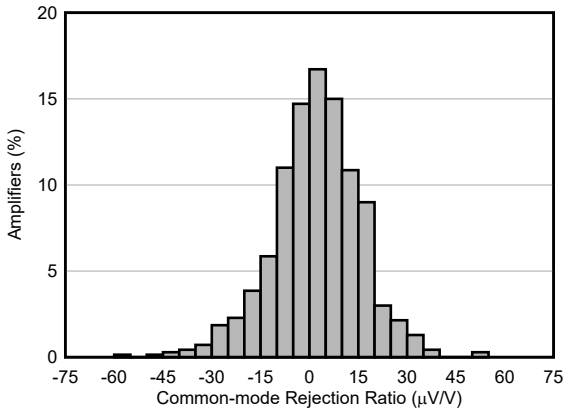
Typical unit shown
G = 1V/V

Figure 6-14. Positive and Negative PSRR vs Frequency



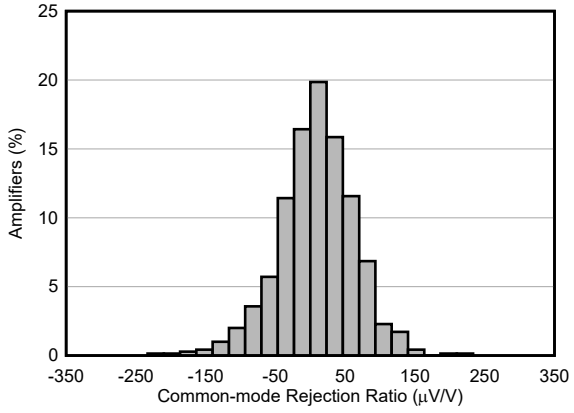
N = 700 Mean = –0.0075µV/V Std. dev. = 0.294µV/V
G = 100V/V

Figure 6-15. CMRR Distribution



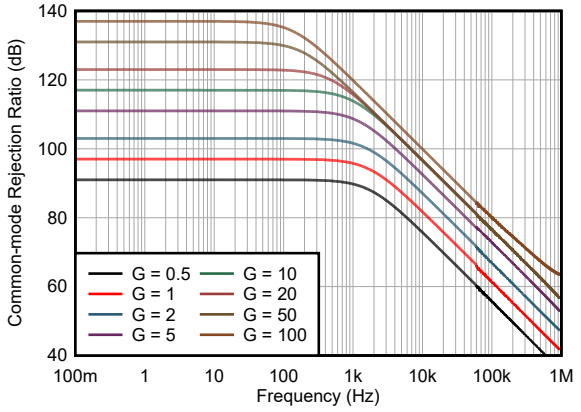
N = 700 Mean = 2.619µV/V Std. dev = 13.71µV/V
G = 2V/V

Figure 6-16. CMRR Distribution



N = 700 Mean = 10.377µV/V Std. dev = 54.846µV/V
G = 0.5V/V

Figure 6-17. CMRR Distribution

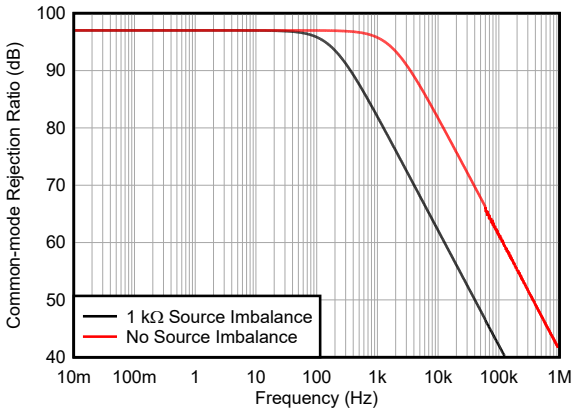


Typical unit shown
.

Figure 6-18. CMRR vs Frequency (RTI)

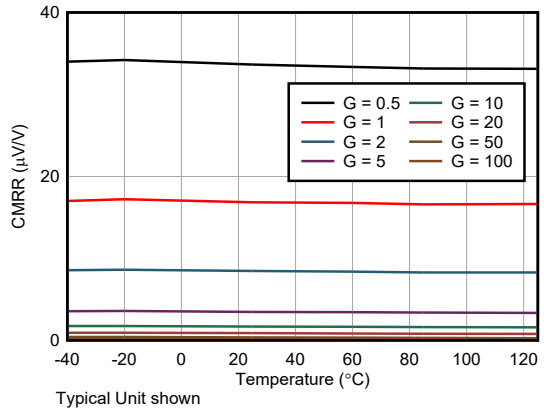
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



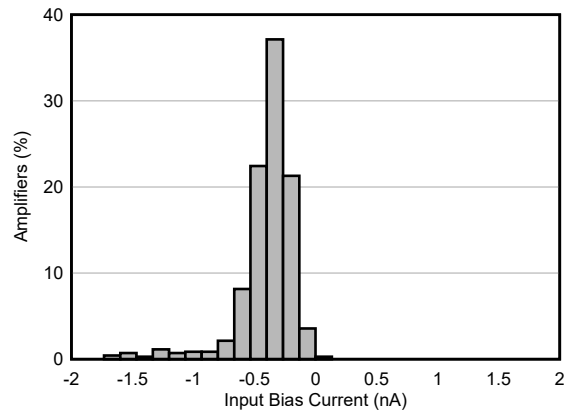
Typical unit shown
G = 1V/V

Figure 6-19. CMRR vs Frequency (Unbalanced)



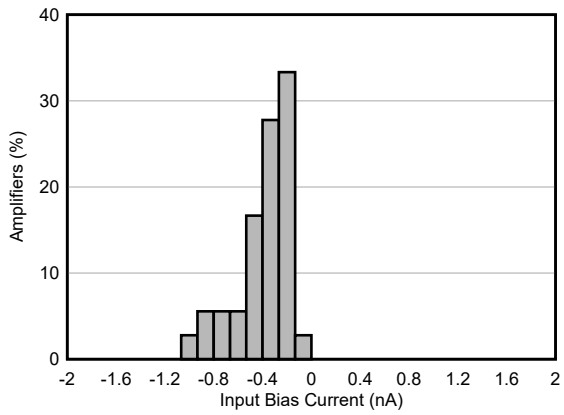
Typical unit shown
.

Figure 6-20. CMRR vs Temperature



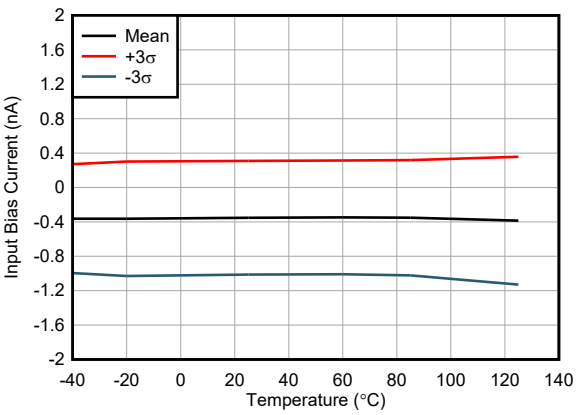
N = 700 Mean = –0.353nA Std. dev. = 0.238nA
G = 1V/V

Figure 6-21. Distribution of Input Bias Current



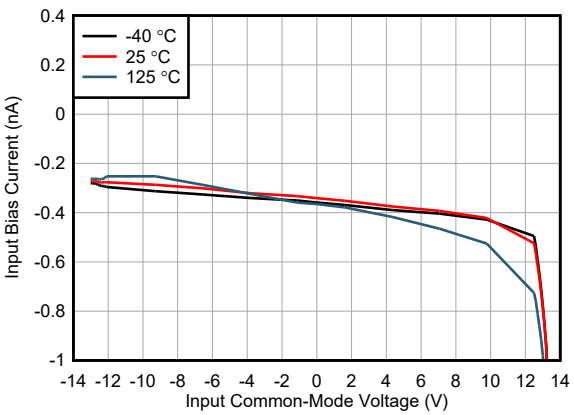
N = 36 Mean = –0.325nA Std. dev. = 0.225nA
G = 1V/V T_A = 85°C

Figure 6-22. Distribution of Input Bias Current



N = 58 1 wafer lot
G = 1V/V

Figure 6-23. Input Bias Current vs Temperature

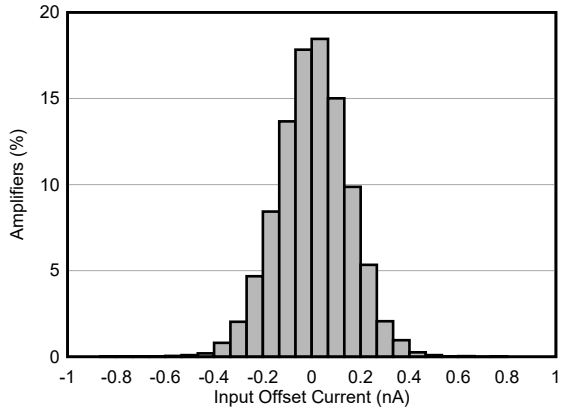


Typical unit shown
G = 1V/V

Figure 6-24. Input Bias Current vs V_{ICM}

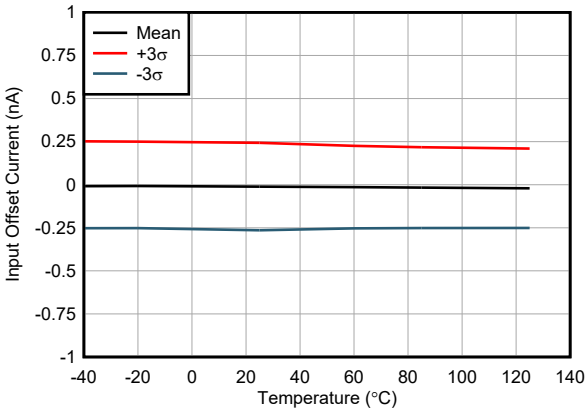
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



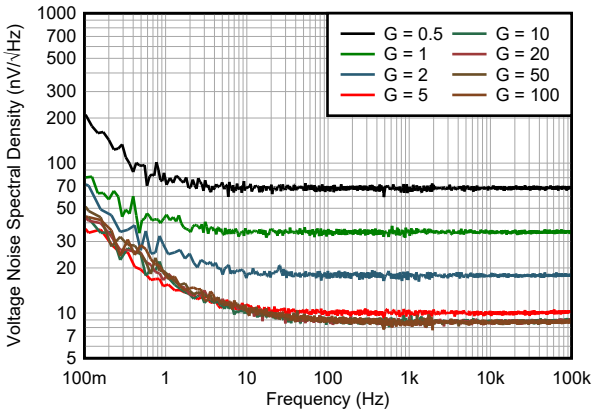
N = 8126 Mean = 0.0067nA Std. dev = 0.1473nA
G = 1V/V

Figure 6-25. Distribution of Input Offset Current



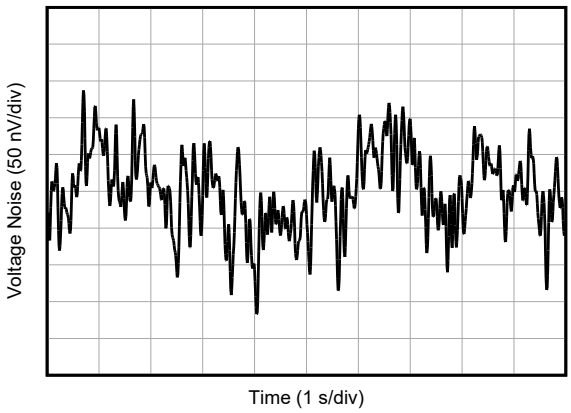
N = 36 1 wafer lot
G = 1V/V

Figure 6-26. Input Offset Current vs Temperature



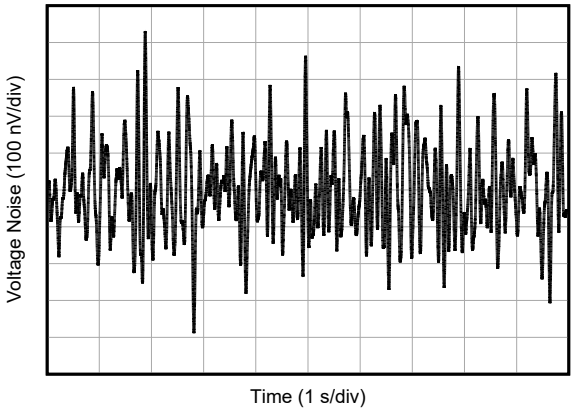
Typical unit shown
.

Figure 6-27. Voltage Noise Spectral Density (RTI) vs Frequency



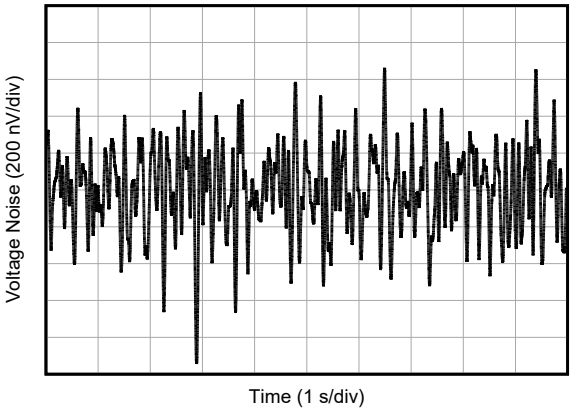
Typical unit shown
G = 100V/V

Figure 6-28. 0.1Hz to 10Hz Voltage Noise (RTI)



Typical unit shown
G = 1V/V

Figure 6-29. 0.1Hz to 10Hz Voltage Noise (RTI)

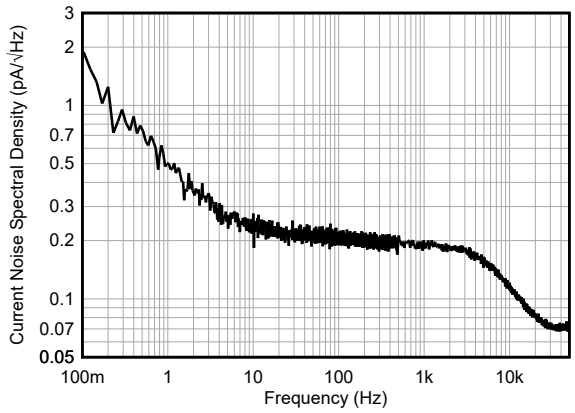


Typical unit shown
G = 0.5V/V

Figure 6-30. 0.1Hz to 10Hz Voltage Noise (RTI)

6.6 Typical Characteristics (continued)

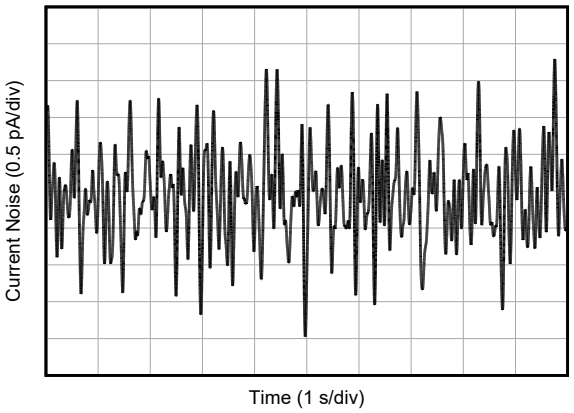
at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



G = 1V/V

.

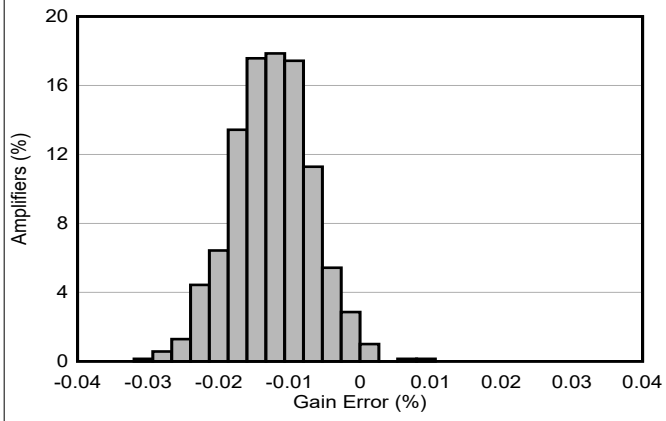
Figure 6-31. Current Noise Spectral Density vs Frequency



Typical unit shown

G = 1V/V

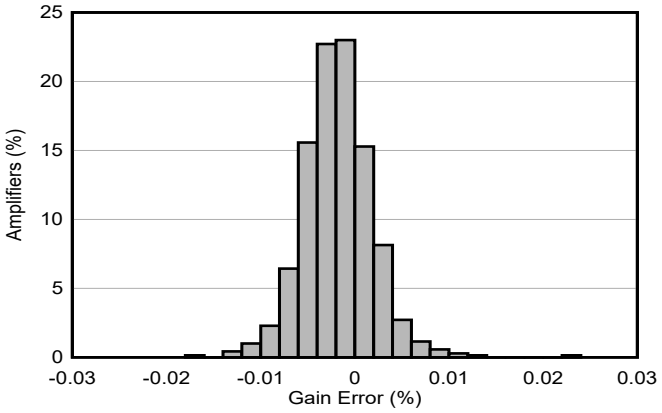
Figure 6-32. 0.1Hz to 10Hz Current Noise



N = 700 Mean = –0.0125% Std. dev. = 0.0056%

G = 100V/V

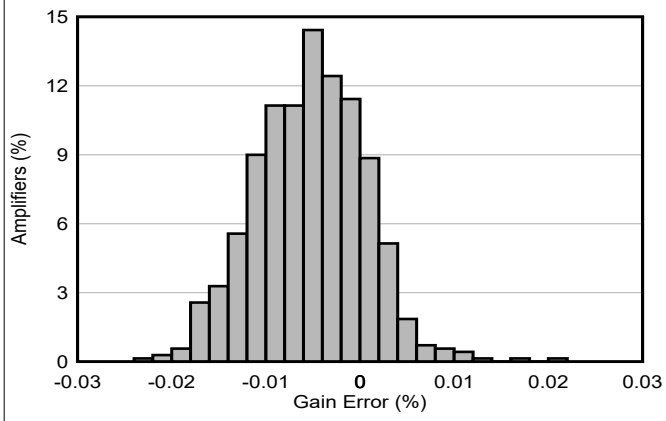
Figure 6-33. Distribution of Gain Error



N = 700 Mean = –0.0019% Std. dev. = 0.0037%

G = 2V/V

Figure 6-34. Distribution of Gain Error



N = 700 Mean = –0.005% Std. dev. = 0.0058%

G = 0.5V/V

Figure 6-35. Distribution of Gain Error

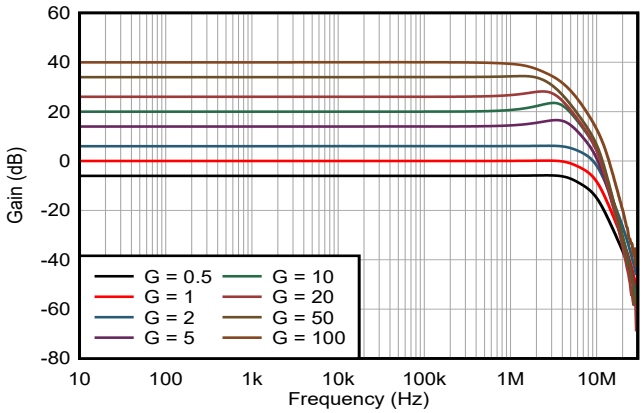
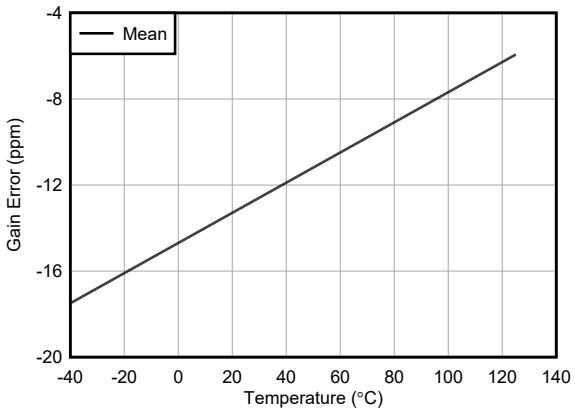


Figure 6-36. Gain vs Frequency

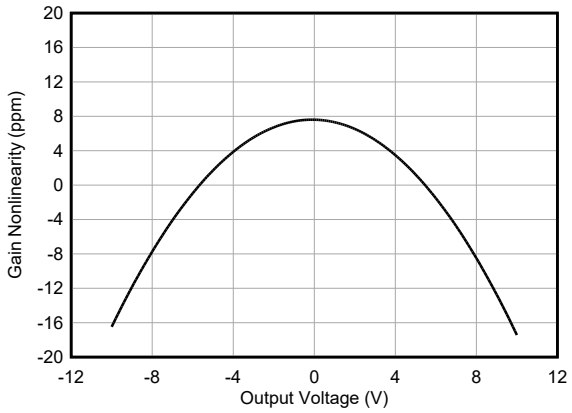
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



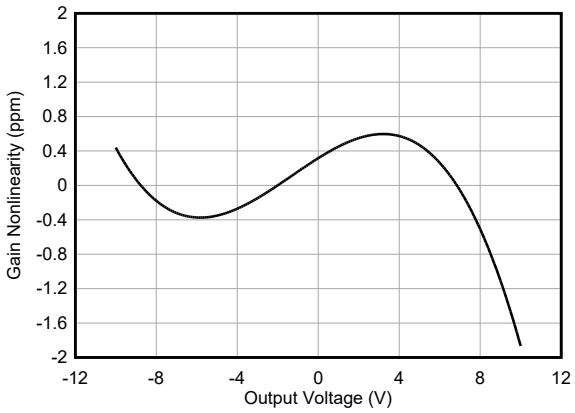
Typical unit shown
G = 2V/V

Figure 6-37. Gain Error vs Temperature



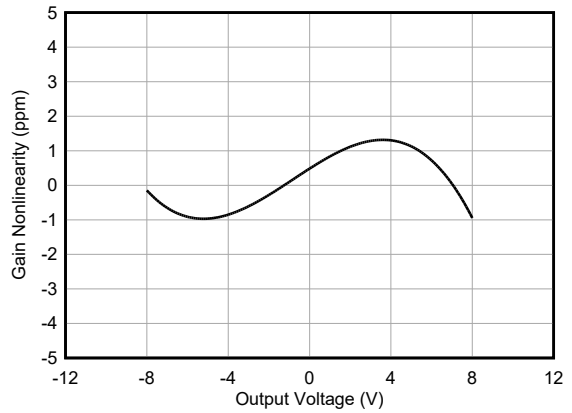
V_{OUT} = ±10V G = 100V/V
Typical unit shown

Figure 6-38. Gain Nonlinearity



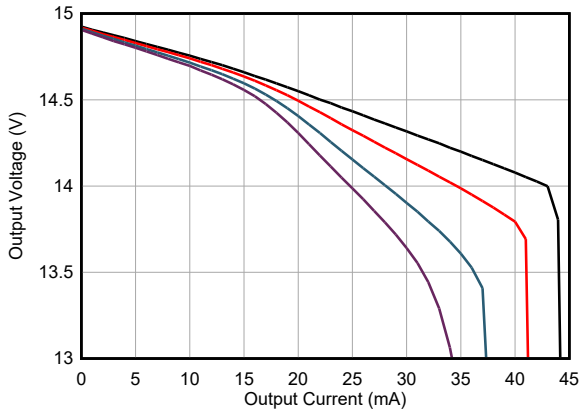
V_{OUT} = ±10V G = 1V/V
Typical unit shown

Figure 6-39. Gain Nonlinearity



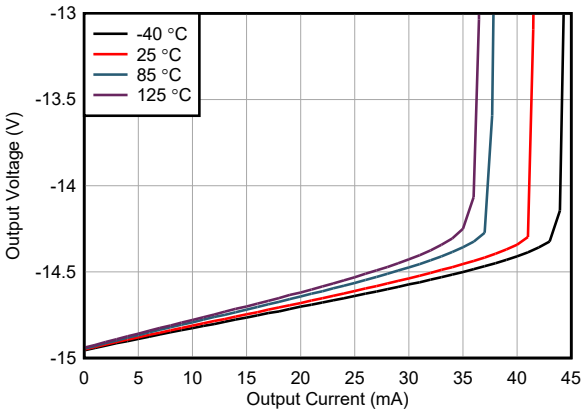
V_{OUT} = ±8V G = 0.5V/V
Typical unit shown

Figure 6-40. Gain Nonlinearity



V_S = ±18V V_{OUT} = ±15V G = 100V/V
.

Figure 6-41. Positive Output Voltage vs Output Current

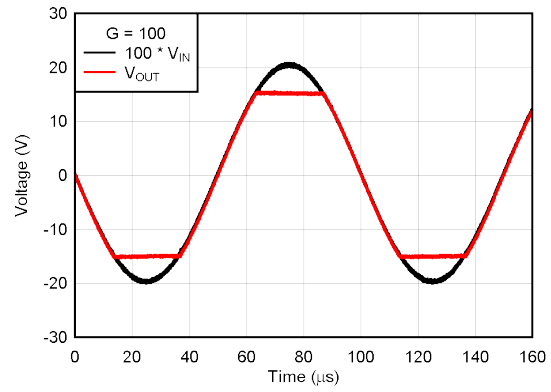


V_S = ±18V V_{OUT} = ±15V G = 100V/V

Figure 6-42. Negative Output Voltage vs Output Current

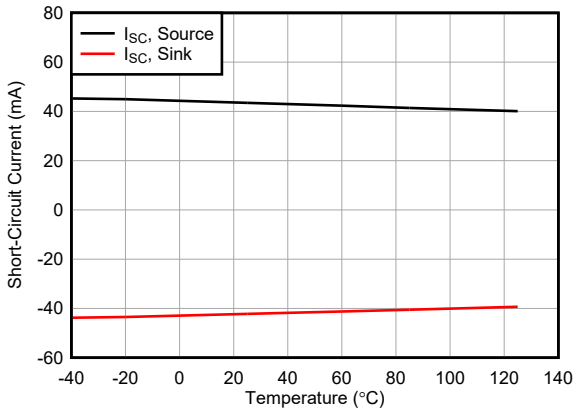
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



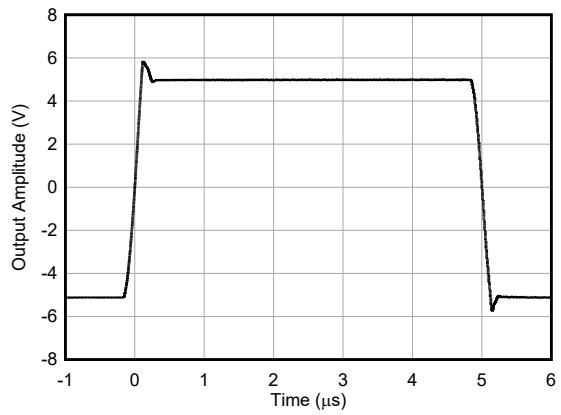
G =
100V/V

Figure 6-43. Overload Recovery



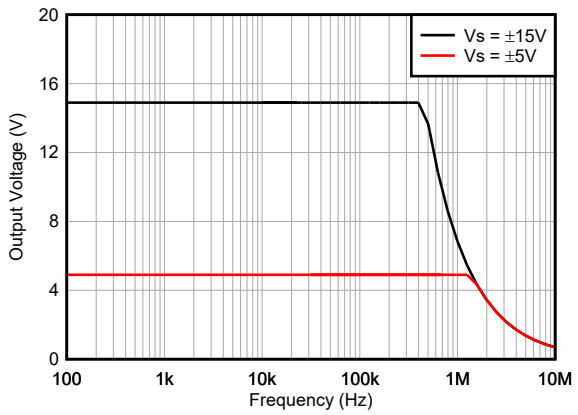
Short to V_{SOUT}/ 2
G = 1V/V

Figure 6-44. Output Short-Circuit Current vs Temperature



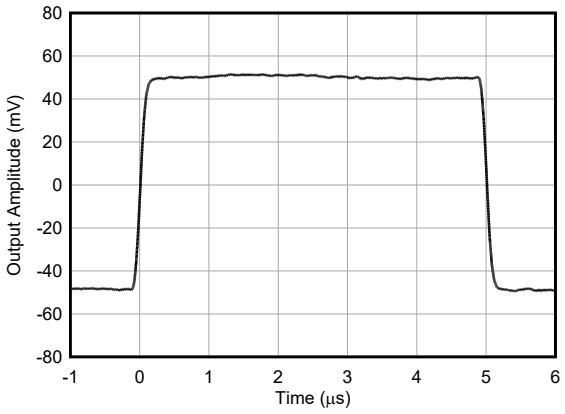
G = 1V/V

Figure 6-45. Large-Signal Step Response



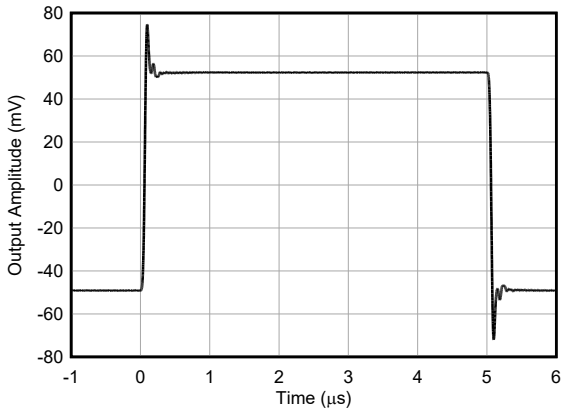
G = 1V/V

Figure 6-46. Large-Signal Step Response vs Frequency



G = 100V/V C_L = 100pF

Figure 6-47. Small-Signal Step Response

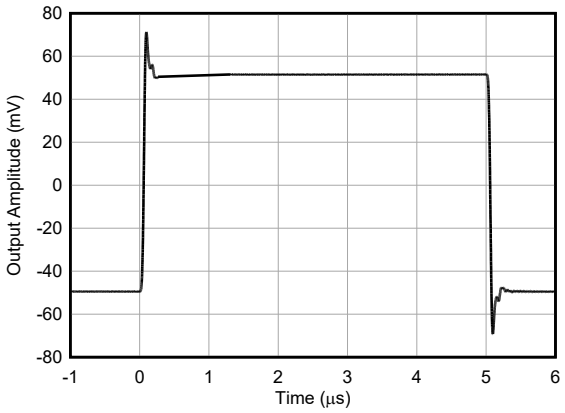


G = 1V/V C_L = 100pF

Figure 6-48. Small-Signal Step Response

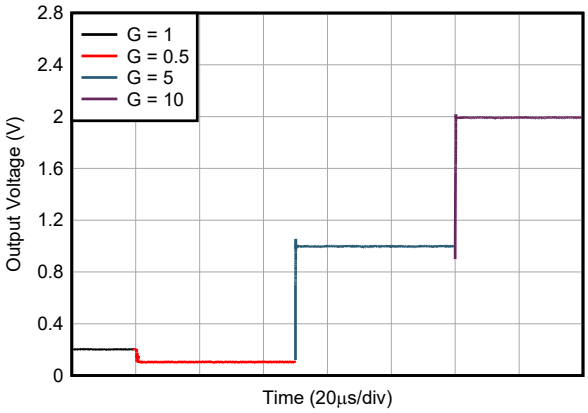
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



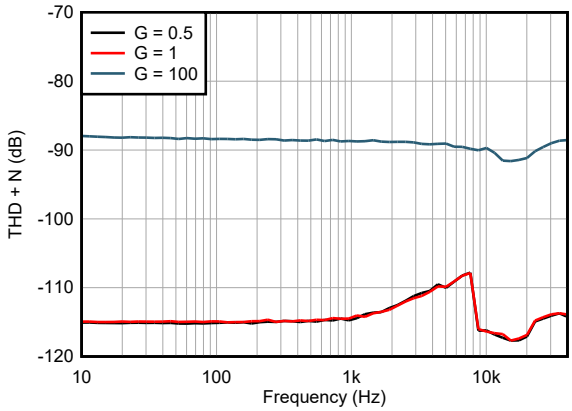
G = 0.5V/V C_L = 100pF

Figure 6-49. Small-Signal Step Response



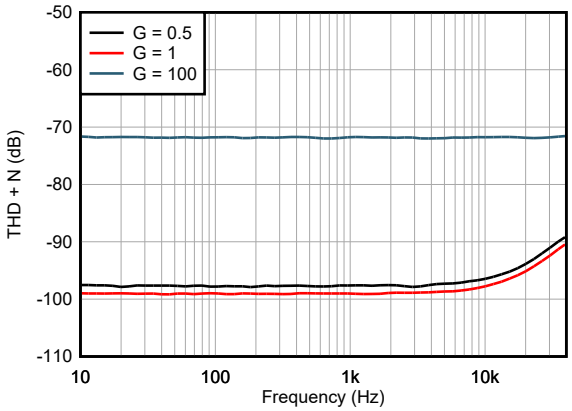
V_{IN} = 200mV_{PP}

Figure 6-50. Gain Switching Transient Response



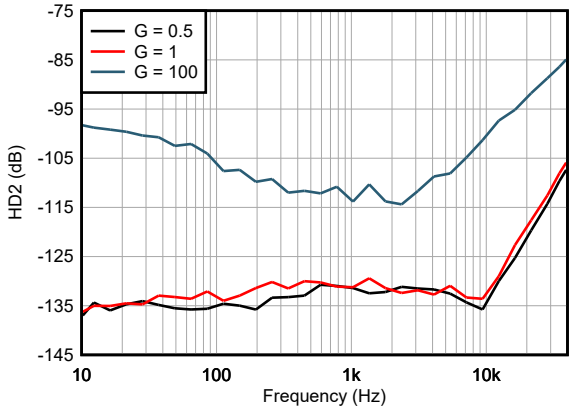
10Hz to 22kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-51. Total Harmonic Distortion + Noise vs Frequency



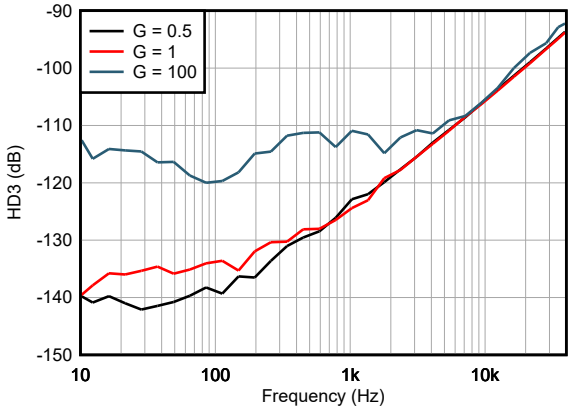
10Hz to 500kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-52. Total Harmonic Distortion + Noise vs Frequency



10Hz to 500kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-53. 2nd Harmonic Distortion vs Frequency

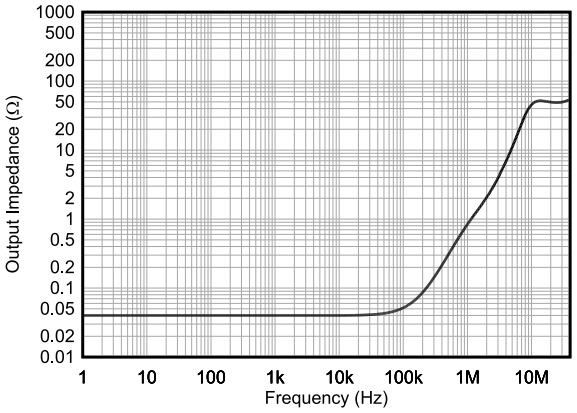


10Hz to 500kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-54. 3rd Harmonic Distortion vs Frequency

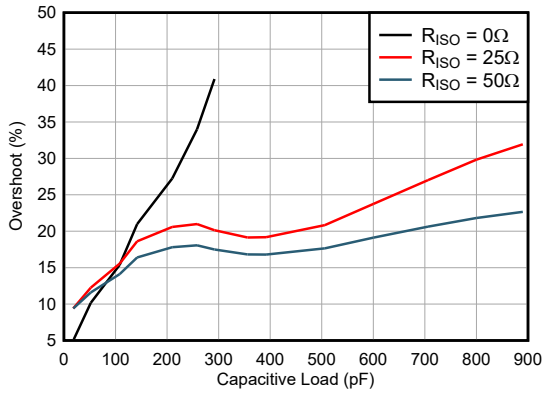
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



G = 1V/V

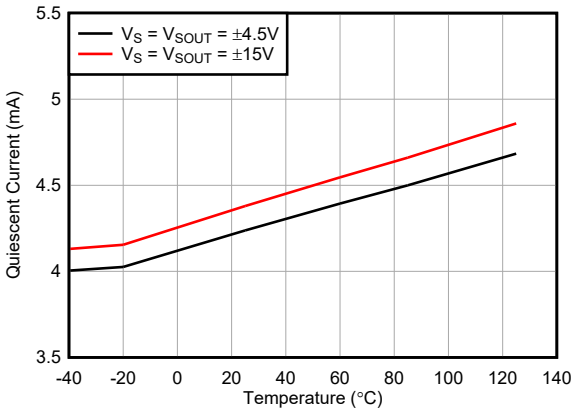
Figure 6-55. Closed-Loop Output Impedance vs Frequency



G = 1V/V

$V_{OUTDIFF}$ = 100mV_{PP}

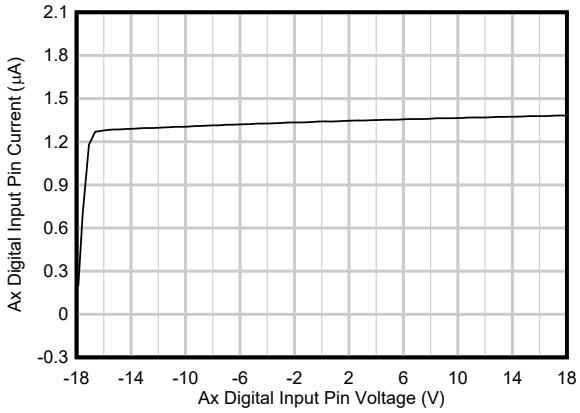
Figure 6-56. Overshoot vs Capacitive Load



Input stage

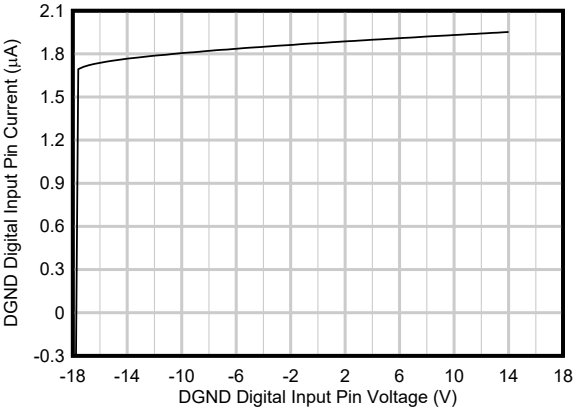
G = 0.5V/V

Figure 6-57. Quiescent Current vs Temperature



DGND = –18V

Figure 6-58. Ax Digital Input Pin Current vs Ax Digital Input Pin Voltage



Ax = DGND

Figure 6-59. DGND Digital Input Pin Current vs DGND Digital Input Pin Voltage

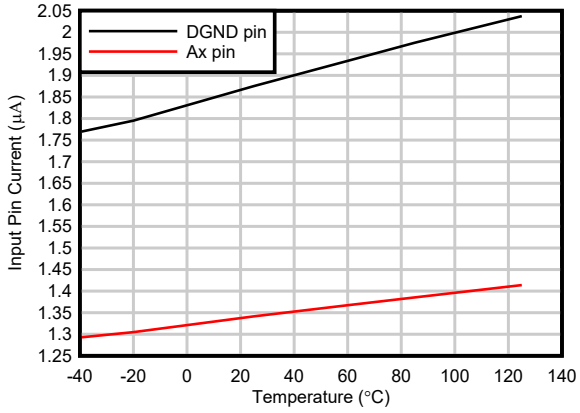


Figure 6-60. Digital Input Pin Current vs Temperature

7 Detailed Description

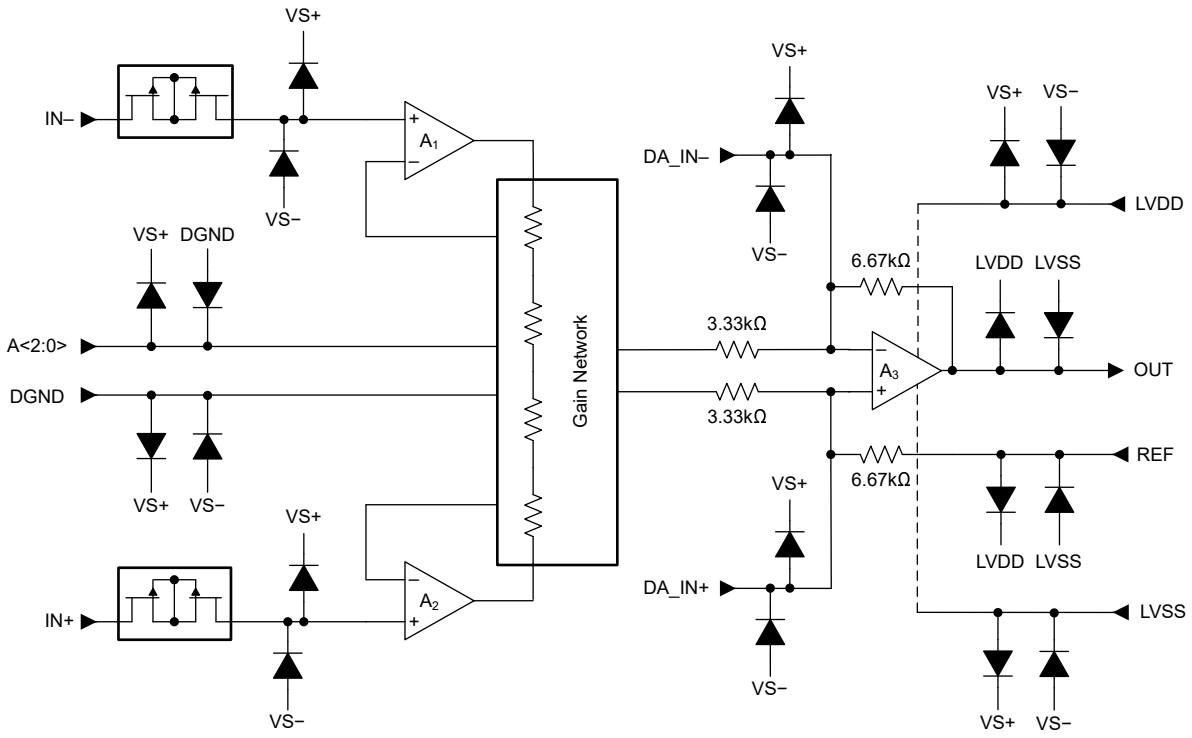
7.1 Overview

The PGA848 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA848 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, difference amplifier output stage. Eight preprogrammed decade gains are selectable using gain-select pins A0, A1, and A2. Gains range from 0.5V/V to 100V/V, discussed in greater detail in Section 7.3.1.

A functional block diagram for the PGA848 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input, current-feedback amplifiers. An integrated precision-matched gain resistor network amplifies the differential input voltage. An output difference amplifier, A_3, rejects the input common-mode component and refers the output signal to the voltage level set by the REF pin.

The PGA848 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1MSPS, without additional ADC drivers. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage resulting from inadvertent overvoltage conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Gain Control

The PGA848 uses three pins to set the amplifier gain. These gain-select pins are set with respect to DGND. This configuration simplifies the design when compared to programmable-gain amplifiers requiring a SPI or other digital interface options for gain changes. Figure 7-1 shows the gain-setting block diagram. Table 7-1 lists the gain options. Any gain-select pin not driven by an external source is automatically biased at DGND using internal pulldown options.

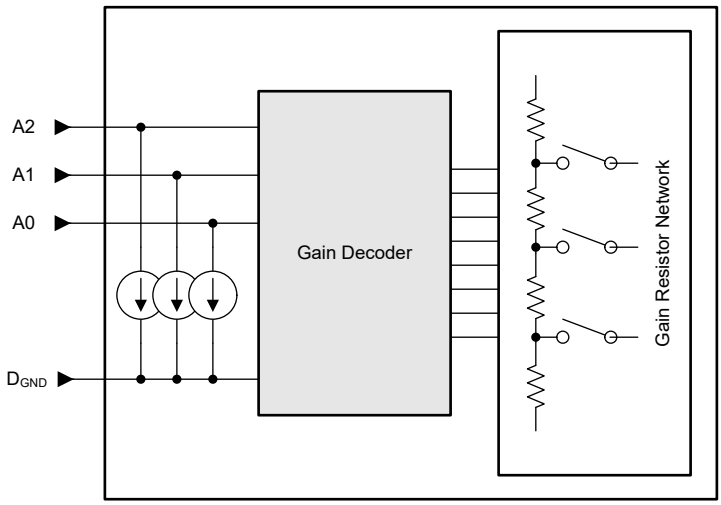


Figure 7-1. PGA848 Gain Setting Block Diagram

Table 7-1. Gain Options

A2:A0	GAIN
000	0.5
001	1
010	2
011	5
100	10
101	20
110	50
111	100

7.3.2 Input Protection

The inputs of the PGA848 are individually protected for voltages up to ±40V beyond either supply. For example, an input common-mode voltage anywhere between –55V and +55V does not cause damage when powered from ±15V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8mA. Figure 7-2 shows the input protection functionality during an overvoltage condition on IN+ or IN- inputs.

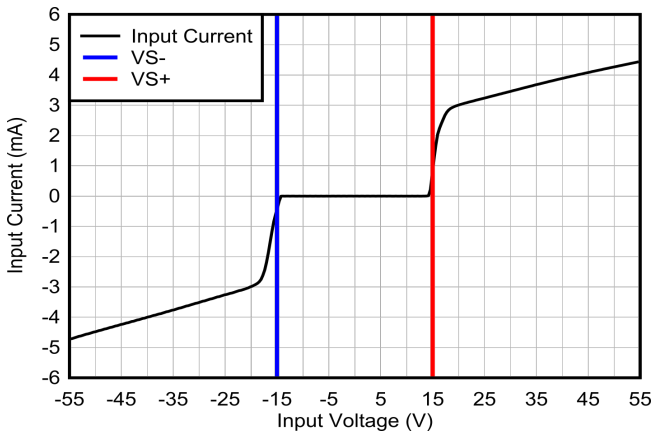


Figure 7-2. Input Current vs Input Overvoltage

Figure 7-3 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies. These Zener diodes provide a current pathway to ground.

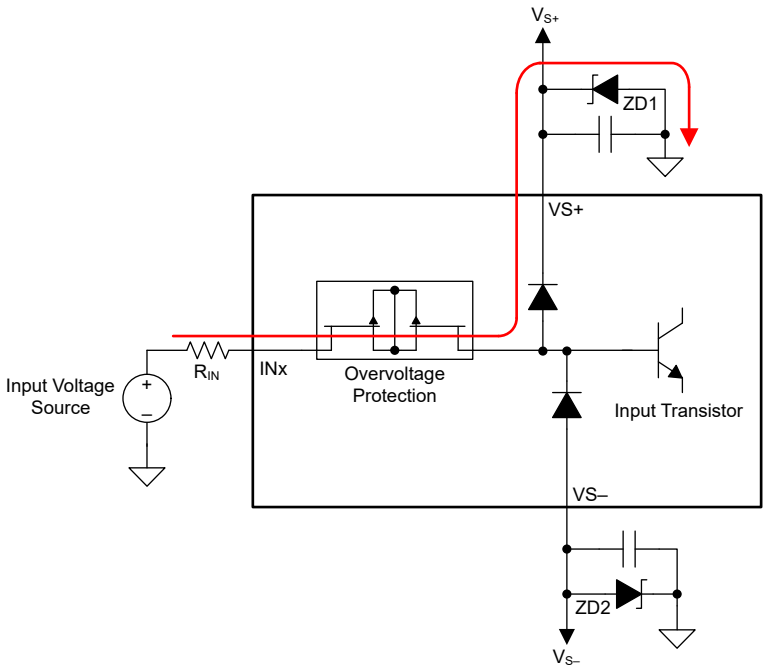


Figure 7-3. Input Current Path During an Overvoltage Condition

7.3.3 Using the Output Difference Amplifier to Shape Noise

The functional block diagram in Section 7.2 shows that the PGA848 output-stage difference amplifier uses a 6.67kΩ feedback resistor between the output and the inverting input. External direct access to the inverting and noninverting inputs of the difference amplifier is provided through the DA_IN– and DA_IN+ pins, respectively. This option allows circuit designers to add external capacitors in parallel with the internal resistors to implement noise-filtering or noise-shaping techniques. These pins are also used to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal resistors:

- The accuracy of the internal resistor network is 0.01% or better. This accuracy results in a common-mode rejection (CMRR) of 80dB or better. Mismatched leakage currents on these pins potentially cause CMRR degradation.
- The internal resistors have ±15% absolute resistance variation. Consider this variation when implementing custom attenuating gains or noise filters.

CAUTION

Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors potentially cause permanent damage to internal circuitry.

7.4 Device Functional Modes

The PGA848 has a single functional mode. The device operates when the input-stage power supply is greater than ±4.5V (9V) and the output stage power supply is greater than ±2.25V (4.5V). Additionally, see Section 6.3.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

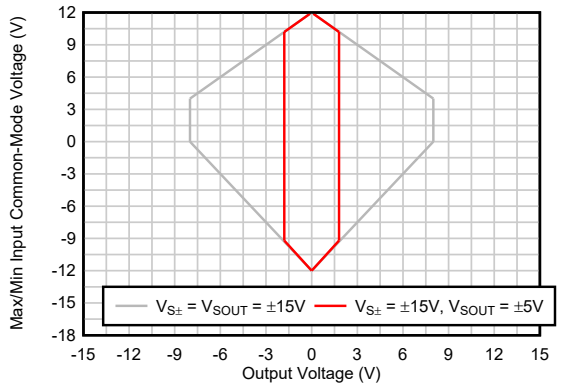
The PGA848 is a monolithic, high-voltage, high-bandwidth, precision programmable gain instrumentation amplifier with a single-ended output. The PGA848 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, differential amplifier output stage. The PGA848 is equipped with eight binary-gain settings, from 0.5V/V to 100V/V, using three digital gain-selection pins: A0, A1, and A2.

The PGA848 is designed for applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

8.1.1 Linear Operating Input Range

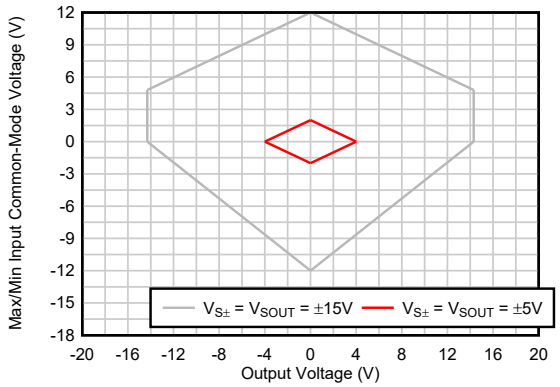
The linear operating input voltage range of the PGA848 input circuitry extends within 3V (maximum) of either power supply. The device maintains excellent common-mode rejection throughout this range at all temperatures. The linear operating input common-mode range is a function of the input common-mode voltage, input differential voltage, gain, and reference input voltage.

The valid common-mode range to enable valid output voltage at no load condition are shown in Figure 8-4 to Figure 8-3.



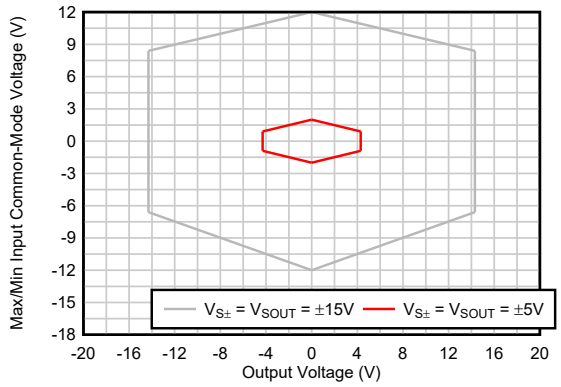
$V_S = V_{SOUT} = \pm 15V$ $V_S = \pm 15V, V_{SOUT} = \pm 5V$
$V_{REF} = 0V$ $G = 0.5V/V$

Figure 8-1. Input Common-Mode Voltage vs Output Voltage



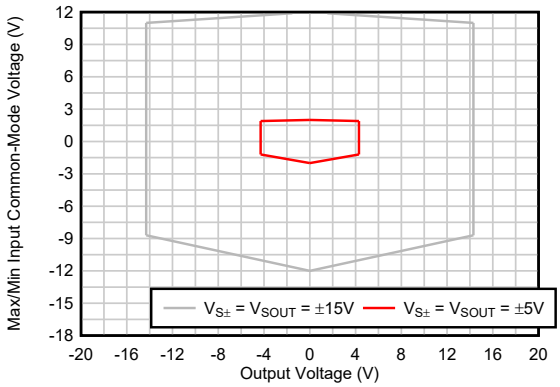
$V_S = V_{SOUT} = \pm 15V$ $V_S = V_{SOUT} = \pm 5V$
$V_{REF} = 0V$ $G = 1V/V$

Figure 8-2. Input Common-Mode Voltage vs Output Voltage



$V_S = V_{SOUT} = \pm 15V$ $V_S = V_{SOUT} = \pm 5V$
$V_{REF} = 0V$ $G = 2V/V$

Figure 8-3. Input Common-Mode Voltage vs Output Voltage



$V_S = V_{SOUT} = \pm 15V$ $V_S = V_{SOUT} = \pm 5V$
$V_{REF} = 0V$ $G = 100V/V$

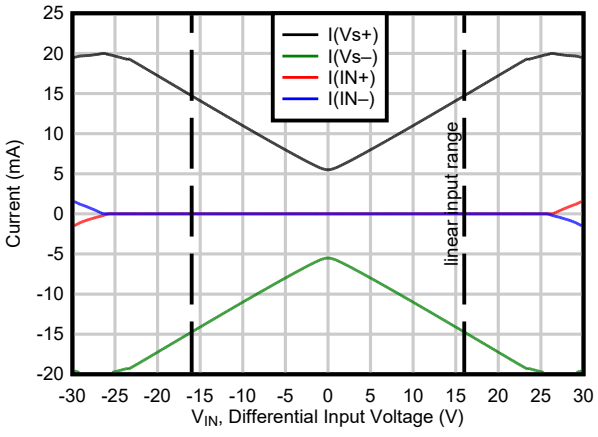
Figure 8-4. Input Common-Mode Voltage vs Output Voltage

8.1.2 Current Consumption with Differential Inputs

Programmable gain amplifiers such as the PGA848 use internal resistors to set the gain. Consequently, the current consumption is increased by the current that passes through these resistors. The largest supply current consumption occurs at G = 2V/V when applying large amplitude differential signals.

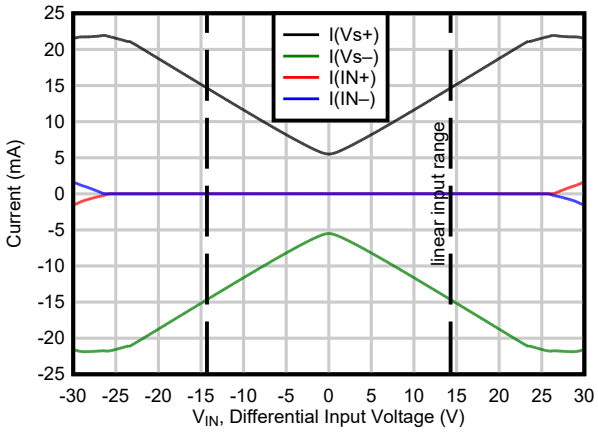
Note that $I_Q$values in the specifications section are under the condition V_{IN} = 0V. Higher supply current is to be expected for higher differential input levels. Same goes to bias current I_B, which is specified with zero differential input. Input bias current increases slightly with increased differential inputs up to the linear input range limit (see Section 8.1.1 for details), If the input exceeds the linear input range limit (inputs are overdriven), the input bias current significantly increases

Figure 8-5 to Figure 8-8 show typical current consumption versus input differential voltage for the input stage supply, and the current drawn by the PGA848 inputs when the device is overdriven. The dashed vertical reference lines outline the linear operating region of the device at that given gain (V_{IN}), outside of this region is when the inputs of the device are overdriven.



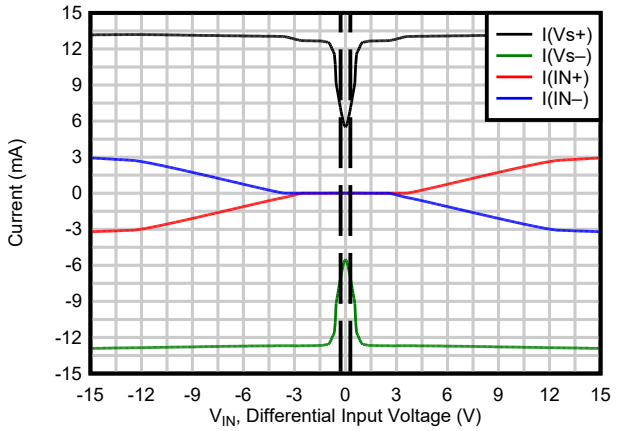
$V_S = V_{SOUT} = \pm 15V$ $V_{ICM} = V_{REF} = 0V$
$G = 0.5V/V$ V_{IN} linear limits = ±16V

Figure 8-5. Current Consumption versus Differential Input Voltage



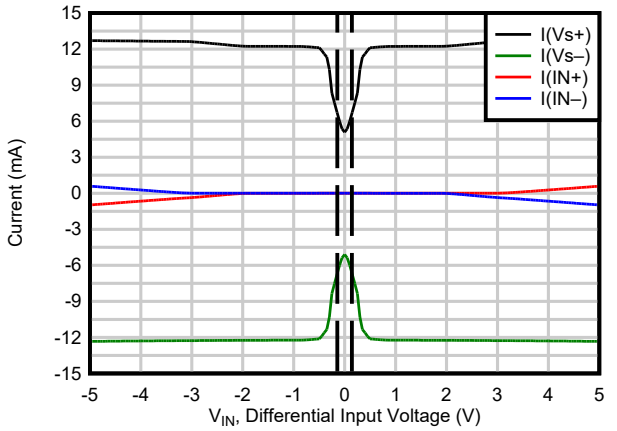
$V_S = V_{SOUT} = \pm 15V$ $V_{ICM} = V_{REF} = 0V$
$G = 1V/V$ V_{IN} linear limits = ±14.3V

Figure 8-6. Current Consumption versus Differential Input Voltage



$V_S = V_{SOUT} = \pm 15V$ $V_{ICM} = V_{REF} = 0V$
G = 50V/V V_{IN} linear limits = ±0.286V

Figure 8-7. Current Consumption versus Differential Input Voltage



$V_S = V_{SOUT} = \pm 15V$ $V_{ICM} = V_{REF} = 0V$
G = 100V/V V_{IN} linear limits = ±0.143V

Figure 8-8. Current Consumption versus Differential Input Voltage

8.2 Typical Applications

8.2.1 Driving a Single-Ended Input SAR ADC

Figure 8-9 shows the schematic for a 16-bit, precision, 1MSPS, successive approximation register (SAR), analog-to-digital converter (ADC). This circuit shows the driving capability of the PGA848 with the ADS8860 single-ended input ADC.

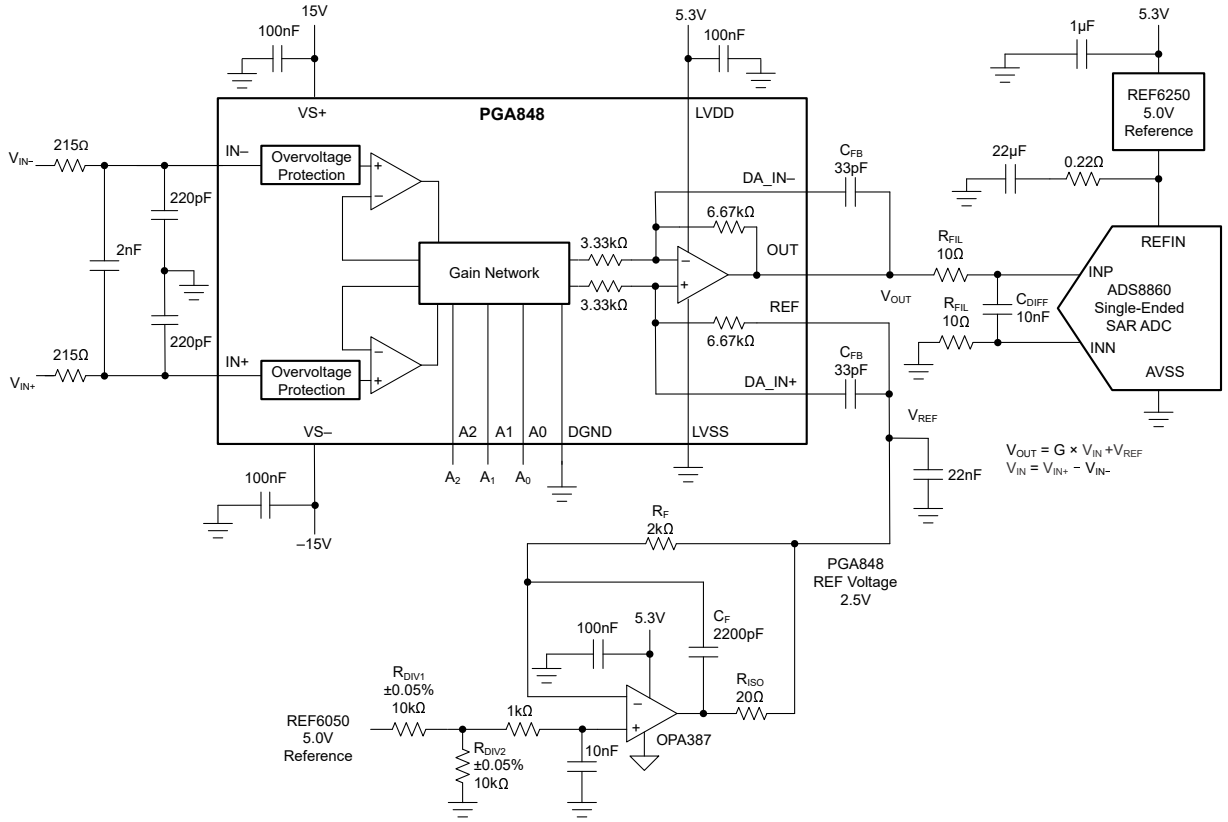


Figure 8-9. Driving the ADS8860 SAR ADC

The circuit accepts single-ended or differential input signals. The PGA848 operates with independent input and output power supplies. In this example, ±15V power supplies power the input stage, and a unipolar 5.3V supply powers the output stage. The PGA848 output stage supply is powered by the same 5.3V ADC supply. The 5.3V output supply operation prevents overloading the ADC inputs during PGA overdrive conditions. The REF6250 is selected as the ADC voltage reference. The REF6250 is a low-noise, low-drift, precision, 5V reference connected to the ADS8860 reference input ADC REFIN pin.

The PGA848 output voltage is developed with respect to the REF pin. The REF pin is set to the SAR ADC midscale voltage by dividing the REF6250 ADC reference with a precision resistive voltage divider. The OPA387 buffer drives the PGA848 REF pin. The OPA387 is a precision amplifier with low offset, low drift, and 5.7MHz gain bandwidth product.

8.2.1.1 Design Requirements

Table 8-1 lists the design requirements for the application driving the ADS8860 ADC.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltages	$V_{S\pm}$ = ±15V, V_{LVDD} = 5.3V, V_{LVSS} = GND, ADC REFIN = 5V
PGA848 reference pin	V_{REF} = 2.5V
Full-scale range of the ADC	FSR = 5V
Sampling rate of the ADC	f_{SAMPLE} = 1MSPS
Signal frequency	1kHz
RC kickback filter	R_{FIL} = 10Ω, C_{DIFF} = 10nF

8.2.1.2 Detailed Design Procedure

The first filter located at the input of the PGA (see Figure 8-9) helps reduce electromagnetic interference (EMI) and radio frequency interference (RFI), high-frequency, extrinsic noise. Customize this filter as per the application bandwidth and anti-aliasing requirements.

The second filter is provided by C_{FB} in parallel with the PGA 6.67kΩ feedback resistors. The PGA resistors are ±15% absolute tolerance, as such, consider the effect of the tolerance on the filter cutoff frequency. C_{FB} = 33pF results in a filter cutoff frequency of 723kHz. On the high side of the resistor tolerance, the filter frequency changes to 629kHz. The device allows for flexibility to modify the C_{FB} capacitor value to adjust bandwidth, with a trade-off on the broadband noise of the circuit.

The third filter placed at the ADS8860 inputs works as a charge reservoir filter to drive the SAR ADC. The charge kickback filter reduces the instantaneous charge demand of the amplifier, maintaining low distortion that otherwise potentially degrades because of incomplete ADC sample-and-hold settling. The RC filter combination (R_{FIL}, C_{DIFF}) is tuned for ADC sample-and-hold settling and total harmonic distortion (THD) performance, while maintaining stability of the PGA. High-grade C0G capacitors are used everywhere in the signal path for the low distortion properties.

The PGA848 front end, accounting for all three filters, provides a nominal f_{-3dB} bandwidth of 160kHz. On the high side of the internal 6.67kΩ feedback resistor tolerance, the PGA848 f_{-3dB} bandwidth changes to 157kHz. However, the circuit maintains –0.1dB flatness to 25kHz (derived from simulation of the cascaded filter stages).

The ADS8860 requires a full-scale input in the range of 0V to the 5V ADC reference. The PGA848 REF pin is set to a nominal voltage of 2.5V to shift the signal to the ADC midscale voltage.

Generate the PGA848 REF voltage by feeding the REF6250 5V reference through a 10kΩ-to-10kΩ precision voltage divider implemented with ±0.05% tolerance, low-drift ±5ppm/°C resistors. Drive the PGA848 REF pin with a low-impedance source. Use an op amp such as the OPA387 as a buffer to drive the REF pin.

The OPA387 buffer is configured in a dual-feedback configuration to provide stability while driving the REF pin and 22nF bypass capacitor. R_{ISO} is a 20Ω isolation resistor that provides separation of two feedback paths for optimized stability. The first feedback path through the feedback resistor, R_F = 2kΩ, connected directly to the

REF pin. The second feedback path is through the feedback capacitor, C_F = 2200pF, connected to the output of the op amp. The circuit provides a loop gain phase margin of 86°. The noninverting input of the OPA387 buffer has a low-pass filter with R = 1kΩ, C = 10nF to reduce the resistive divider thermal noise. Using any other load capacitance requires recalculation of the stability components: R_F, C_F, and R_{ISO}. If modifying the REF bypass capacitance, verify the circuit is stable with simulation using the OPA387 TINA-TI model (or PSpice®-for-TI model). Confirm the circuit provides more than 60° of phase margin.

The results are shown in Table 8-2, which includes the typical signal-to-noise ratio (SNR) and total harmonic distortion (THD) measurements. A 1kHz differential signal is applied and the signal amplitude is adjusted to produce PGA848 output at -0.5dBFS of the ADC.

Table 8-2. PGA848 and ADS8860 FFT Data Summary, f_{SAMPLE} = 1 MSPS, f_{IN} = 1kHz, BW = 160kHz

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.5	9.79	91.84	-95.34	14.70
1	4.886	91.72	-95.45	14.69
2	2.443	91.35	-95.33	14.64
5	977.5m	88.57	-95.32	14.28
10	488.5m	84.00	-95.18	13.61
20	244.1m	78.98	-95.10	12.81
50	97.8m	72.36	-94.75	11.72
100	48.85m	67.16	-92.75	10.86

Performance and SNR are function of the system bandwidth. Setting the system bandwidth to fit application requirements enables higher performance. In the previous example, reducing the PGA bandwidth to 23kHz by setting C_{FB} = 1nF improves the SNR at higher gains by almost 12dB as shown in Table 8-3.

Table 8-3. PGA848 and ADS8860 FFT Data Summary, f_{SAMPLE} = 1 MSPS, f_{IN} = 1kHz, BW = 23kHz

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.5	9.79	92.69	-93.90	14.69
1	4.886	92.70	-93.64	14.68
2	2.443	92.59	-93.28	14.64
5	977.5m	92.36	-93.25	14.62
10	488.5m	91.66	-93.17	14.55
20	244.1m	89.75	-93.27	14.35
50	97.8m	84.16	-93.15	13.60
100	48.85m	78.80	-92.64	12.77

8.3 Power Supply Recommendations

The nominal performance of the PGA848 is specified with input-stage supply and output-stage supply voltages of ±15V, and V_{ICM} and V_{REF} at mid-supply. Within the specified limits, custom input common-mode and output common-mode voltages are usable without compromising performance; see also Section 6.3. To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see also Section 7.2.

CAUTION

Supply voltages higher than 40V (±20V) permanently damage the device. Parameters that vary over supply voltage or temperature are shown in Typical characteristics section of this document.

8.4 Layout

8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), verify both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise potentially propagates into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the DA_IN+ and DA_IN– pins potentially causes dc offset errors in the output voltages. Additionally, excessive parasitic capacitance at these pins potentially results in decreased phase margin and affects the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes located immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the thermal energy source effects on both sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

8.4.2 Layout Example

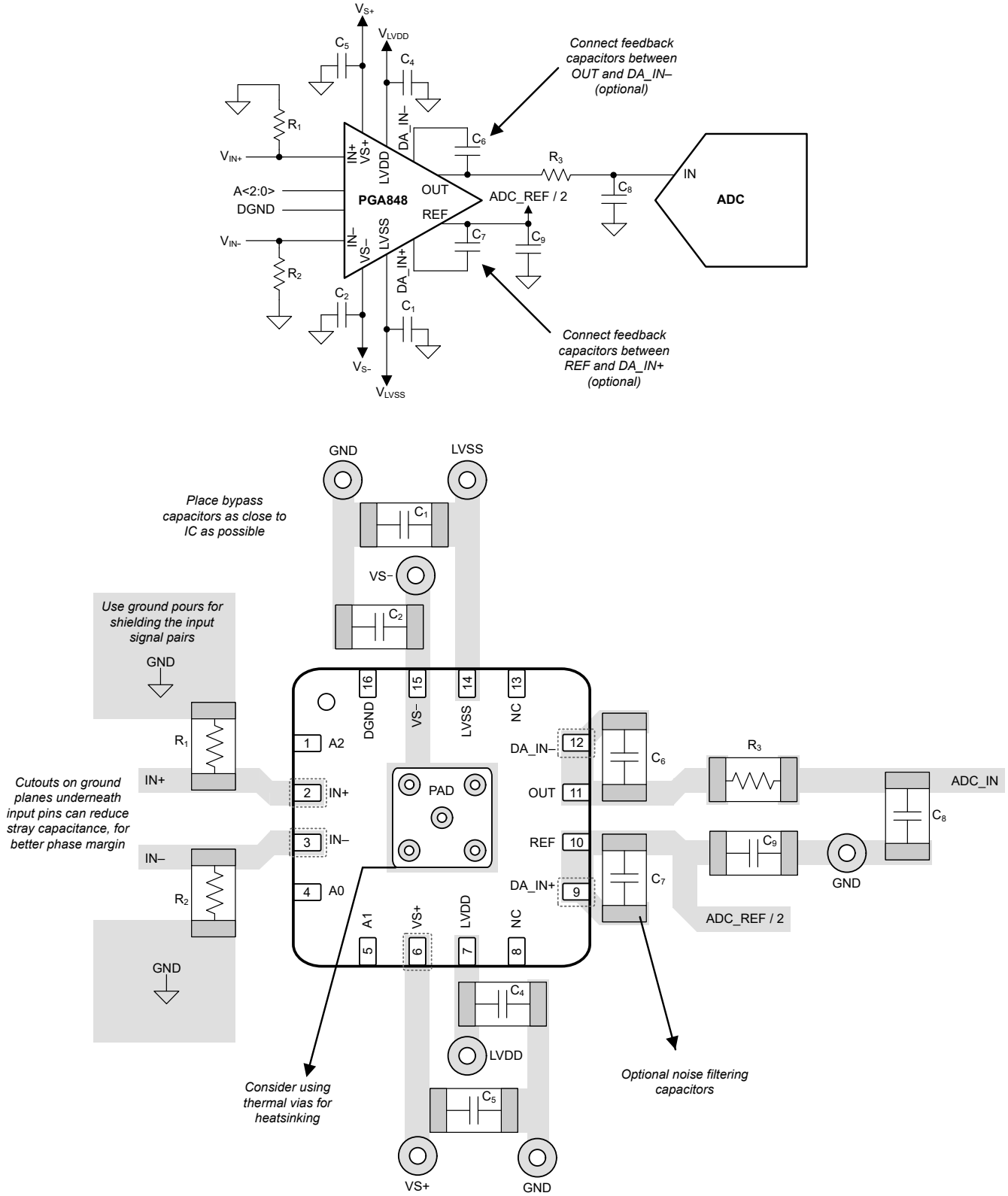


Figure 8-10. Example Schematic and Associated PCB Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem and prototype designs before committing to layout and fabrication, thus reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, including a range of passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability. This capability allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note
- Texas Instruments, *ADS8860 16-Bit, 1MSPS, Serial Interface, Micropower, Miniature, Single-Ended Input, SAR Analog-to-Digital Converter* data sheet
- Texas Instruments, *REF62xx High-Precision Voltage Reference With Integrated ADC Drive Buffer* data sheet
- Texas Instruments, *OPAx387 Ultra-High Precision, Zero-Drift, Low-Input-Bias-Current Op Amps* data sheet

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2025) to Revision A (December 2025) — **Page**

- Updated data sheet status from *Advanced Information* to *Production Data* 1
- Changed common mode input impedance from 7pF to 4.4pF 6
- Changed differential input voltage limits from ±20V to ±16V 6
- Modified CMRR for G = 2, 10, and 20 from 81dB, 96dB, and 102dB to 80dB, 95dB, and 100dB respectively. 6
- Added the Voltage Noise section 6
- Modified Nonlinearity test conditions for G=0.5 from VOUT=10V to 8V 6
- Added the differential gain nonlinearity parameter values 6
- Changed the BW parameter value for G=10,20 from 4.2MHz to 5MHz 6
- Modified slew rate test conditions for G=0.5 from VOUT=10V to 8V 6
- Added Slew Rate, and Gain Switching Time parameter values, and Settling Time parameter 6
- Added the THD and HD2, and HD3 parameters 6
- Changed IQ_input parameter typical value from 3mA to 3.2mA, and maximum value from 3.7mA to 3.9mA 6
- Changed IQ_input over temperature parameter maximum value from 4.5mA to 4.9mA 6
- Added all Typical Characteristics figures apart from *Gain Error*, *Offset and Offset Drift Distribution*, and *Gain vs. Frequency*, which existed in the previous version 9
- Modified the gain settings block diagram to have current sources at the input instead of resistors 20
- Updated Input common mode vs. output differential voltage curves for G=0.5, G=1, and G=2 23
- Added current consumption with differential inputs section 24
- Changed the opamp used in SAR ADC circuit from OPA192 to OPA387, also reflected in the application circuit figure 25
- Changed input filter and kickback filter for SAR ADC circuit, reflected in the application circuit figure 26
- Added the results table of the SAR ADC application circuit 26
- Updated the caution statement to refer to typical characteristics section 27

DATE	REVISION	NOTES
August 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PGA848RGTR	Active	Production	VQFN (RGT) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGA848

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

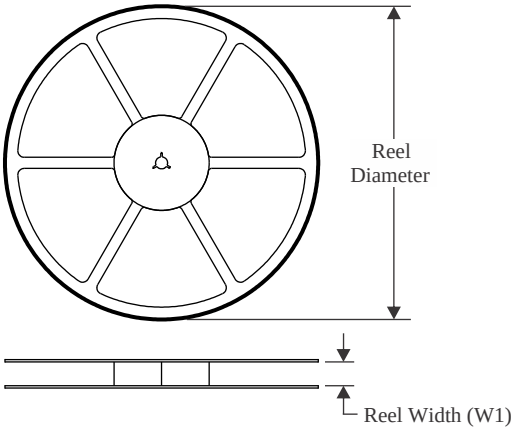
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

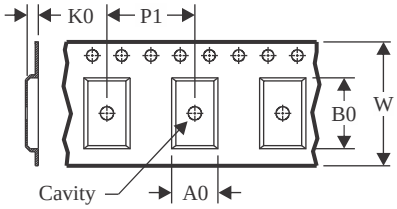
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

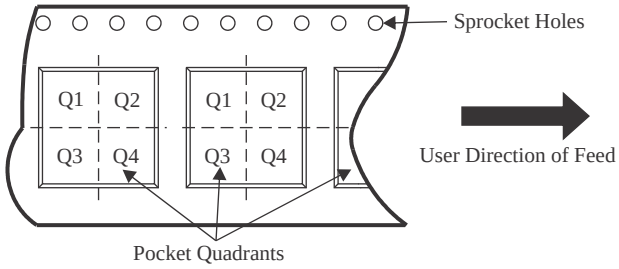


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

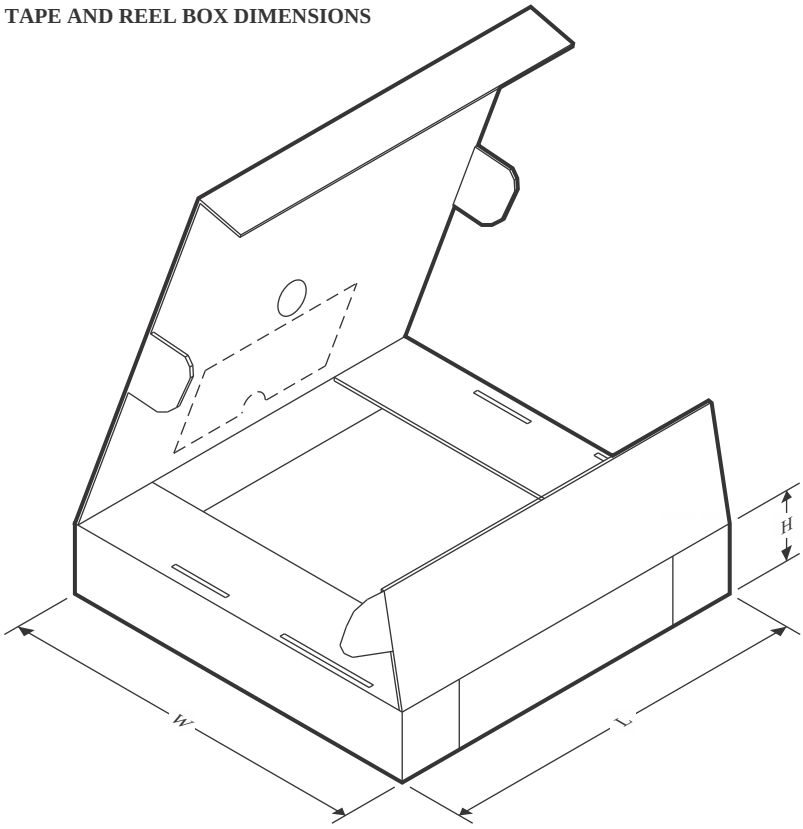
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA848RGTR	VQFN	RGT	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

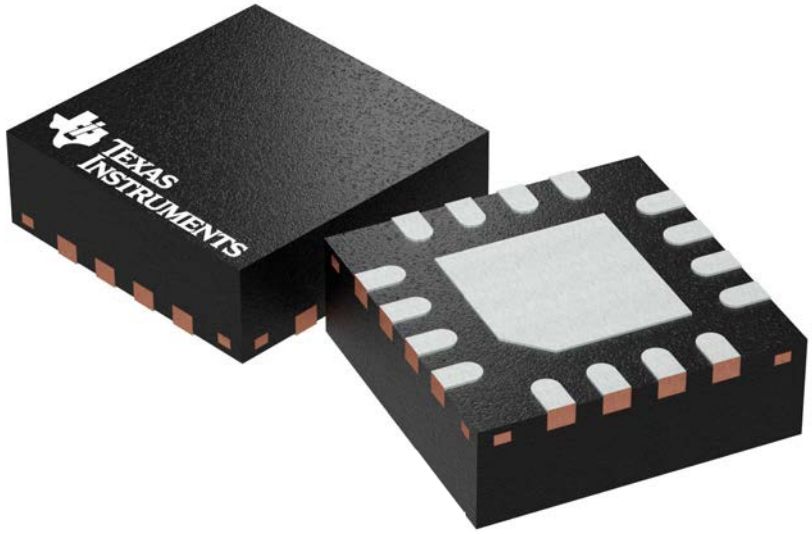


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA848RGTR	VQFN	RGT	16	5000	360.0	360.0	36.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



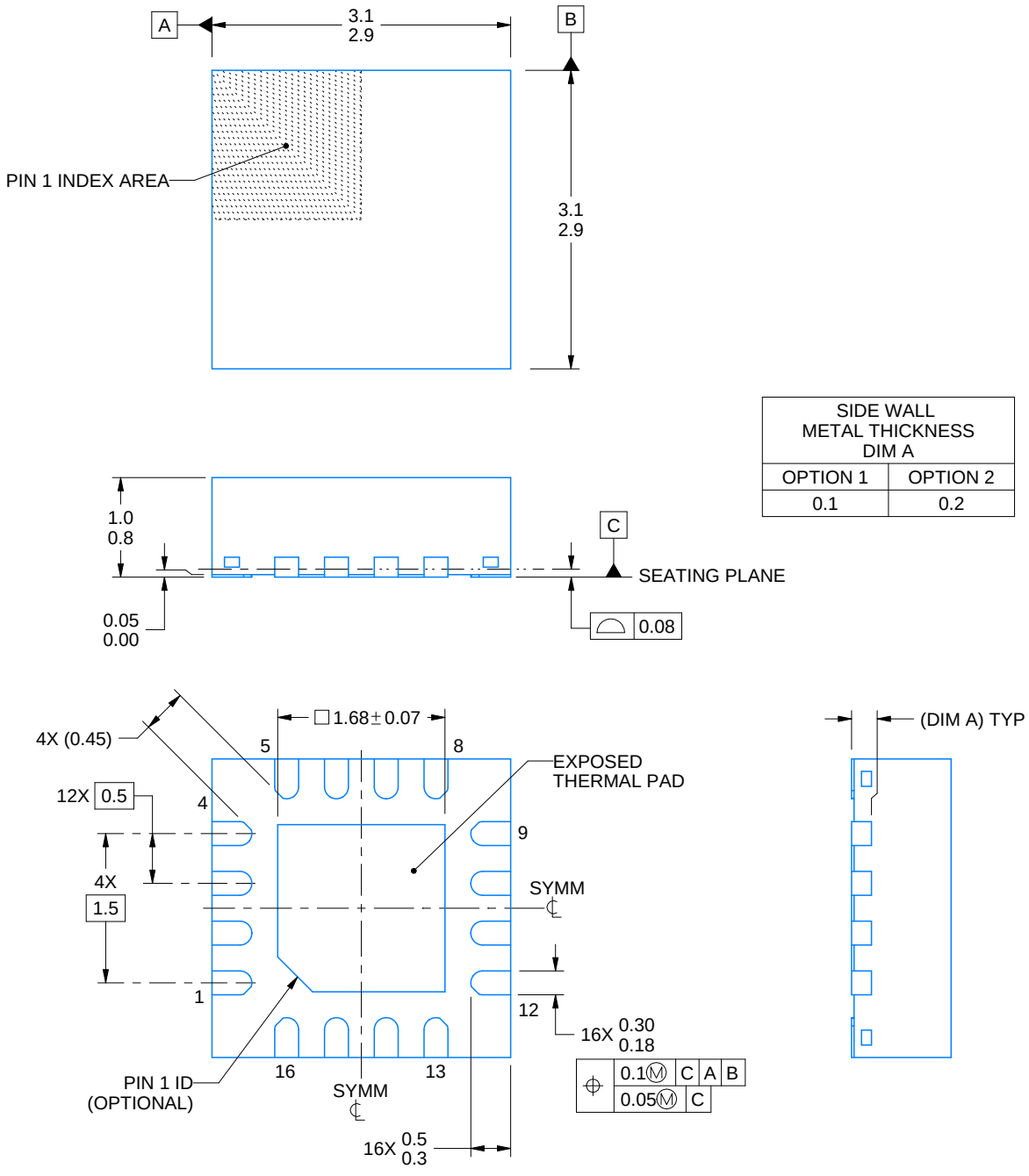
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

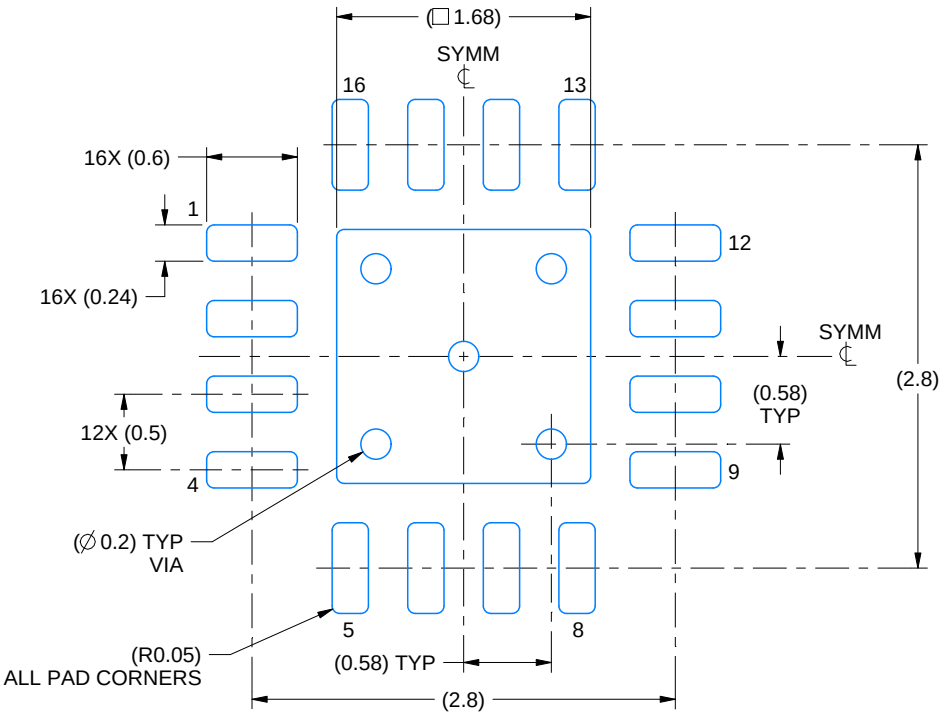
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

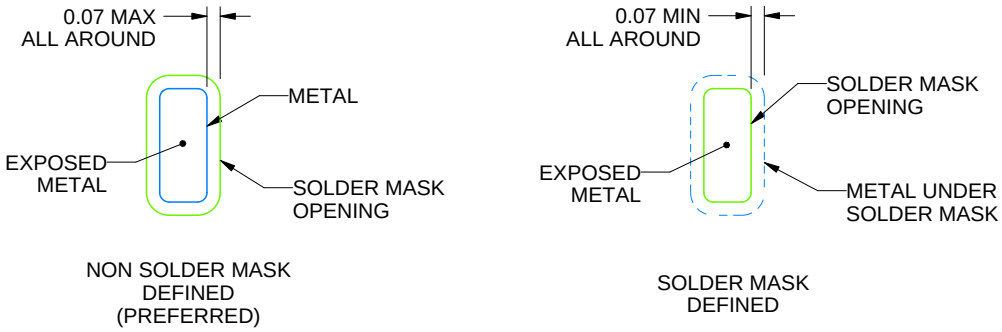


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

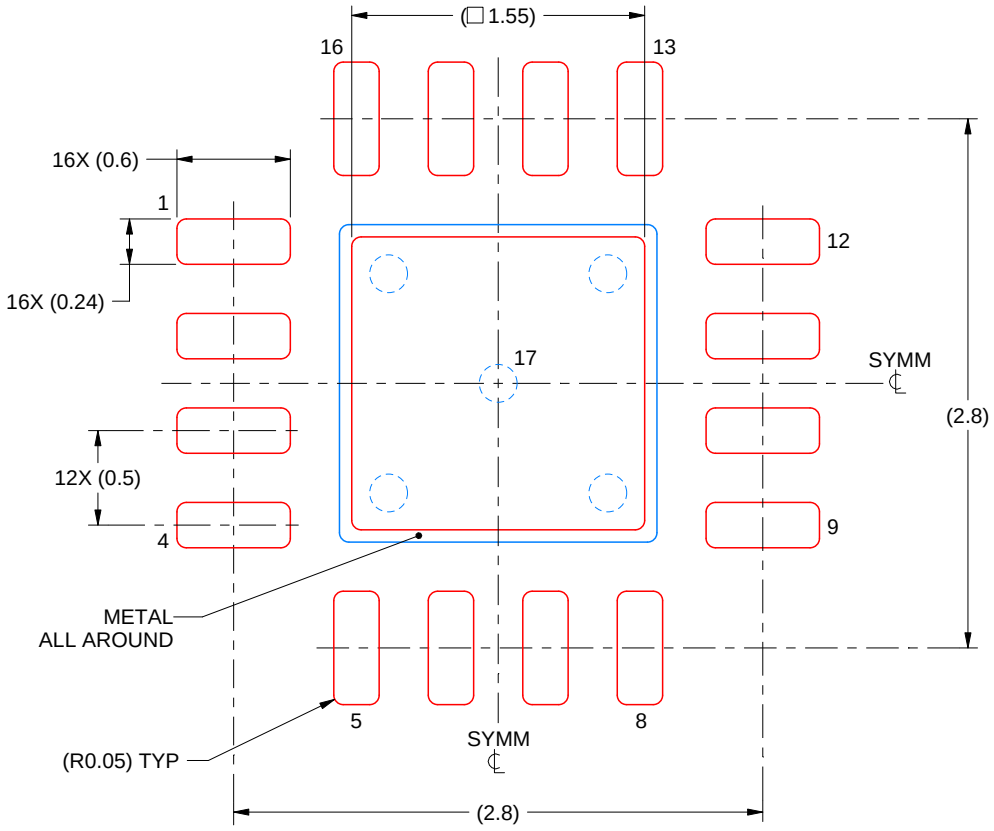


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025